Thermoplastic Substrates: Performance of Materials to Meet WEEE

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Abstract
Following the implementation of WEEE legislation, there will be an increasing interest in adopting more sustainable manufacturing processes and materials as targets are increased, and must be achieved without a loss in performance. These innovations may well lead to alternative failure modes. This work studies the performance of specific favoured materials to qualify the failure mechanisms and the effective stress screening regimes, and hence put in place the underpinning work for developing a test method for characterising these materials.

Three systems are evaluated; thermoplastic printed circuit assemblies based on copper-clad polyetherimide, polymer thick film on PET, and direct write copper on PET, were assembled using electrically conductive adhesives and tested using damp heat, dry heat and thermal cycling. All combinations showed very good reliability during the arduous testing. Chip resistor components generally showed less than 5% failures due to increased joint resistance after 1000 hours at 85°C/85%RH or 1000 thermal cycles from –55°C to +125°C. Results from gull-wing SOIC components were less promising but current work is investigating assembly methods to improve reliability of these components. Results were found to be conductive adhesive dependent, but results show that if the right combination of materials is chosen, thermoplastic substrates can be reliable for a wide range of electronics applications. The thermoplastic substrate technology offers great flexibility, for example 3D manufacturing or using the housing as the circuit board are all feasible. The lower energy and cost of manufacture and the improved potential for recycling indicate the value of further work.

Introduction
The introduction of WEEE with recycling targets, and take back issues, will result in many high volume manufacturers increasingly looking at their circuit assemblies and how they can reduce these future costs. The glass reinforced epoxy substrates represent by far the highest mass of any single component on the circuit assembly, but they are virtually unrecyclable, with burning for energy reclamation the only route. It was recently estimated in a DTI-funded report that around 85% of all PCB scrap board waste goes to landfill, with around 70% of this being of non-metallic content (primarily reinforced epoxy substrate material) with little opportunity for recycling. Waste from electronics products currently amounts to over 1 million tonnes annually or around 5% of the municipal waste stream. Growth in the WEEE waste stream is currently three times higher than the average municipal waste stream (References 1 to 4).

A potential route to enable higher levels of recycling in electronics assemblies is to use low temperature curing electrically conductive polymer adhesives (CAs) in conjunction with low cost recyclable thermoplastic substrates. These substrates can be fabricated by a number of routes. A drop in for existing FR4 type technologies would follow a similar manufacturing route of electroless plating of the plastic, followed by imaging, electroplating and etching. Conventional electroless surface finishes such as ENIG (electroless nickel/immersion gold) and immersion Ag can be applied. Such subtractive substrates (additional material is added and then removed during their manufacture) have the advantage of being able to be fabricated using the existing PCB fabrication industry infrastructure. Alternatively, thermoplastic substrates can be manufactured by application of polymer thick film inks, screen printed through a mesh screen. Substrates may also be fabricated by ink-jetting a catalyst onto the surface of the substrate and then electroless plating metals preferentially onto the catalyst. Such additive substrates have the advantage of being applicable to flexible substrates, which can subsequently be formed into complex shapes.

The adhesives used are generally silver filled epoxy systems, but alternative fillers may be used in the future. These adhesives typically have isotropic electrical properties, which can be applied and cured using the same equipment required for solder paste printing and reflow. There is no current test method for assessing the reliability of such systems, which differ in fundamental construction from the traditional solder/epoxy/glass constructions typical of electronics today. The failure modes for these novel ‘solder and glass free’ systems are very different from those experienced with conventional solder joints.

Previous work at NPL (References 5 to 7) has indicated that thermal cycling, the conventional methods of reliability assessment for soldered assemblies, is not the best method for stressing ICA joints. This is because these materials are compliant and thus deform to take up the thermal coefficient of expansion (TCE) mismatches between components and PCBs. Prolonged exposure to damp heat causes a more significant degradation in conductive performance of isotropic

conductive adhesives (ICA) joints. Whilst the conductivity of the bulk material is generally unaffected by the damp heat conditioning because any silver oxide formed is still electrically conductive, the conditioning affects the conductivity of the surface finishes of the component terminations and PCB pads, due to the formation of oxides which are not conducting. The damp heat may also have the effect of reducing the adhesive bond between the epoxy based adhesive and the component and PCB terminations. It should be noted that thermoplastic subtractive substrates generally have a higher TCE than their conventional glass fibre reinforced equivalents.

The work described here covers a series of damp heat, dry heat and thermal cycling test methods for the measurement of relative reliability of isotropic conductive adhesive (ICA) assemblies.

Test Vehicle Design & Manufacture

From a basic substrate design, three types of substrates were made, as shown in Figure 1. The test vehicle design incorporated Sn finished R1206, R0603 and SOIC gull-wing lead formats. A single-sided version was used for the additive substrates, a double-sided version with through vias for the subtractive substrates. The assembly utilised daisy-chained components and zero ohm jumpers to enable electrical continuity to be measured. The subtractive test substrates were manufactured using conventional PCB fabrication methods from 150 × 150 mm × 2 mm thick moulded plates of 30% glass-filled polyetherimide. Scrap from moulding process is recycled into more substrates. After drilling, the plates are electroless plated with copper and then electroplated with copper to produce a 1oz/sq. foot copper thickness. After imaging, Sn plating, etching, and stripping, a surface finish of immersion gold on electroless nickel (ENIG) was added. A solder mask was incorporated onto the board. Whilst not required for restricted solder spread, the mask does provide surface insulation between tracks and pads.

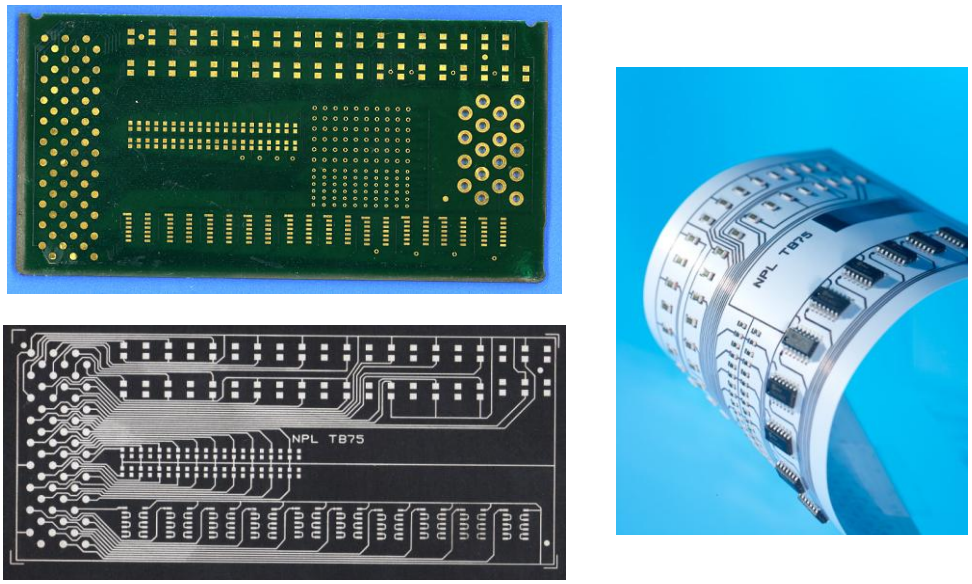

Figure 1: Examples of thermoplastic substrates manufactured for testing (copper-clad polyetherimide (top left), polymer thick film of PET (bottom left) and direct write Cu on PET (right)

Polymer thick film circuits were manufactured by printing silver loaded conductive inks onto PET flexible substrates using mesh screens. The inks were cured using a simple batch air circulation oven. Substrates were also manufactured by jetting a surface catalyst onto PET substrates and then preferentially plating electroless copper onto the catalyst. This copper was then electroless silver plated to inhibit surface oxidation.

Two different silver-filled epoxy electrically conductive adhesives were used (P and X), and printed using a laser cut 75µm stainless steel stencil. For chip resistor components, adhesive was printed on the inner half of the component lands only. For the gull-wing components, a full land print was utilised to overcome any variations in component lead bend configuration. Normal 60^{o} metal squeegees were utilised.

After stencil printing, the components were placed using an automatic placement system. Cure of material P was undertaken in an air-circulation oven for 30 minutes at 150°C, and material X was cured in a 5-zone reflow oven for 5 minutes at 150°C, both in accordance with the manufacturer's recommendations. The assembly route followed standard SM assembly practices.

Substrates were also assembled using a SnBi solder paste (Bi57Sn43 eutectic with a melting point of 137°C). Conventional SM assembly practices were employed with a peak reflow temperature of ~150°C).

Stress Screening Regimes & Electrical Continuity Monitoring

After manufacture, groups of conductive adhesive assemblies were separately subjected to damp heat ageing at 85°C/85%RH for 1000 hours, dry heat ageing at 125°C for 1000 hours and thermal cycling (-55°C to +125°C, 10 minute dwells, 10°C /minute ramps) for 1000 cycles. SnBi soldered samples were subjected to two different thermal cycling regimes of –55°C to +125°C, 10 minute dwells, 10°C /minute ramps and –20°C to +80°C, 10 minute dwells, 10°C /minute ramps, both for 1000 cycles.

Every 250 hours during stress screening, the samples were tested at room temperature and the resistance of each circuit on the assembly logged via a PC, DVM and programmable switching system.

Results

Damp Heat, Dry Heat And Thermal Cycling Stress Screening Results For Subtractive Substrates

A comparison of the electrical failures for R1206 and SOICs on subtractive substrates for damp heat, dry heat and thermal cycle testing are given in Figures 2 and 3. For R1206 components, thermal cycle testing proved most damaging to the adhesive joints with 6 to 8% failures depending on the adhesive used. Conductive adhesive material X performed better than material P. For damp heat testing, very few failures were logged. Failures for R0603 components were less than for the larger R1206 components with < 5% failures after 1000 hours/cycles of testing.

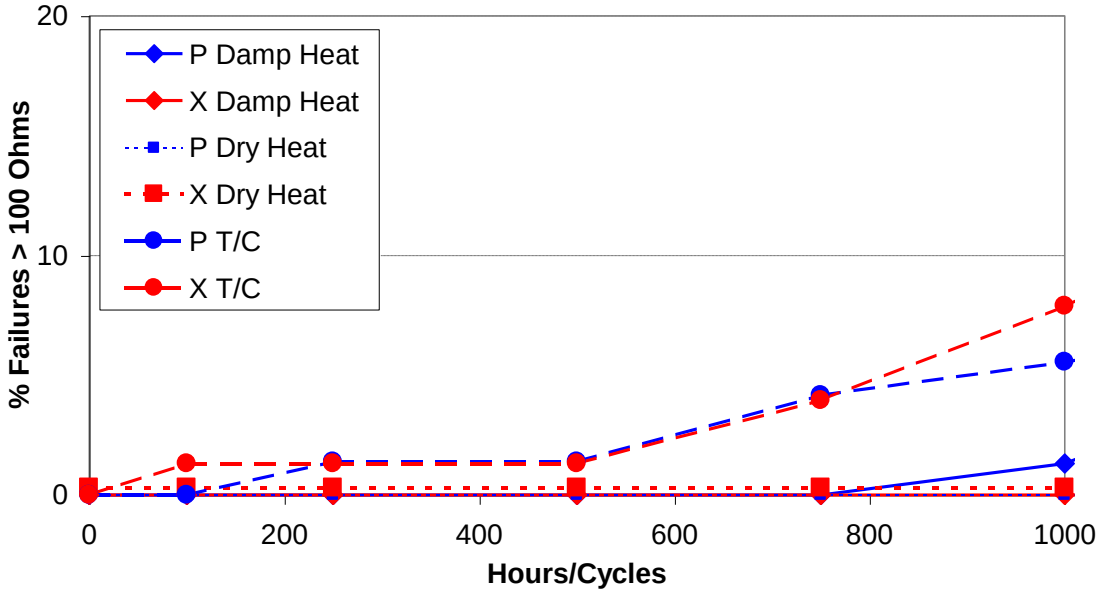

Figure 2: Comparison of electrical failures of R1206 on subtractive substrates for damp heat, dry heat and thermal cycle testing

Failure levels for the gull-wing SOIC components were higher, with results again being adhesive dependent. Results from material X were superior with <20% failures after 1000 hours/cycles.

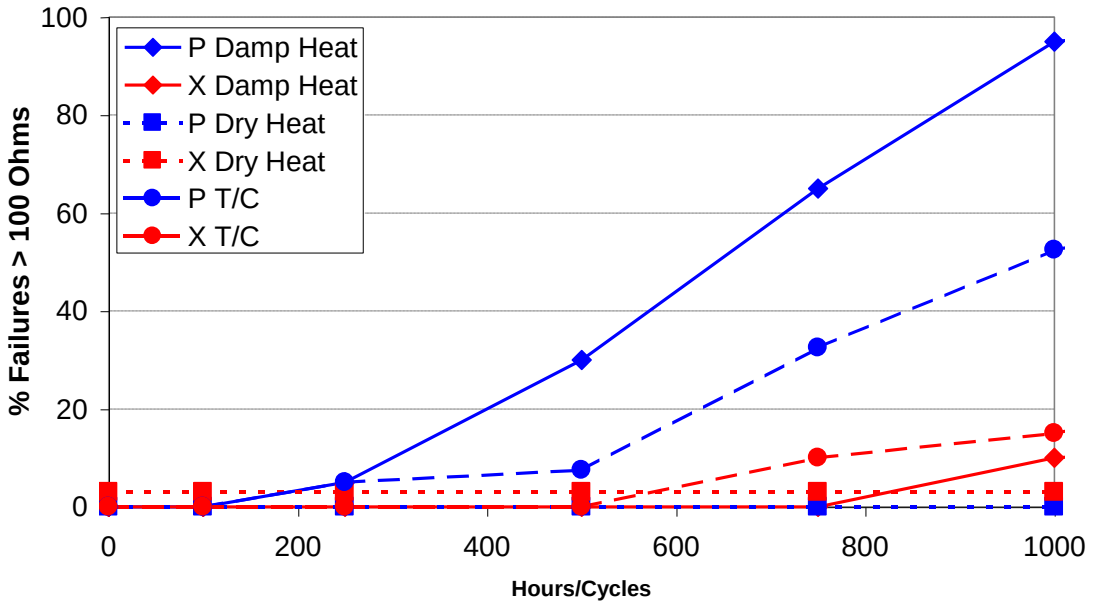

Figure 3: Comparison of electrical failures of SOICs on subtractive substrates for damp heat, dry heat and thermal cycle testing

Damp Heat And Thermal Cycling Stress Screening Results For Additive PTF Substrates

For the polymer thick film substrates, comparisons of the electrical failures for R1206 and SOICs for damp heat and thermal cycle testing are given in Figures 4 and 5. For R1206 components, testing failed to provide many failures after 1000 hours/cycles, with less than 4% failures for any materials combinations. Failures for R0603 components were less than for the larger R1206 components with < 2% failures after 1000 hours/cycles of testing.

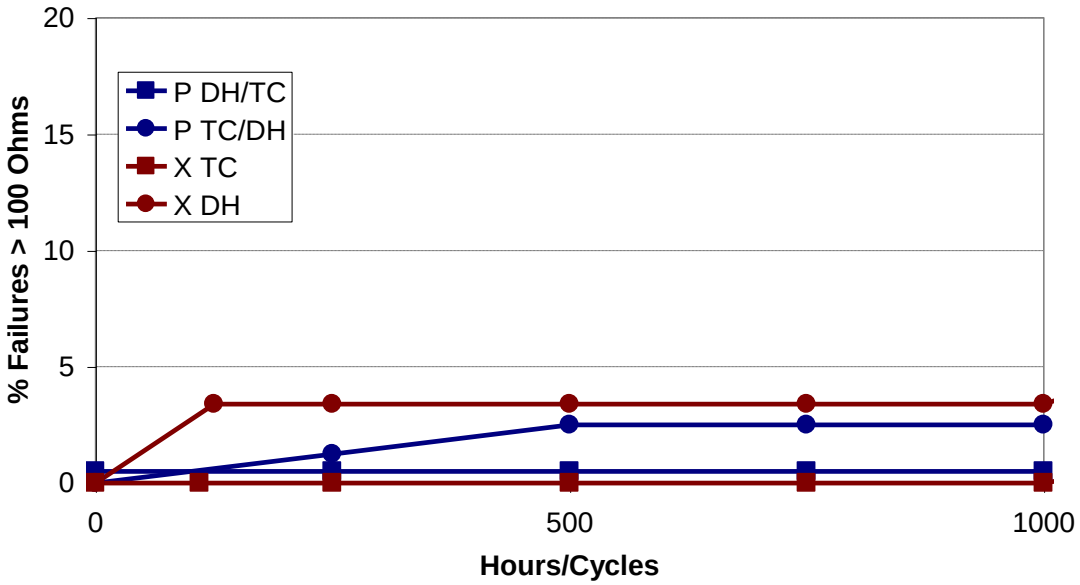

Figure 4: Comparison of electrical failures of R1206 on PTF additive substrates for damp heat and thermal cycle testing

Failure levels for the gull-wing SOIC components were again higher than for the chip components. Material X showed no failures after 1000 thermal cycles, but failures were around 60% for damp heat testing.

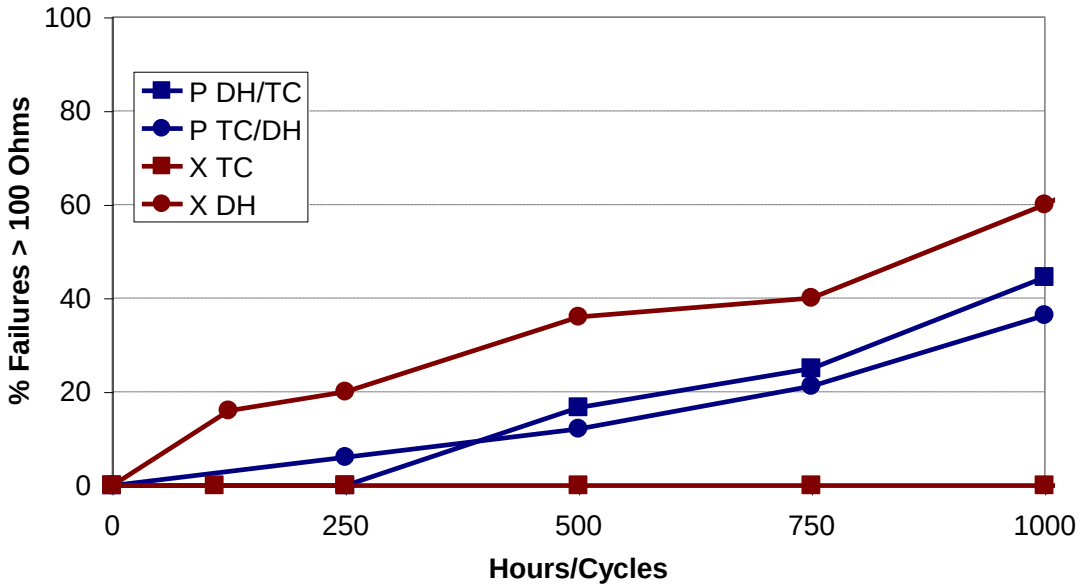

Figure 5: Comparison of electrical failures of SOICs on PTF additive substrates for damp heat and thermal cycle testing

Damp Heat and Thermal Cycling Stress Screening Results For Additive Direct Write Substrates

The comparisons of the electrical failures for R1206 and SOICs on the direct write additive substrates are given in Figures 6 and 7. As with the PTF substrates, the R1206 components failed to provide many failures after 1000 hours/cycles, with less than 3% failures for any materials combinations. Failures for R0603 components were slightly greater in this instance with < 10% failures after 1000 hours/cycles of testing.

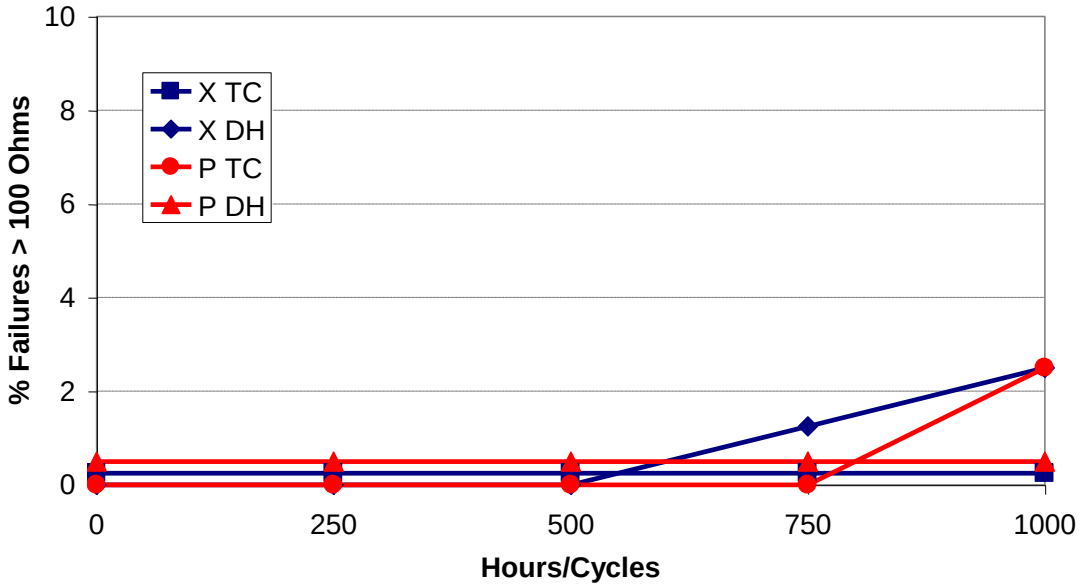

Figure 6: Comparison of electrical failures of R1206 on direct write additive substrates for damp heat and thermal cycle testing

Failure levels for the gull-wing SOIC components were higher, with results again being adhesive dependent. Results from material X were superior with <20% failures after 1000 thermal cycles and around 40% failures for 1000 hours damp heat testing.

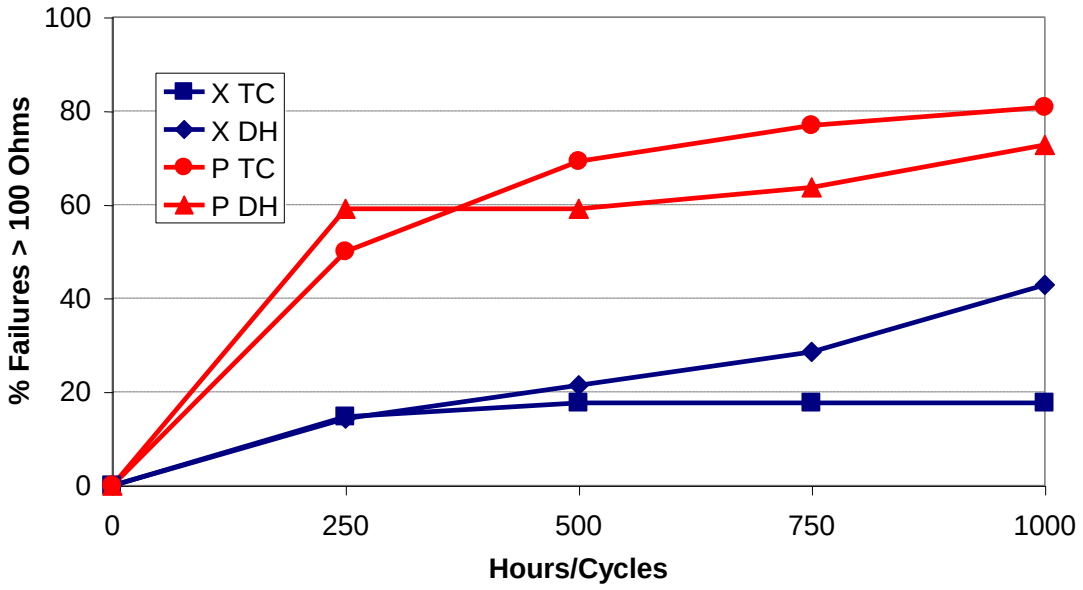

Figure 7: Comparison of electrical failures of SOICs on direct write additive substrates for damp heat and thermal cycle testing

Tin Bismuth Results
No electrical test failures were generated in 1250 cycles, –20 to +80°C or 1200 cycles, –55 to +125°C.

Discussion
Previous work at the National Physical Laboratory using isotropic conductive adhesives with conventional glass re-enforced thermoset (FR4) substrates (references 5 to 7), has shown that the bulk properties of the ICAs changed little during damp heat, dry heat or thermal cycling. ICA joints had inherently flexible characteristics, which enabled them to overcome the coefficient of thermal expansion (CTE) mismatch between the substrate (16 to 20 ppm/^{o}C) and chip resistors (6 to 8 ppm/^{o}C). For the adhesive types used, damp heat stressing proved more effective at inducing electrical failures due to oxidation of the tin plated component terminations and an adhesion failure at the component to conductive adhesive interface. However, in this work, the CTE of the PEI substrate material is significantly higher at around 50 ppm/^{o}C (reference 8) as the material did not contain glass re-enforcement, comparing to the previous work with FR4. This is generally borne out by the results, with 1000 thermal cycles proving more harmful than 1000 hours damp heat testing. There were no significant via failures during testing. The Z-axis expansion of PEI substrates (~50 ppm/^{o}C below Tg) is similar to that of a typical FR4 material (reference 9) and hence is not unexpected.

For both additive and subtractive thermoplastic assemblies, significant failures were only generated for SOIC components. As the termination finish of these components is nominally the same as that for the chip components, electroplated tin, it is postulated that the difference in joint configuration is critical. For the SOIC the angled termination of the feet creates a variable bondline, compared with the chip components where a thin uniform bond is formed. Also with the chip component the bond extends under the component, increasing the adhesion of the component to the substrate. The increased failure rate of the SOICs therefore may simply be a lower overall adhesive force, compared to the mass of the component. Further work is currently underway to determine if the use of an additional adhesive to lock the lead and pad together, can improve the reliability of SOICs on these substrates. Microsectioning of failed joints show similar failure modes for both damp heat and thermal cycling conditioning, with the tin plated component to adhesive interfaces failing.

Assemblies manufactured using SnBi solder paste proved extremely reliable with no failures during 1000 thermal cycles at –55 to +125°C or –20 to +80°C.

Conclusions
This work has shown that these thermoplastic circuit assemblies, that are inherently recyclable, have intrinsically good reliability performance, with chip resistor joints surviving 1000 hours/cycles of damp heat and thermal cycle testing with less than 10% failures. In relatively benign environments where product introductions with these materials are most likely to be seen initially the material performance is likely to exceed most application requirements.

These structures are susceptible to increasing resistance failures due to interfacial changes, which is principally due to oxidation of tin. The intrinsic resistance of these materials are reasonably stable. The failure rate is product dependent, reflecting the complexities of a successful adhesive/component/substrate package. Future studies will broaden the materials covered and look in more detail at the resistance failure mechanism.

Susceptibility to failure was found to be dependent on the stress regime. Simple dry heat exposure was the most innocuous, whereas damp heat was most deleterious. The adhesive itself is relatively resilient to moisture effects, but the metallisation at the substrate and component suffer oxidation that leads to resistance increases. In terms of electrical failures, the order of robustness for the components tested was (most robust first): Vias>R0603>R1206>SOIC. This may reflect the mechanical load the joint is carrying, if so technology solutions to improve the SOIC reliability to that of the chip components would be straightforward.

Assemblies manufactured using a similar process window but using a metal interconnect, SnBi solder paste, did not show any failures during 1000 thermal cycles at -55 to +125°C. The metallic interconnect was of course impervious to damp heat.

Acknowledgements
The work was carried out as part of a project in the Materials Processing Metrology Programme of the UK Department of Innovation, Universities & Skills. The authors also wish to acknowledge the assistance to the project provided by the following companies:
Conductive Inkjet Technology
Emerson & Cuming
Gwent Electronic Materials
Heraeus Materials Ltd.
In2Tec
Merlin Circuit Technology Ltd.
Moulded Circuits Ltd.
Henkel ~ Multicore Solders

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Introduction

- WEEE legislation will increasingly impact on electronic design
- Existing designs are not easily recycled
- New systems are potential replacements for traditional FR4, with plate and etch copper
- There are a range of options for replacement material systems, but they are not currently being pursued.

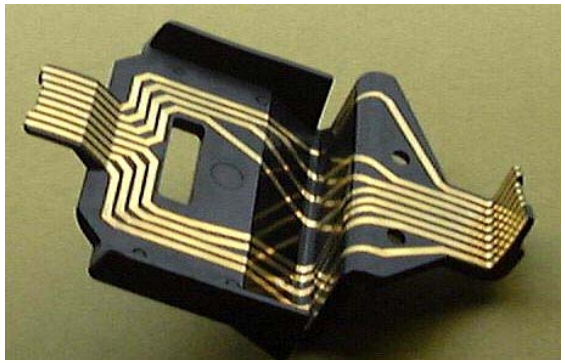
Commercially Available Thermoplastic Laminates

- Few commercially available thermoplastic laminates available
- Discussions with major laminate suppliers indicates that are not currently working on suitable materials
- Those available (PTFE/LCP/PEEK) are reinforced with woven glass or similar and therefore less attractive from a recycling point of view.

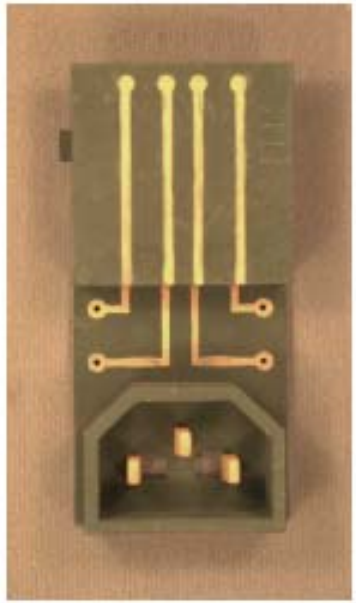
– Rogers Ultralam 3000
  - LCP based, single and multilayer constructions
  - CTE, 17ppm/^{o}C (X,Y), 150ppm/^{o}C (Z)
  - Aimed at high frequency applications
– Victrex Peek films
  - Misubishi's Ibuki® dielectric film
  - High Density Multilayer PWB, High Speed Multi-Pin LSI packages and System in Package (SIP) printed wire boards
  - CTE 15ppm/^{o}C

Moulded Substrates

- Moulded Interconnection Devices (MIDs)
- Integrates electrical and mechanical functions
- Typically single or double layer but multilayer techniques reported in development
- Manufacturing techniques
  - Single shot moulding
  - Two-shot moulding
  - Film techniques



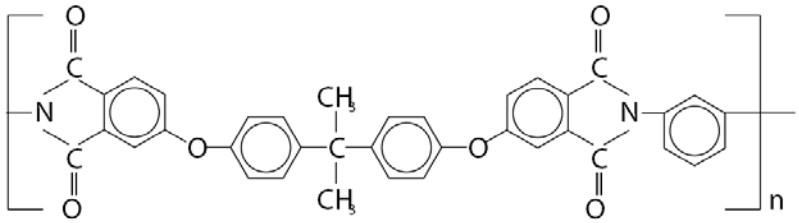
Pluggable connector
source: Moulded Circuits Ltd.

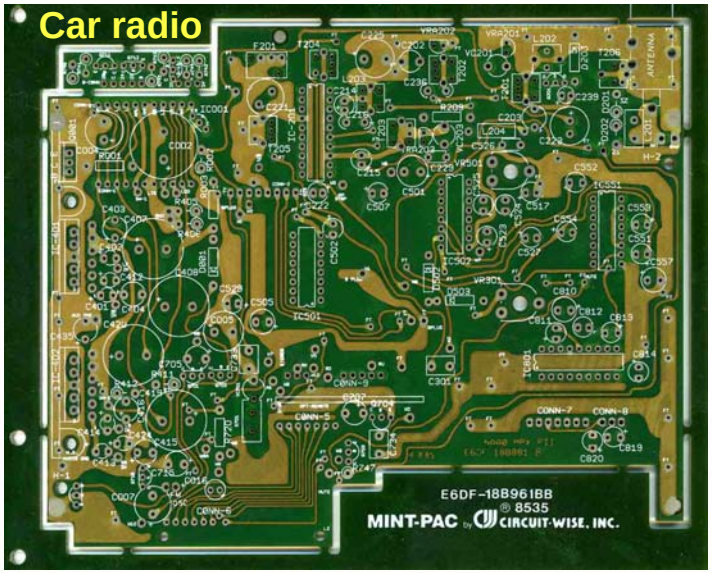


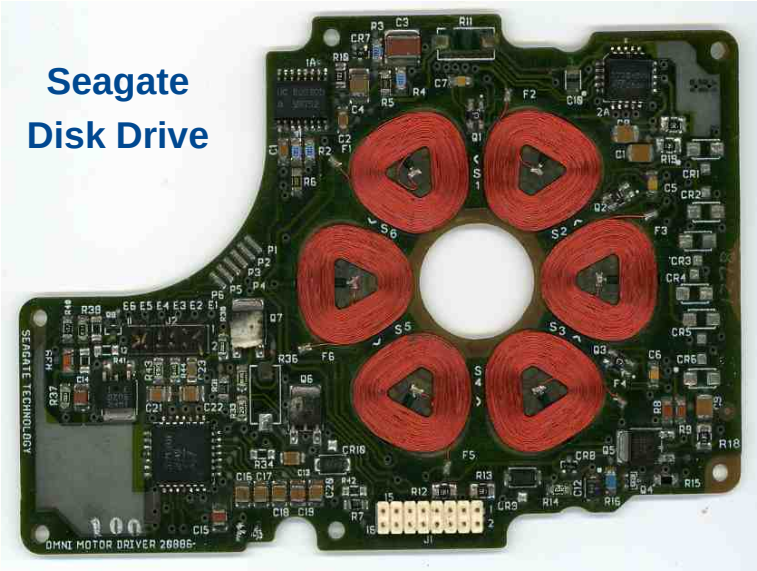
2-shot moulded in PBT
source: SIMtech

Blue Tooth high gain antenna
source: Moulded Circuits Ltd.

Thermoplastic PCBs - PEI







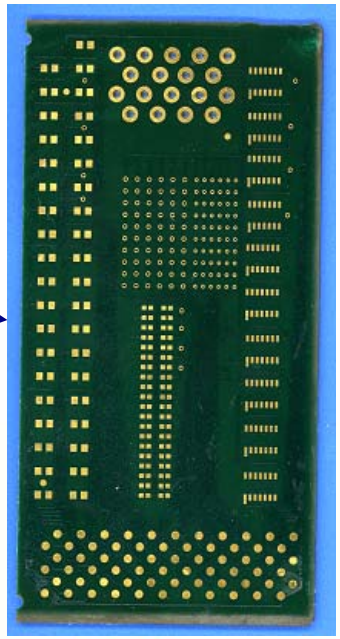
Subtractive PEI PCB

Drilled

Electroless Copper

Electroplated Copper

Imaging
Plating/Etching
Finishing



Properties

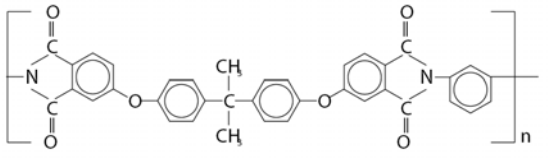
- Are alternative systems fit for purpose
- Thermal stability, dielectric properties, etc
  - CTE, a particular issue
- Fabrication process
  - Interconnect system:conductive adhesives
- Durability
- Processing advantages
- Failure modes
  - How to test for these?

Recyclable Electronic Substrates Utilising Subtractive Technology

- Test vehicles manufactured using subtractive PCB technology on recyclable substrates subjected to dry heat, damp heat and thermal cycling.
- Interconnection joint strength and electrical resistance will performance were monitored.
- Test vehicles were manufactured from the subtractive substrates with different process variables to determine the test method sensitivity

Commercially Available Thermoplastic Laminates

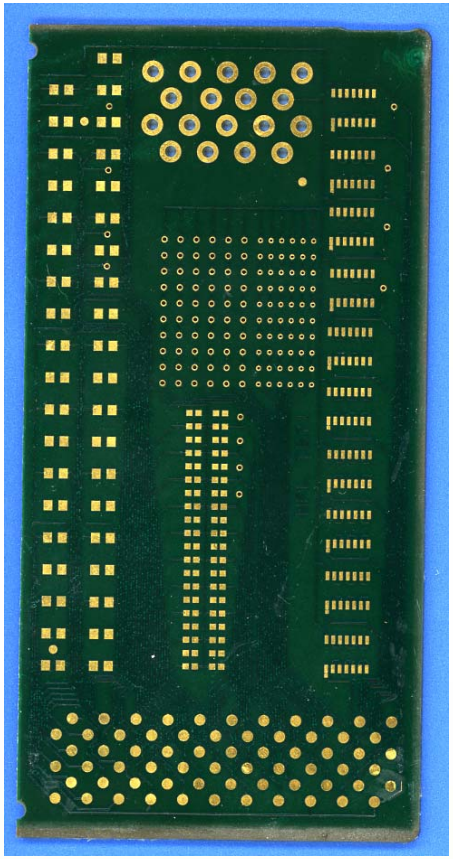
- Formed partnership with Moulded Circuits and Merlin Circuits to fabricate copper clad substrates
- Polyetherimide (Ultem) 30% glass filled



Properties	FR4 (150C Tg)	Ultem (30% filled)
CTE z-axis (ppm/degC)	60	20-60
CTE x/y axis (ppm/degC)	13-16	20-60
Thermal Conductivity (W/mdegC)	0.4-0.5	0.3
Tg (deg C)	150	217

Test Assembly

- Double-sided assembly incorporating daisy-chained R0603, R1206 and SOIC
- Also daisy-chain of two via sizes (0.7 and 0.5mm drilled)
- 1oz copper, ENIG surface finish, solder resist

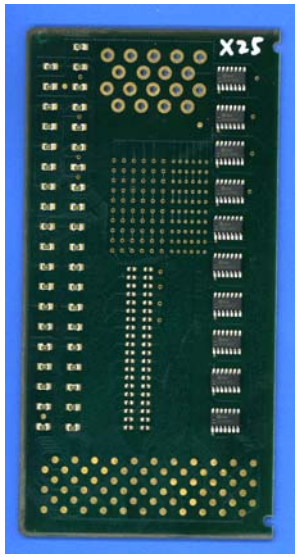


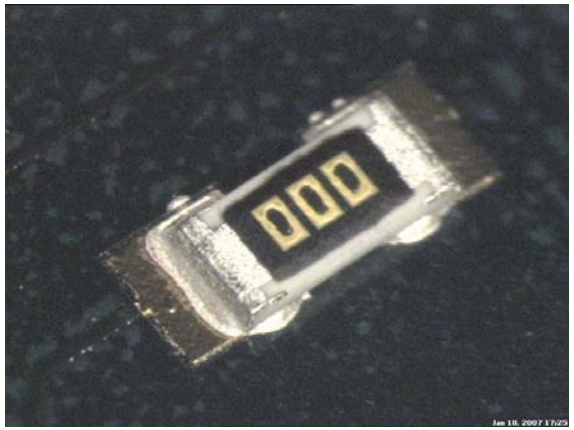
PEI Processing

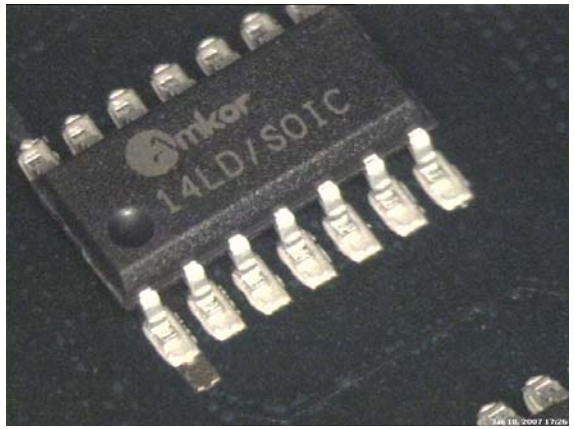
- Substrates moulded by Moulded Circuits
- Substrates tooled and drilled by Merlin
- Substrates returned to Moulded Circuits for electroless copper plating
- Substrates returned to Merlin for electro-plating, imaging, etching, finishing
- Phase 1 build using 2 ICAs
- As for solder paste
- Print - Dek265 with 75μm s/s laser-cut stencil
- Place - Sanyo auto placement system
- Cure (Reflow)
  - IR convection reflow
  - Batch air circulation oven

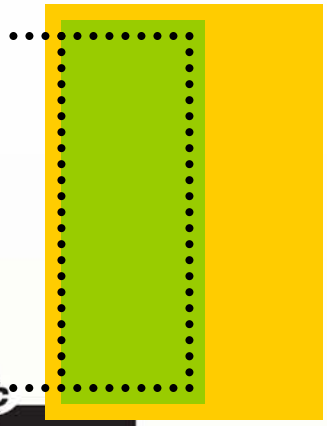
Components

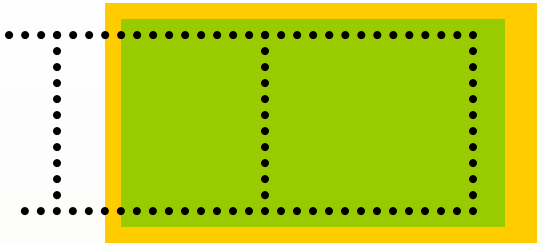
- Sn finish
- R1206/0603, half pad stencil aperture
- SOIC, full pad stencil aperture







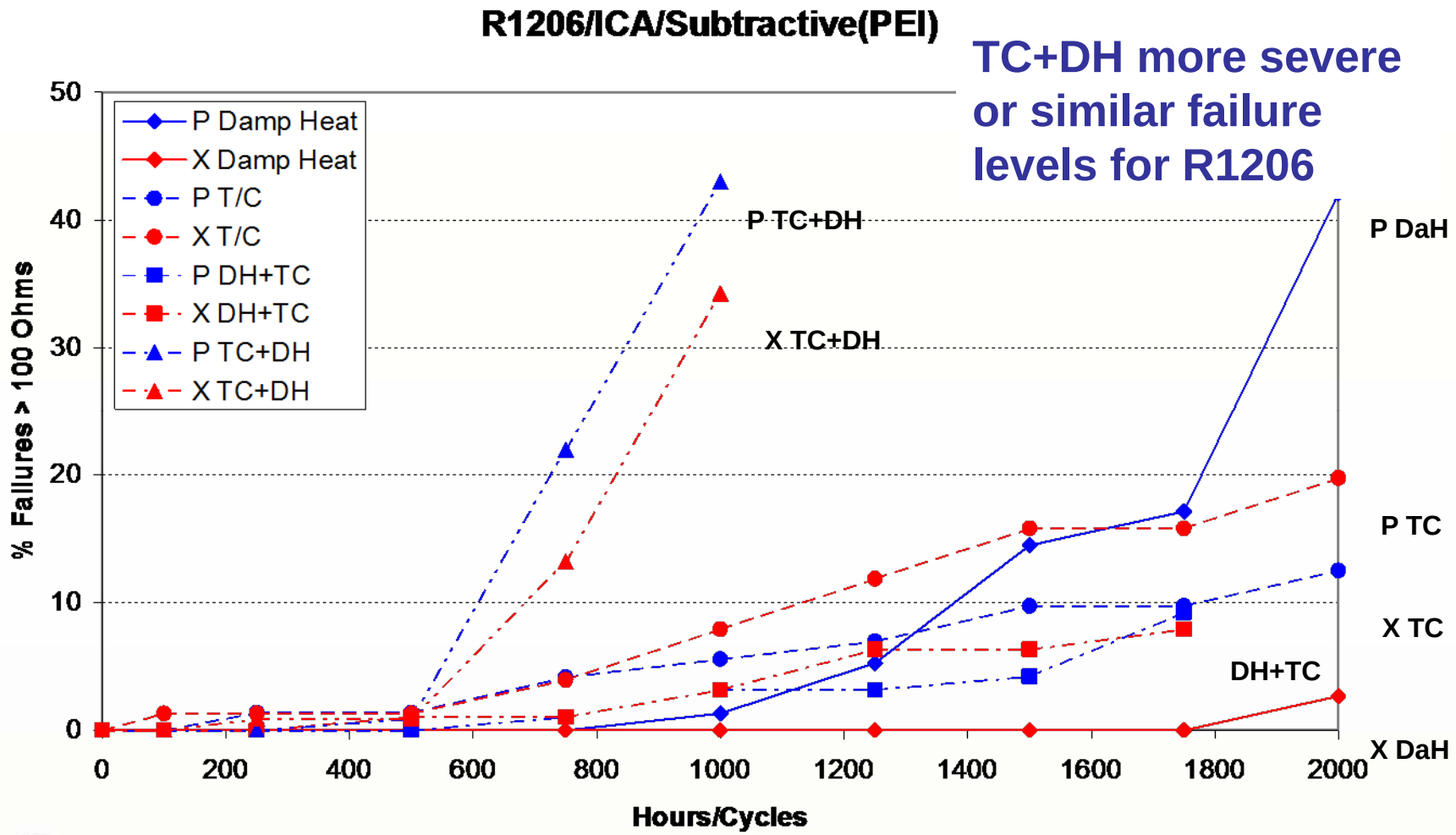




Reliability Conditioning

- Damp heat testing - 85%RH/85°C for 2000 hours
- Thermal cycling - -55 to +125°C for 2000 cycles
- Dry heat - 125°C for 2000 hours
- Combinational testing
  - 85%RH/85°C for 500 hours followed by -55 to +125°C for 500 cycles
  - -55 to +125°C for 500 cycles followed by 85%RH/85°C for 500 hours

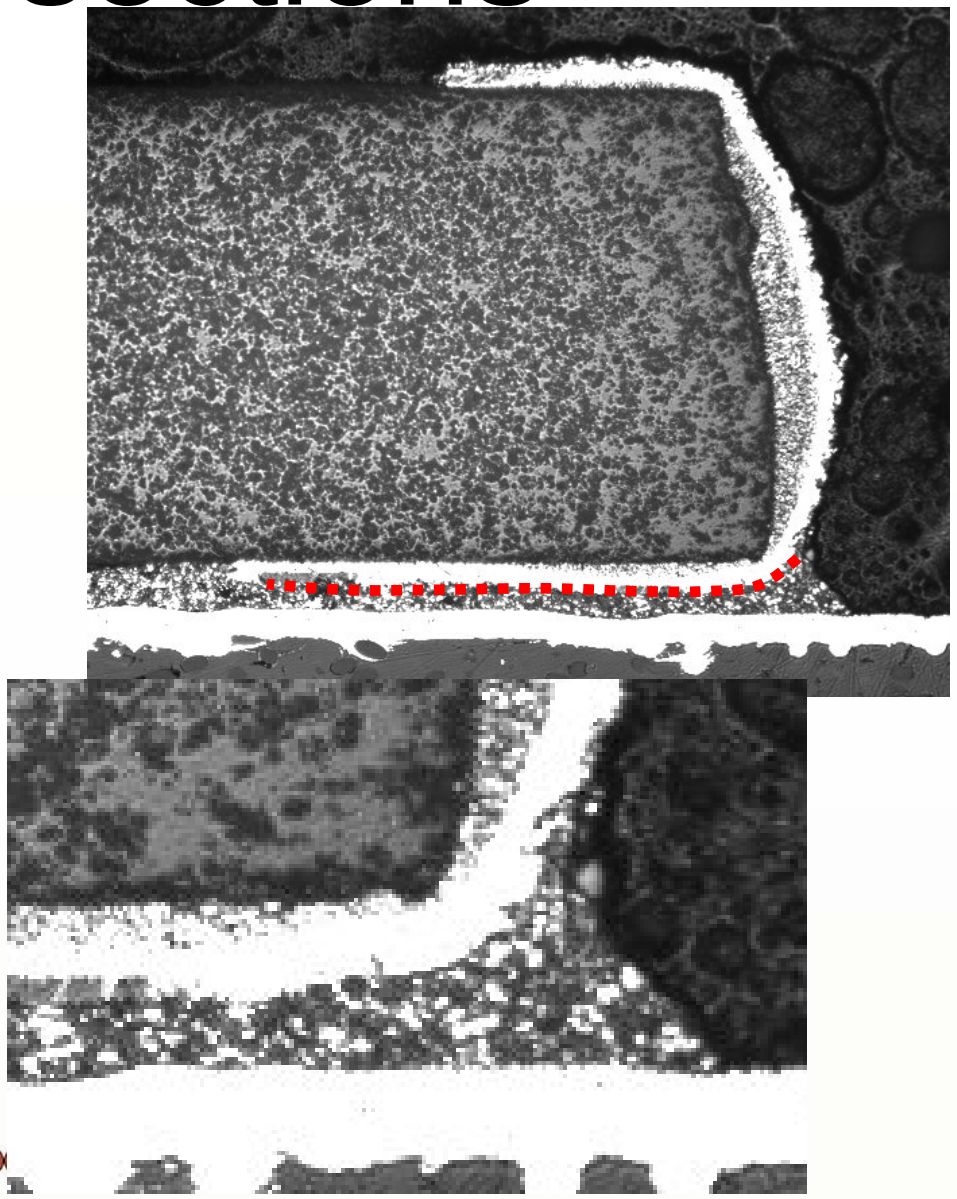
R1206 Comparison



TC+DH more severe or similar failure levels for R1206

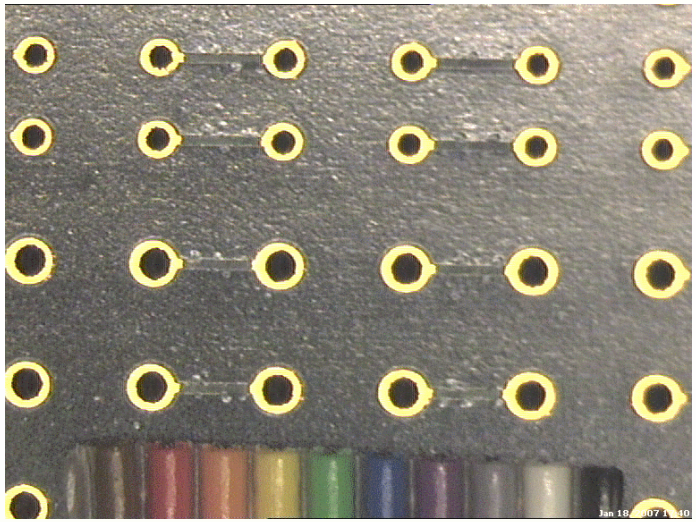
Micro-sections

- X Material
- Damp heat
- 2000 hours
- Adhesion failure at component/ adhesive interface



Vias

- No significant via failures
- Z-axis CTE, 20-60 ppm/^{o}C



Summary: Subtractive 1

- Significant failures only generated after 1000 hours/cycles
  - Damp heat produced earlier failures than thermal cycling
  - Robustness: Vias>R0603>R1206>SOIC
- No significant failures for ageing @ 125^{o}C
- Material X out performed materials P, for both damp heat and thermal cycling
- Evidence of interfacial failure between component and conductive adhesive

Summary: Subtractive 2

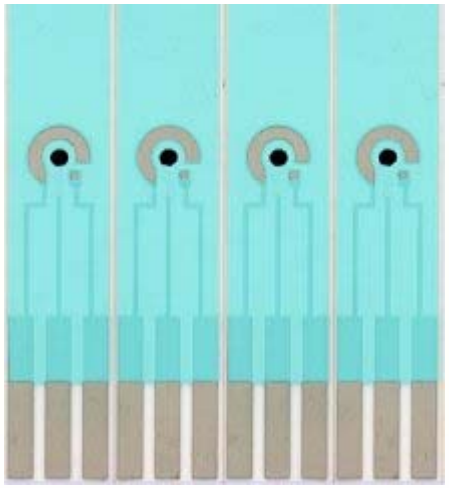
- The combination of thermal cycling followed by damp heat conditioning has been found to develop high resistance failures in conductive adhesive joints earlier than either damp heat testing or thermal cycling alone.
- The combination in this order also develops earlier failures than damp heat testing followed by thermal cycling.

Additive approach

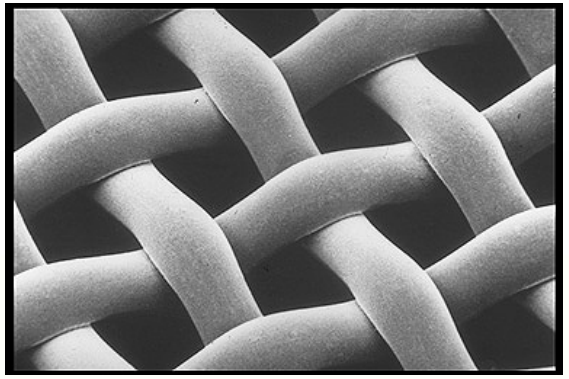
- Again a thermoplastic substrate is used but alternative methods of writing the traces is considered.
  - Conductive polymer inks
  - Direct write

Conductive Polymer Inks

- Familiar route for hybrid manufacturers
- Print conductive inks through mesh screen rather than stencil
  - No problems with stencil support
- Multilayer circuits can be built up with alternate layers of conductors and dielectrics with holes in dielectric layer to give connection between layers
- Polymer thick film uses low temperature curing inks



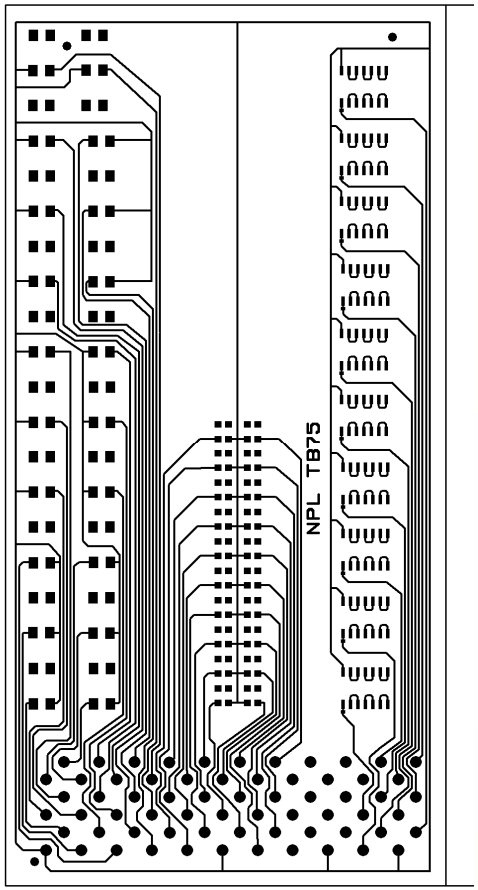
Source: GEM



Source: ***SEFAR PRINTING SOLUTIONS***

NPL Flex Test Circuit Design

- Single sided assembly
- Version of subtractive design
- Width of card reduced to meet production constraints
- 0.3mm lines and spaces
  - For PTF

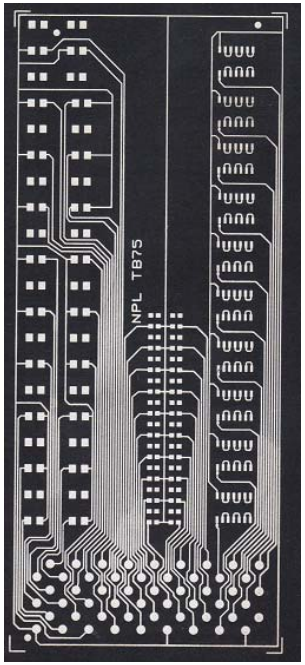


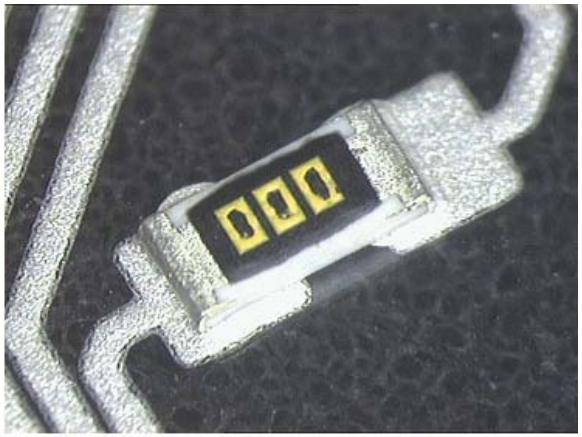
Polymer Thick Film (PTF)

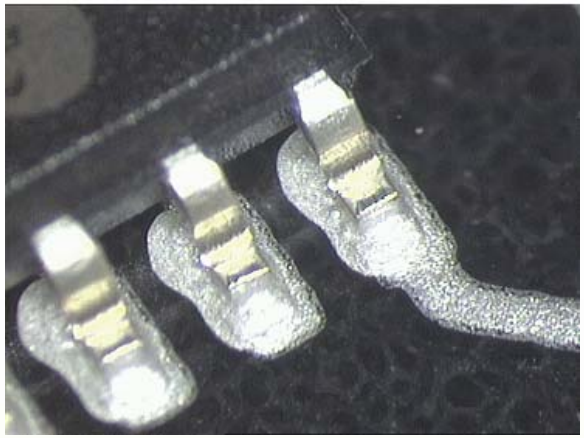
- Ag conductive ink on PET
  - Gwent Electronic Materials (www.g-e-m.com)
- Screen print
  - Dek265, mesh screen
- Cure 130^{o}C for 15mins
- Build using ICA
- Print
  - Dek265 with 75mm s/s laser-cut stencil and vacuum bed
- Place
  - Sanyo auto placement system
- Cure (Reflow)
  - Batch air circulation oven

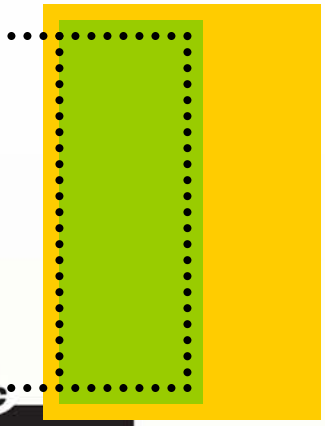
Components

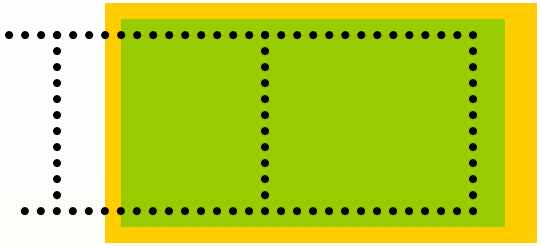
- Sn finish
- R1206/0603, half pad stencil aperture
- SOIC, full pad stencil aperture



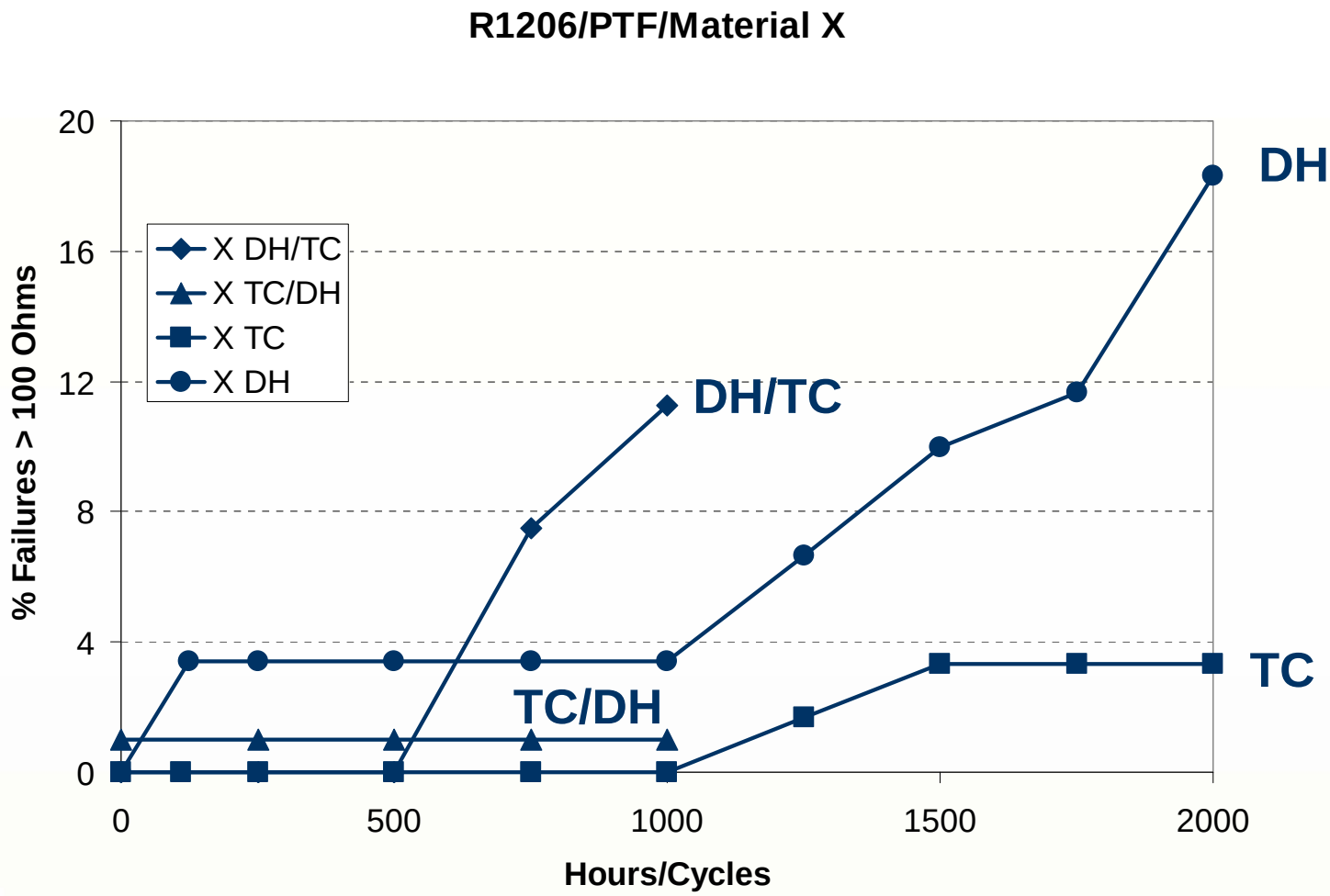




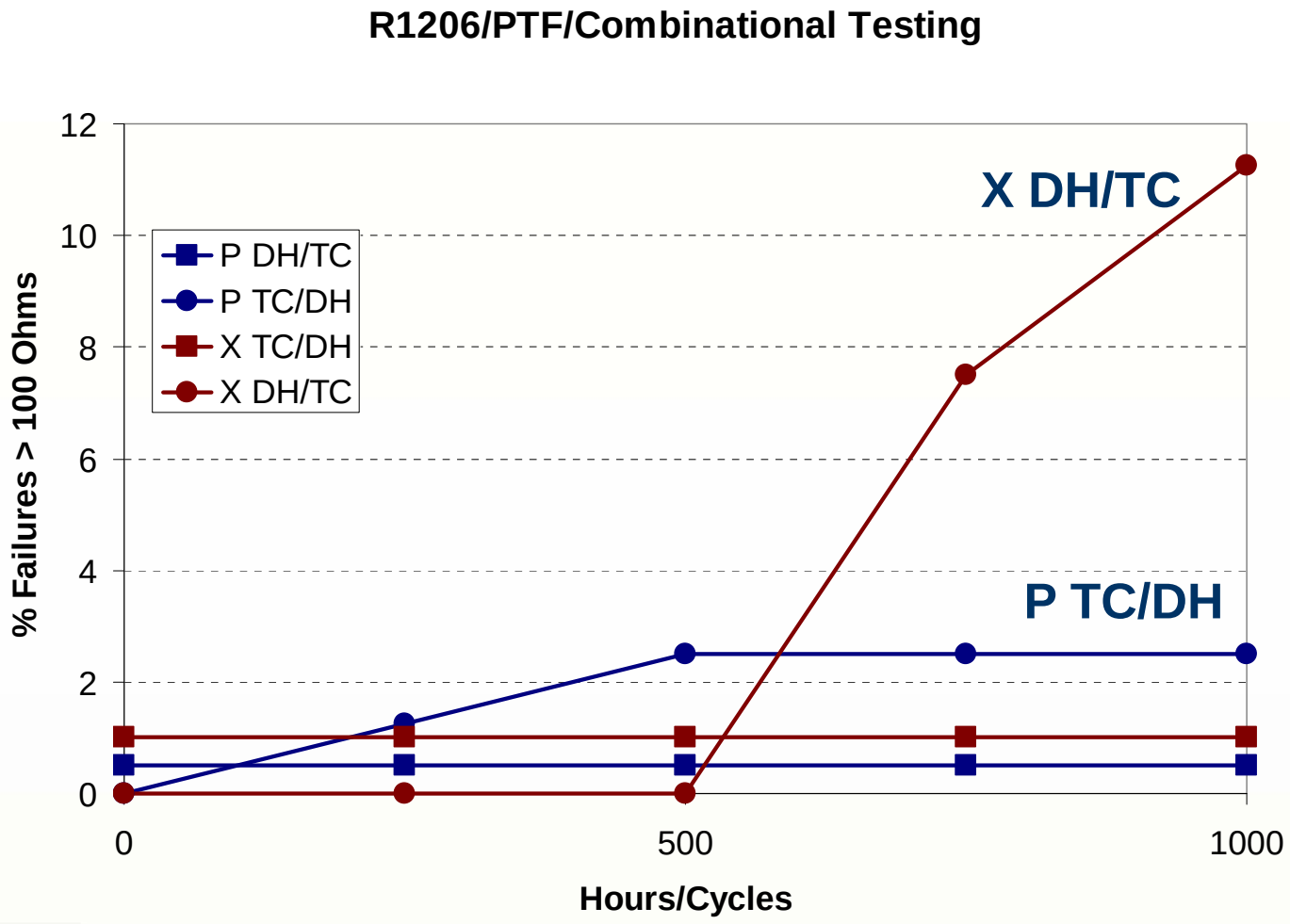




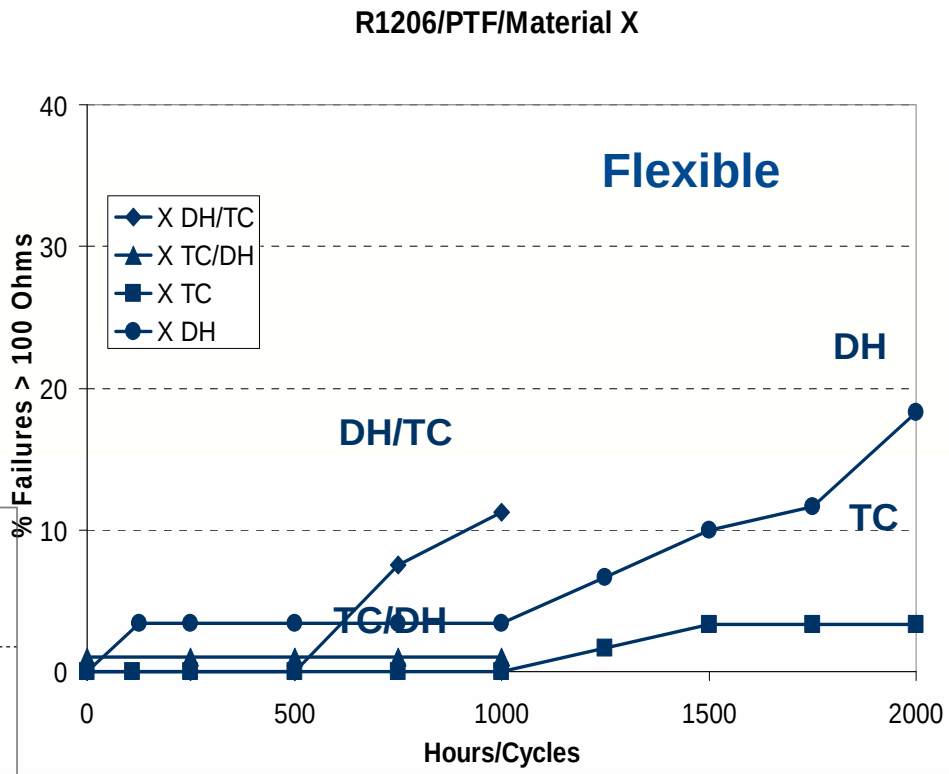
Reliability Testing PTF R1206

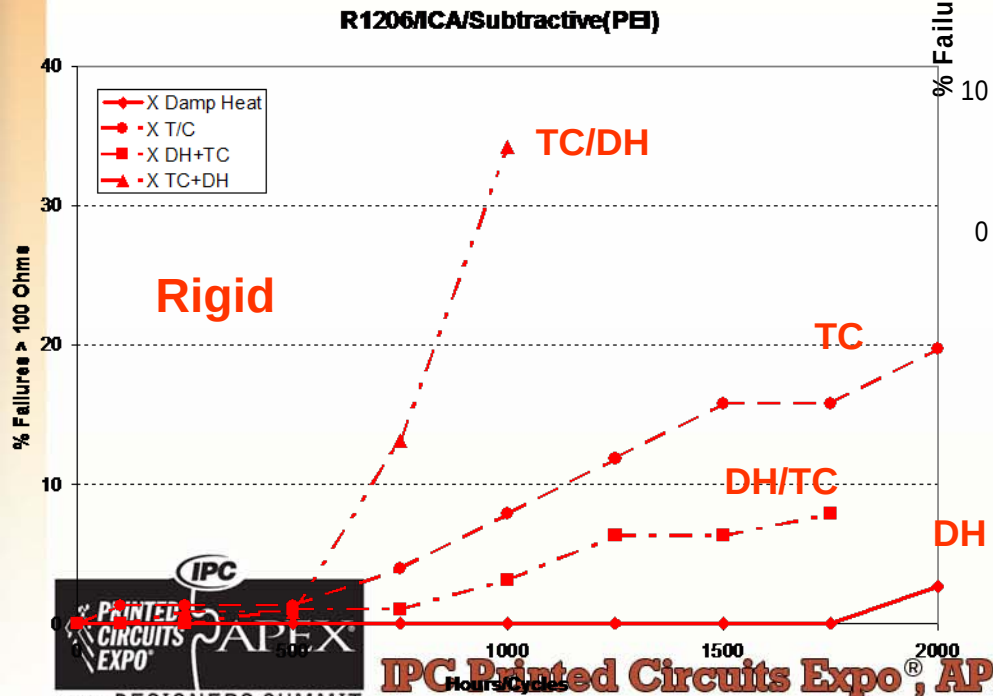


Reliability Testing PTF R1206



Comparison PTF and Subtractive





PTF Conclusions

- Adhesive performance variations
- Chip resistors survive 1000 hours/cycles
- Failures occur at component/adhesive interface
- Combinational testing does not produce significantly earlier failures than DH or TC alone
- Recommendation to continue with damp heat for PTF/ICA combinations

Direct Write

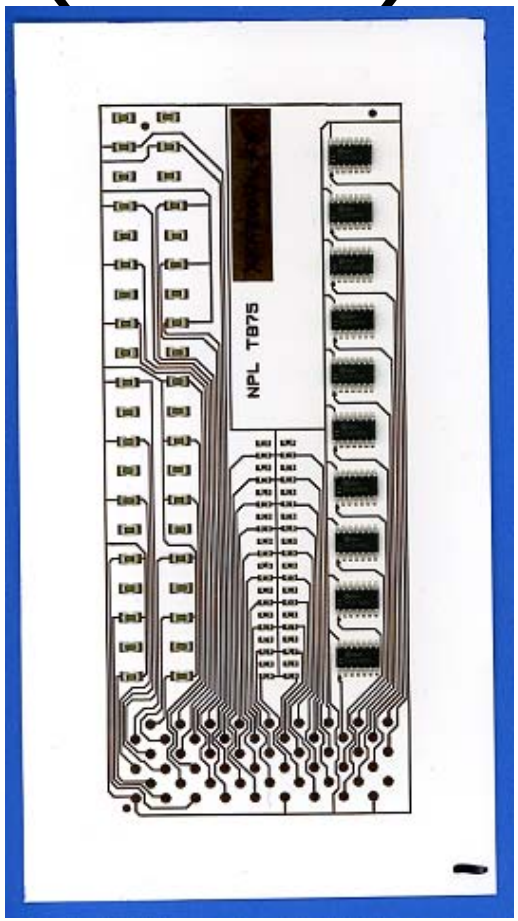
- Direct write printing of conductive inks/catalyst
  - UV curable inks for antenna manufacture
  - Writing conductive inks onto PET and Polycarbonate
  - Writing of catalyst followed by electroless Cu

"The digital print engine at the heart of the MetalJet accurately dispenses CIT's unique UV curable ink for the direct write of metals onto non-porous substrates"

Source: Conductive Inkjet Technology

Direct Write Copper (DWC)

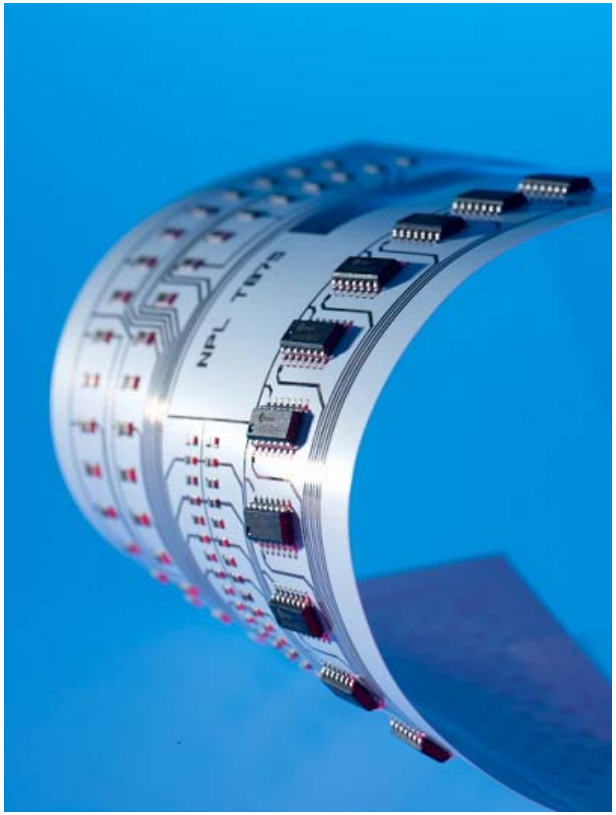
- Single sided assembly
- 1μm thick Cu tracks and pads
- 0.3mm lines and spaces
  - For PTF, finer capability for direct write
- Direct write on Melinex 339 (PET), 100μm thickness
- Immersion Ag applied to protect Cu, *courtesy of Artetch*



Supplied by
Conductive Ink Technology
(www.conductiveinkjet.com)

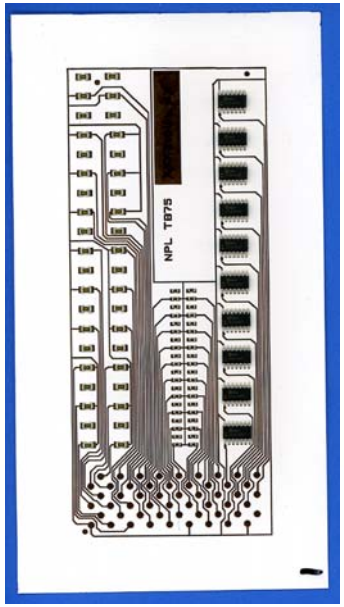
Test Assembly Build (DWC)

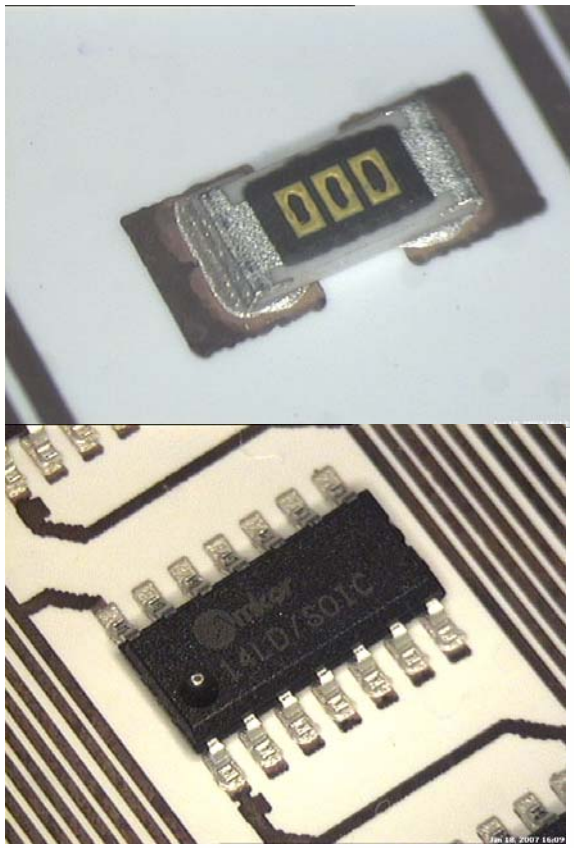
- Build using ICA
- Print Material X
  - Dek265 with 75μm s/s laser-cut stencil
  - Flex taped to backing board
  - Some issues with fiducial recognition due to poor positional repeatability
- Place
  - Sanyo auto placement system
- Cure (Reflow)
  - Batch air circulation oven

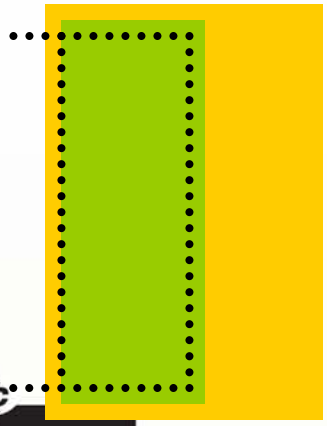


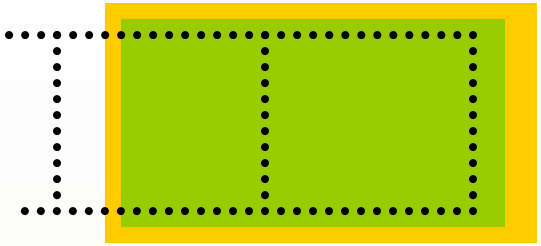
Components

- Sn finish
- R1206/0603, half pad stencil aperture
- SOIC, full pad stencil aperture





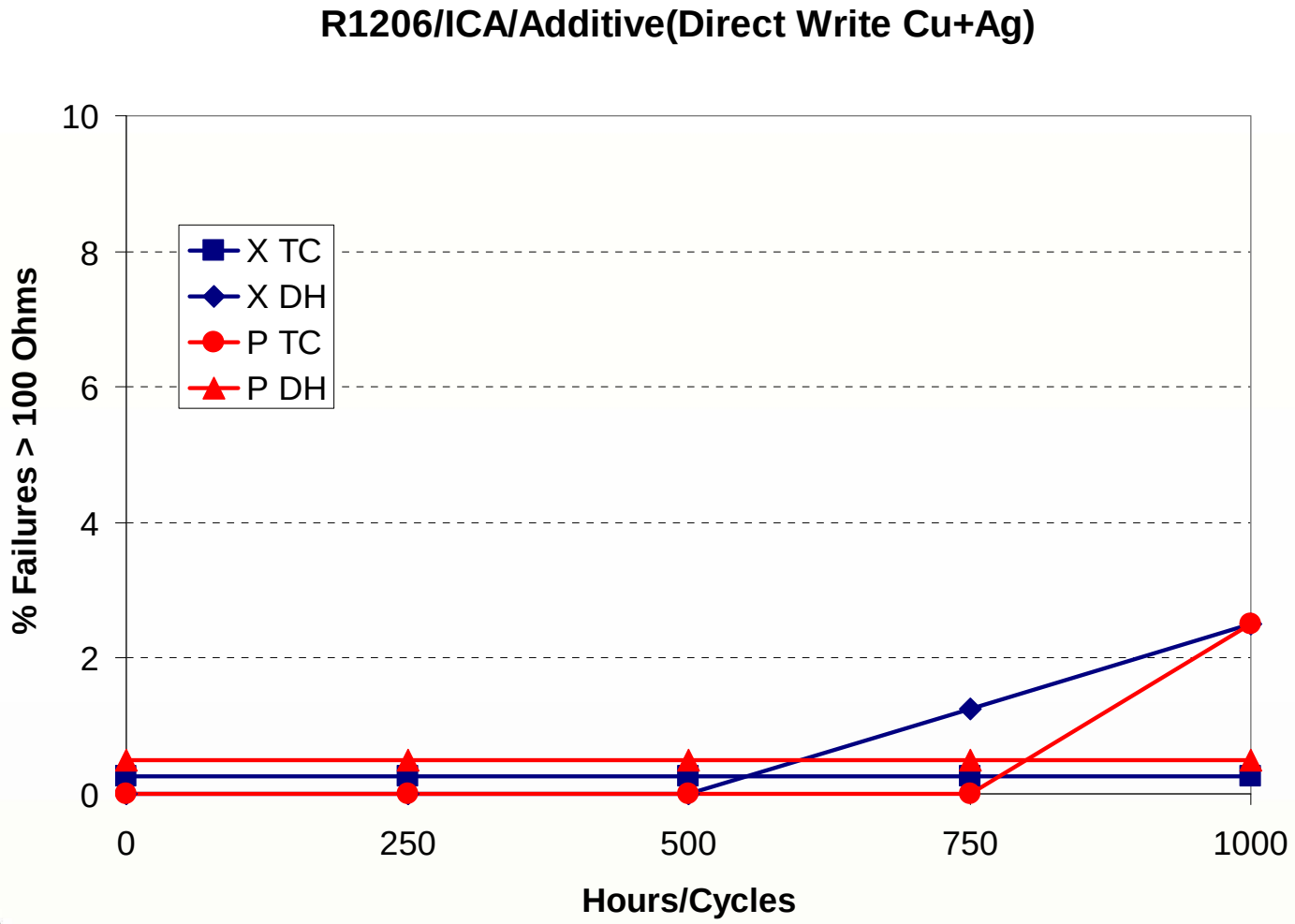




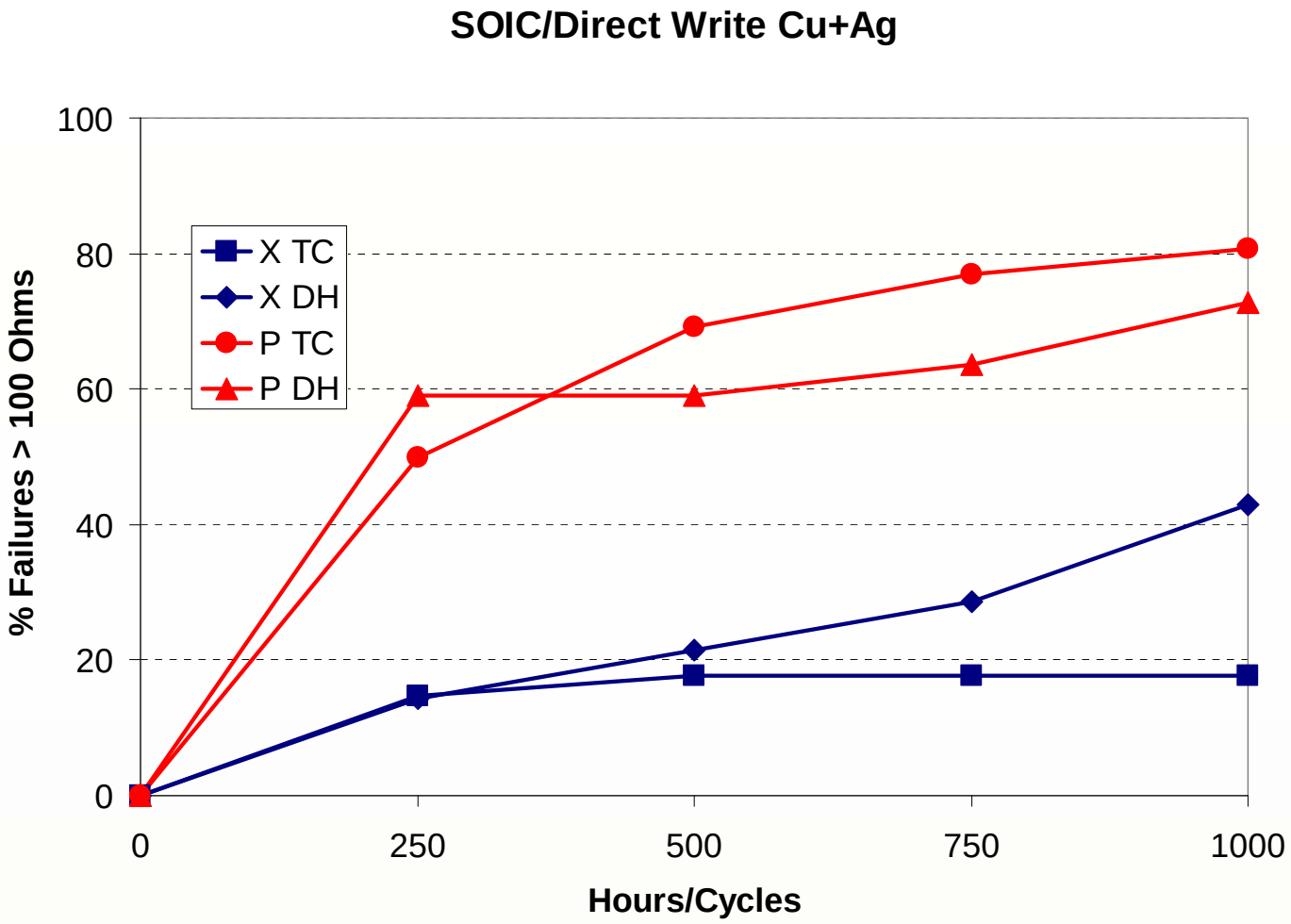
Reliability Testing

- Thermal cycling
  - Resistance testing during and after 1000 cycles –55 to 125°C
- Damp heat
  - Resistance testing during and after 1000 hours @ 85°C/85%RH

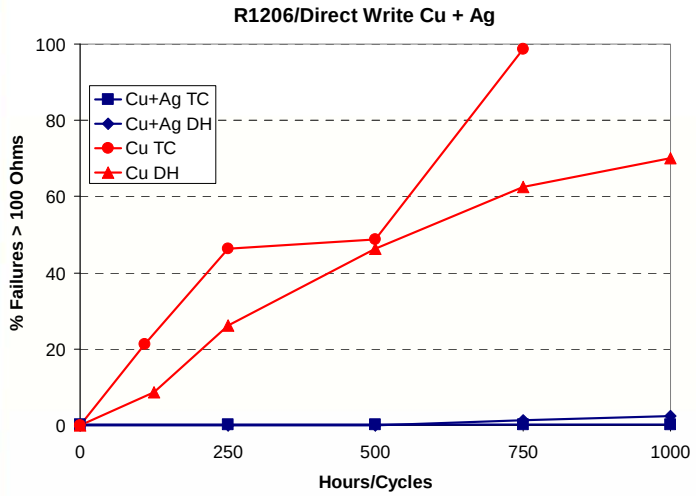
R1206 on DW Cu+Ag

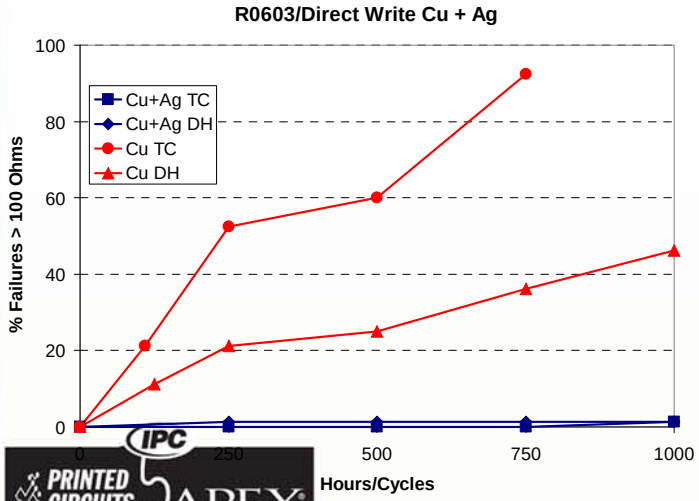


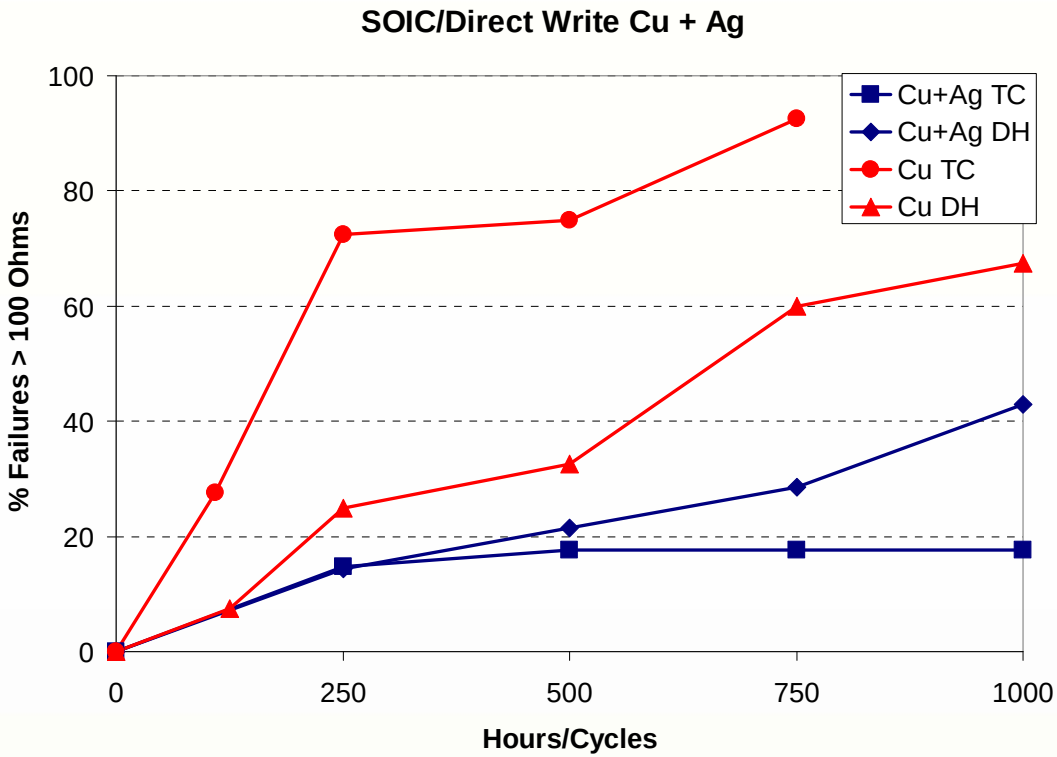
SOIC on DW Cu+Ag



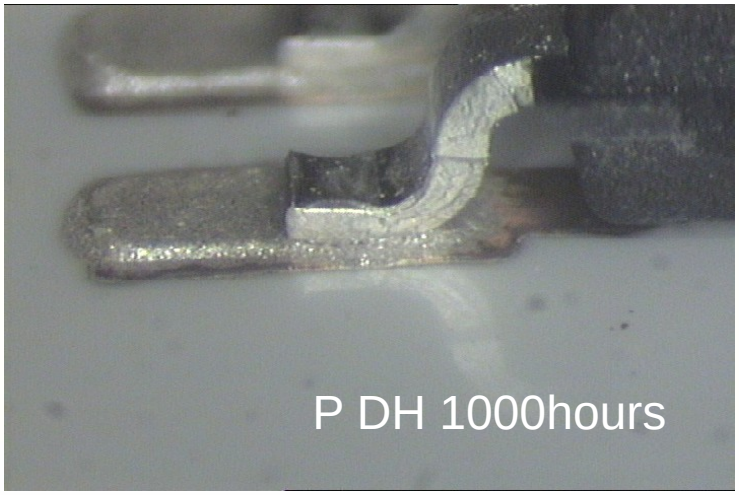
Comparison DW Cu and DW Cu+Ag

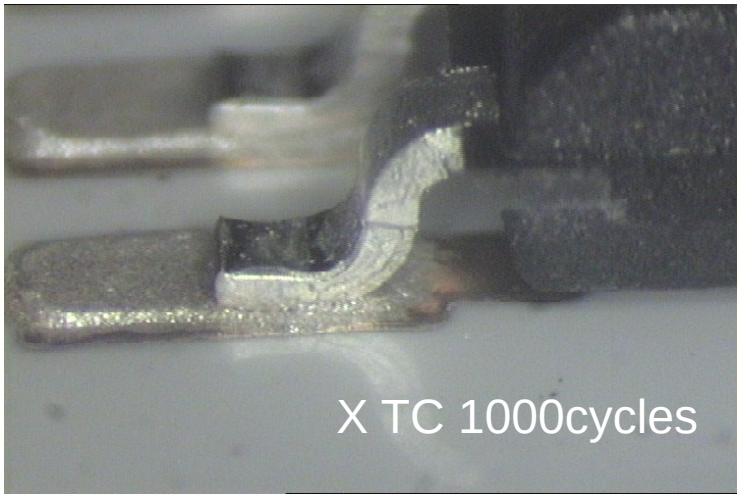


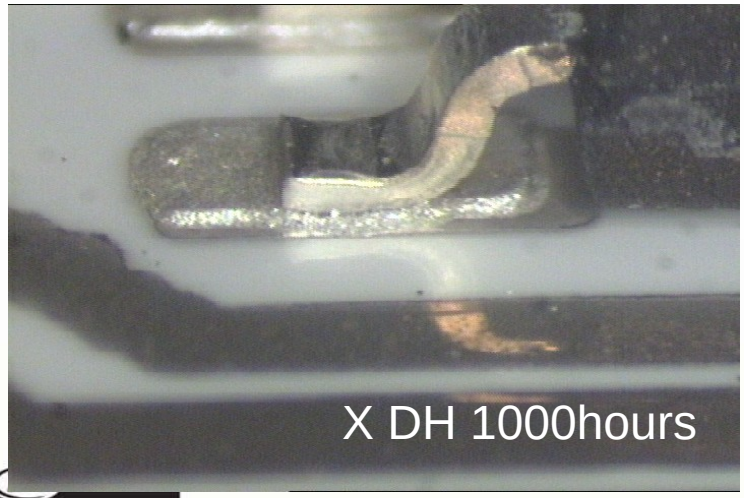




DW SOIC Joint Failures







DW Conclusions

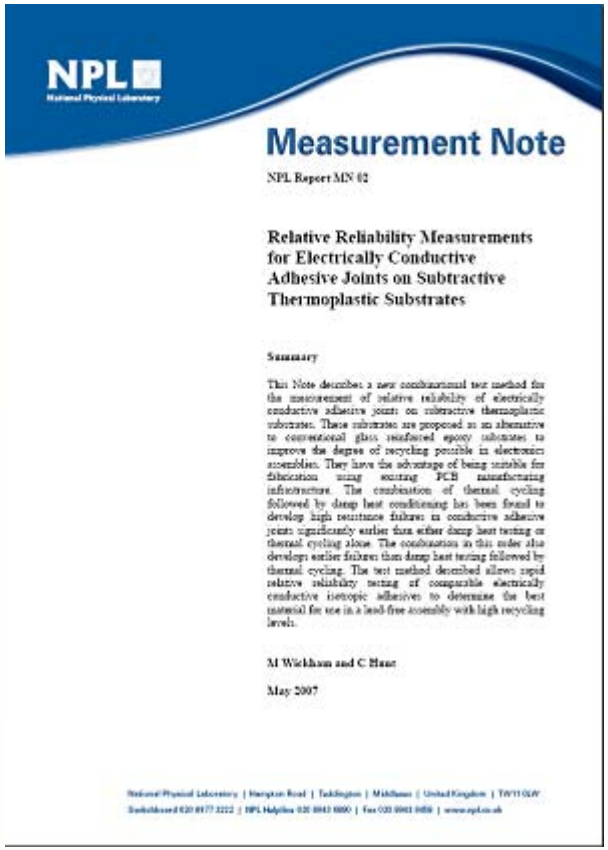
- Significant improvement in damp heat and and thermal cycling performance with immersion Ag
- Adhesive performance variations
- Failures occur at component/adhesive interface
- Insufficient failures at 1000 hours/cycles to distinguish between damp heat and thermal cycling

Conclusions

- New systems perform relatively well under harsh testing, performing beyond likely niche introduction areas.
- Major weakness is the deterioration in the conductive adhesive interconnect with the Sn finish

Measurement Note

- Relative reliability measurements for electrically conductive adhesive joints on subtractive thermoplastic substrates.
- Wickham, M, Hunt, C
- MN 2, May 2007, ISSN: 1754-3002
- Contact:
  - ling.zou@npl.couk


NPL
National Physical Laboratory

Measurement Note

NPL Report MN 02

Relative Reliability Measurements for Electrically Conductive Adhesive Joints on Subtractive Thermoplastic Substrates

Summary

This Note describes a new combinational test method for the measurement of relative reliability of electrically conductive adhesive joints on subtractive thermoplastic substrates. These substrates are proposed as an alternative to conventional glass reinforced epoxy substrates to improve the degree of recycling possible in electronics assemblies. They have the advantage of being suitable for fabrication using existing PCB manufacturing infrastructure. The combination of thermal cycling followed by damp heat conditioning has been found to develop high resistance failures in conductive adhesive joints significantly earlier than either damp heat testing or thermal cycling alone. The combination in this order also develops earlier failures than damp heat testing followed by thermal cycling. The test method described allows rapid relative reliability testing of comparable electrically conductive isotropic adhesives to determine the best material for use in a lead-free assembly with high recycling levels.

M Wickham and C Hunt

May 2007

Rigid Thermoplastic Substrate Report

- Preliminary measurements for thermoplastic electronics: developing a stress screening test.
- Wickham, M, Zou, L, Hunt, C
- MAT 6, November 2007
- ISSN: 1754-2979
- Contact:
  - ling.zou@npl.couk