Towards a PCB Production Floor Metric for Go/No Go Testing of Lossy High Speed Transmission Lines

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Introduction

As designers strive to extract ever more performance from high speed transmission lines on FR4 substrates and their high speed derivatives, a requirement has arisen for a practical and robust "Go / No Go" test technique for loss to be deployed on the PCB production floor. The intent of this paper is to propose that RIE (Root Impulse Energy) testing is a practical and achievable test method. It is easily deployed and offers repeatable, reliable discrimination between PCBs fabricated with a range of varying base material loss characteristics.

Until recently digital signals on PCB transmission lines operated at sub gigabit data rates. Consequently, losses were safely ignored while characteristic impedance was the major transmission factor. Today loss is a major consideration when pushing the limits of transmission lines on PCB boards. A board may be designed to take advantage of the transmission capabilities of a high specification dielectric, but an inadvertent substitution of an inferior specification core or prepreg during the manufacturing cycle, which may easily go unnoticed, could be fatal to the electrical performance of the system.

This test is designed to give fabricators a first indication of a change in loss characteristic on a given transmission line structure / layer stackup. This change in characteristic loss may be due to a number of factors including incorrect material used in a stackup. It may also be used in conjunction with other techniques (more suited to lab / QA use) to flag the need to escalate problem builds for more detailed laboratory analysis.

The RIE method has been presented in previous papers and presentations [1]. This paper looks at some of the more practical implementations of deploying this method in a conventional production environment. TDRs from two manufacturers were used for the acquisition of results in this paper.

RIE – Root Impulse Energy

The RIE method employs a modified version of the standard impedance test coupon, which contains a short reference line, and a longer test line. The RIE method compares the reflected TDR signal of the short trace with the longer sample, and by differentiating the resultant reflection and taking the root of the area under the resultant curve, calculates a measurement proportional to the high speed losses encountered on the structure [1].

PRACTICAL Considerations FOR THE IMPLEMENTATION OF RIE TESTING

Goals

An ideal RIE measurement system would

- Ensure robust and reliable contact
- Occupy minimal room on a production panel
- Generate repeatable measurements
- Use reliable instrumentation
- Be instrument manufacturer agnostic
- Be tolerant of local environmental conditions
- Produce measurements which are predictable
- Be suitable for High Volume Manufacturing (HVM) conditions
 - Cost effective equipment
 - Robust equipment
 - o Straightforward operation/analysis

Instrumentation

For practical purposes the robustness of a 250ps TDR is preferred on the PCB fabrication floor. A 250ps system, while still a sensitive RF measurement tool, is not as susceptible to ESD performance degradation as can be the case with faster risetime systems. In addition, at 250ps the influences of the probe coupon interconnect are not as critical as with higher speed systems. Overall, it presents a more repeatable and reproducible test solution in the current factory environment, compared to laboratory equipment with faster risetimes.

For the purpose of this study, instruments from two different vendors were used. TDR1 hardware has a reflected risetime of

250ps. TDR2 has a faster risetime, so the waveforms were mathematically filtered to simulate the results of using a 250ps risetime using software features embedded in that equipment.

Test BOARD DESIGN

A test board was designed to identify the answers to some practical problems.

- 1) Can RIE discern the difference in significant changes in Df (Dissipation Factor, aka Loss Tangent)?
- 2) How long must the RIE trace be in order to attain suitably precise RIE results?
- 3) Is an HVM-compatible probe footprint (2.54mm, or 0.1") adequate, or do we need a more precise micro-probe footprint?
- 4) If serpentine routing is necessary (to accommodate a lengthy trace), what is the minimum separation required between "legs" of the serpentine?
- 5) Is there a significant difference between microstrip and stripline?
- 6) Do vias have a significant effect?
- 7) What are the environmental (Relative Humidity, temperature) effects on loss measurements?

The following board (Figure 1 and Figure 2) was manufactured in several materials: - Isola IS410 (1080), IS410 (2116), IS408 and Nelco N4000-13. The board was designed to be \sim 2.34mm (0.092") thick to mimic thick server boards, in which via effects are worst.

Stackup

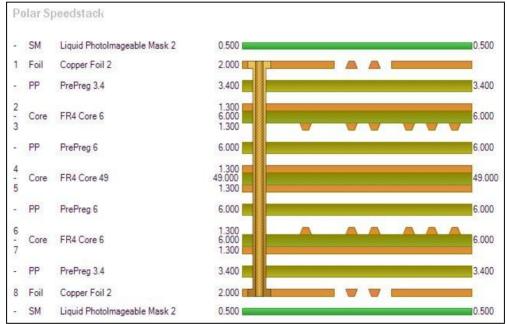


Figure 1 Test board stackup

Board layout

The test traces were placed at a slant of 10° (Figure 2) to avoid the trace running with the warp or weft of the material, thus minimizing the effect of dielectric variation sometimes caused by trace alignment with the fibre weave [3].

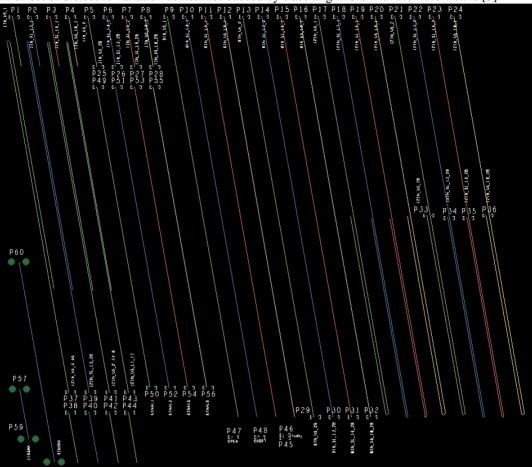


Figure 2 Test board layout

Different length traces were included on this board to see if reliable results could be obtained from shorter lengths. In addition, the 300mm (12") traces were folded back on themselves to try to eliminate the need for a large amount of linear board space.

Probe layout

A consistent interconnect to the coupon under test is key to achieving good R&R. For production use this has to be easy, repeatable and ideally, suited to both hand and automated test systems.

A "Back to Back" layout of coupon was investigated (Figure 3) so that both the long and short reference lines could be addressed in a single probing action if required.

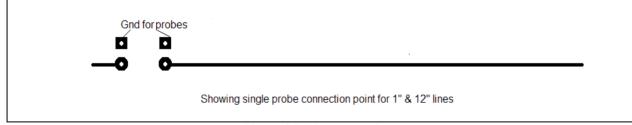
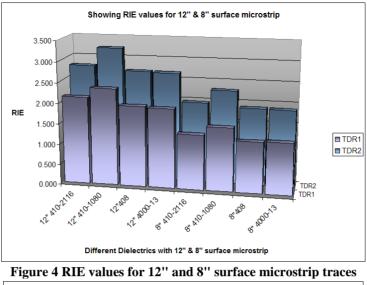


Figure 3 Probe connections

Results

Different length traces

In a production environment there is significant pressure to minimize board panel area consumed by coupons and other 'non productive artefacts'. To this end two coupon styles were evaluated. Both would have the 25mm(1") reference trace but the second trace would be 300mm(12") long in one case and 200mm(8") long in the other.



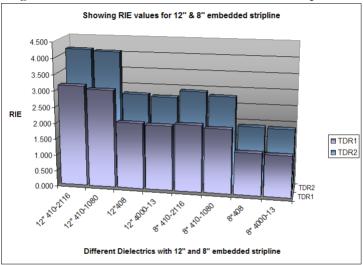


Figure 5 RIE values for 12" and 8" stripline traces

It is interesting that there is a significant difference in the magnitude of the returned RIE result between the two TDR systems used. Although there is a "block shift" in the data magnitude of TDR results, the underlying differences between materials are similar in both data sets. In previous studies using these same systems a much closer correlation was achieved. This magnitude difference needs further work to identify its cause.

From the above graphs (Figure 4 and Figure 5) it can be concluded that the data from the 200mm still allow a distinction between the higher specified dielectrics and the more lossy 410 material, but the difference between RIE values is smaller (as expected). A 200mm trace could be used for gross material differentiation, but a 300mm trace would be necessary for more subtle distinctions. The choice between the two may be based on availability of board space versus desired precision.

Switchback Results

In order to save on board space it would be convenient if the 200mm trace could be laid out in a manner such that it folded back on itself, thus occupying less linear space. The closest spacing, included on this board, between the two parallel lines of the switchback was 0.432mm (0.017"). This figure was calculated from a conventional rule of thumb to space aggressor traces (>5x height above the ground plane for microstrip, >3xh for stripline). The following TDR trace (Figure 6) shows clearly the unwanted effects of that folding, with the two halves of the traces running parallel.

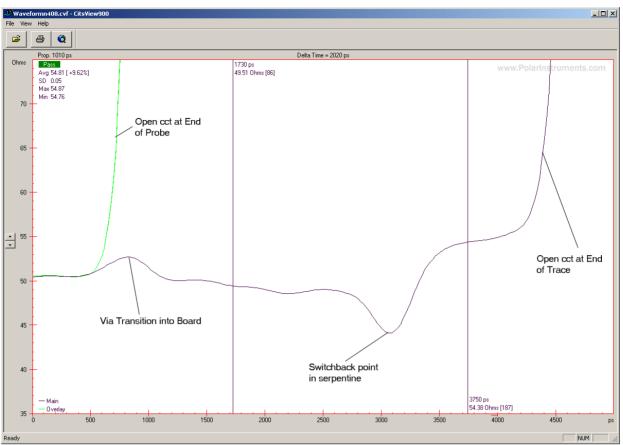


Figure 6 TDR trace showing the effects of switchback on the microstrip test trace

On the surface microstrip TDR trace shown in Figure 6, the switchback can clearly be seen as a large capacitive dip at 3200ps with the following portion of the trace raised by additional reflections and crosstalk.

Switchback effects could still be seen with a spacing of 1.42mm (0.056"). From these practical results in would seem that any surface microstrip trace, laid out to include a switchback, would have to have the trace separation in excess of this value. As expected, the embedded stripline trace with a separation of 0.889mm (0.035") shows no sign of coupling or erroneous reflections because FEXT effects are minimal. Corners will always have a subtle effect, but at these frequencies, the stripline trace could be laid out in either a linear or switchback fashion.

Via effects

Some traces were manufactured with an entry pad and via at one end of the trace only, mimicking expected production coupons. Other traces included a contact pad and via at both ends allowing investigation using TDT and VNA techniques. The following graphs (Figure 7 and Figure 8) show that the vias as manufactured on this board have no significant effect on the RIE result at these frequencies.

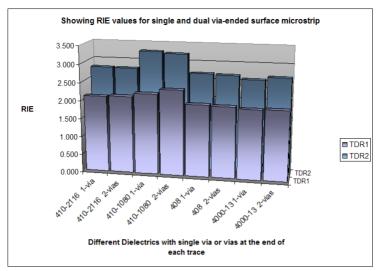


Figure 7 RIE values for single and dual-via ended surface microstrip traces

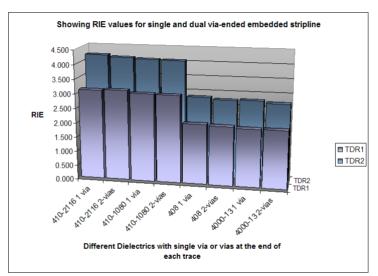


Figure 8 RIE values for single and dual-via ended stripline traces

Probes/R&R

Using repeated measurements taken by three appraisers the R&R of two probing scenarios were investigated. In the first case the short reference trace and the longer trace were measured in two separate probing actions. In the second case a specially configured probe was used to capture the data from both of the traces in one probing action.

Table 1 Variations in RIE values				
	Surface microstrip	Embedded stripline	Dual-probe surface	
	(2 separate contacts)	(2 separate contacts)	microstrip	
			(1 contact action)	
Repeatability - equipment variation (EV)	0.241	0.124	0.115	
Reproducibility - appraiser variation (AV)	0.079	0.027	0.107	
Repeatability & reproducibility (R&R)	0.253	0.127	0.157	
Part variation (PV) - (actual variation of samples)	0.148	0.094	n/a (*1)	
Total variation (TV)	0.293	0.157	n/a (*2)	

*1: Multiple parts containing these particular structures were not available; thus, this test could not be conducted. The results are expected to be similar to those for Surface microstrip with 2 separate contacts.

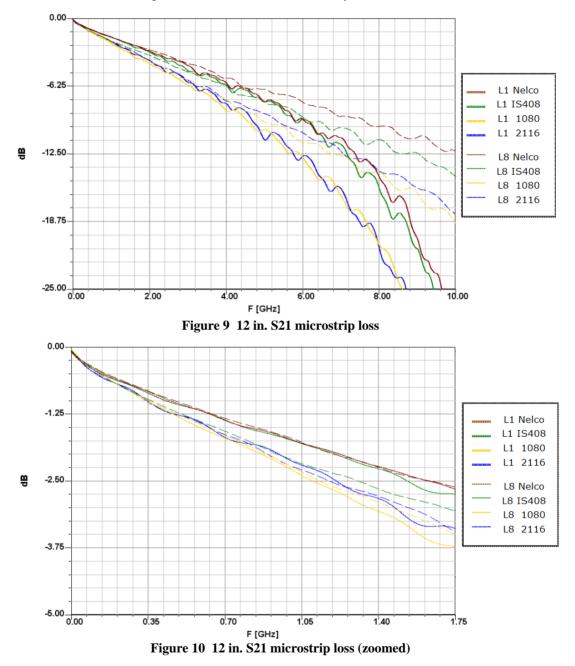
*2: Total variation cannot be calculated in the absence of PV for this case, but can be expected to be significantly less than that for Surface microstrip with two separate contacts, given the smaller values for 2 of the 3 constituent elements.

The figures in Table 1 show the calculated variations in RIE due to different contributing factors. It was found that a better R&R was achieved by using a single probing action over addressing the coupon twice. There are also obvious test time and error benefits to be made in the test / production environment.

In addition, stripline results show far less part variation than those of surface microstrip.

VNA correlation

The loss of the 300mm (12") traces (Figures 9, 10, 11, 12) was measured by VNA.



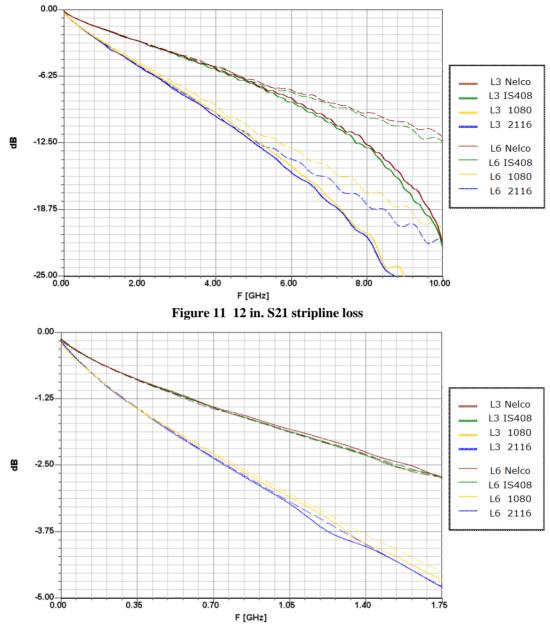


Figure 12 12 in. S21 stripline loss (zoomed)

In both the stripline and microstrip through (S21) loss, two distinct groups of curves are seen that represent the different material types. The Nelco 4000-13-SI and the IS408 materials are characterized with a lower loss relative to the IS410 (1080) and the IS410 (2116). An exception to this grouping is seen for layer 8 of the IS408 material. This layer of this particular material appears, in Figure 10, to have similar loss characteristics to lower loss materials below 1.1 GHz. This effect needs further exploration; however, the RIE ratio is in agreement with the VNA findings.

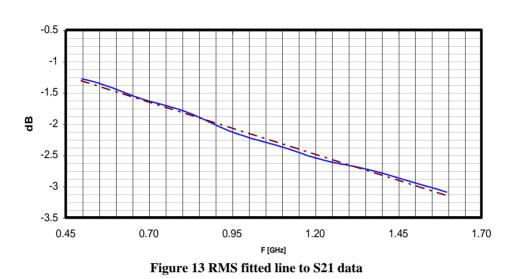
The S21 measurements also demonstrate a greater reliability in the stripline manufacturing process represented in the above graphs as tighter curves groupings for layers 3 and 6 (striplines). Layers 1 and 8 (microstrips) exhibit a greater impedance target variation seen in the undulations of the S21 measurements.

Contrary to expectations, the inner layer loss characterizations for the IS410 (2116) is greater than the IS410 (1080). The microstrip layers do not show a greater loss characterization for the IS410 (1080) because of the impedance mismatch induced undulations of the measurements. It is important that the impedance mismatches be limited to insure accurate S21 measurements.

The above results from the VNA measurements were also indicated in the RIE values.

Table 2 contains direct correlation between the VNA measurements and the computed RIE values. An RMS line was fitted to the S21 measurements between 0.5GHz and 1.6GHz, shown in Figure 13[2], to counteract the impedance mismatches. A single frequency point of 1.4GHz from this fitted line was chosen for correlation. The value was determined using the equation 0.35/250ps.

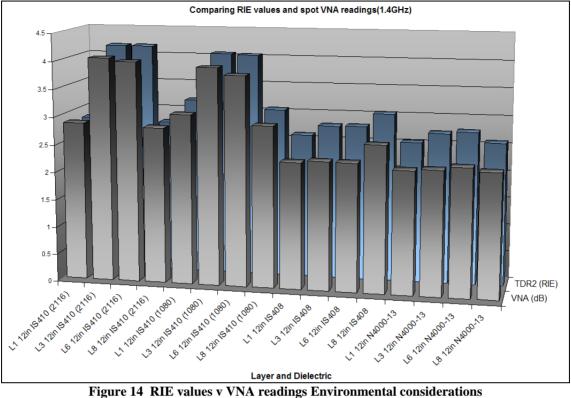
S21



Trace/material RIE (TDR2) VNA L1 12in IS410 (2116) 2.869 2.82 L3 12in IS410 (2116) 4.18 4.052 L6 12in IS410 (2116) 4.18 3.995 L8 12in IS410 (2116) 2.78 2.823 L1 12in IS410 (1080) 3.2 3.074 L3 12in IS410 (1080) 4.07 3.924 L6 12in IS410 (1080) 4.05 3.798 L8 12in IS410 (1080) 3.07 2.923 L1 12in IS408 2.62 2.290 L3 12in IS408 2.8 2.325 L6 12in IS408 2.81 2.318 L8 12in IS408 3.05 2.655 L1 12in N4000-13 2.55 2.223 L3 12in N4000-13 2.73 2.252 L6 12in N4000-13 2.77 2.313 L8 12in N4000-13 2.59 2.246

Table 2 RIE v VNA

The results recorded in Table 2 and shown below (Figure 14) show a high degree of correlation between the loss measurement from the VNA and TDR2.



FR4 is fundamentally hygroscopic (i.e. absorbs moisture from the environment). Inevitably this means that different conditions around the world will alter the loss properties exhibited by transmission lines as differing amounts of water are taken into the dielectric. As expected, the RIE measurement on the surface microstrip agrees with this. When the boards are subjected to different environmental conditions, the effect can be seen. Results were obtained using TDR1 only.

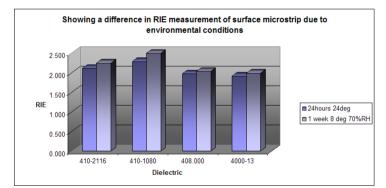


Figure 15 Variations in RIE due to environmental conditions (surface microstrip)

The RIE results from the embedded microstrip (Figure 16) show that this structure is less susceptible to immediate changes of humidity than the surface microstrip (Figure 15).

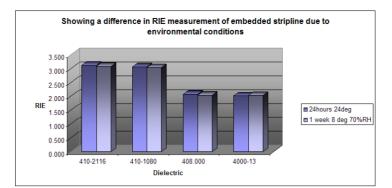


Figure 16 Variations in RIE due to environmental conditions (stripline)

Discussion

When testing the characteristic impedance of PCB traces, designers and fabricators have often taken an informal approach to impedance coupon design. The effect of this has been that perhaps not as much attention was paid to the launch characteristic of the test probe / coupon interface as would be desirable. Launch of the test signal into a coupon for trace loss measurement takes on a more critical aspect, with a much higher chance of inaccurate or misleading measurements if the coupon design is not fully considered along with the test probe interconnect.

This paper proposes that where possible a standard approach to coupon design should be adopted – especially where product is being sourced from multiple vendors. Good progress has been made in defining a candidate layout for this standard. A dual-line probe using the "back to back" pin layout improves R&R. These results show that the RIE figures for the embedded stripline structure have the greatest differentiation between materials. It is also known that inner layer traces can be manufactured more reliably and precisely, so a more consistent test structure can be created.

Currently most manufacturing PCB transmission line testing is done at frequencies and geometries where the environment causes little variation. Ideally, localised RH should only minimally affect the proposed production floor metric.

Previously suggestions have included baking of boards prior to testing and / or soaking of boards in a controlled RH environment. We believe that in a production environment these options may prove uneconomic due to additional process time rendering them suitable only for batch testing. Inner layer traces are far less responsive to immediate changes of environment, so are more suitable for this testing.

It is important to realize that the test methodology outlined in this paper is aimed at material validation and fabrication, not validation of the design, validation of the design should have been done elsewhere.

From the above it may be concluded that the best structure for material validation will be a stripline structure – even if this is not representative of the structures used on the board.

Although the absolute RIE numbers are different when obtained by different TDRs, with the corresponding methods of filtering, the RIE numbers show the same relationship and identify similar trends. These numbers also show a similar relationship to the loss figures measured by VNA. The difference in RIE figure implies that a measurement taken with one TDR under certain conditions cannot currently be directly compared to another instrument or location around the world without reference to an independent loss standard.

Provision of a uniform loss standard is key to the successful adoption of a test metric where worldwide correlation and acceptance of measurements have to be made. Such is the case in the impedance world where air conductor co-axial transmission lines (airlines) are universally accepted as such a standard.

Conclusion And Recommendations

RIE with a 250ps reflected risetime appears suitable for discerning significant differences in material loss properties, provided:

- Proper coupon design is incorporated into the panel design.
 - Traces must be at least 200mm (8") long, and 300mm (12") length is desired for higher precision.
 - \circ Serpentine routing must have adequate spacing between legs of the serpentine
 - o Vias are acceptable; back-drilling (or similar mitigation technique) is not required

• The frequencies of interest are limited to 1.4GHz or a limit commensurate with high reliability and repeatability.

For material differentiation stripline gives better results than microstrip, thus it is suggested that an embedded stripline coupon be employed as the test vehicle even if this structure does not represent those used on the board.

This recommendation requires a conceptual shift from conventional impedance testing where the test trace is designed to be a typical board trace.

The RIE test proposed here does not replace conventional impedance control techniques that are currently in use.

A suitable standard for loss and cross test equipment calibration is key and will need to be established, before this new measurement technique can gain widespread trust throughout the industry.

References

[1] R. Mellitz, T. Ballou, S. G. Pytel, "Low Cost Energy Based TDR Loss Method for PWB Manufacturers," presented at IPC Works 2005 in the D-24b Committee Meeting, Las Vegas, NV, 2005.

[2] IPC Test Methods, IPC-TM-650 2.5.5.12 rev 0.5, Nov. 2007.

[3] Jeff Loyer, Richard Kunze and Xiaoning Ye, "Fiber Weave Effect: Practical Impact Analysis and Mitigation Strategies", Proceedings of DesignCon 2007.

- [4] Wadell, Brian C. Transmission Line Design Handbook, Artech House, 1991
- [5] Si9000e PCB Transmission Line Design System, www.polarinstruments.com, 2005
- [6] Bogatin, Eric Signal Integrity Simplified, Prentice Hall, 2004
- [7] Johnson, Howard & Graham, Martin High-Speed Signal Propagation, Prentice Hall, 2003
- [8] Staniforth, J.Alan, Gaudion, Martyn, "Impedance Modelling on Multiple Dielectric Builds", 2004

RIE – Root Impulse Energy

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Why RIE?

- High data rates create need for simple loss test
 for volume production environment
- VNA requires expertise to set up very sensitive to interconnect
- RIE test easily deployed offers reliable discrimination of PCB base materials with different loss characteristics



RIE – Root Impulse Energy

- Employs test boards with short reference line and longer test line
- Compares reflected TDR signals of the two traces
- Produces a measurement proportional to the structure's high speed loss



RIE goals

- The ideal RIE measurement system:
 - Produces repeatable measurements which correlate to known standards
 - Is suitable for High Volume Manufacturing (HVM) conditions:
 - Cost effective equipment
 - Robust equipment
 - Straightforward operation/analysis
 - Fast, robust, and reliable contact, similar to existing ones
 - Occupies minimal room on a production panel
 - Takes local environmental conditions into account

Suggested Instrumentation

- Suggested instrument 250ps TDR:
 - Less susceptible to ESD degradation than faster risetime TDRs
 - Probe coupon interconnect influences less critical than with higher speed systems
 - Offers a more repeatable and reproducible test solution in a factory environment than faster risetime laboratory equipment



Test Board Study Instrumentation

- Two TDRs used:
 - TDR1 with reflected risetime of 250ps and hand held probes
 - TDR2 with unfiltered risetime and microprobes



Test board design

- Practical problems/questions:
 - Can RIE detect significant changes in Dissipation Factor (Loss tangent)?
 - How long does the RIE trace need to be?
 - Is an HVM compatible probe footprint (2.54mm/0.1") adequate – or is a more precise micro-probe footprint necessary?



Test board design

- Practical problems/questions:
 - Minimum separation between serpentine legs on long traces?
 - Differences between microstrip and stripline?
 - Do vias have a significant effect?
 - Environmental effects on loss measurement?

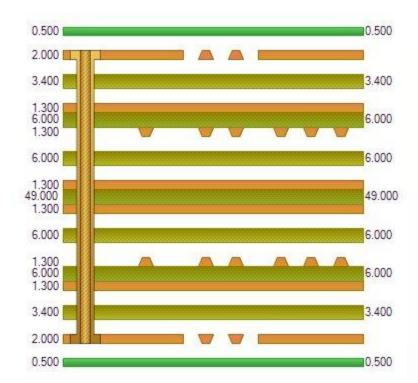


Test board design

- Board materials:
 - Isola IS410 (1080) → tanδ ~ 0.026
 - Isola IS410 (2116) → tanδ ~ 0.021
 - Isola IS408 → tanδ ~ 0.012
 - Nelco N4000-13 → tanδ ~ 0.008
- Board thickness:
 - 2.34mm (0.092in) (to mimic thick server boards where via effects are worst)

Test board stackup – 2D

-	SM	Liquid Photolmageable Mask 2
1	Foil	Copper Foil 2
-	PP	PrePreg 3.4
2-3	Core	FR4 Core 6
•	PP	PrePreg 6
4	Core	FR4 Core 49
2	PP	PrePreg 6
6 - 7	Core	FR4 Core 6
-	PP	PrePreg 3.4
8	Foil	Copper Foil 2
-	SM	Liquid Photolmageable Mask 2





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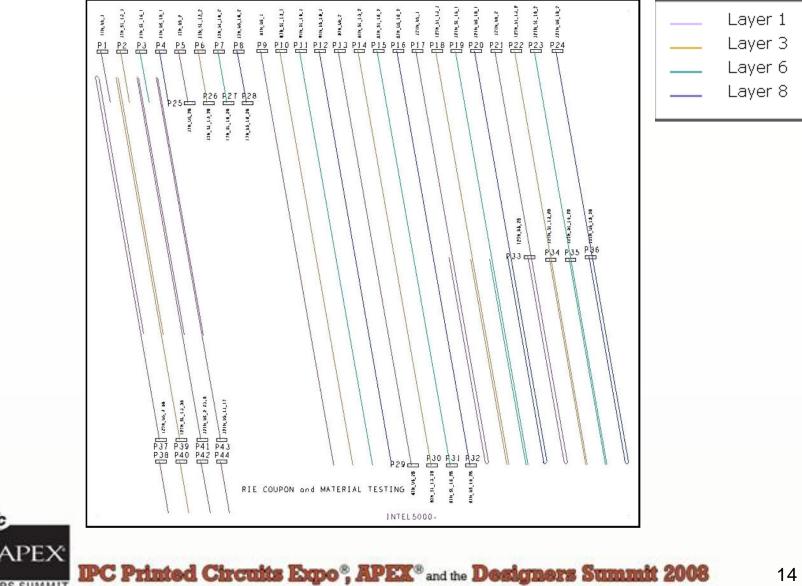
Test board layout

- Board design:
 - Test traces placed at slant of 10° to avoid running with warp and weft of material
 - Different length traces used to test for reliable results from shorter lengths
 - 12" (300mm) traces folded back to reduce linear board space



13

Test board layout



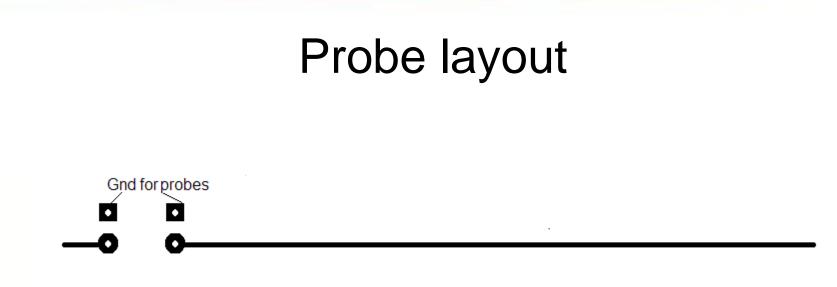
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Probe layout

- Consistent interconnect is key to achieving good R&R
- For production, must be easy, repeatable and suitable for hand and automated test





Showing single probe connection point for 1" & 12" lines

Back to back coupon layout – allows addressing long and short reference lines in a single probing action



Results

- Pressure in a production environment to minimize test coupon area, so...
 - Two coupon styles evaluated
 - 1" (25mm) reference trace 12" (300mm) test trace
 - 1" (25mm) reference trace 8" (200mm) test trace



Results

- 8" (200mm) traces allow gross distinction between materials
- 12" (300mm) traces necessary for finer distinction of materials
- Trade-off between board space availability and required precision

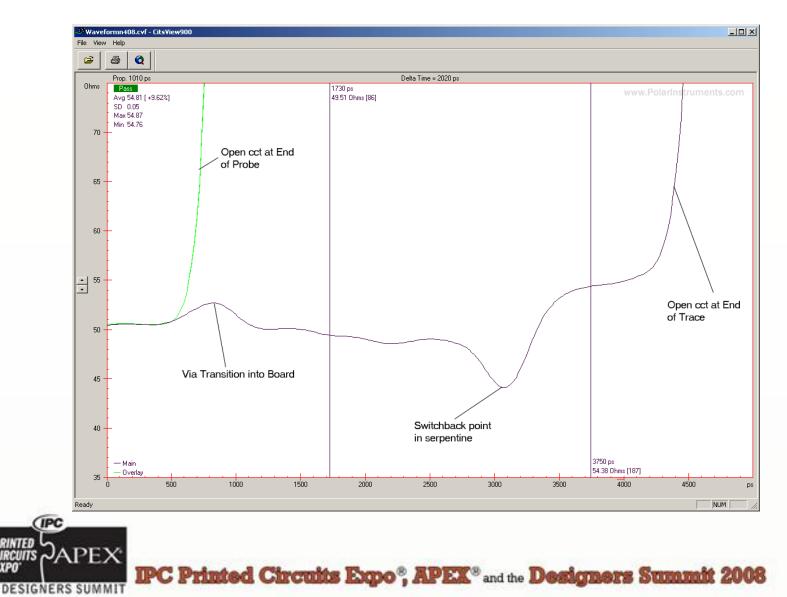


RIE values – switchback effects

- 12" (300mm) test traces folded to reduce linear board space
- TDR waveform shows unwanted effects of folding on surface microstrip – capacitive dip at 3200ps followed by a plateau of forward crosstalk
- Need to ensure minimum spacing on surface microstrip between trace and folded back portion

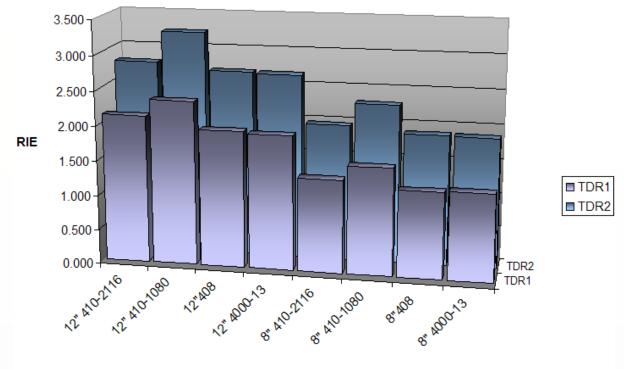


TDR trace – surface microstrip



and the

RIE values – 12" & 8" surface microstrip

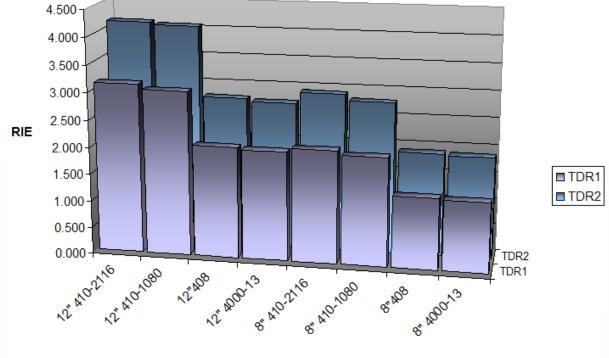


Different Dielectrics with 12" & 8" surface microstrip



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RIE values – 12" & 8" embedded stripline



Different Dielectrics with 12" and 8" embedded stripline

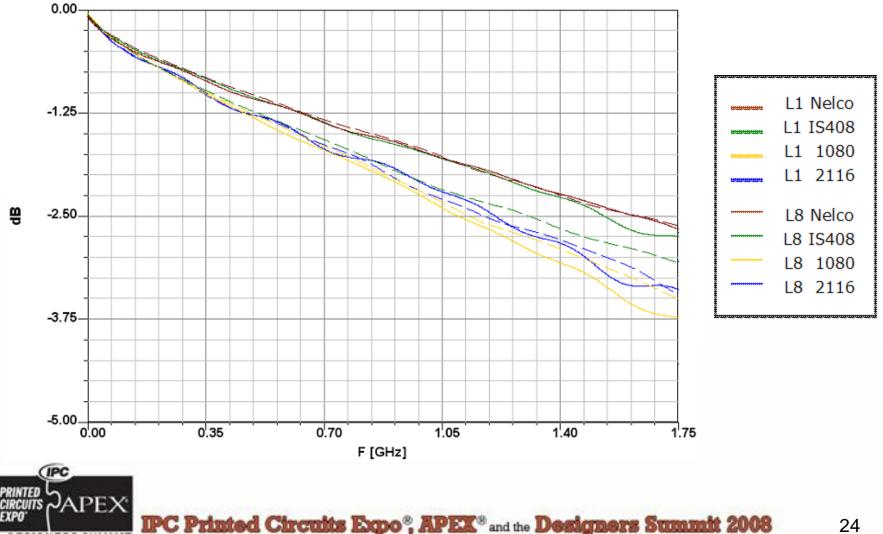


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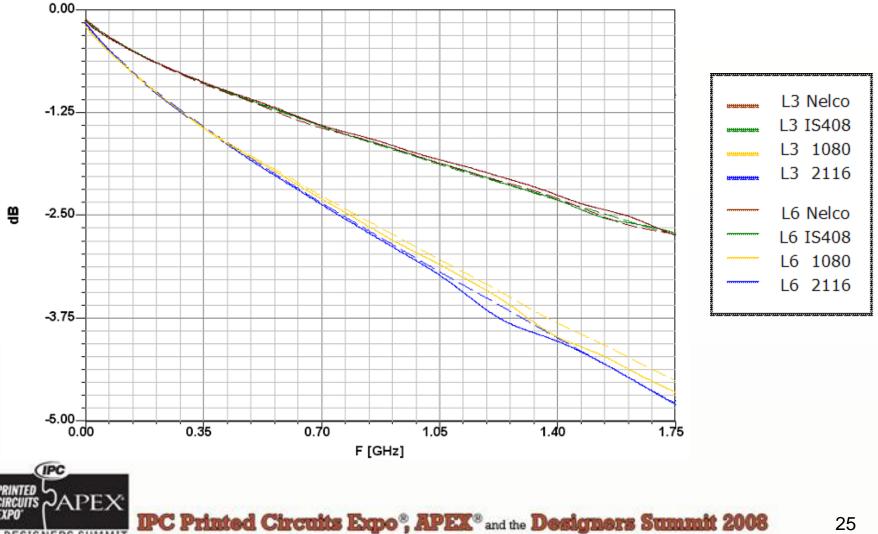
VNA correlation – 12" S21 trace losses

- Material types clearly distinguished by two distinct S21 curves in both microstrip and stripline
- Tighter groupings in S21 L3 & L6 (stripline) curves imply greater reliability in manufacturing process
- Inner layer losses for IS410 (2116) greater than those for IS410 (1080)
- Anomaly on L8 of IS408 confirmed with VNA
- VNA results also indicated in RIE values

VNA correlation – 12" S21 microstrip loss (zoomed)



VNA correlation – 12" S21 stripline loss (zoomed)

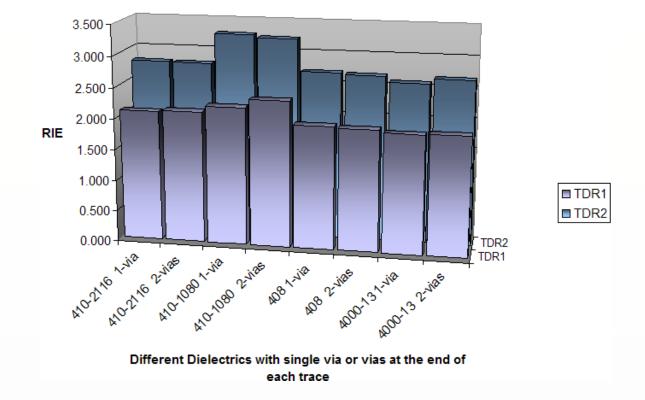


RIE values – via effects

- Two via/entry pad configurations:
 - Via/entry pad one end of trace to simulate production coupons
 - Contact pad/via both ends of trace to allow TDT and VNA techniques
- Vias show no significant effect on RIE results at test frequencies used

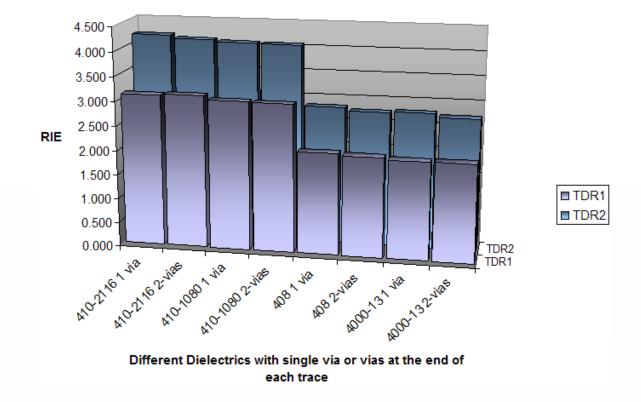


RIE values – single & dual via-ended surface microstrip





RIE values – single & dual via-ended stripline



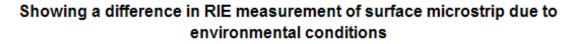


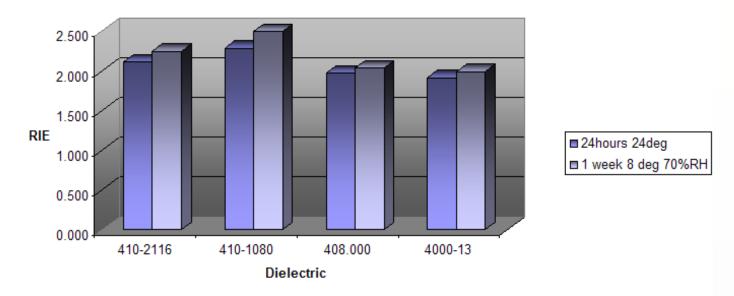
Environmental considerations

- FR4 fundamentally hydroscopic
- Loss properties will therefore vary with quantities of moisture absorbed by dielectric
- RIE measurements on surface microstrip reflect environmental conditions (results from TDR1 only)
- Results from embedded stripline show inner layers less susceptible to immediate changes in humidity



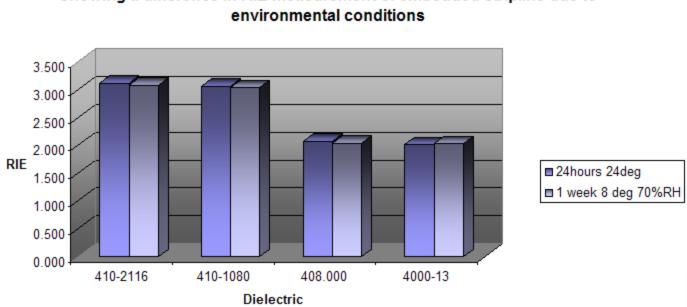
Environmental variations in RIE – surface microstrip







Environmental variations in RIE – stripline



Showing a difference in RIE measurement of embedded stripline due to



Discussion

- Test probe interconnect/coupon design critical requires standard approach to accommodate multiple vendors
- RIE figures for embedded stripline show greatest differentiation between materials
- Close control of production environment uneconomical so testing using stripline only
- RIE numbers correlate to loss figures obtained via VNA
- Uniform loss standard is key to adoption of test metric for worldwide correlation and acceptance

Conclusions/recommendations

- RIE with 250ps reflected risetime is suitable for discerning significant differences in material loss properties provided:
 - Proper coupon design incorporated into panel design:
 - Traces must be at least 8" (200mm) long
 - Traces should be 12" (300mm) for higher precision
 - Serpentine routing requires adequate spacing between traces
 - Vias are acceptable: back drilling (or similar mitigation) is not required
 - Frequency of interest is 1.4GHz, or relative total loss does not change for greater frequencies



Conclusions/recommendations

- Stripline coupon yields better material differentiation than microstrip
- RIE test proposed does not replace currently used conventional impedance testing
- A suitable standard for loss and cross test equipment calibration is key – must be established before RIE testing can gain widespread trust throughout the industry





Questions?



IPC Printed Circuits Expo[®], APEX[®] and the Designers Summit 2008

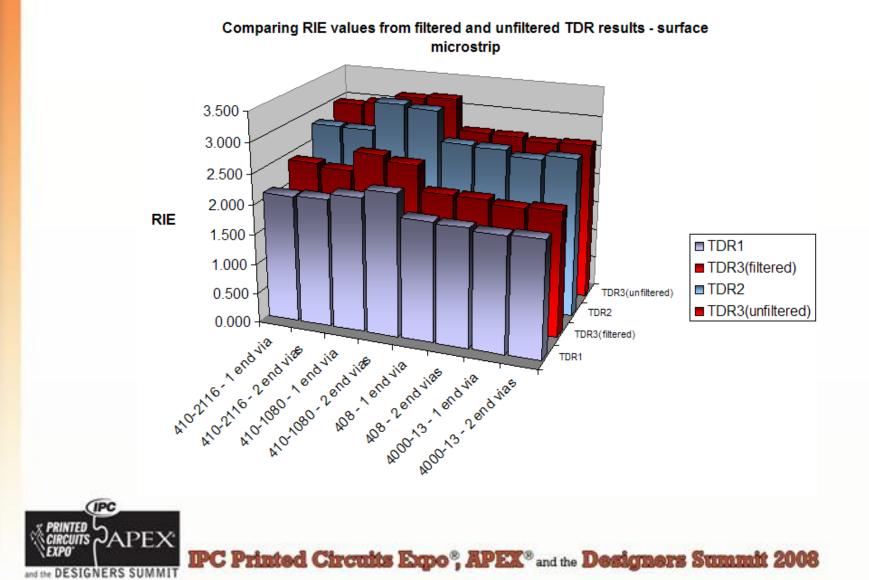


Additional information

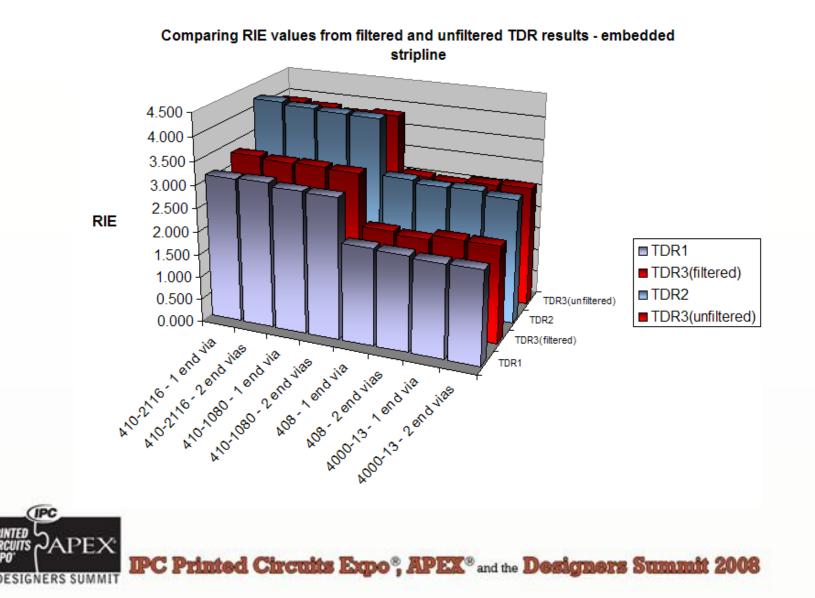


PC Printed Circuits Eqpo[®], APEX[®] and the Designers Summit 2008

RIE values - filtered and unfiltered TDR results



RIE values - filtered and unfiltered TDR results



RIE values and spot VNA readings

Comparing RIE values and spot VNA readings(1.4GHz)

