Manufacture and Performance of a Z-interconnect HDI Circuit Card

Michael Rowlands, Rabindra Das, John Lauffer, Voya Markovich
EI (Endicott Interconnect Technologies)
1093 Clark Street, Endicott, NY 13760
Michael.rowlands@eitny.com,
607.755.5143 Fax 755.6151

Abstract

More and more circuit board designs require signals paths that can handle multi-gigahertz frequencies. The challenges for organic circuit boards, in meeting these electrical requirements, include using high-speed, low-loss materials, manufacturing precise structures and making a reliable finished product. A new circuit board HDI technology, using Z-interconnect, is presented that addresses these challenges. The Z-interconnect technology involves building mini-circuit boards of 3 or 4 layers each, then assembling several thin circuit boards together to make the finished product. Designing and manufacturing the thin circuit boards separately, then assembling them together, makes it possible to reliably manufacture circuit boards with no via stubs, very low-loss materials, nearly arbitrary transmission line structures and a lot of flexibility in tuning features to reduce signal loss. In the present paper, we have designed and built a circuit board test vehicle (TV) to make new RF structures, using Z-axis interconnection (Z-interconnect) building blocks. A typical 50-ohm stripline was designed with a ground-signal-ground structure. The stack-up had 23 metal layers, including 5 0S1P joining cores and 6 2S1P signals cores. Teflon-based Taconic materials TPG30 and TLG30 were used for the dielectric layers. Laminated conducting joints show low resistance in the range of 1 milliohm for a 0.3mm diameter, 250um length joint. Electrically, S-parameter measurements showed very low loss at multi-gigahertz frequencies. The losses were low enough to support typical SERDES links up to 15 Gbps over 30" net length. This effort is an integrated approach on three fronts: materials development and characterization, fabrication, and design and electrical characterization at the board level.

Introduction

Many new designs require multi-GHz signals, dense wiring due to high I/O count, and both wide lines for RF or high-speed digital signals and narrower lines for digital signals [1-3]. With standard circuit board stack-ups it is difficult to satisfy all those constraints at once. Most existing organic circuit board technologies create via stubs which can only be avoided with restrictive design rules, and do not have the flexibility to build arbitrary transmission-line structures. A Z-axis interconnect technology (Z-interconnect) stack-up is developed to solidly satisfy all the constraints. Using Z-interconnect, via stubs can be eliminated and all of the signal requirements can be satisfied [4-7]. Z-interconnect involves building thin circuit boards of 3 or 4 layers each, then assembling several thin circuit boards together to make the finished product. It is used to connect PCB metal layers vertically, using a conductive paste. Designing and manufacturing the thin circuit boards separately makes it possible to reliably manufacture circuit boards with no via stubs, very low-loss materials, nearly arbitrary transmission line structures and a lot of flexibility in tuning features to reduce signal loss.

Currently there are a number of choices for a core plus build-up circuit board that satisfy multi-gigabit data rates. [1, 5] The core plus build-up construction allows good performance and wireability in the build-up layers, but at a cost of less flexibility in the core layers. For instance, the core layers typically have a restrictive minimum via pitch, must be mostly a copper plane, and cannot have large clearances in them.

In the present paper, a new design is shown that uses Z-interconnect building blocks to make multi-GHz structures. New stack-ups are developed using Teflon-based Taconic materials which achieve the main features that a multi-GHz circuit board needs:

- Low-loss signal path
- Small, medium, large width, controlled-impedance lines
- Embedded passive components, discrete resistors and capacitors, plus capacitance layers
- Delay matching
- Islands in all plane layers, can be either power or ground
- Narrow lines for digital and low-frequency signals
- Arbitrary stack-up, symmetric or not, all layers have ground and signal regions
- Large, arbitrary-shaped clearances in planes
- Lightweight, thin

The work involved optimizing dielectric and conducting adhesive materials for the structures and includes embedded resistors. The various requirements lead to development in three main areas: (1) materials optimization; (2) fabrication, and (3) electrical performance.

Z-interconnect construction

Electrically, in circuit boards, there is always a need for circuit boards that can handle a diverse range of signal types. Focusing resources, such as area on the circuit board and expensive materials, where needed maximizes performance versus cost. The fastest signals get the widest lines and well-controlled impedance. The slower signals have narrower lines while still controlling impedance. Digital signals are just wide enough to carry their data and are squeezed as close as possible without violating crosstalk specifications. Low frequency interface signals (MHz) are very narrow and fit in around the critical signals. Power and DC nets are put in last. A Z-interconnect stack-up gives a design engineer quite a bit of flexibility to place wide signals, narrow signals and grounds and clearances only where needed. [7] The result is sketched below in **Figure 1**.

Red = RF or Gbps digital signals **Purple = digital**

Brown = all other signals **Gray = Z-interconnect joint**

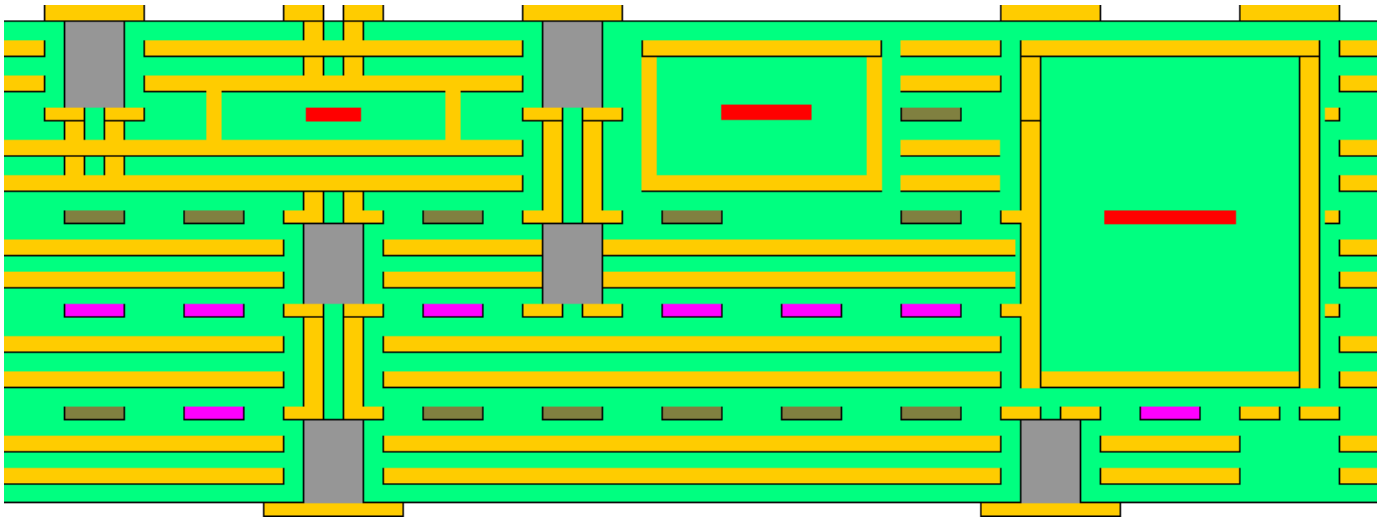
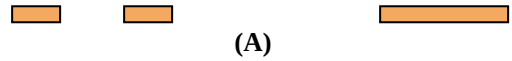
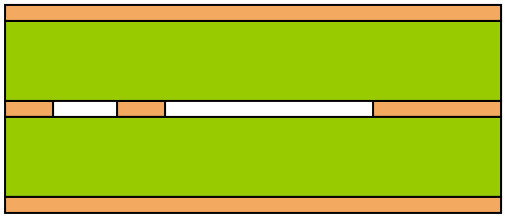


Figure 1 Versatile, Arbitrary Stack-up

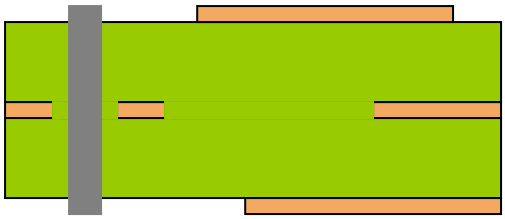
The method used to build a Z-interconnect structure includes a series of building blocks called cores. The main building blocks are a single plane core (0S1P) and a signal-plane-signal core (2S1P). The joining core is the name given to the 0S1P building block because it has a conductive, adhesive paste which allows it to attach to other cores. Manfacturing the joining core involves three main steps. It starts with a layer of copper, and then shapes are etched into the copper. A layer of dielectric and copper is stuck to both sides of the etched plane. Holes are then drilled all the way through the structure. Lastly, the hole is filled with paste and the outer copper is etched away, yielding a 0S1P joining core **(C)**. These steps are sketched below.



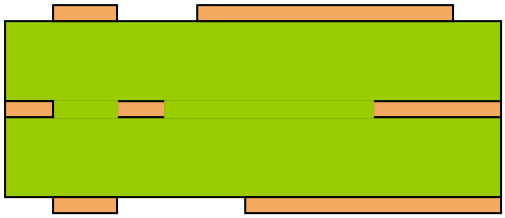
(A)



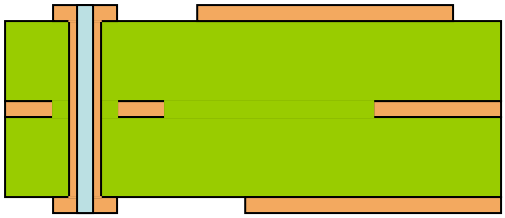
(B)



(C)



(D)



(E)

Figure 2 Fabrication of joining and signal cores (A) Etch 1P core; (B) Drill laminated 1P core; (C) Paste fill drilled 1P core; (D) Etch laminated 1P core (E) Drill and plate laminated 1P core

The 2S1P signal core process starts the same as the 0S1P core, up to attaching the dielectric and metal layers to the 1P core. As the next step, instead of drilling, the outer copper is etched to create all the signal features. Lastly, the holes are drilled and plated to make the 2S1P core. The 0S1P and 2S1P cores are combined to make a Z-interconnect stack-up. **Figure 2** and **Figure 3** describe simplified diagrams of Z-interconnects which include joining cores, signal cores and their final, combined structure.

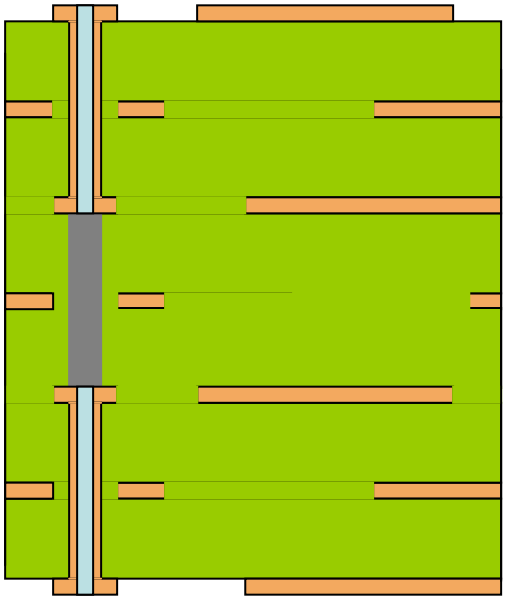


Figure 3 Z-interconnect composite stack-up

In combination with blind and buried vias (see **Figure 4**), the signal and joining core building blocks allow arbitrary via connections starting at any layer and ending at any layer. In the 1P core, vias can be drilled and plated before the additional

dielectric layers are added. Blind vias can be drilled on the outer layers of the 2S1P also. These one-layer micro-vias can be stacked to make arbitrary via connections.

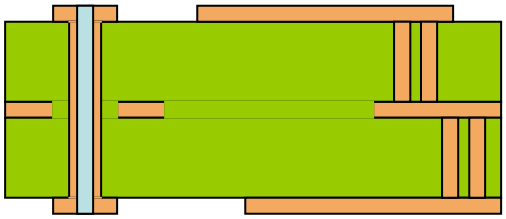


Figure 4 Buried and blind vias in core

In addition, embedded capacitance layers can be inserted by using a 2P core instead of 1P core of the stack-up. (**Figure 5**) Discrete embedded capacitors and resistors can be added to most layers in the stack-up. Barium titanate–fluoropolymer can be used for embedded capacitance layers. Printable barium titanate nano-composites, thick film resistors or resistor foil are typically used for discrete embedded resistors.

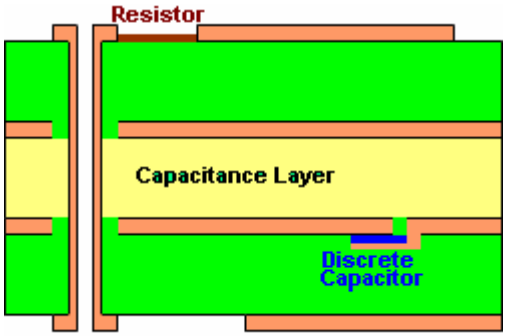


Figure 5 Embedded capacitance layer and embedded discrete caps and resistors

Test Vehicle Design

Test vehicles were designed to make new multi-GHz structures, using the Z-interconnect building blocks. Specifically, large rectangular clearances were cut in multiple ground planes to make a very wide 50-ohm stripline. Also, typical 50-ohm stripline was built with a ground-signal-ground structure. Each stack-up had 23 metal layers, including 5 0S1P joining cores and 6 2S1P signals cores. Each dielectric layer was about 125 um thick. The stack-up used a set of Teflon-based Taconic materials, TLG30 and TPG30. (**Figure 6**) The total thickness of the stack-up was about 4 mm. The dielectric has Dk = 3.2 and $\tan\delta$ = .004.

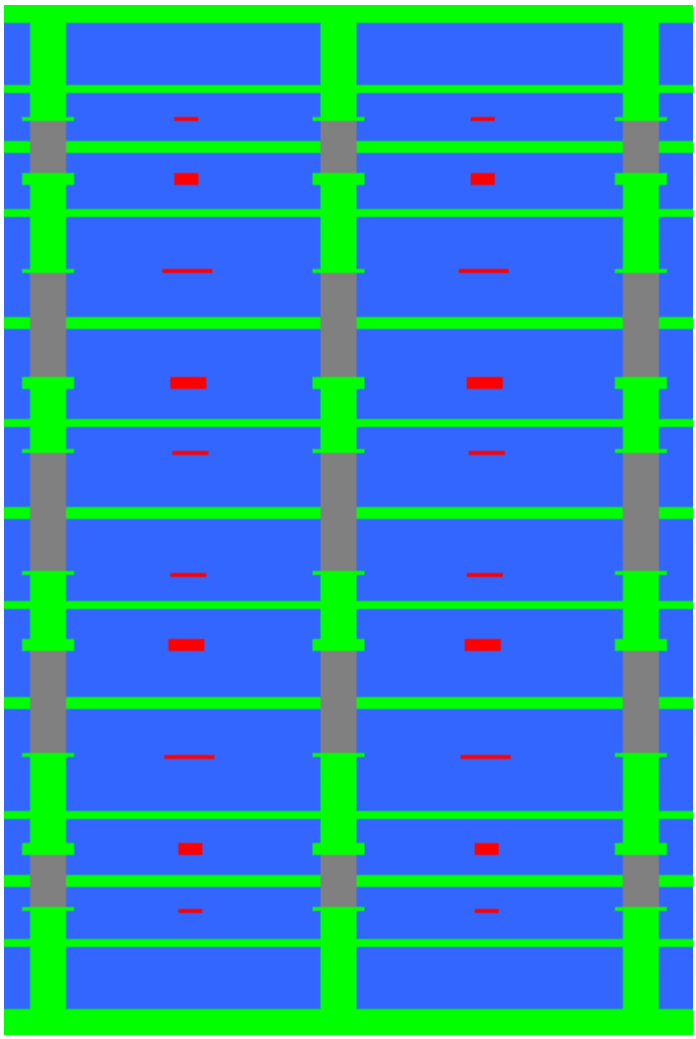


Figure 6 Test Vehicle Stack-up

Electrically, this type of stack-up allows a well-controlled, low-loss, wide, 50-ohm lines. In the test vehicle the widest line width was roughly 180um, with the narrowest at about 80um. There was also a 130um width line. This new construction provides increased wire-ability such that all 3 sizes of transmission lines easily fit in a stack-up less than 5mm thick. With the 80um line at 150mm long, the estimated 3dB bandwidth of a link with vias and pads is about 4.8GHz, and 6dB above 10GHz which is in the range of 20Gbps SERDES. Using an 180um line at 300mm instead, the 3dB point is about 3GHz, and 6dB at 7GHz which meets a typical loss budget for 14Gbps SERDES.

The test vehicle is a large backplane, about 50cm x 50cm in size. The test vehicle includes BGA land patterns. The materials and processes used to manufacture the Z-interconnect circuit board will work with BGA attach assembly steps.

Composite Lamination

Alternating the joining and signal cores, in the lay-up prior to lamination, allows the conductive paste to electrically connect copper pads on the 2S/1P cores that reside on either side of the 0S/1P core. A structure with 12 signal layers composed of 11 sub-composites (6 2S/1P cores and 6 0S/1P cores) is shown schematically back in **Figure 6**. Although this particular construction comprises alternating 2S/1P and 0S/1P cores, it is also possible to place multiple 0S/1P cores adjacent to each other in the stack.

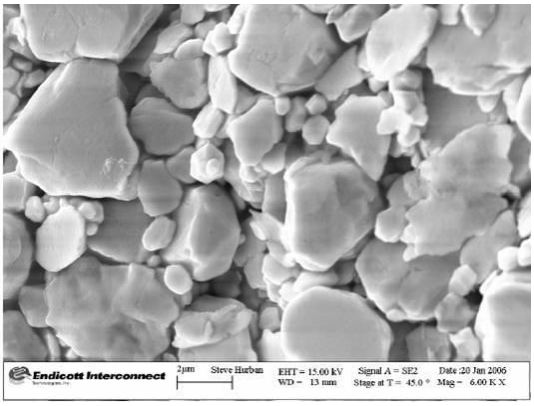


Figure 7 SEM micrograph of conductive adhesive paste with nano and micro particles

Results and Discussion

A Z-interconnect circuit board was built successfully. The conductive paste connects sub-composites and forms an electrical and mechanical path. The formation of a conduction path was observed by SEM images. **Figure 7** shows a SEM image of nano-micro filled conductive adhesive as a typical representative example. In the silver adhesive, the average filler diameter is in the range of 5 µm. Filler loading was high and adjacent particles united mutually, and necking phenomena between fillers occurred; namely, a conduction path was achieved, as shown in **Figure 7**. A variety of silver filled adhesives with a mixture of nano and micro particles were studied. In nano-micro mixtures, nano particles occupy interstitial positions to improve particle-particle contact for conductivity. For the silver nano particles (~80 nm size), the fillers can self sinter and make a continuous conduction path. Because of the high surface area of silver nano-particles, an excess amount of solvent is required to make a high loading silver paste.

The adhesive-filled joining cores were laminated with circuitized sub-composites to produce a composite structure. **Figure 2** and **Figure 3** show a process flow chart for fabrication of adhesive filled 0S/1P cores. High temperature/pressure lamination was used to cure the adhesive in the composite and provide Z-interconnection among the circuitized sub-composites. When the temperature is increased past 200 degrees C, the nano and micro particles melt together and form a more conductive, stronger bond. Reliable metal-epoxy adhesives were used for hole-fill applications to fabricate Z-axis interconnections in laminates.

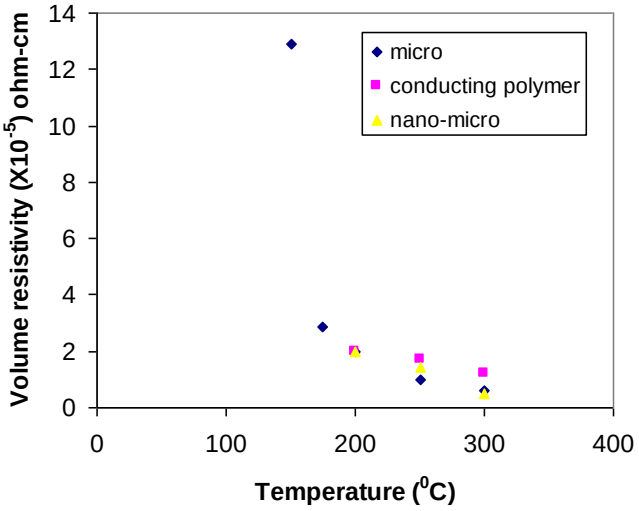


Figure 8 Volume resistivity of silver adhesive as a function of curing temperatures

Below, **Figure 9, Figure 10 and Figure 11** show experimental results. Electrically, S-parameter measurements showed very low loss at multi-gigahertz frequencies. The measured insertion loss for narrow, short lines and wide, long lines are similar. The Z-interconnect stack-up and low dielectric constant, organic dielectric allowed wide, 50-ohm, lines.

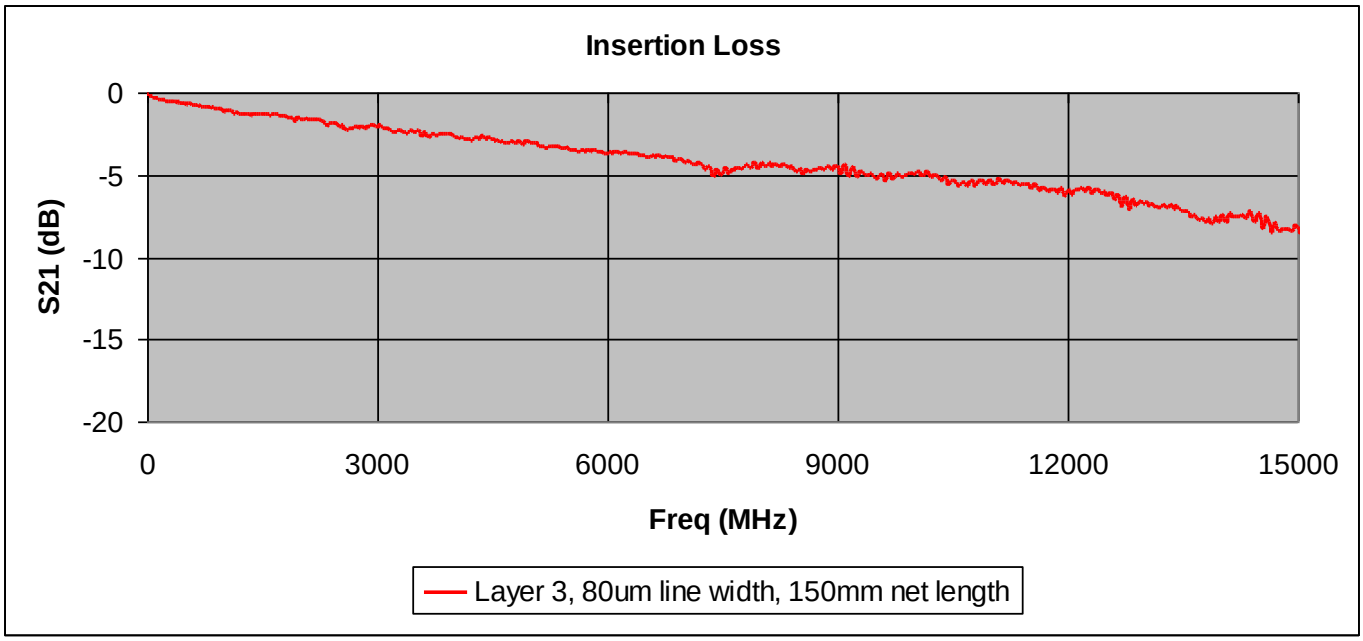


Figure 9 Narrow Line (80um) Insertion Loss

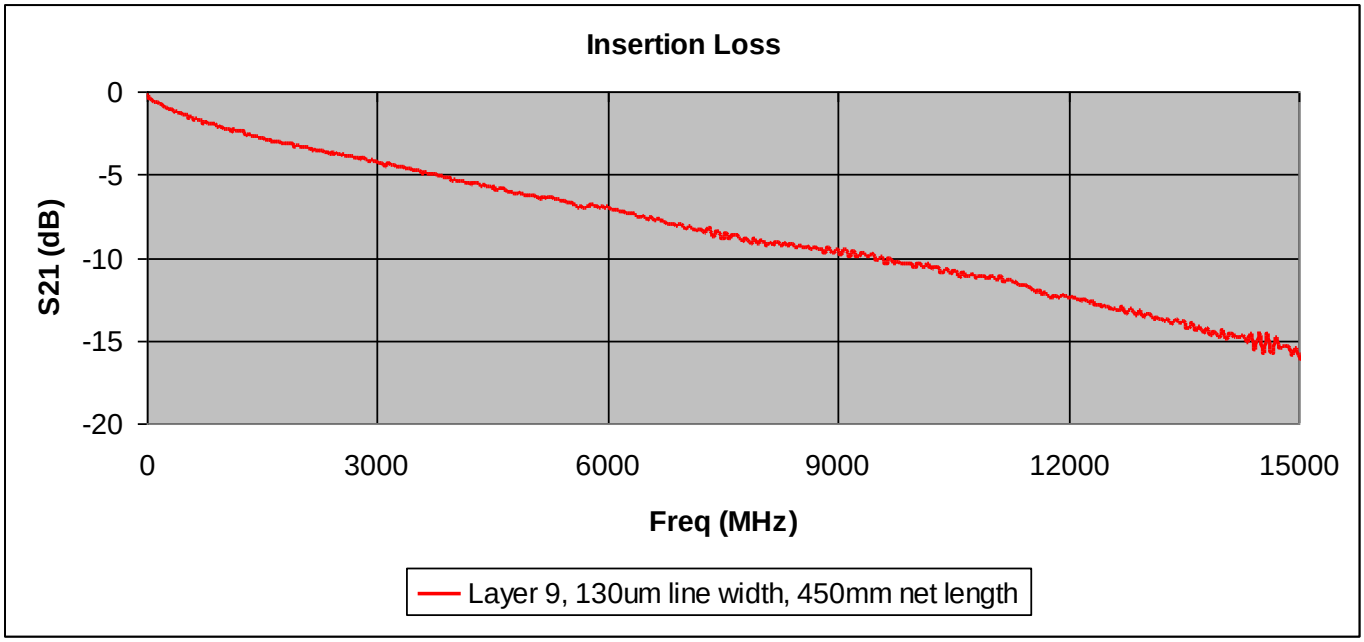


Figure 10 Medium Stripline (130um) Insertion Loss

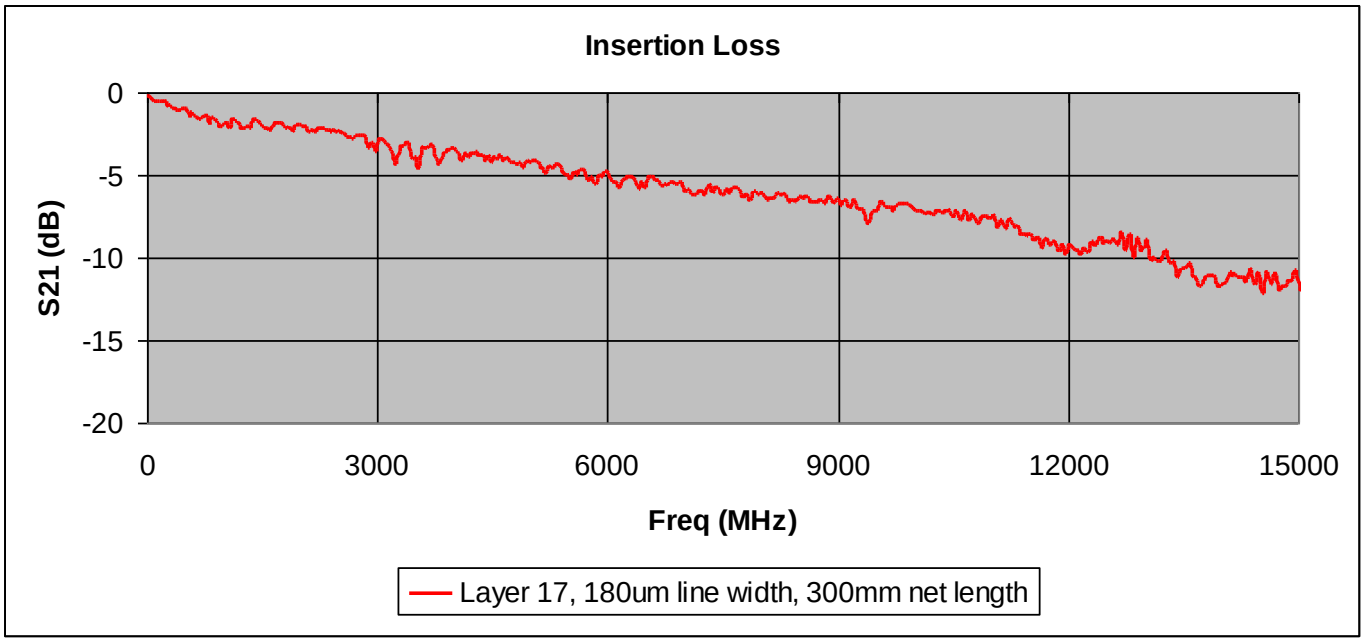


Figure 11 Wide Stripline (180um) Insertion Loss

The Z-interconnect paste has little effect on the signal, except to add a small via length to the signal. The performance is similar to a solid copper barrel. The Z-interconnect paste does not degrade the signal significantly. **Figure 12** is a plot of insertion loss for a net that has no Z-interconnect joints, vs. a net that has 4 joints. Below 10GHz, the difference is negligible, above 10GHz there's a slight degradation due to the additional via length, which is the same as copper plated through-holes.

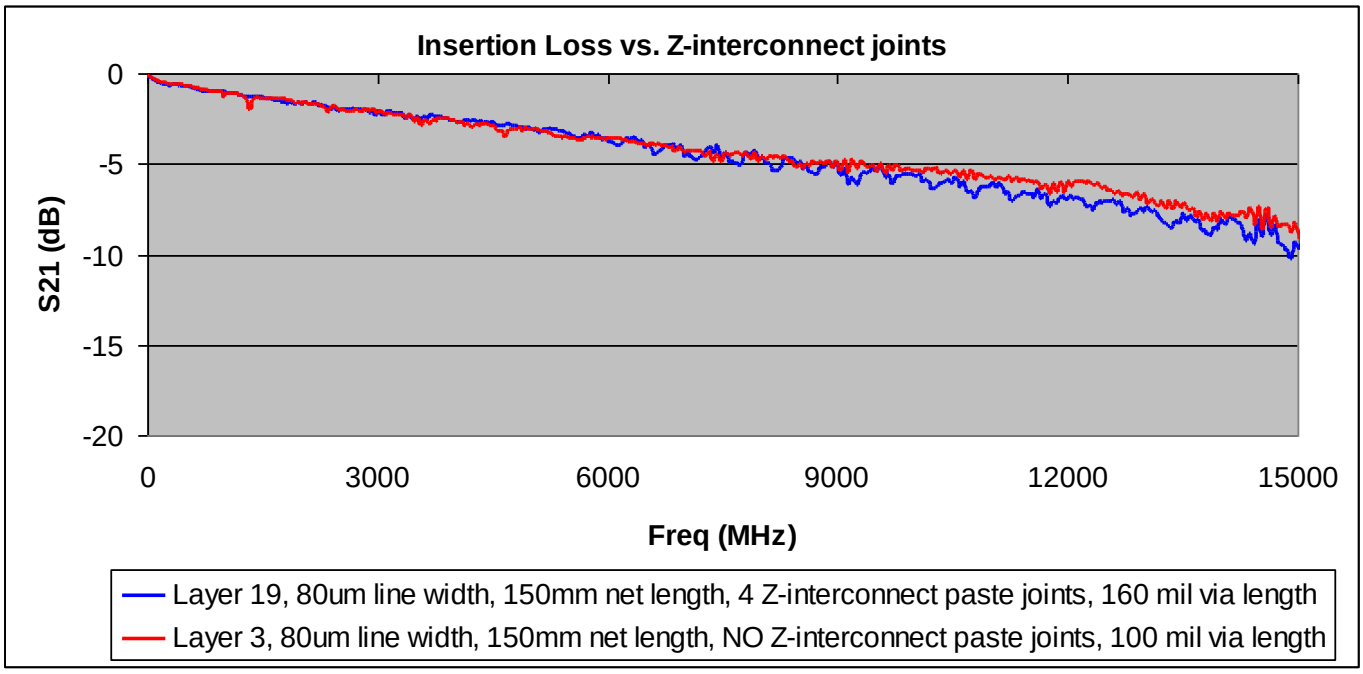


Figure 12 Test results between nets with different numbers of Z-interconnect joints

Conclusions

A Full-Z interconnect circuit board can be built with Taconic materials, numerous metal layers and a range of line widths maintaining a 50-ohm impedance. Using 0S1P and 2S1P building blocks, a nearly arbitrary stack-up of signals and planes can be built. This allows very low-loss 50-ohm stripline to be built by making 180um-wide lines. This also allows narrower 50-ohm lines and narrow digital lines and DC structures to be built on the same layers as the wide lines. A high-performance, mixed signal design can be built in a circuit board less than 4mm thick with the potential to be less than 1mm.

In addition, the electrical performance is outstanding, since the wide lines are low-loss and have smooth frequency response to 15GHz. Very low-loss multi-GHz, controlled-impedance transmission lines can be built using Z-interconnect with organic dielectric materials.

References

1. McBride, R.D., Rosser S.G., and Nowak R., "Modeling and Simulation of 12.5 Gb/s on a HyperBGA® Package" *IEEE / CPMT / SEMI Int'l Electronics Manufacturing Technology Symposium*, July, 2003.
2. Jadhav, V., Moore S., Palomaki, C., and Tran, S., "Flip Chip Assembly Challenges Using High Density, Thin Core Carriers" *Proc 55th Electronic Components and Technology Conf*, May 2005.
3. Das, R., Egitto F., and Lauffer, J., "Electrical Conductivity and Reliability of Nano- and Micro-Filled Conducting Adhesives for Z-axis Interconnections" *Proc 56th Electronic Components and Technology Conf*, May 2006.
4. Rosser, S., and Rowlands, M., "Simulation and Measurement of High Speed Serial Link Performance in a Dense, Thin Core Flip Chip Package" *Proc 56th Electronic Components and Technology Conf*, May 2006.
5. Audet, J., Cranmer, G., et al, "Design Optimization for Isolation in High Wiring Density Packages with High Speed SerDes Links" *Proc 56th Electronic Components and Technology Conf*, May 2006.
6. Blackwell, K., Egitto, F., Krasnak, S., and Rosser, S., "Z-Axis Interconnection for Enhanced Wiring in Organic Laminate Electronic Packages" *Proc 55th Electronic Components and Technology Conf*, May 2005.
7. Das, R., and Rowlands, J., "Electrical Performance of an Organic, Z-interconnect, Flip-Chip Substrate" *Proc 57th Electronic Components and Technology Conf*, May 2007.

Manufacture and Performance of a Z-interconnect HDI Circuit Card

Michael Rowlands

Endicott Interconnect Technologies, Inc.
Research and Development
RF Signal Integrity Engineer

Endicott Interconnect

IPC Printed Circuits Expo®, APEX® and the Designers Summit 2008

Agenda / Outline / Overview

- **Introduction**
- **Z-interconnect construction**
- **Test Vehicle Design**
- **Experimental Results**
  - **Impedance measurements, S-parameters**
  - **Cross-section pictures**
- **Summary & Conclusions**
  - **Comparison to ceramic packages**
- **Acknowledgements**

Introduction

In order to achieve GHz electrical performance goals in a chip package, several requirements must be met:

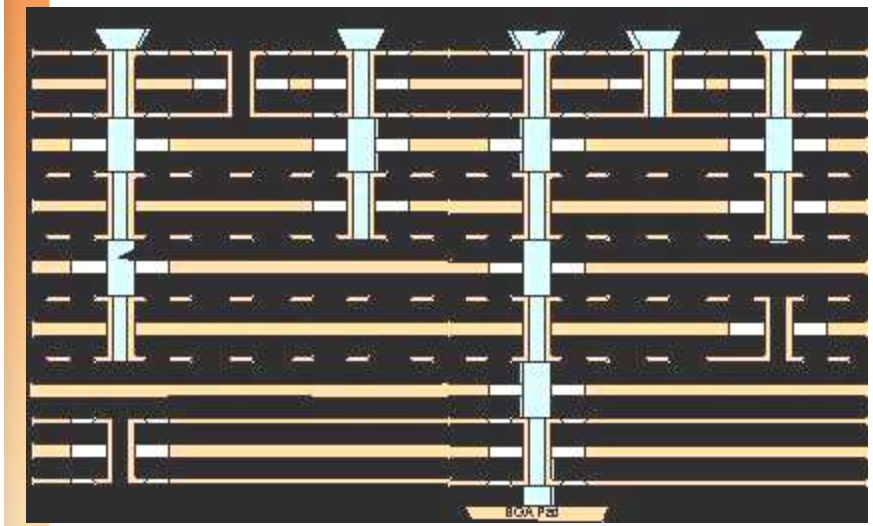
- Low-loss signal path, wide, controlled impedance lines, eliminate via stubs
- Embedded discrete resistors, capacitors, inductors, plus capacitance layers
- Delay matching
- Islands in all plane layers, can be either power or ground
- Narrow lines for digital and low-frequency signals
- Arbitrary stack-up, symmetric or not, all layers have ground and signal regions
- Large, arbitrary-shaped clearances in planes
- Lightweight, thin
- Interconnects must be tuned to reduce signal loss
- Vias must be tuned to reduce signal loss
- Substrate must be manufacturable and reliable

Using Z-interconnect (Z-axis board interconnect), all of these requirements can be satisfied

Why Z-Interconnect?

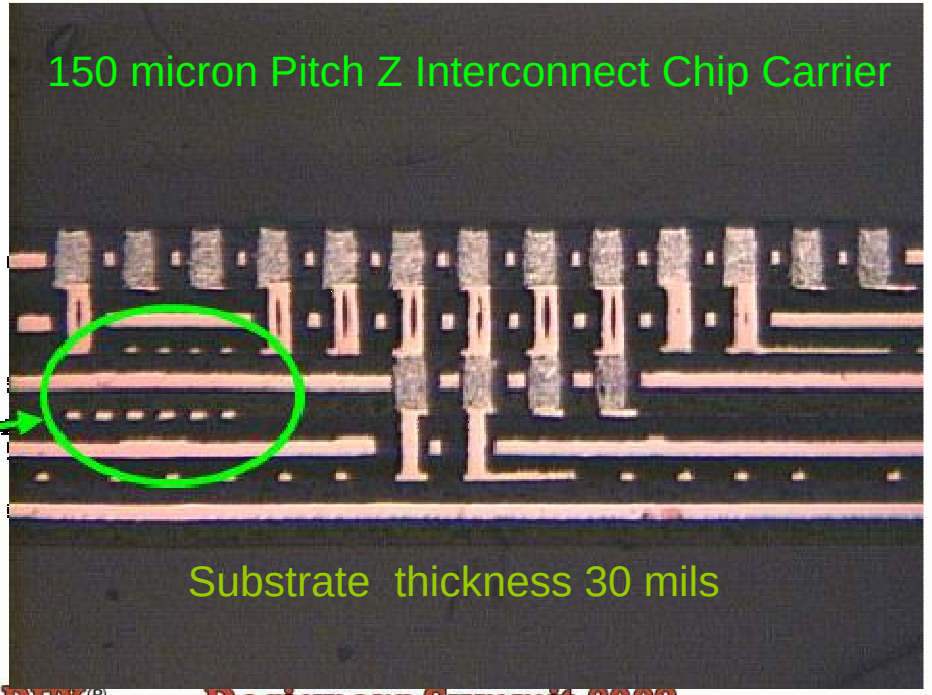
Define Z-interconnect as: Z-axis board interconnect

Z-interconnect Improves electrical performance and increases wiring density



Improved Electrical Performance

- Vias start and stop on any level. No stubs!
- Reduced discontinuities with smaller vias and lands



Maximized Density

- Small vias result in more LPC
- Unlimited wiring channels beneath terminated vias

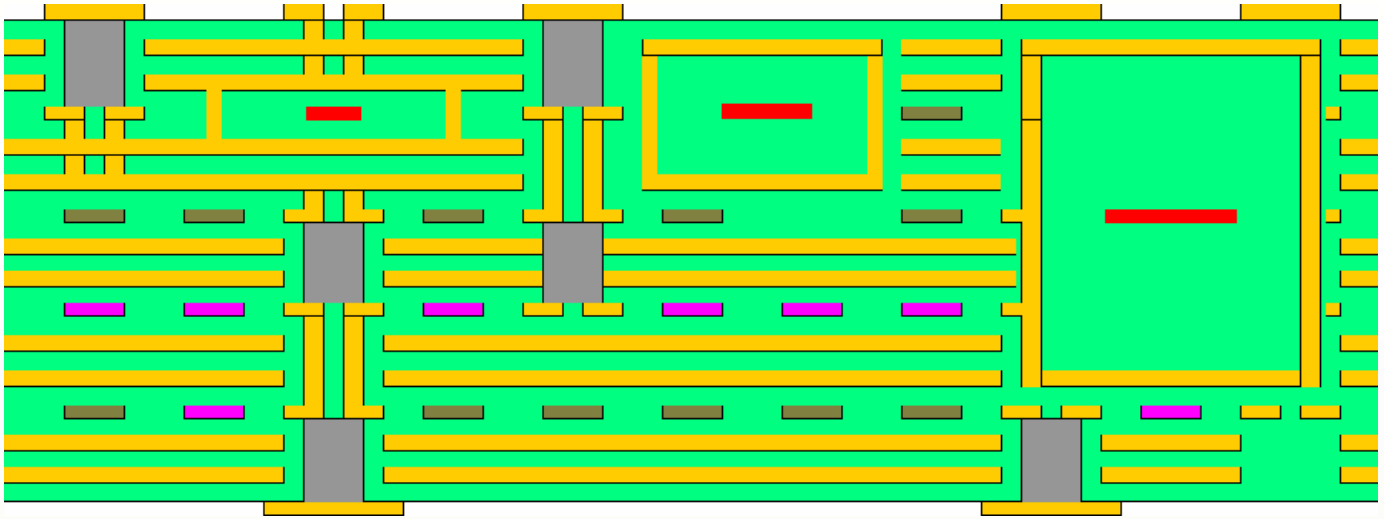
Example Z-interconnect Stack-up

Red = RF or Gbps digital signals

Purple = digital

Brown = all other signals

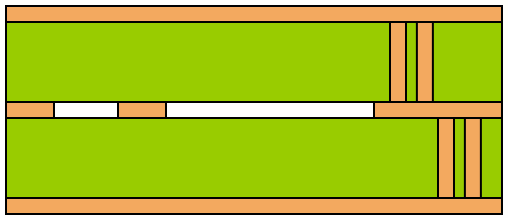
Gray = Z-interconnect joint



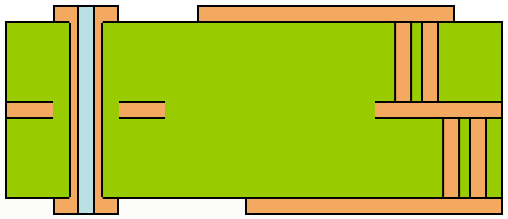
Z-interconnect Construction

- **Side view of 2S1P Building block (2 signals, 1 plane)**

Etch a copper sheet



Laminate copper-clad dielectric layers, then etch signal features, drill and plate micro-vias

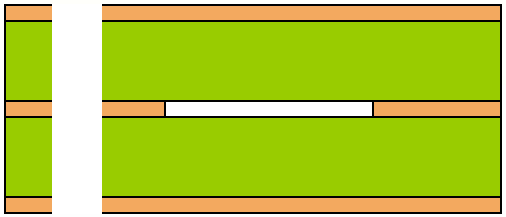


Drill, fill and plate vias to complete the 2S1P

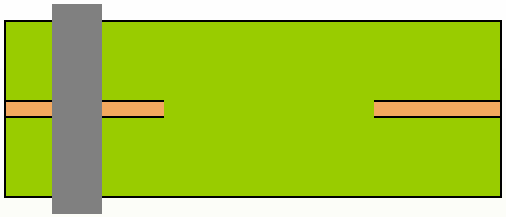
Z-interconnect Construction

Side view of 0S1P Joining layer (0 signals, 1 plane)

Etch a copper sheet



Laminate copper-clad dielectric layers, then drill holes



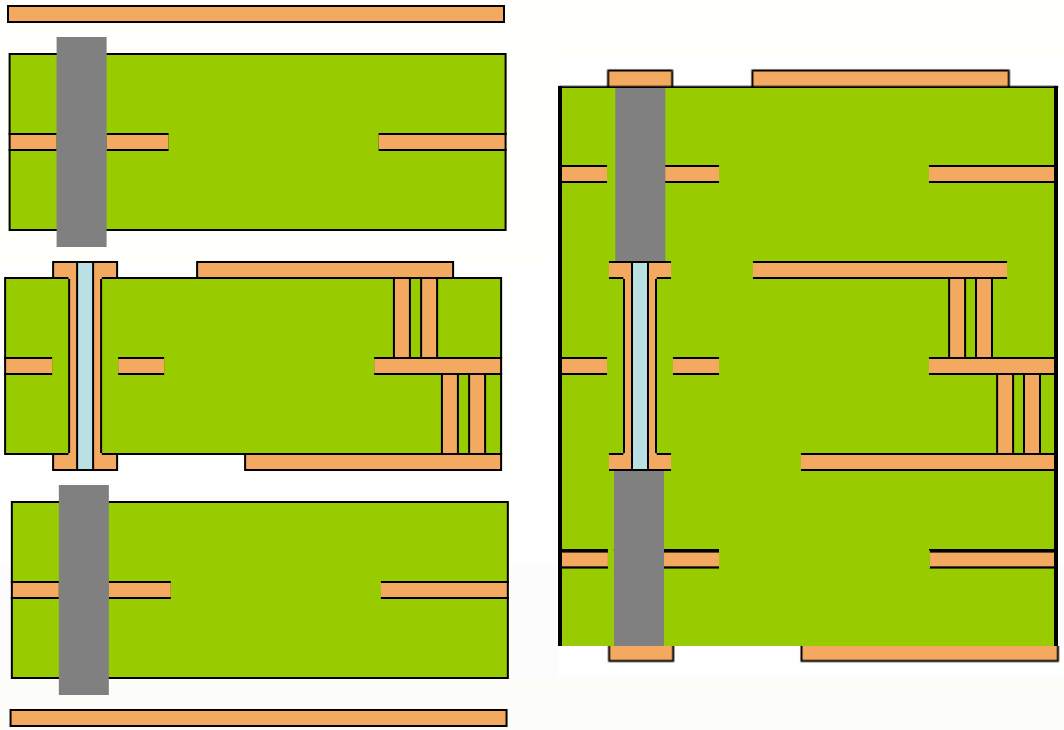
Fill holes with conductive paste, etch off excess copper to complete the joining layer

Z-interconnect Construction

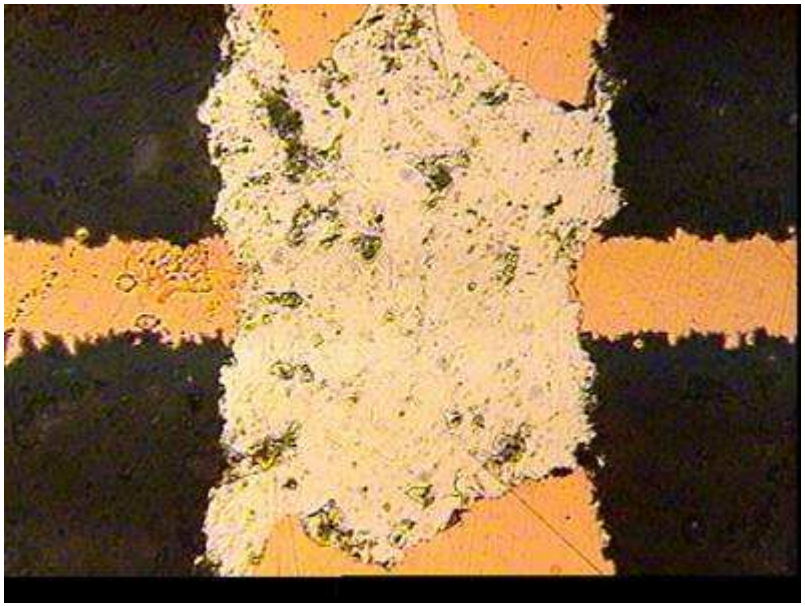
Side view of Composite Lamination

Join 0S1P and 2S1P sub-assemblies

Plate and etch copper on top and bottom to create a finished stack-up



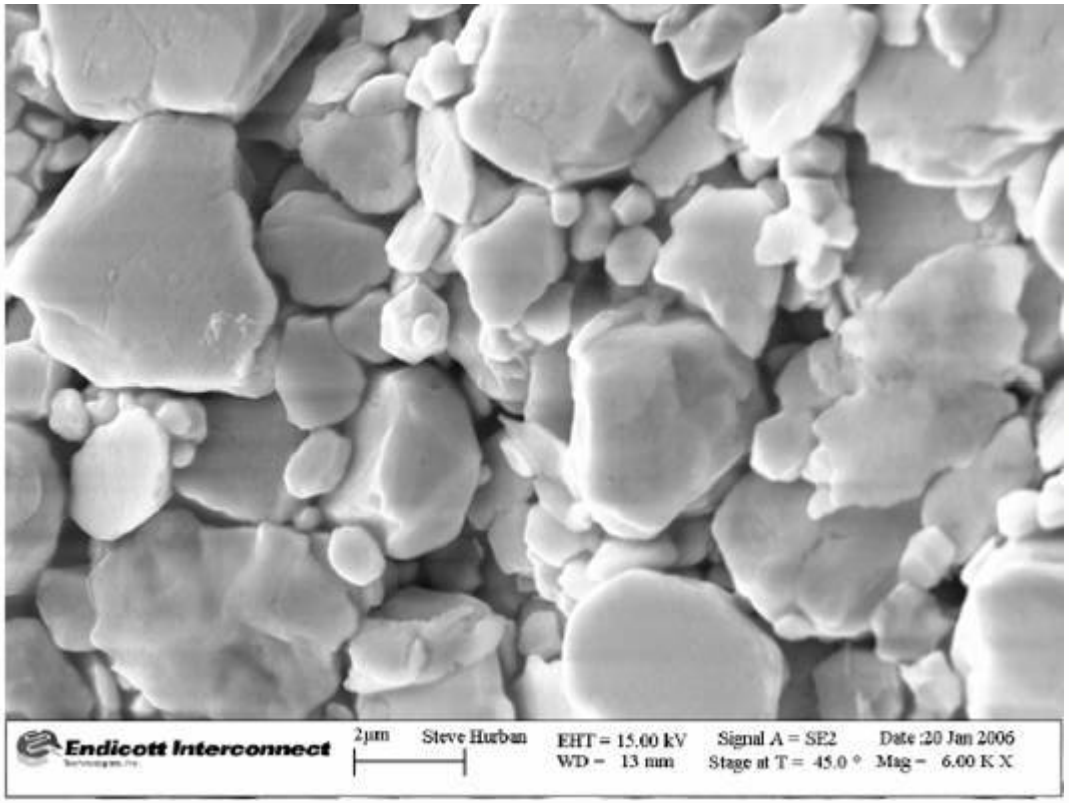
Conductive Adhesives for Z

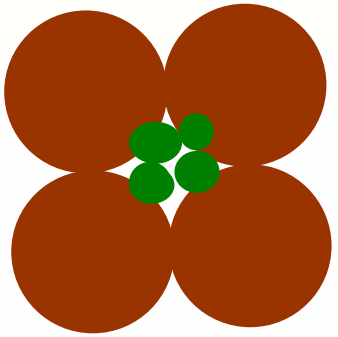


Low Resistance connections (conductive)

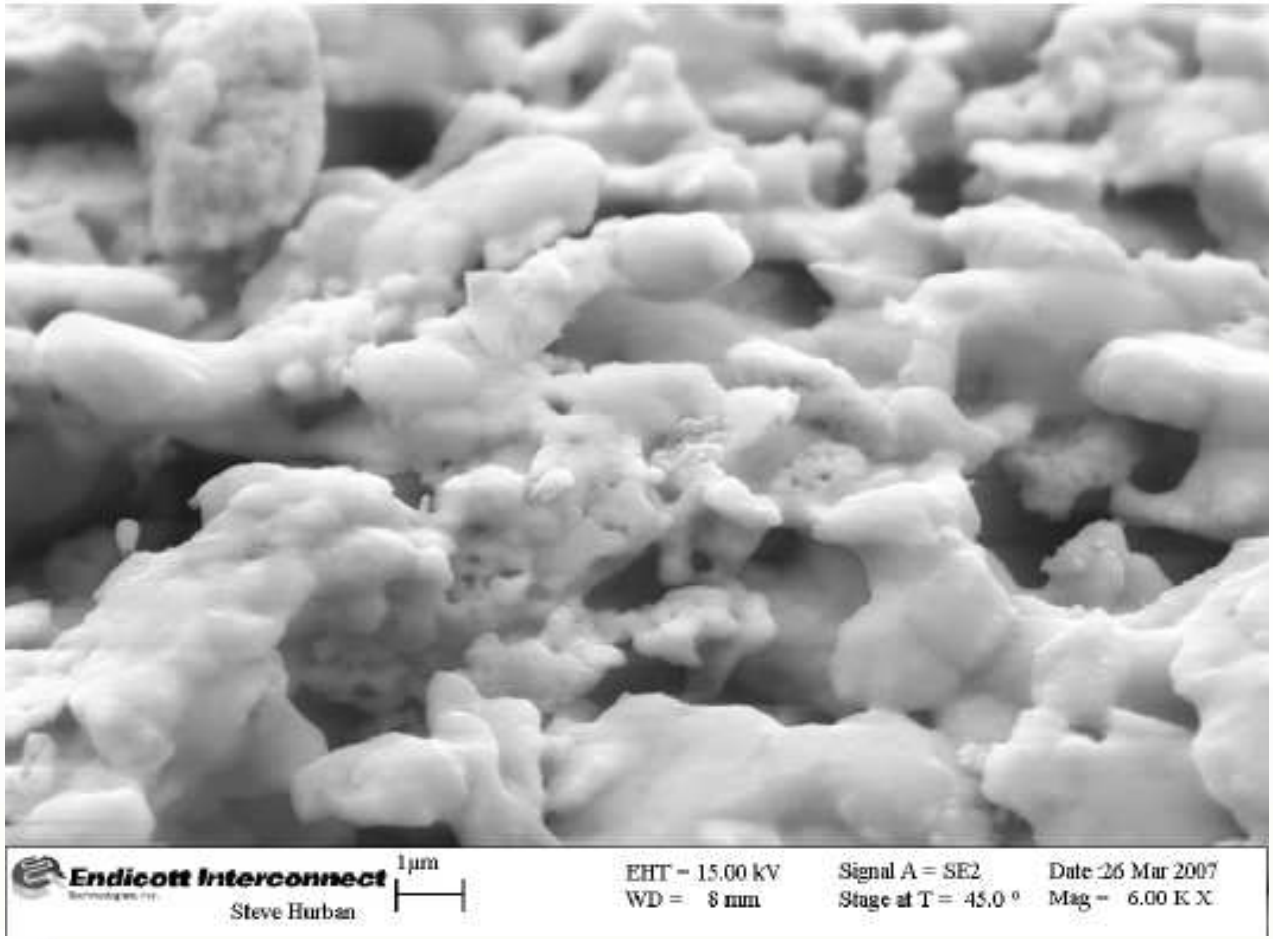
Reliable Joints/bonding (adhesive)

Example : (Nano + Micro) Conductive Adhesive



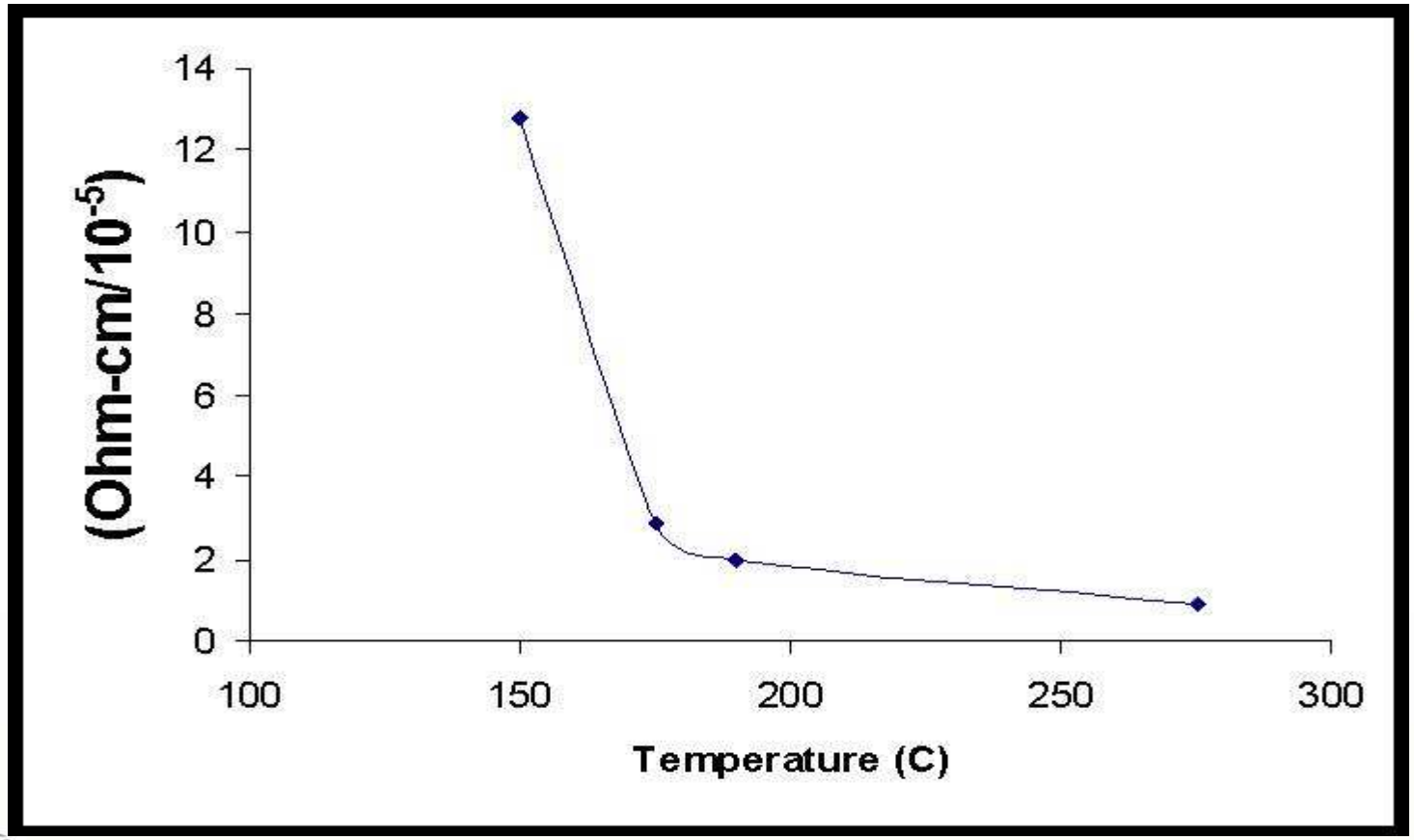


Nano-micro Mixture: Sintering

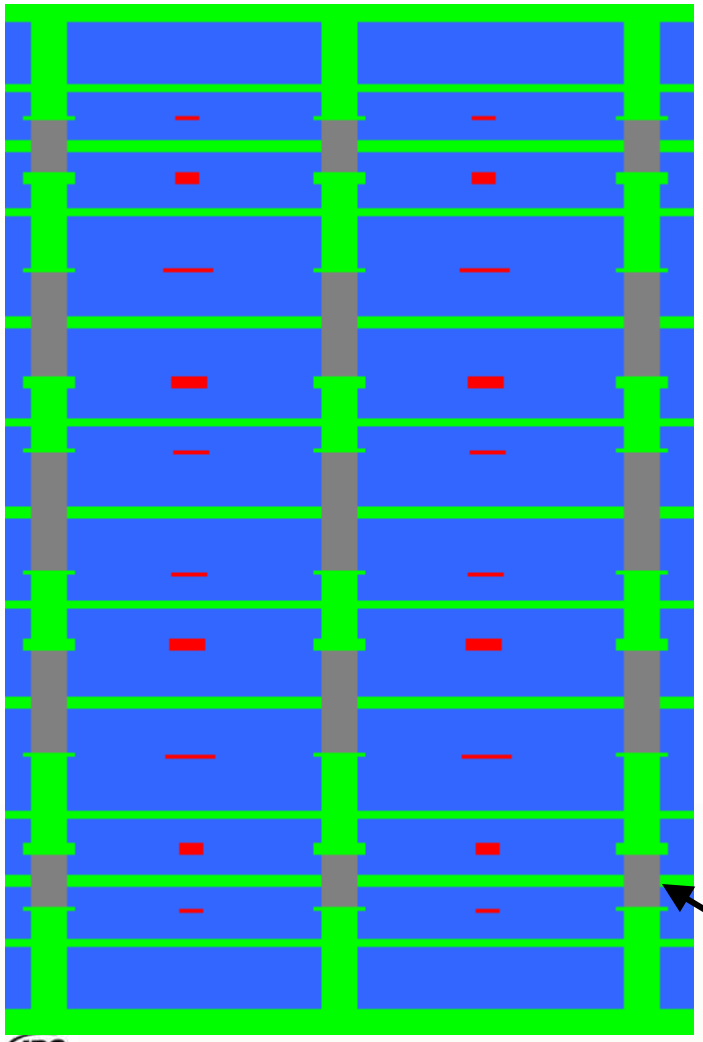


Volume resistivity vs. curing temperature

Resistivity decreases with increasing curing temperature



Test Vehicle Design



23 metal layer Stack-up

6 2S1P signal cores

5 0S1P joining cores

11 planes

Top, Bottom metal

10 Signal layers

(SKETCH NOT TO SCALE)

Paste Joint

Test Vehicle Design

Metal layers 3,19 have 3.6 mil wide lines, 6” long

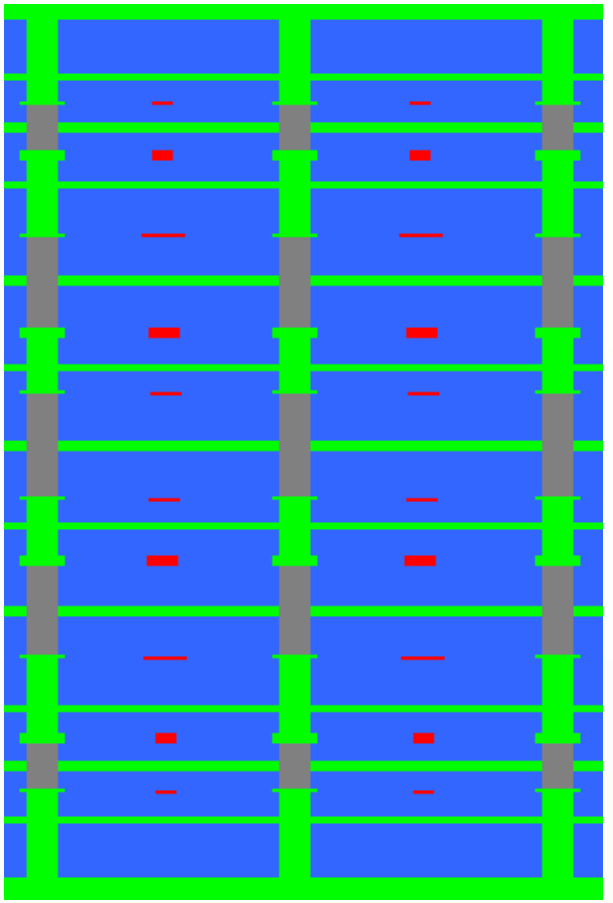
L 5,21: 3.6 mil LW, 12” long

L 7: 7.4mil LW, 18” long

L 9,13,15: 5 mil LW, 17” long

L 11: 5 mil LW, 23” long

L 17: 7.4 mil LW, 23” and 12” long

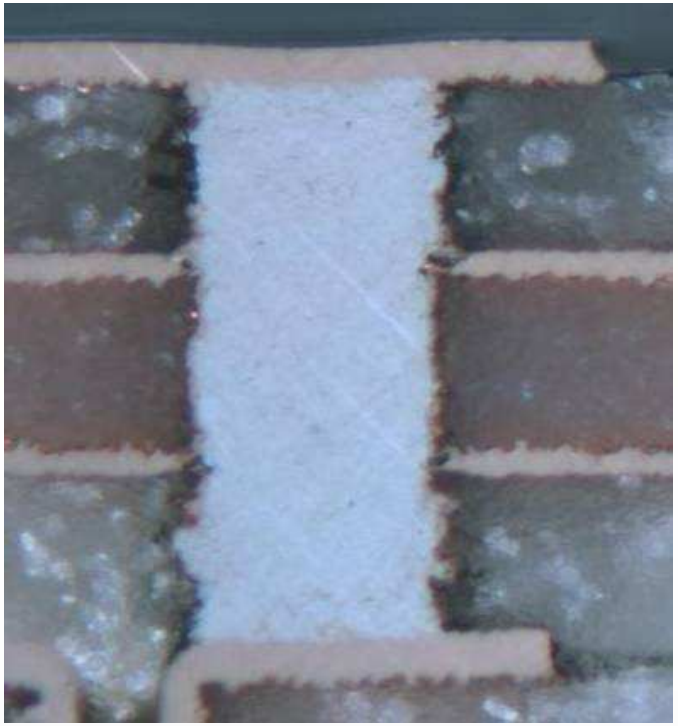


Results

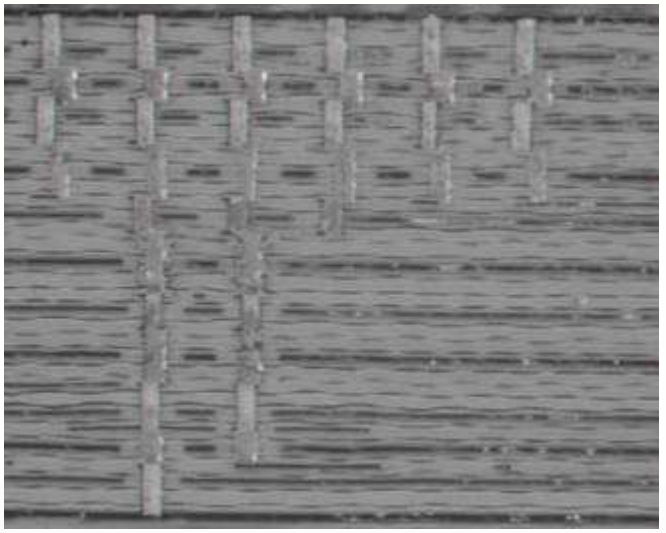
- Test Vehicles were built successfully
- Paste joints showed good electrical connections
- Transmission lines showed good high-speed data delivery

Z-interconnect Manufacturing Results

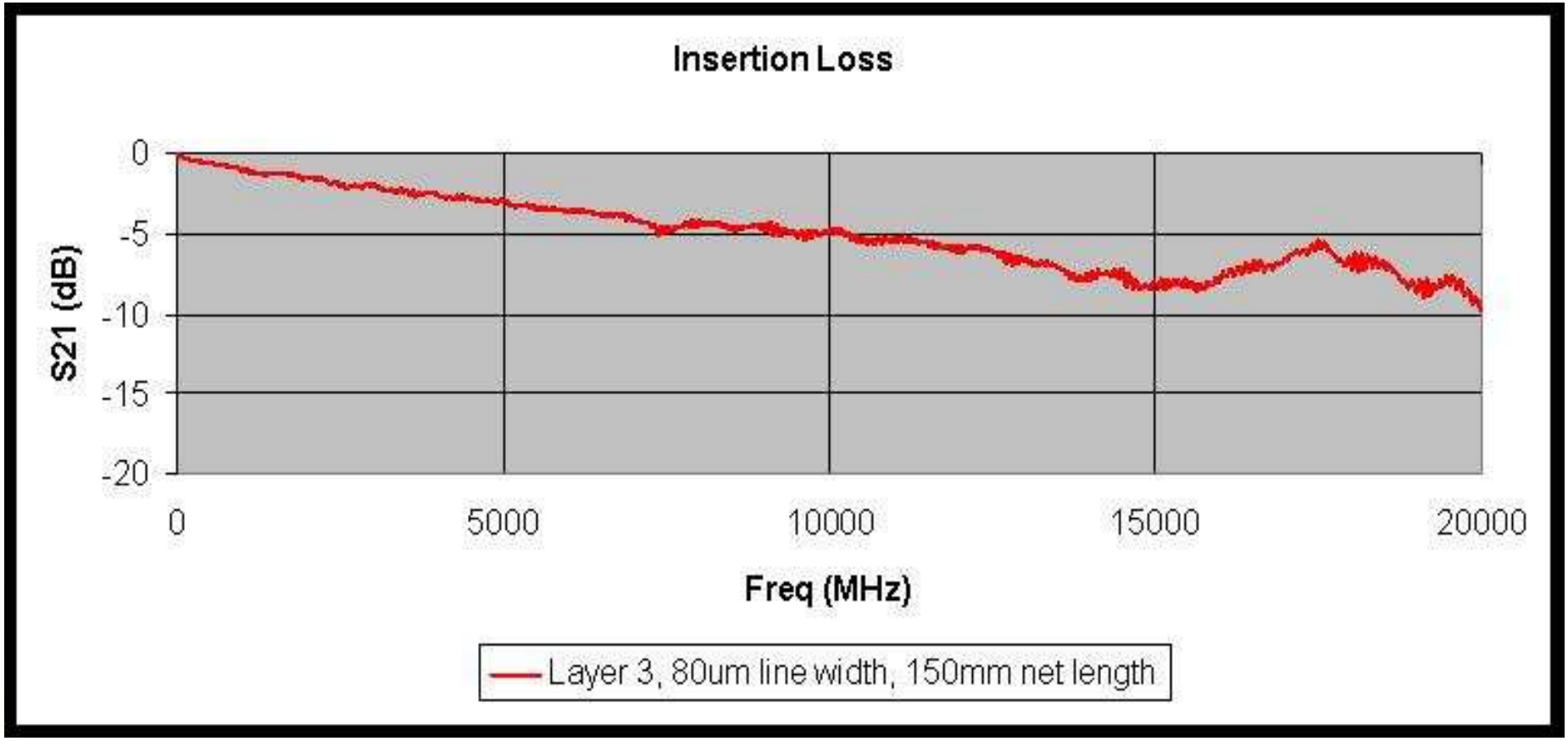
Paste Joint Cross-section, Grounded



Full Stack-up Cross-section



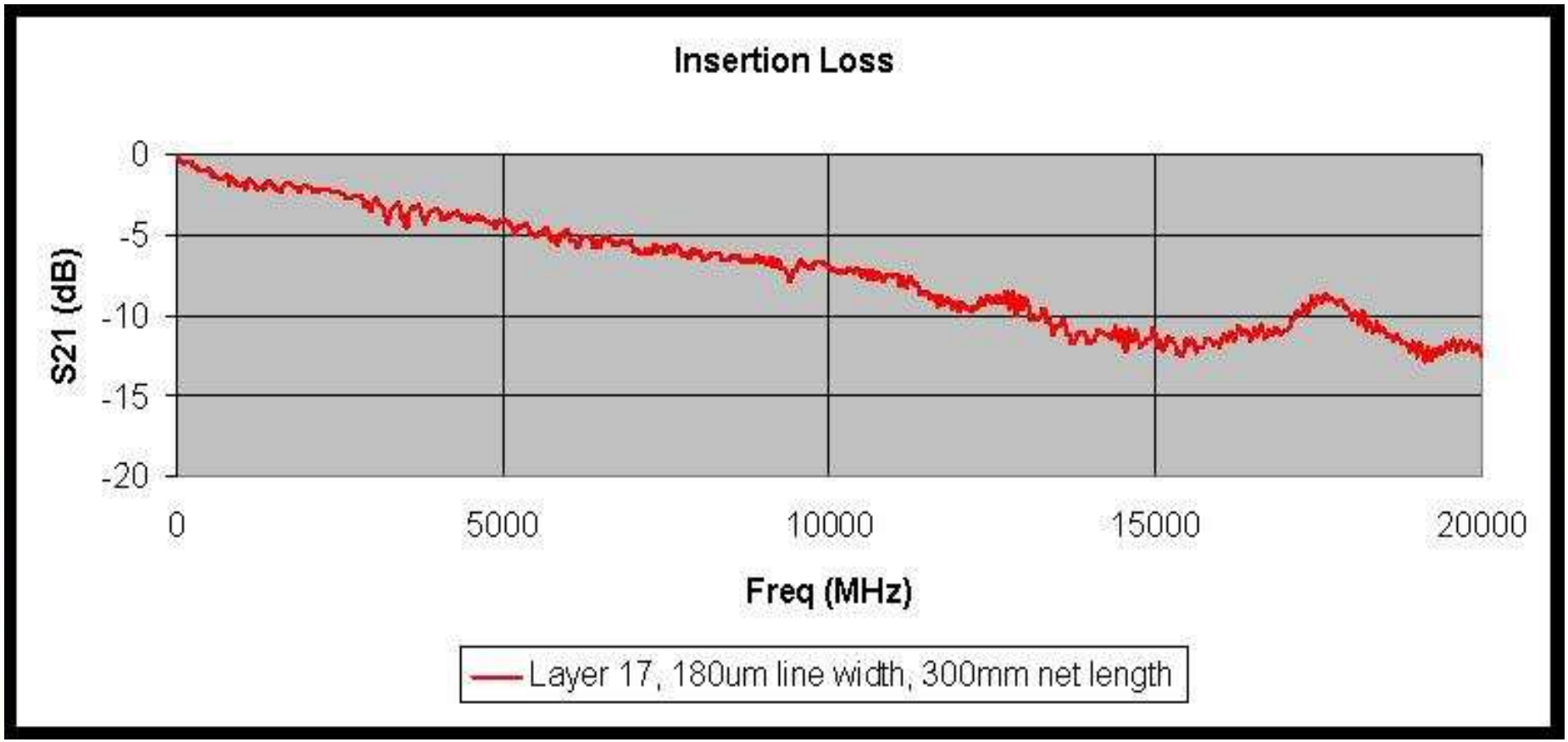
Full-Z Board Electrical Results: Insertion Loss



6” net length, 3.6 mil line width, meets 10dB loss at 40 Gbps

20” net length, 3.6 mil line width, meets 10dB at 10Gbps

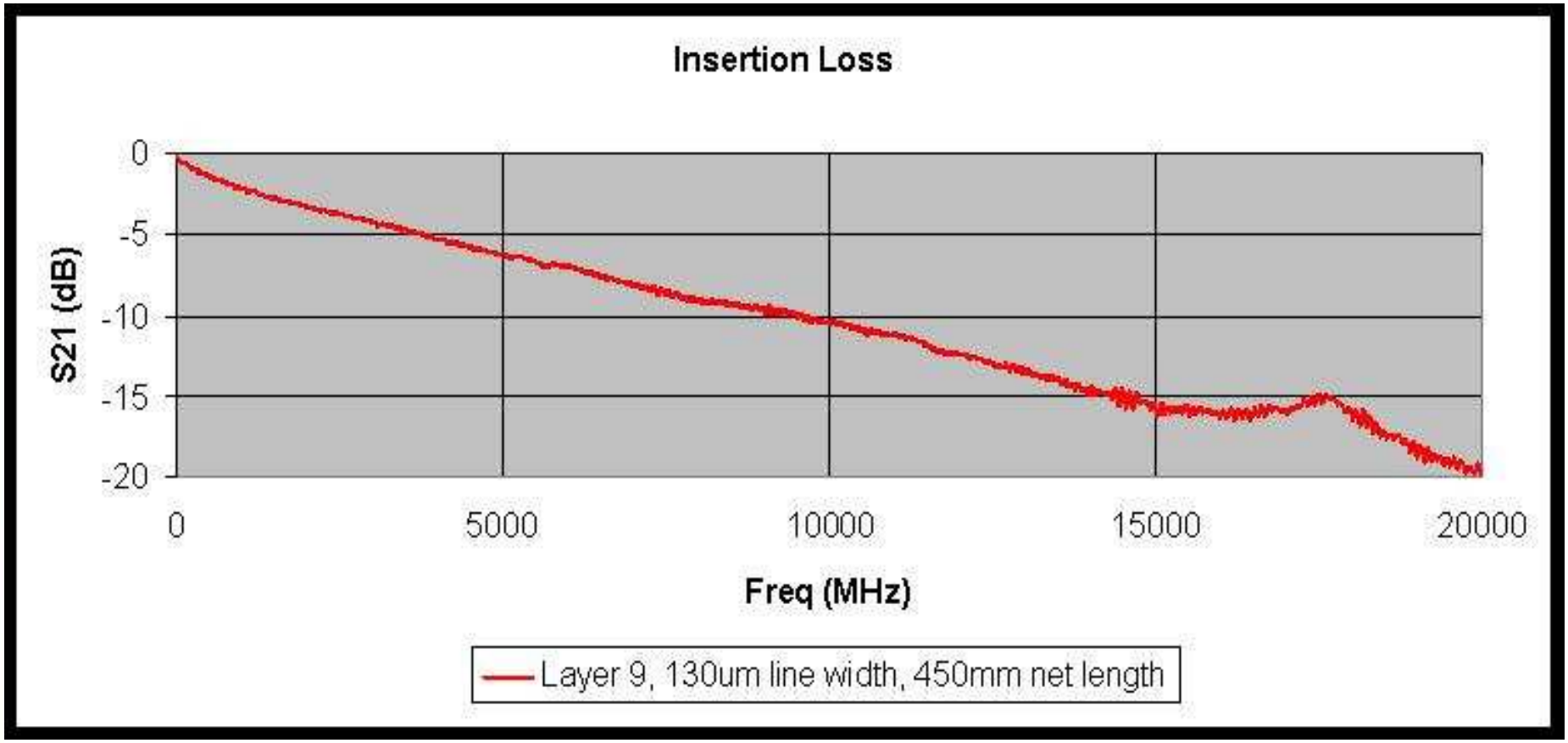
Full-Z Board Electrical Results: Insertion Loss



12” net length, 7.4 mil line, meets 10dB loss at 26 Gbps

25” net length, 7.4 mil line width, meets 10dB at 10Gbps

Full-Z Board Electrical Results: Insertion Loss



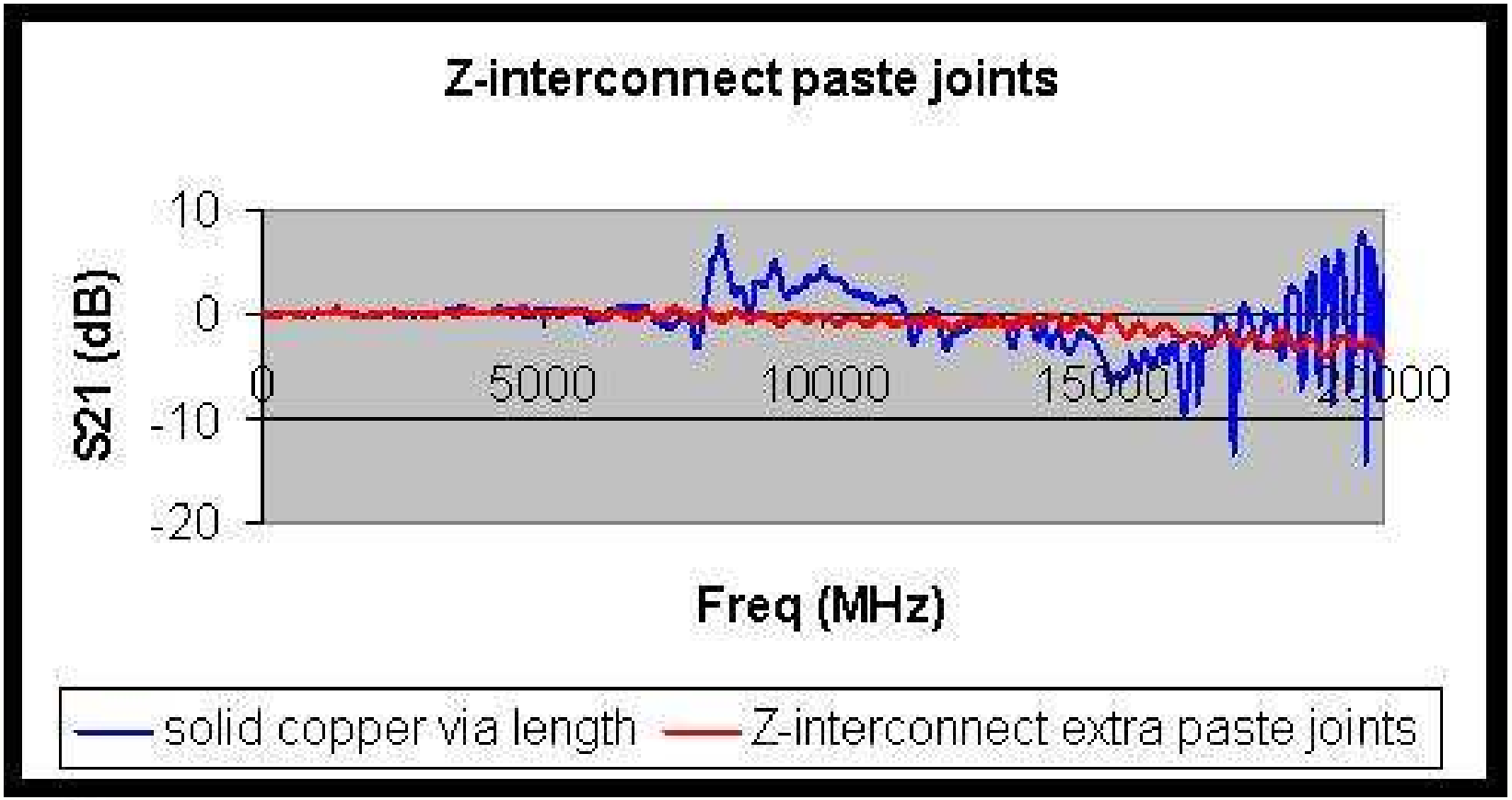
18” net length, 5 mil line, meets 10dB loss at 20 Gbps

24” net length, 5 mil line width, meets 10dB at 10Gbps

Full-Z Board Electrical Results: Insertion Loss, Z-joint

Z-interconnect joints have negligible added loss compared to solid copper vias of same length

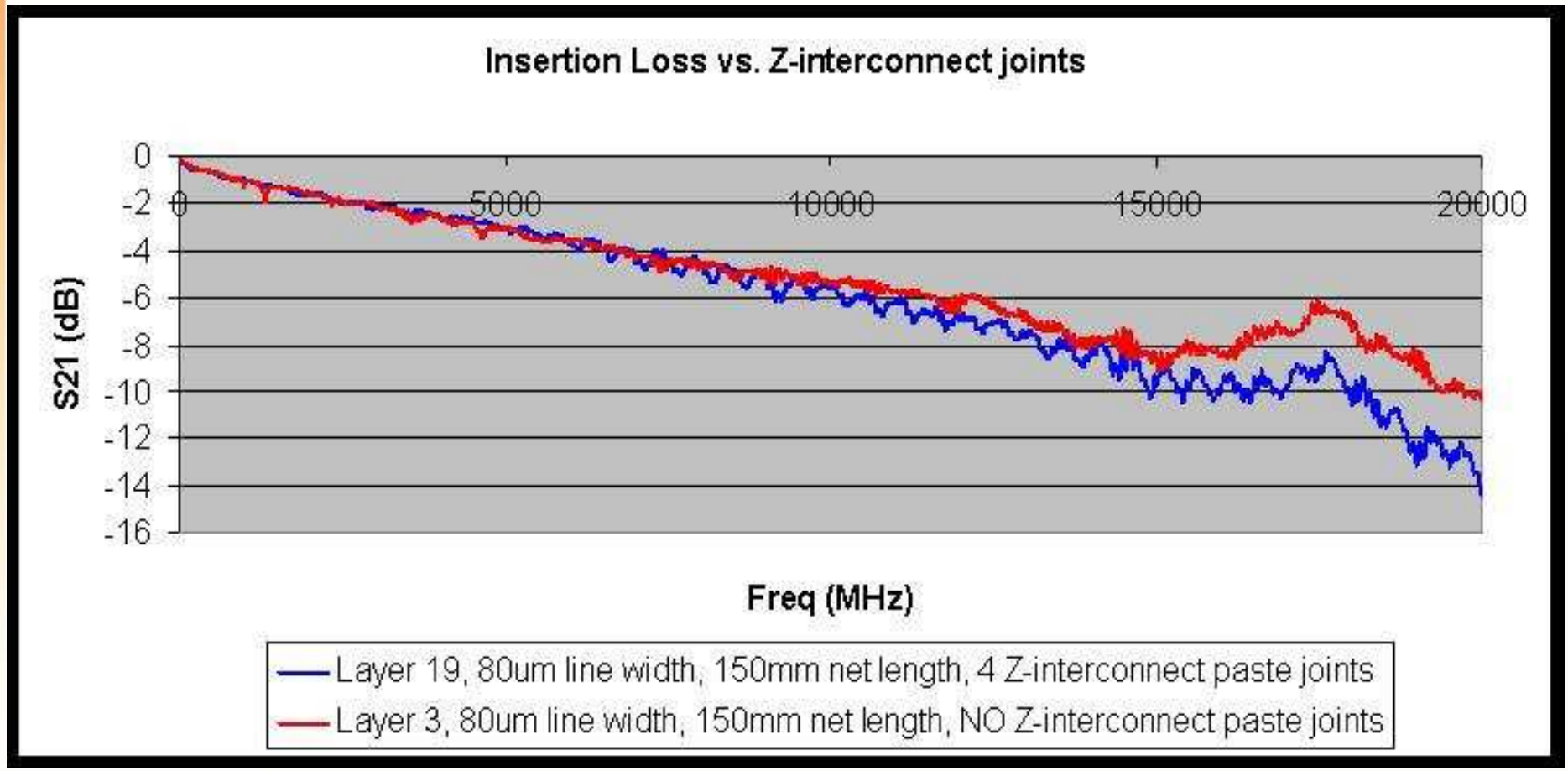
Reflections and discontinuities dominate the via response



Full-Z Board Electrical Results: Insertion Loss, Z-joint

Z-interconnect joints have negligible added loss compared to solid copper vias of same length

No difference to 10GHz, a few dB at 20GHz, primarily due to additional via length to and from layer 19



Summary and Conclusions

- **A Full-Z board (no PTHs, only sub-composites and joining layers) can be built**
- **Conductive paste shows good signal transmission to 25GHz**
- **Z-interconnect construction allows wide lines (7.4 mils and narrow (3.6mils) lines in the same stack-up with the potential for lines >12mils**

Summary and Conclusions

- **Wide lines (7.4 mils) in organic Full Z-interconnect board have signal < 0.6 dB/inch loss @ 10GHz, and < 1.0 dB/inch loss @ 16GHz**
- **A Full-Z Taconic board can carry 25Gbps at least 12”**