Process and Assembly Methods for Increased Yield of Package on Package Devices

Brian Toleno, Ph.D. and Dan Maslyk
Henkel Corporation
Irvine, CA, USA
brian.toleno@us.henkel.com
dan.maslyk@us.henkel.com

Abstract
Increased functionality and smaller devices are significant drivers in innovative packaging designs. One of the newer package types to be introduced into the market place in the past few years is the package on package (PoP) devices. While packaging houses have been stacking die within memory and other packages for several years, this methodology is subject to known good die issues and other challenges that can drive up cost. In addition, this limits the designer on what functionality can be "stacked", since these come packaged together in a single unit. Stacking packages offers significant advantages from a design standpoint. As long as the pad designs are compatible, different device types can be stacked allowing for more versatility in the design and the assembly. On the other hand, assembling these devices on a standard SMT line can present challenges. Some assemblers purchase or acquire these devices pre-assembled, but the trend is towards assembling these on the printed circuit board (PCB) during a standard SMT process. Once solder paste is printed on the PCB and the first level component is placed, the attachment methodology of the second level device is not as clear. Therefore, in order to reflow these all in one pass alternative measures need to be investigated.

In this paper we compare the process conditions and yield achieved when assembling package on package devices utilizing different materials and methodologies. In all cases the devices were Pb-free devices with solder paste used for the bottom package. The material and process and materials were varied for the top package. The materials used for the top package assembly included tacky flux, solder paste, and an epoxy flux system. Once assembled the devices were tested for electrical yield, solder joint metallurgy integrity, and standoff height.

Key words: Package on Package, PoP, SMT Assembly

Introduction
With the continuous drive for smaller lighter and more advanced features on handheld products, Package on Package (PoP) assembly is increasing as a manufacturing option in manufacturing many devices.

Die stacking inside a package is one method that can be used to increase the functionality per unit area on a PCB. However, there can be some drawbacks to the stacked die solution. First, this method is a customized, fixed solution. If any of the functionality or footprint of one of the dies needs to be changed, then the entire die stack needs to be evaluated to see if changes are needed in the package. For example, a die shrink may occur which could change the whole package structure – requiring a change in the package. Second, each package is tested as a whole unit. If one or more of the dies fail, the whole unit will have to be scraped, which would lead to increased cost; this is the well-known "compounded yield" issue. Finally, an assembler having to coordinate the many semiconductor suppliers to provide dies to a packaging house to do the die stacking can be a challenging task.

In the PoP process, one component is placed on top of another package during one single SMT process. This stacked package structure utilizing the three dimensional aspect of the product. The topside of the bottom component has pads similar to the pads on the PCB along the perimeter to allow attachment of the top package. Each package is a single unit that can be fully tested as a normal IC package is done today, so the yield would be comparable to the normal yield commonly seen with CSP devices today. Another advantage would be the ability to have multiple source options that could be fairly easily inserted into the process. The stacked package can be processed in a traditional SMT environment with a few upgrades that are readily available. Therefore, package stacking enables configurable assemblies and provides greater flexibility in the supply chain. It can be used for memory applications or processor with memory, with faster time to market and better management of package testing and compounded yield issues.

The two main challenges in the assembly of these types of devices are top level component attachment and package warpage. While component warpage for CSPs is not often an issue, having two packages stacked on top of one another can amplify the effect of warpage. This warpage can affect yield, for example if the bottom package has a downward or "frown" warpage and

the top package has a upward or "smile" warpage, then the solder joints can be stretched or even become opens during reflow. This can be controlled by utilizing low-warpage mold compounds [1].

The other challenge, and the one addressed in this paper, is the attachment method used for the top package. After printing solder paste on the bare PCB and placing the components, the pads on the top of the bottom package are bare, therefore there needs to be a way of forming the interconnect for the top package.

The most common method used in early development is to dip the package in tacky flux [2]. In this study we explore additional interconnection options such as dipping the package in solder paste and an innovative epoxy flux system and explored the effect that these alternative methods have on reliability of the PoP devices.

First pass yield has been an issue with PoP for the top side package. This failure has been attributed to warpage of the components. It is proposed to test dipping a component into solder paste to see if any benefit could be detected that would assist in yield improvement.

Experimental

In this study we first examined different solder paste formulations for their component dip process capability.

The initial study looked at dipping the top CSPs in solder pastes of different configurations, see Table 1. In this experiment we chose to vary the amount of metal in the solder paste (metal loading) and metal particle size, as per the IPC J-STD-005 and J-STD-006 [4].

Table 1. Solder Paste Formulations for Dip Test

Metal Loading	Particle Size
88.5%	Type III (25-45 μm)
80%	Type III (25-45 μm)
70%	Type III (25-45 μm)
88.5%	Type IV (20-38 μm)
80%	Type IV (20-38 μm)
70%	Type IV (20-38 μm)
0%[1]	N/A[1]

1. Tacky Flux was also used as a control

All components were dipped to a height of 200 um, using an Universal Advantis pick and place machine using a modified flux dip tray. Initially, we examined the pattern and amount of material deposited by placing components bump side down on a glass plate and looked for bridging and the ability of the component to be dipped into the dip station and be removed. The mass of the material deposited was measured and the formulations that did not bridge and were able to be dipped were assembled and the solder joint gap size measured.

Based on this initial study we down selected a set of materials to test in the next phase where we built test vehicles for drop testing, see Table 2. In all cases a Pb-free solder paste (SAC 305 alloy), Type III particle size, was printed onto the PCB for the bottom component attachment.

Table 2. Materials for Top Component Interconnect

Tacky Flux A
Tacky Flux B
Solder Paste (70%, Type IV)
Epoxy Flux

Test vehicle printed circuit boards (PCBs) were designed according to the JEDEC specification [3], Figure 1. The PCBs used in this study were an 8-layer board, 1mm thick and an OSP finish. The components used in this study were Amkor (PSvfBGA) 12x12 305 PoP packages, Figure 2. The bottom device had a 0.5mm pitch and the top package a 0.65mm pitch; both devices were bumped with SAC305 alloy. The test vehicles were assembled in Henkel's SMT laboratory in Irvine, CA. The SMT line consisted of: DEK Viking Screen Printer, Universal Advantis Pick and Place, and Heller 1700W reflow oven.

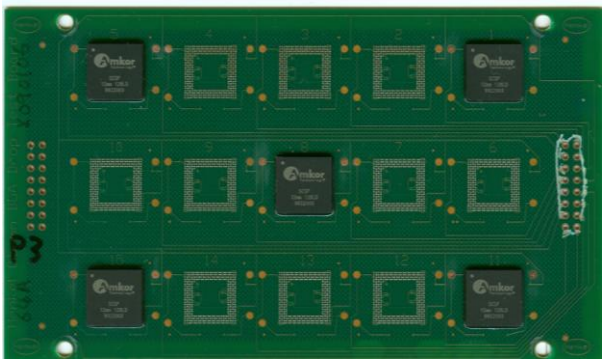

Figure 1. Drop test vehicle as per JESD22-B104.

Figure 2a. Images of PoP packages, bottom package (left) and top package (right).

Figure 2b. Cross section image of an assembled PoP device (underfilled).

Drop testing was conducted as per the JEDEC J22-B111 specification using a Landsmont model 15-D shock tester. Test boards are placed component side down on the fixture and dropped such that they experience a pulse of 500g with a pulse width of 0.5 ms, Figure 3. A change of resistance 10% or greater was determined to be a failure in this test.

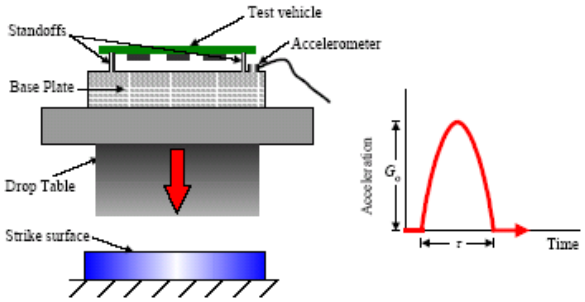

Figure 3. Sketch of drop test and pulse.

Drop Testing Methodology

As is widely acknowledged throughout the industry, many electronics manufacturers developed their own, custom-designed drop test requirements and test methods; an approach that has made similar materials and product comparisons virtually impossible. Because of this confusion and the inability to make valid, equal materials and product evaluations, the JEDEC

JESD22-B111 drop test standard was developed [4]. Now, using this standard, OEMs, CEMs and materials suppliers can make meaningful comparisons.

By definition, JEDEC JESD22-B111 provides a common test platform for handheld electronics products that fall under the consumer and portable market segments. Because these products are more prone to being dropped, electrical failures can occur and may result from various failure modes, including cracking of solder interconnections between the component and the board arising from excessive flexing of the board due to dropping of the handheld device. The test method provides a standard test vehicle design (Figure 1) and the drop test parameters in terms of pulse width and G forces (Figure 3). These drop test parameters are outlined in further detail in the JEDEC JESD22-B104 Mechanical Shock standard. This combination allows for the user to know the force being applied to any single site when the test is performed according to the specification. These standards provide a common test platform for evaluation of these potential failures.

Results

The initial solder paste dip testing showed that solder pastes with the highest metal loading proved to have too much tack force to allow for consistent solder paste dip. Also, the two materials with type III powder that were able to be dipped showed significant bridging, Figure 4.

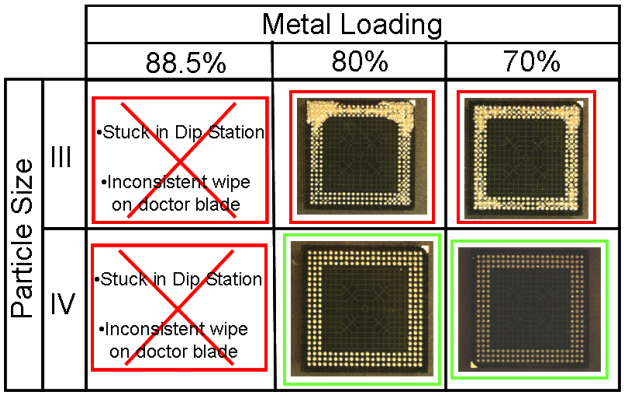

Figure 4. Images of top components dipped in solder paste.

The various gap heights measured using the different gap materials. The gap heights measured are shown in Figure 5. The largest variability can be seen with the tacky flux (which also provides the smallest overall gap). As expected the solder paste materials provide a larger gap, also the 80% Type IV (DAP) has the tightest distribution.

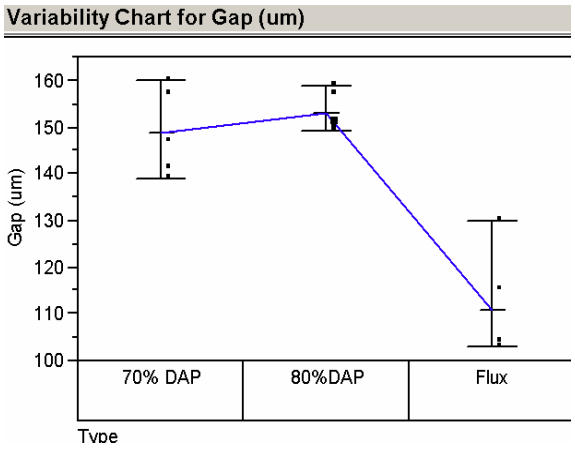

Figure 5. Gap height between top and bottom package as a function of attachment method.

Based on the results of the solder paste dipping studies above we moved forward with assembling PCBs with three different attachment methods for the top component: tacky flux (2 materials), solder paste dip (80% Type IV powder), and epoxy flux. The number of failures, determined by a 10% or higher rise in resistance, by drop is shown in Figure 6.

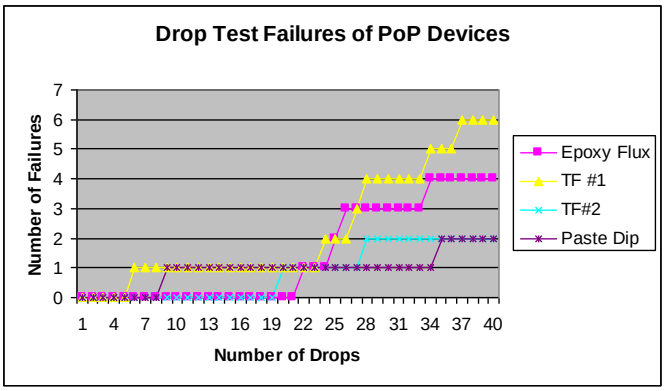

Figure 6. Drop test data on PoP devices.

Even though there is some variation between top device attachment methods, all but 2 of the failures detected were at the bottom package to PCB interface.

Failure analysis was performed on a small subset of devices that showed failures, utilizing a dye and pry method [5]. Devices were tested that showed failures at both top and bottom interconnections as well as devices that electrical failures detected only at the bottom interconnection. For the tacky flux system, in both cases we saw cracks on the top interconnection

Figure 7. Cracks found at the top interconnect on both tack flux devices tested using dye and pry.

On the left in Figure 7 we can see full cracks (these are the devices that had electrical failures on the top and bottom). On the right in Figure 7 we can see partial cracks – this is the device where we only detected electrical failures on the bottom interconnection.

For the solder paste dip system we found cracks on the top where we have electrical failures top and bottom (Figure 8, left). On the device where we only see electrical failures on the bottom, the dye and pry causes the device to fracture at the top interconnect, but there is no dye penetrating into the solder connection (Figure 8, right).

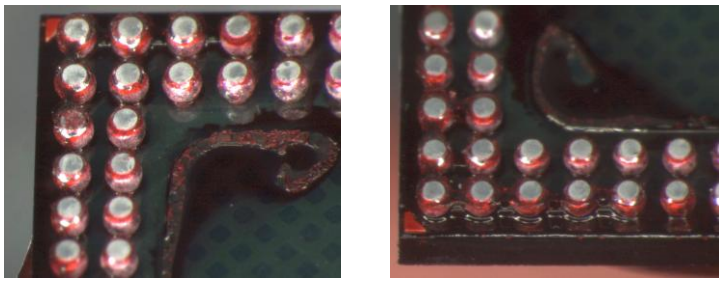

Figure 8. Cracks found on top interconnect only where there is an electrical failure at the top level for the solder dip process.

In the epoxy flux system we found that on the two devices tested, no cracks were found at the top interconnect. In fact, only one device fractured at all (at the top interconnection), the other had the stud, used to pry the devices apart, fail first, Figure 9.

Figure 9. No cracks found on epoxy flux system.

Conclusions

In this study we demonstrate three separate viable methodologies for assembling PoP devices. In addition to the more common tacky flux dip method, we have shown that utilizing a dip in a solder paste with the proper formulation provides a robust attachment method. In addition, a new epoxy flux system is also shown to provide a reliable attachment method.

The initial dye and pry results show that even when we only detect electrical failures at the bottom interconnect, we still see the weakest connection at the top interconnect. The flux dip also shows some partial cracks at the top interconnect, even with no electrical failure detected. In the case of the epoxy flux, where we also have an adhesive bond in addition to the solder joint, we see no cracks on the top interconnect. In one case with the epoxy flux we found that the device did not fracture at all, indicating a stronger interconnection.

We are continuing to explore the failure mechanisms of the devices in this initial study. In addition, we are looking into thermal cycling reliability and the effect of different underfill processes on the reliability of these devices. Some preliminary work shows a significant increase in shock/drop reliability when an underfill material is used (Figure 10).

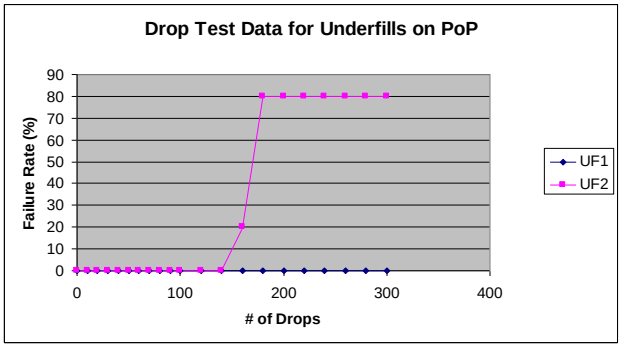

Figure 10. Preliminary Drop Test Data on Underfilled PoP Devices.

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5. ISTFA 2005: Proceedings of the 31st International Symposium for Testing.

PROCESS AND ASSEMBLY METHODS FOR INCREASED YIELD of PACKAGE ON PACKAGE DEVICES

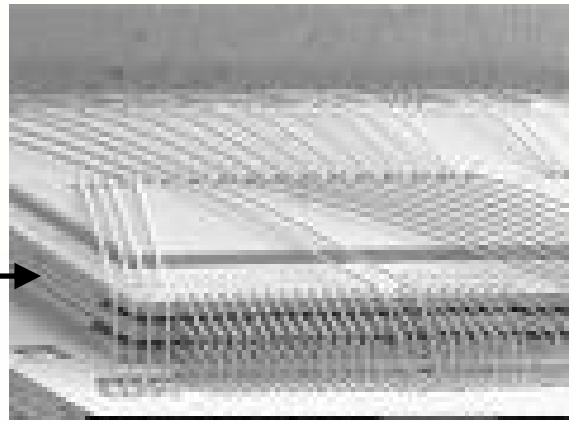
Dr. Brian Toleno and Dan Maslyk
Henkel Corporation
Irvine, California, USA

Outline

- Background
- Challenges
- Test Vehicles and Materials
- Results and Failure Analysis
- Conclusions
- Future Testing

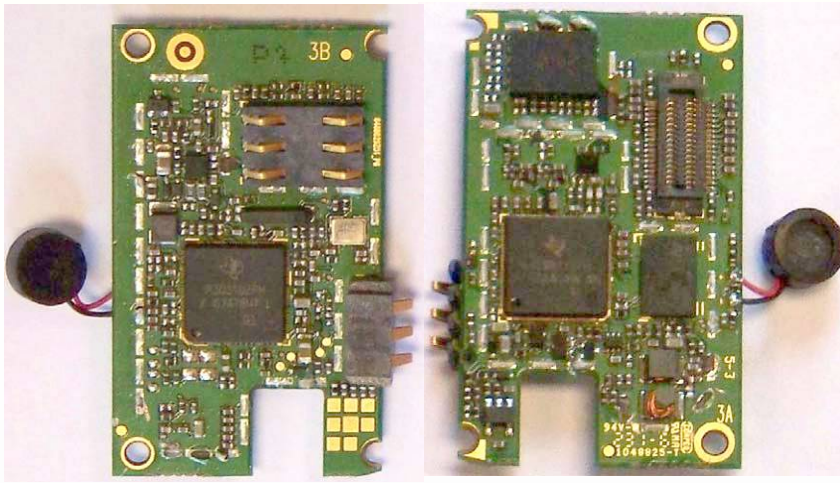
Background

- More functionality in a smaller footprint
- Stacked die in packages is "commonplace"
- Next step is to stack packages (CSP devices)
- Allows you to bypass some failure modes

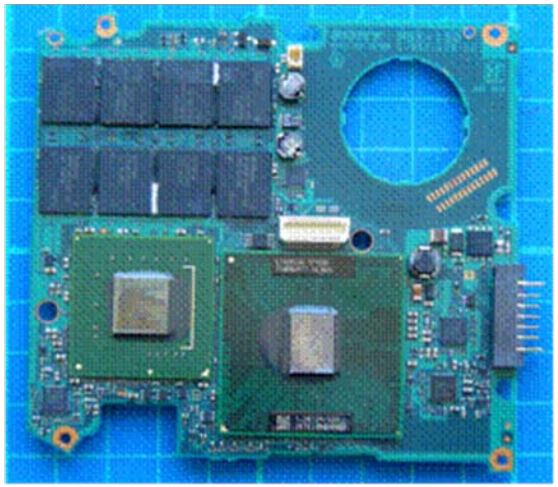


Mobile Phones

- Thinner Board
- PoP
- WLCSP



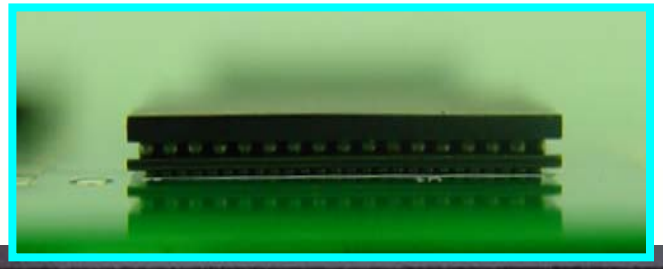
Laptop and UltraMobile PC



DDR2 DRAM Underfilled

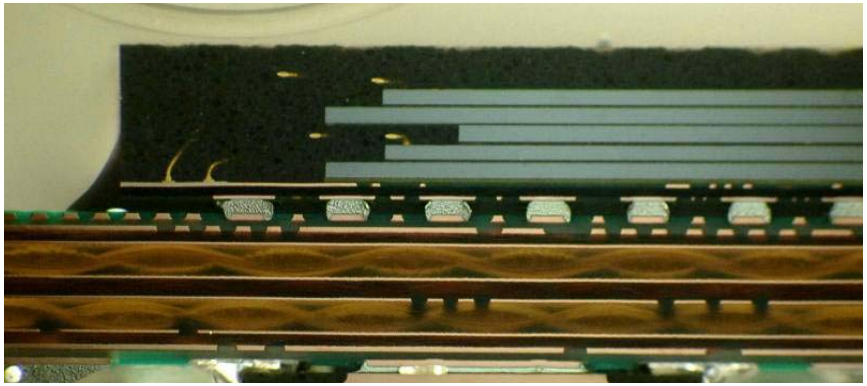
PoP (Package-on-Package)

CSP on CSP



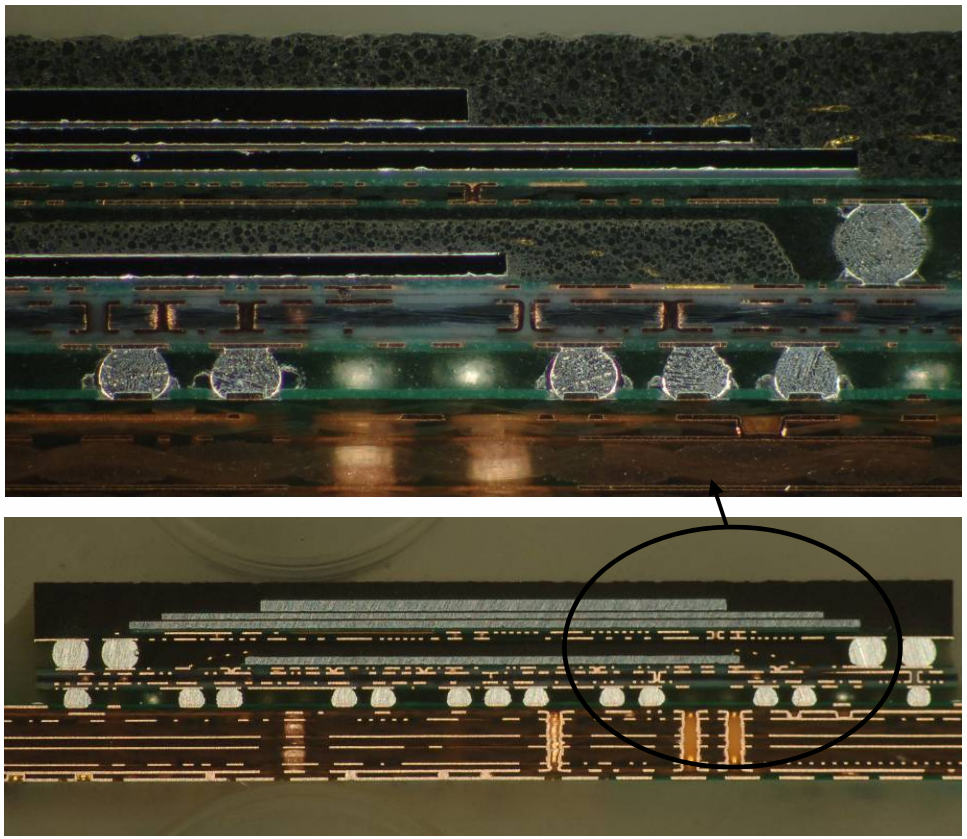
TSOP on CSP

CSP vs PoP



SCSP

Four Die Stacked Memory
with One Spacer Die



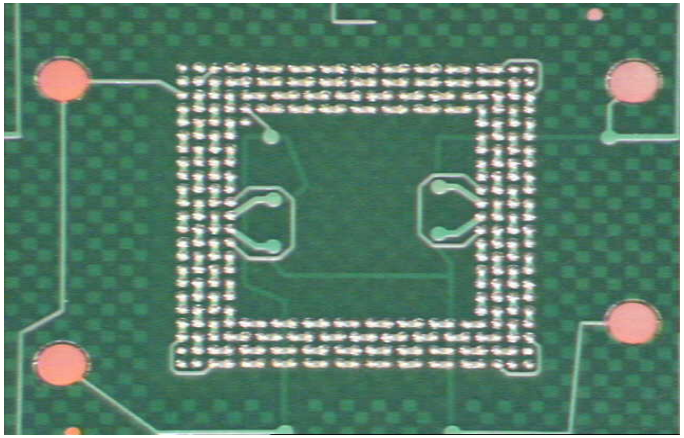
PoP

- Top; Three Die Stacked Memory
- Bottom; Single Die Digital Baseband

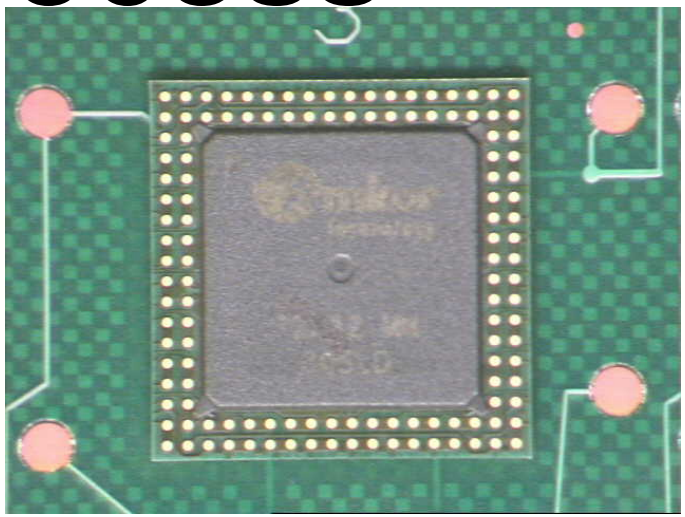
PoP Advantages over CSP

- Stacking fully tested memory and logic packages eliminates known good die(KGD) issues
- PoP stacking provides flexibility in mixing and matching IC technologies
- Devices can be procured from multiple mfg sources
- Meets accepted package and board level reliability standards for CSP

PoP Process



Solder Paste Printing

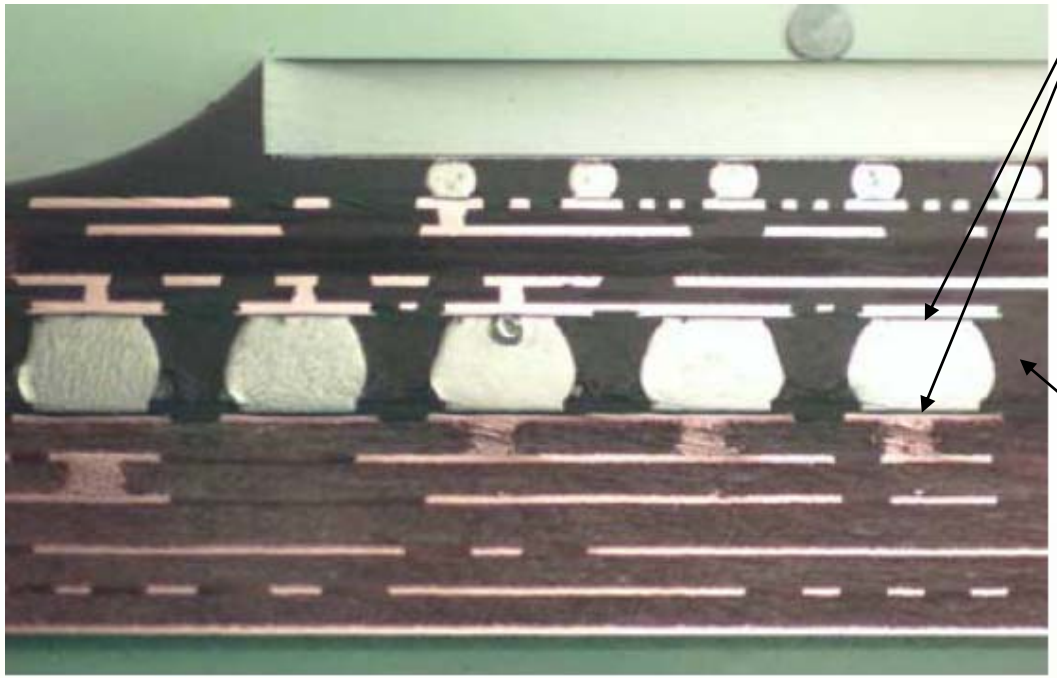


Bottom Cmpt Placement

Top Cmpt Placement

Reflow and Underfilling

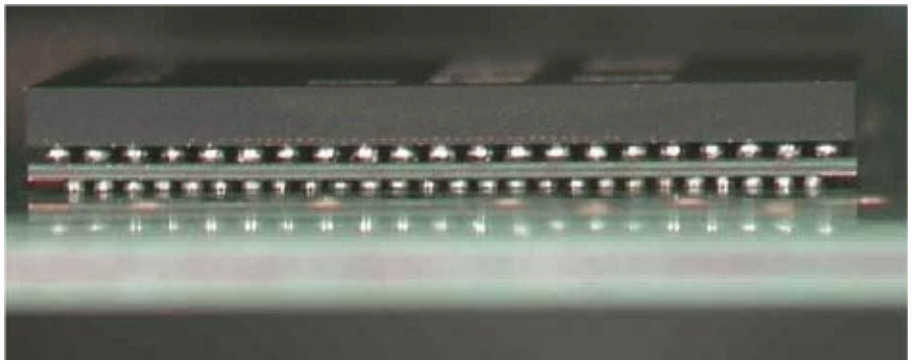
PoP Materials

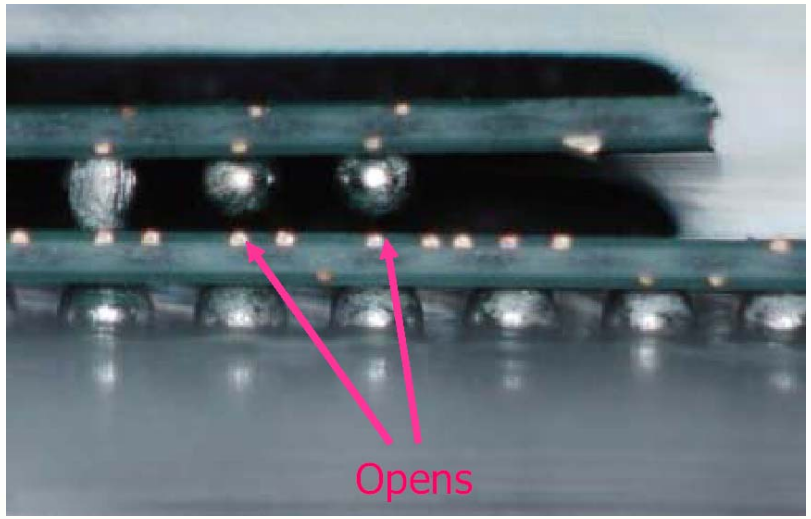


- **2nd Interconnect**
  - Solder Paste
  - Tacky Flux
  - Epoxy Flux
- **Reinforcement**
  - Underfill
  - CornerBond
  - EdgeBond

Factors affecting PoP Reliability

- **Package Warpage**
- **Alloy Composition of Solder Sphere**
- **Soldering Aids (Tacky Flux or Solder Paste)**
- **CSP Underfill**

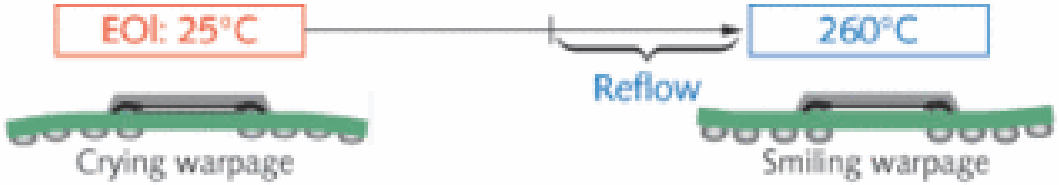




No Solder Connection on PoP Top Component because of Package Warpage.

Challenges

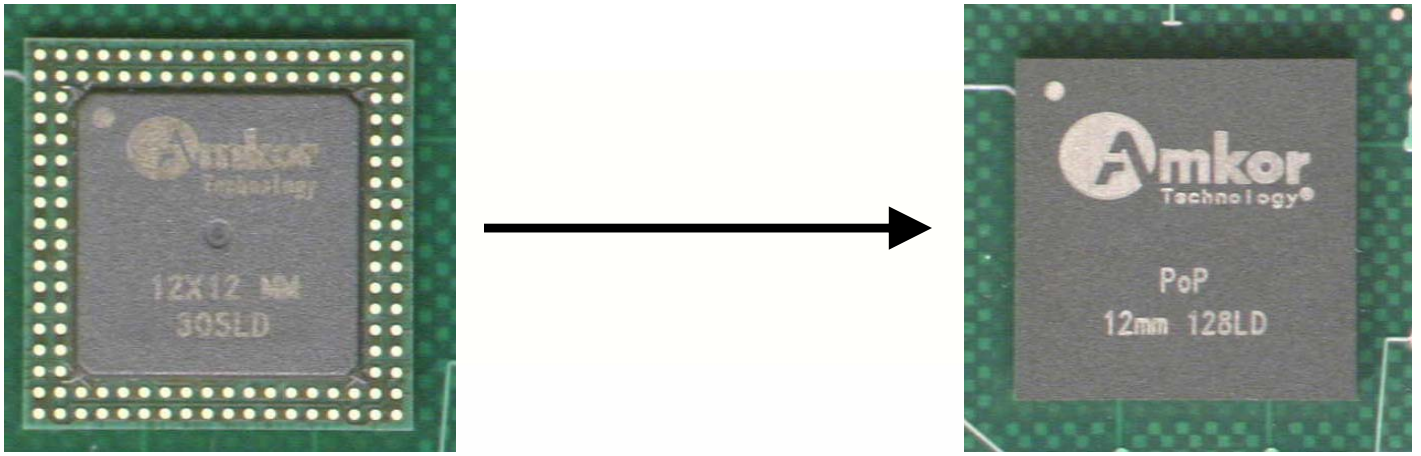
- New design and methodology
  - Obtain packages with “matching patterns”
- Warpage
  - Solder joint stres
  - Mold Compound



- How to connect at the second level?

Image from Advances Packaging, F. Carson and M. Bunyan, 2006

Challenges



- How to make the connection between the bottom and top package
  - Tacky Flux
  - Solder Paste
  - Epoxy Flux

Image from Advances Packaging, F. Carson and M. Bunyan, 2006

Experimental

- Examine various top PoP attach methods:
  - Connectivity
  - Drop test reliability
- Connection methods
  - Tacky Flux
  - Solder Paste
  - Epoxy Flux

Solder Paste Dip

Table 1. Solder Paste Formulations for Dip Test	
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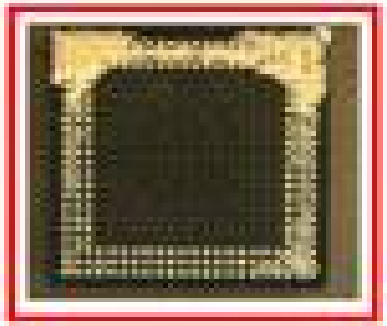
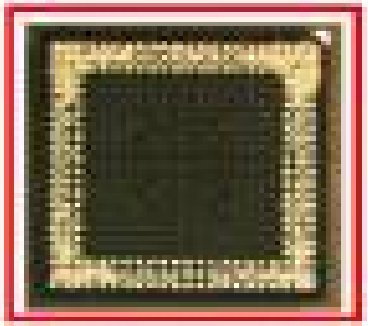
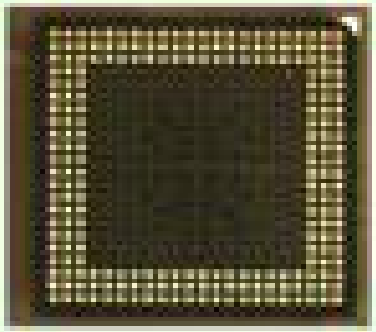
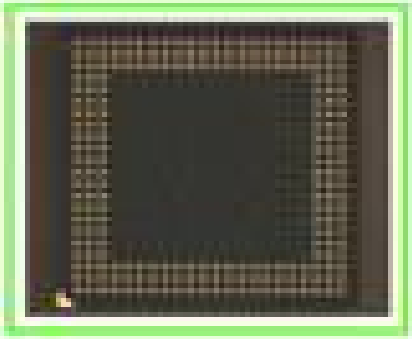
70%	Type IV (20-38 µm)
0%[1]	N/A[1]

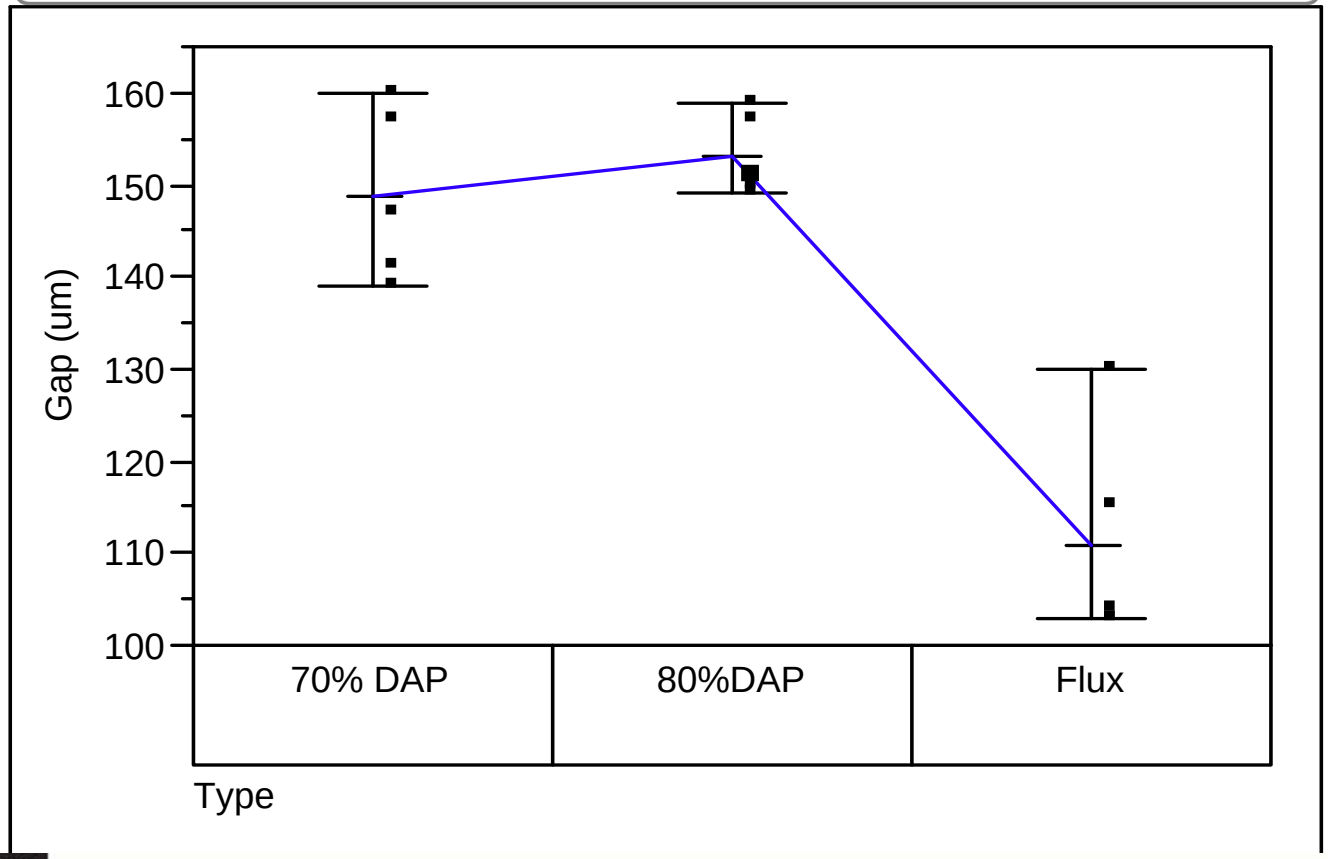
Solder Paste Dip

Particle Size	Metal Loading 88.5%	Metal Loading 80%	Metal Loading 70%
III	•Stuck in Dip Station •Inconsistent wipe on doctor blade		
IV	•Stuck in Dip Station •Inconsistent wipe on doctor blade		

Solder Paste Dip

Variability Gage

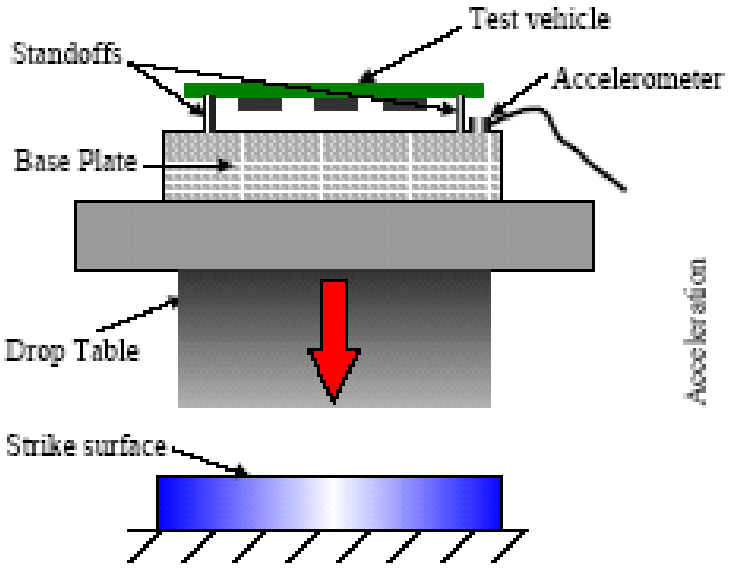
Variability Chart for Gap (um)

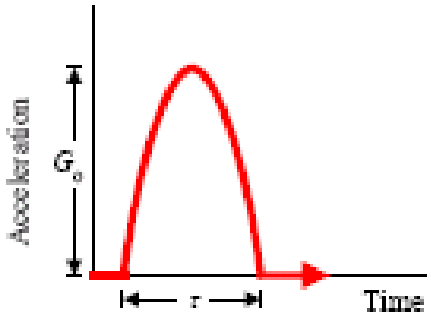


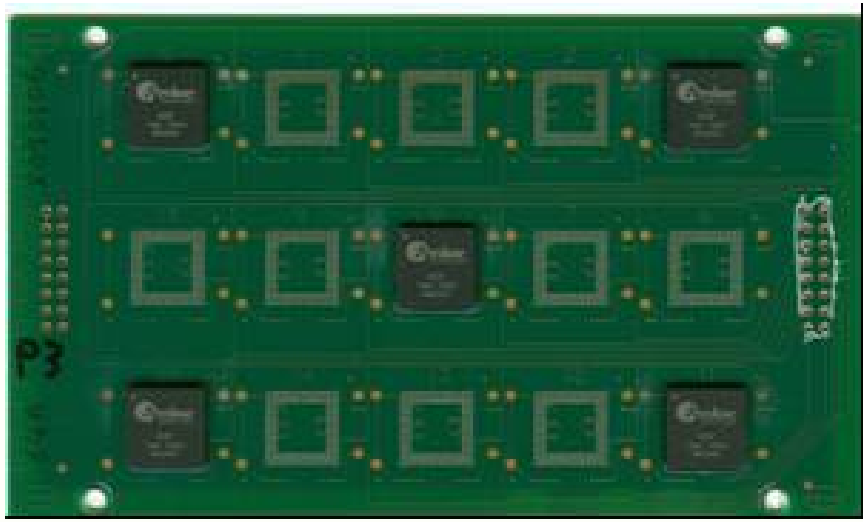
Drop Testing

- The drive for PoP is on mobile devices
- Mobile devices need impact resistance
- Test vehicles tested according to JEDEC JESD22-B111

Drop Test Method

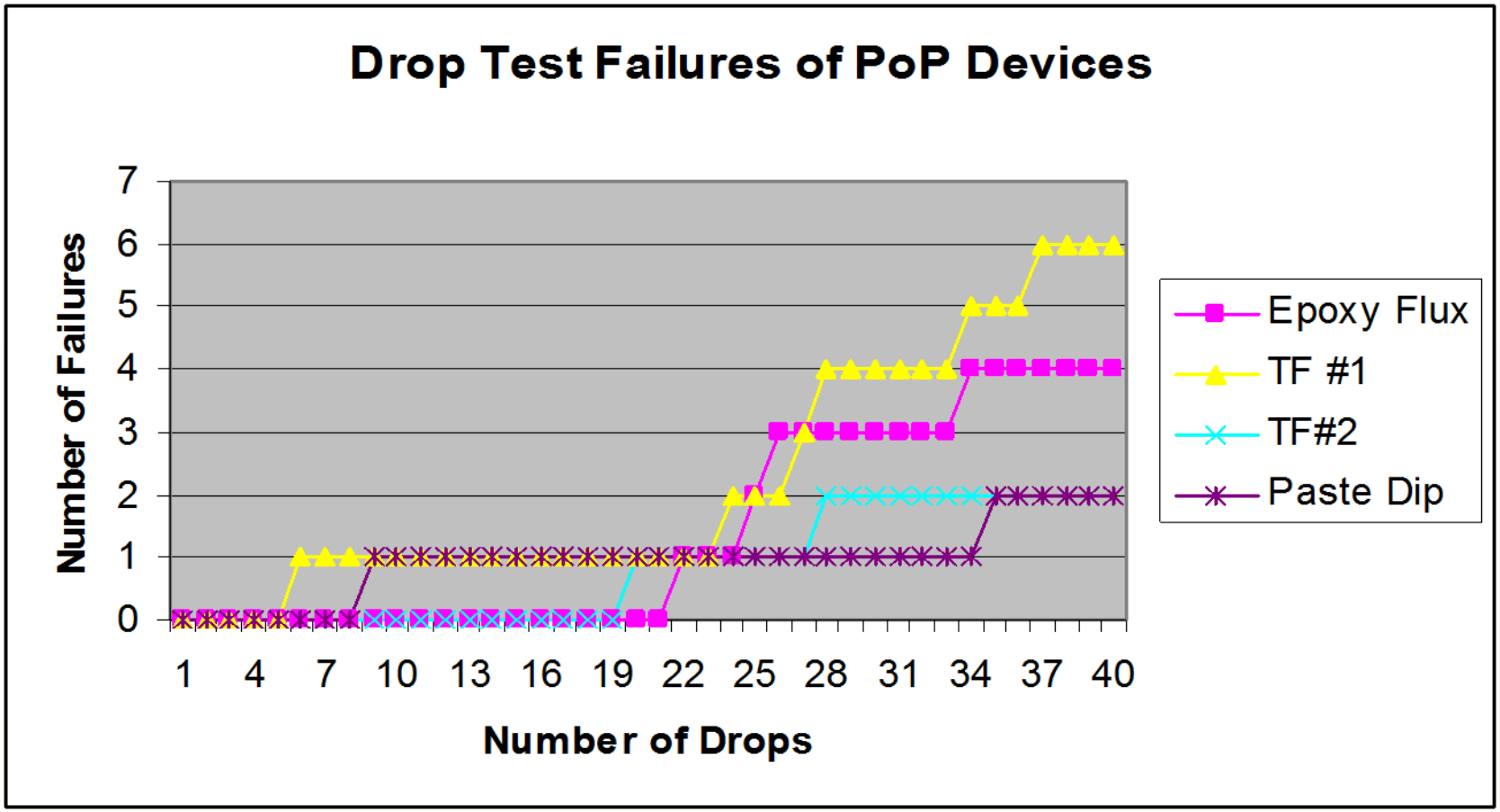






Drop Test

Drop Test Data

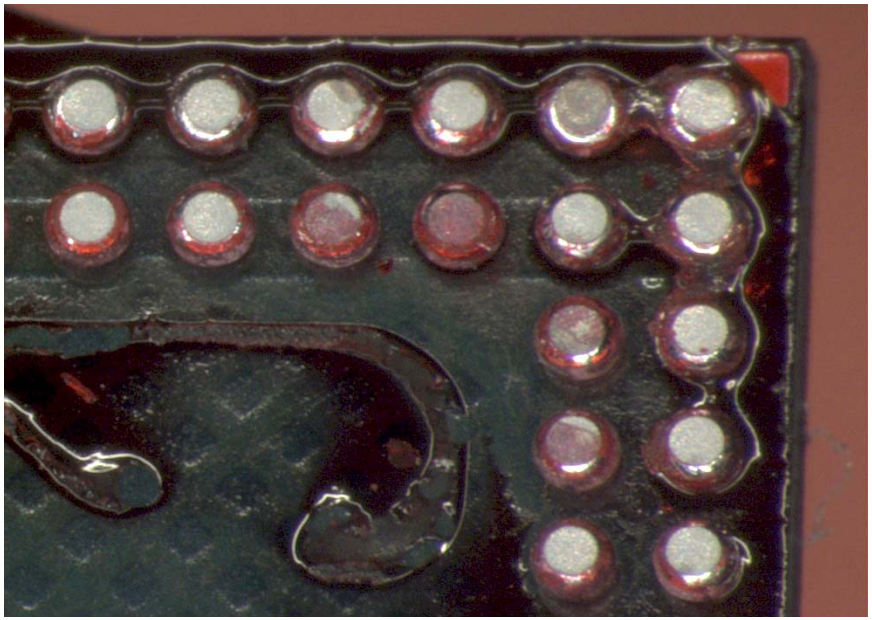


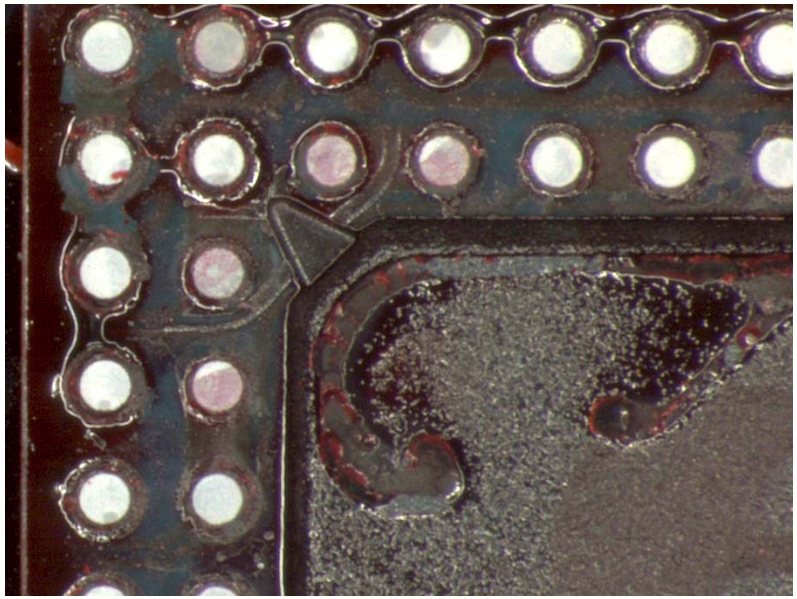
Drop Test Failures

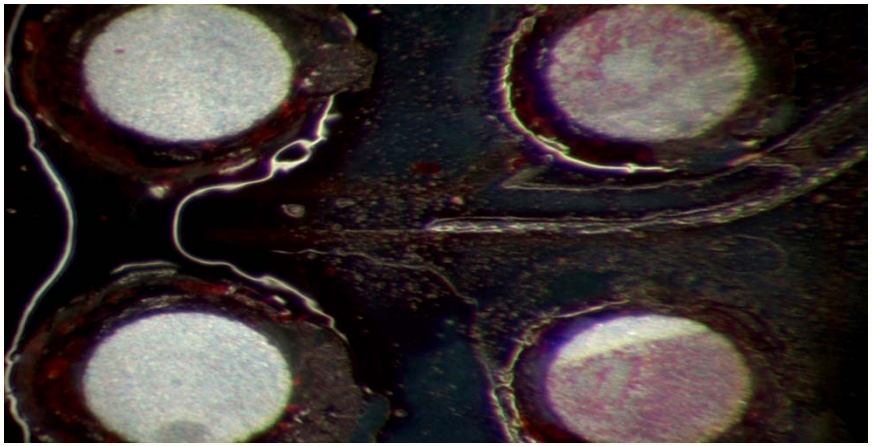
- Electrical resistance testing showed most failures at package-board interface
  - 12 out of 14
  - Greater than 10% resistance change
- Dye and pry of boards with and without top level failure

Failure Analysis – TF1

- Tacky Flux 1 system
- Electrical failure top and bottom
- Pre-existing cracks

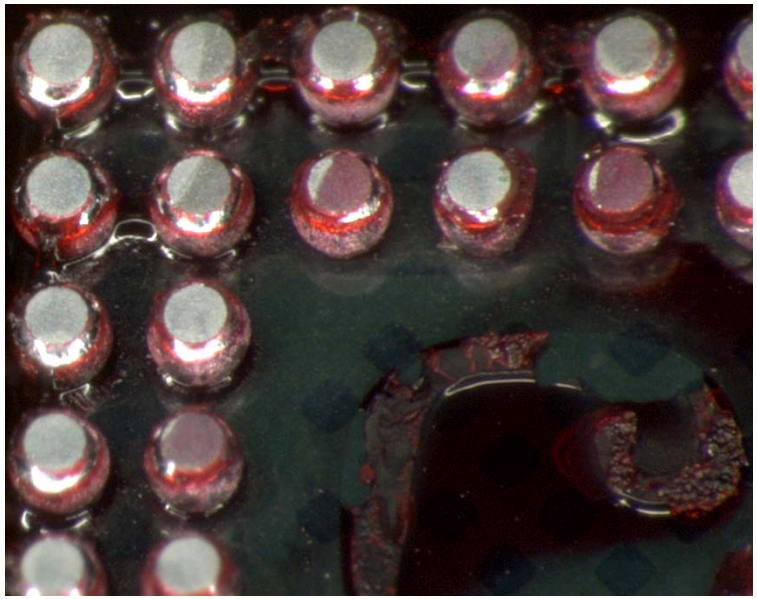


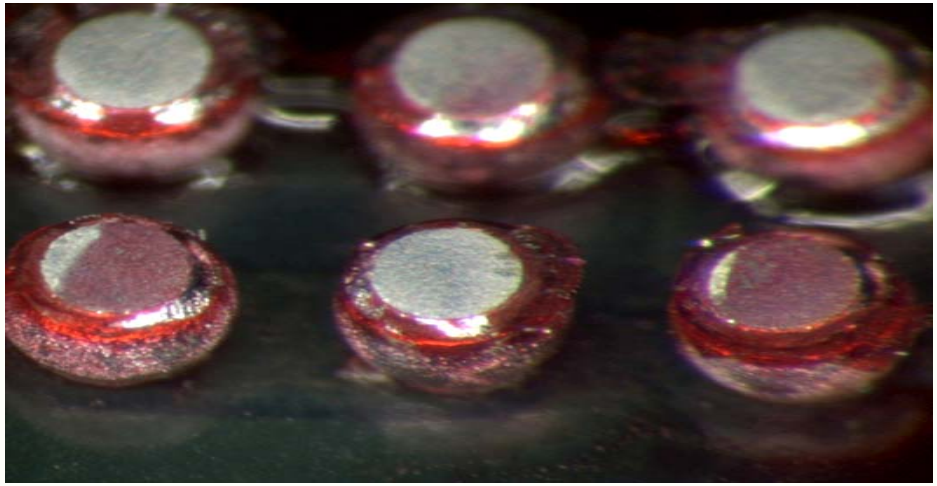




Failure Analysis - TF2

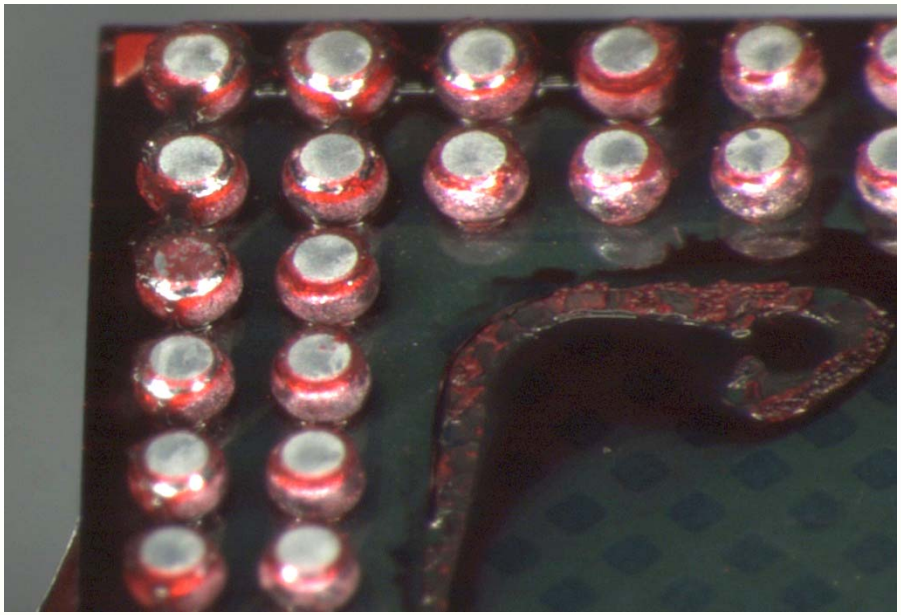
- Tacky Flux 2 System
- Electrical failure bottom
- Pre-existing cracks on top

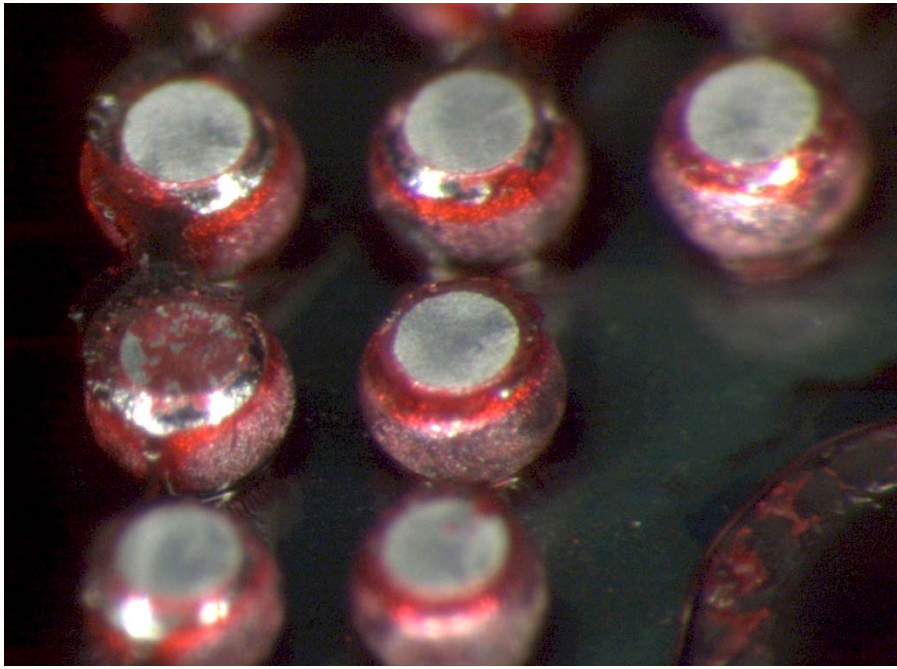




Failure Analysis – Solder Dip

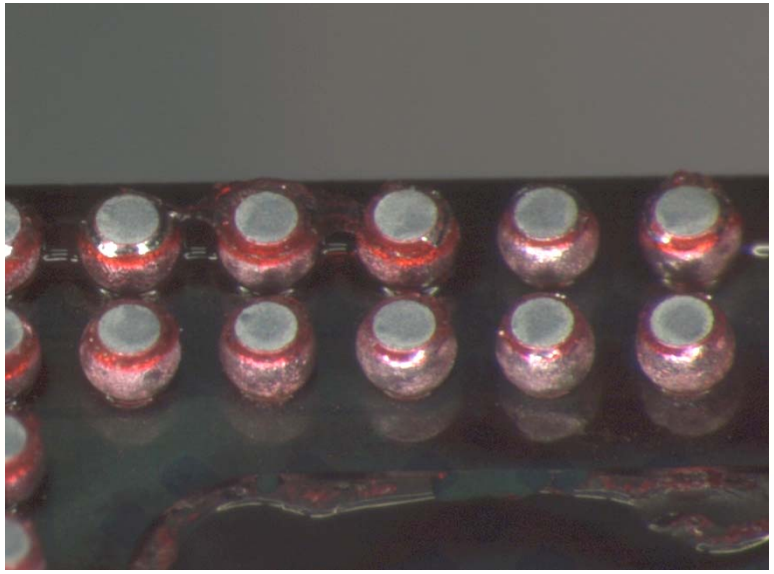
- Solder Paste system
- Electrical failure top and bottom
- Pre-existing cracks

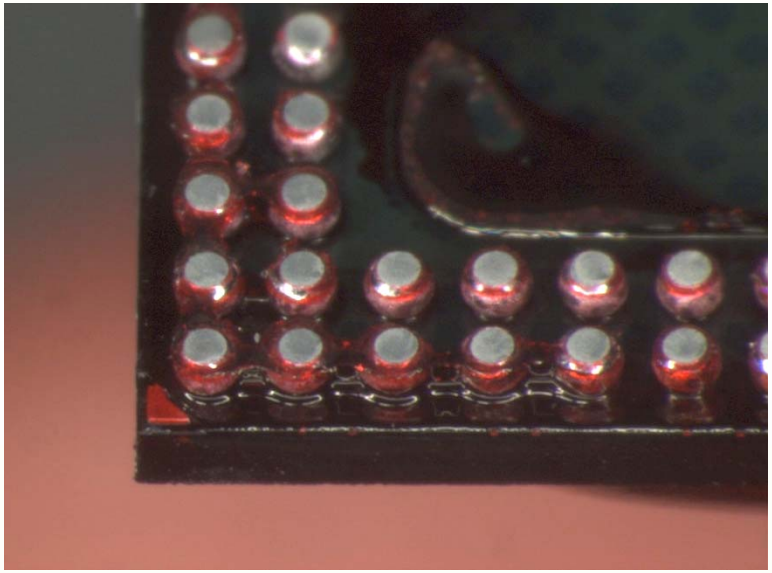


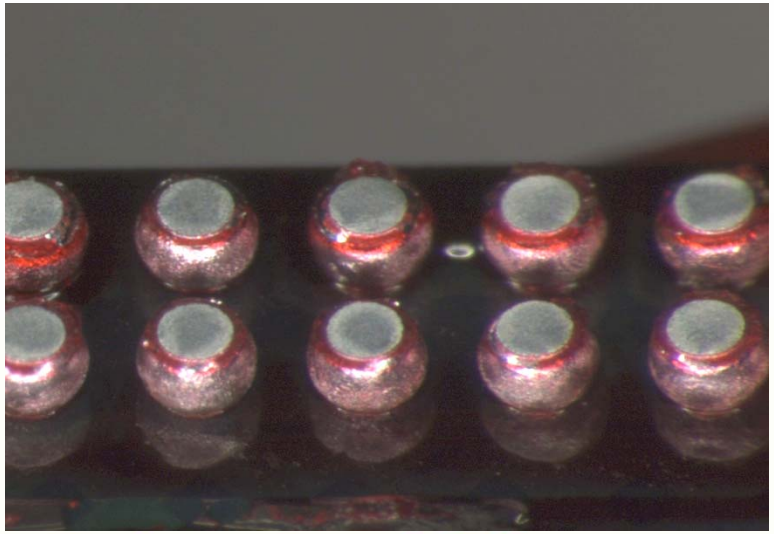


Failure Analysis – Solder Dip

- Solder Paste System
- Electrical failure bottom
- No Pre-existing cracks on top

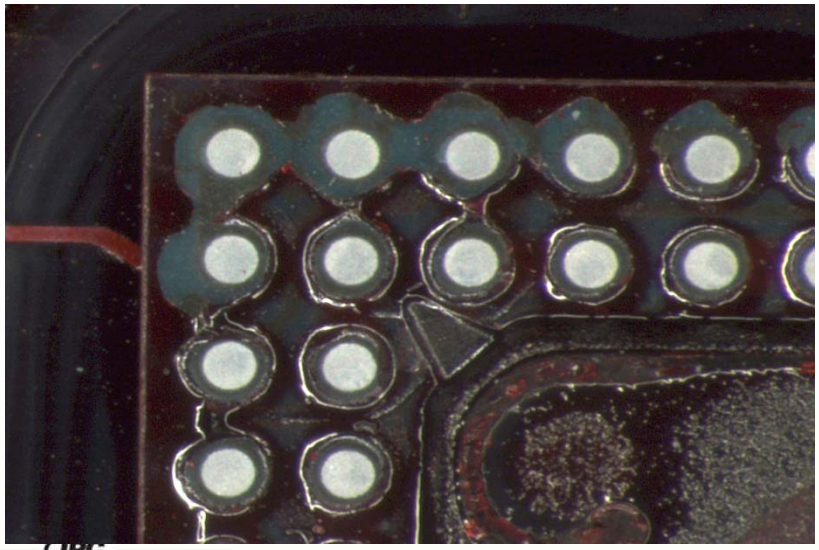


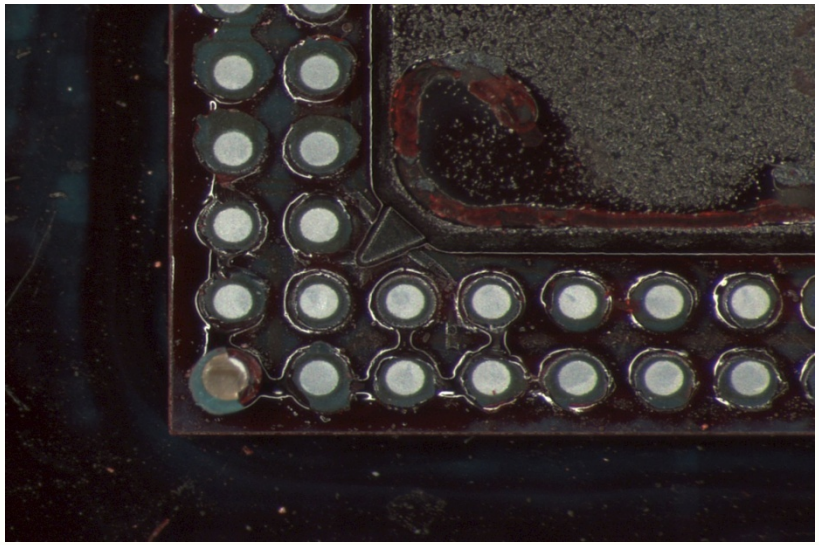




Failure Analysis – Epoxy Flux

- Epoxy Flux System
- Electrical failure bottom
- No Pre-existing cracks on top
- Second device, stud epoxy failure first





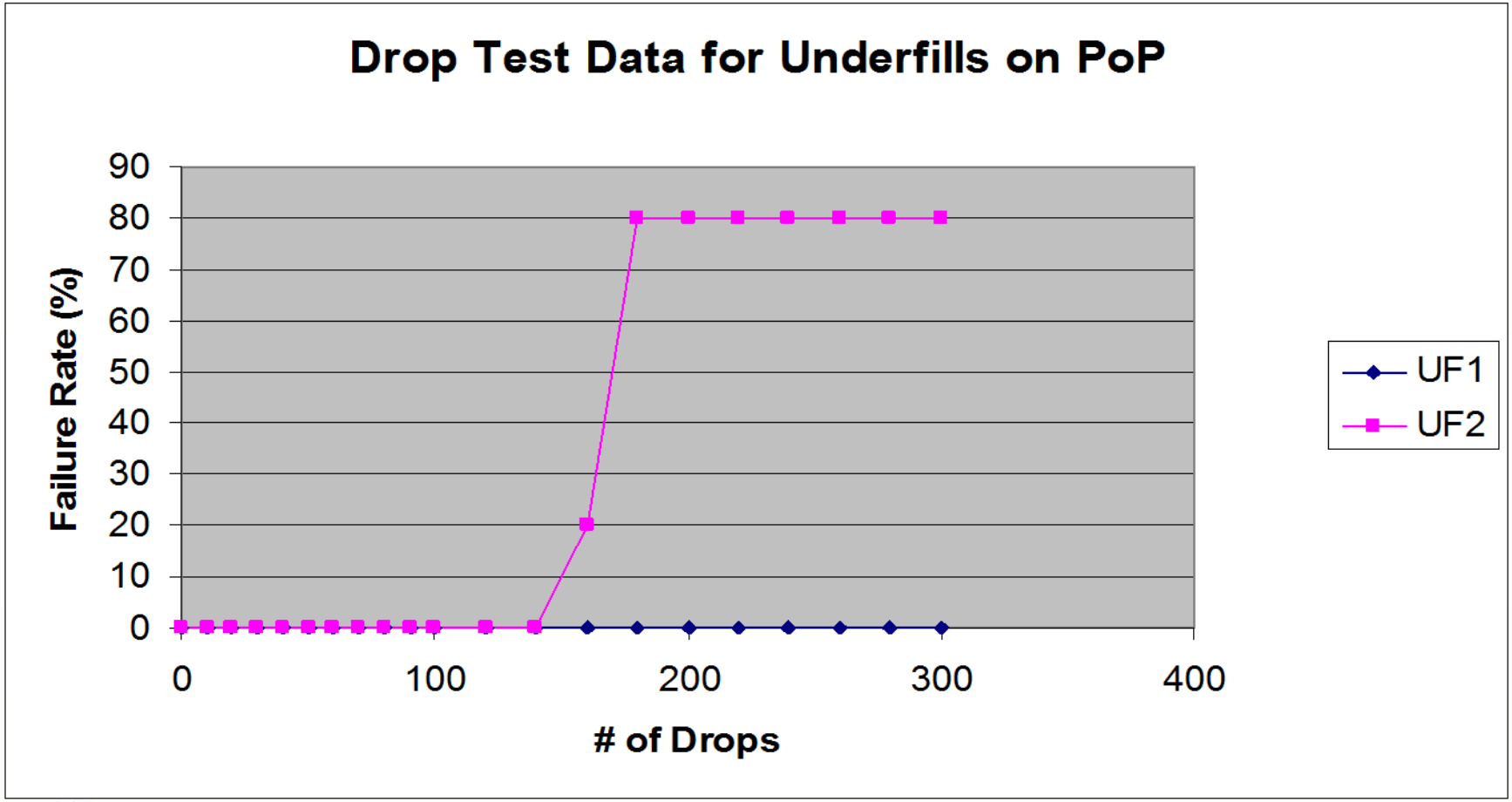
Conclusions

- Standard “off the shelf” solder paste formulations do not work well for “dipping”
- Variations in tacky flux will show slight differences in drop test performance
- Solder paste (dip formulation) provides increased strength and standoff height
- New epoxy dip flux materials provide connectivity and increased reinforcement
- First failure occurs at the board level with no underfill present

Future Work

- Working on evaluation of various underfill systems
  - Bottom underfill versus full underfill
  - Thermal cycling reliability
- Failure analysis of devices tested ongoing
  - Small samples size tested so far
  - Need additional samples to verify

Preliminary UF Data



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Thank You

Questions