Ultra-Thin 3D Package Development and Qualification Testing

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Abstract
The motivation for developing higher density IC packaging continues to be the personal entertainment and the portable handset markets. Consumers' expectations are that each new generation of products be smaller, thinner, lighter in weight and furnish greater functionality. The challenge electronic manufacturers face when competing in the global marketplace is to offer a product that will meet all functional and performance expectations without increasing product cost. To address the need for more functionality without increasing product size, a number of companies have adapted various forms of multiple die

3D packaging. A majority of these early, multiple function devices relied on the sequential stacking of die elements onto a single substrate interposer using a conventional wire-bond process. Because the wire-bonding of multiple tiers of uncased die is rather specialized and the die used may have had relatively poor wafer-level yields, overall manufacturing yield of the stacked-die packaged devices have not always met acceptable levels.

The information presented in this paper focuses on the stringent qualification requirements for a very-thin, vertically configure dμPILR package developed for high-volume memory and mixed function products. A key advantage of this innovative package-on-package (PoP) configuration is that each layer of the package can be pre-tested before joining. This capability greatly improves the overall manufacturing yield and the functionality of the final package assembly is assured. The material developed for this program will outline current environmental expectations for multiple function packaging for hand-held and portable electronic applications and detail the qualification test results for a number of memory variations using this unique, vertically-stacked package technology.

Introduction
The need for multiple function system-like packages has steadily grown in recent years and is expected to exceed ten billion units by the year 2010 (according to DataQuest). Most of the multiple die configurations (except some of the stacked memory devices) have been developed to service the consumer electronics market although they are also increasingly being used in medical and military applications as well. Consumer applications may include a number of functions unique to the product. For wireless handsets, for example, companies are looking for miniature package solutions for mixed functions. The device may combine logic and memory, logic + baseband + front-end functions, a full-function transmitter or transceiver. Any solution developed for this product category must be very thin, furnish a minimal package outline, be producible in very high volume and meet very competitive cost objectives.

Three primary factors that must be considered when developing a solution for high-density IC packaging are performance, reliability and cost. Although each factor carries equal status when assessing the merits of any packaging innovation, cost of the product will always influence adoption of one technology over the other. For a number of products, the stacking of several die within a single package outline provided a reasonably simple solution for a wide range of applications; however, when attempting to combine die having mixed functionality, overall package yield begins to rapidly diminish.
When silicon die having different functions are combined within a single component several negative issues must be addressed.

- Managing multiple IC vendors
- Known good die, test and burn-in
- Die and wafer availability/uniform quality
- Compound yield of less mature ICs• Accommodating incompatible die shrinks

In regard to 'die shrink', suppliers often attempt to refine the die to gain higher yield or to enable additional units to be furnished within the fixed wafer area. With each revision or refinement, the die could shrink 5% to 10% in area, changing the die outline and often rearranging the wire-bond sites. For die-stacked packaging, this occurrence often leads to major redesign of the package substrate and component stacking sequence.

Die stacking does have appeal for some applications because two or more die can share a single substrate. Stacking die, however, is not without its share of problems. Stacking the same size die, as an example, becomes more of a sequential die

attach/wire-bond process that requires spacers between each die layer. When different size die are used in the stack, the assembly process is somewhat simplified. With the larger die as the base, the progressively smaller die can be attached in a pyramid fashion for a single stage wire-bond process. The concerns package assemblers have struggled with, with these tiered-die configurations, is uniform quality of each die in the stack and uniformity of the plating on the wire-bond sites.

Early Package-on-Package Innovations

To overcome many of the yield problems manufacturers have experienced with multiple-die packaging, companies are each layer before they are joined to the other (or others). Stacked solutions also enables consecutive pre-test and burn-in for memory and other functions before joining (typical of ball-stack configurations shown in Figure 1).

Figure 1. Vertically stacked µZ® FBGA for high-performanceand higher density applications ***(Tessera).***

The process of layering packages allows the sourcing from several suppliers for the same function. Even though the die size and wire-bond sites may be unique from one supplier to the other, the substrate can be designed with a common outline and with a compatible I/O configuration.

Addressing the Need for Greater Contact Density

Although the ball contact has proven to be ideal for a majority of array package applications, the developers of chip sets for handheld electronics have expressed their goal to develop multiple function packages that have a smaller foot print than currently offered. Their goal is to furnish packaged devices with an outline no greater than 12.0 mm square. A package outline of 10mm square would be even better; however, current FBGA configurations restrict contact pitch capability. To meet the I/O density for the next generation of mixed function 3D packaging, companies are already addressing the adoption of 0.4mm and even 0.3mm contact pitch. Although widely used for single die wafer-level CSP (WLCSP) and flip-chip applications, the finer pitch for BGA packaging is proving to be very difficult to adapt using current solder assembly processes.

Companies are finding limited success when printing and reflowing the solder on the contact sites but the profile on the resulting bump contacts do not always meet the established tolerance criteria for uniformity. Attaching preformed solder spheres to the package has, up to now, proved very satisfactory but handling and attaching the preformed < 250 micron diameter solder spheres needed for the reduced pitch product has proven to be very difficult for package assemblers and test service providers. Table 1 reflects the contact size variations and recommended land pattern geometry for future ultra fine pitch package variations of 0.4mm or less.

Table 1: Contact diameter to land pattern recommendations

Nominal ball or bump diameter (mm)	Nominal land diameter (mm)	Ball-to-land size reduction (mm)	Land diameter Variation (mm)
0.25	0.20	20%	0.20 - 0.17
0.20	0.15	20%	0.15 - 0.12
0.15	0.10	20%	0.10 - 0.08

Source: IPC-7094

As a solution for improving component density, it becomes evident that the traditional ball contact may have become a roadblock for both package developers and users. To better accommodate the expectations of higher density array packaging, it was inevitable that a totally different approach to contact design must be explored.

New Innovation for Package Substrates

The dielectric base widely used for array packaging relies on copper conductors to interface die and land patterns for attaching ball contact features. The ball contacts are added after the package assembly and encapsulation processes are completed. The µPILR™ package substrate platform described in the following text is different. The substrate is actually furnished with all contact features in place before package assembly.

Rather than providing solder bumps or attaching solder spheres to the substrate following package assembly, the contact features are furnished as an integral part of the base substrate as shown in Figure 2.

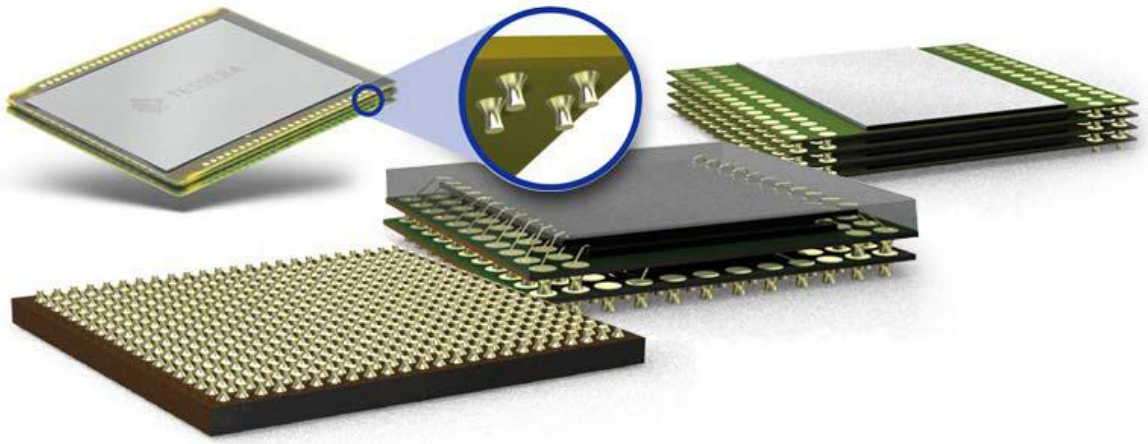

Figure 2. The etched µPILR™ contact array provides near perfect planarity for all contact features *(Tessera)***.**

When comparing the µPILR package structure to the current stacked solder ball package configurations, the fabrication process enables a much smaller diameter and lower profile contact feature providing the user with a significantly thinner finished package profile.

Substrate Fabrication Process

The contact features are etched into a unique tri-metal copper-nickel-copper composite having an 80 to 180 micron thick rolled copper base. The additional metal layers are furnished by electroplating a very thin < 1 micron layer of nickel alloy followed by the electroplating of 9 to 18 micron thick copper. The nickel layer provides an etch barrier when chemically etching the thin copper for in-package circuit routing. The thicker rolled copper layer is reserved for the µPILR contact formation. The typical single circuit layer substrate fabrication process begins with imaging and chemically etching the circuit pattern. A dielectric is laminated over the etched circuit pattern side of the base composite. The contact pattern is imaged onto the thicker copper surface and chemically etched to yield the finished solid copper contact profile. Following the etching process a photo-imaged mask is applied onto the contact side of the substrate, wire-bond and outboard contact sites are laser ablated and all exposed copper features are protected with electroless nickel and immersion gold. The µPILR package platform not only enables a much finer pitch capability, it maintains a near perfect contact coplanarity. The key to the µPILR interconnect technology is the tri-metal base material (see Figure 3).

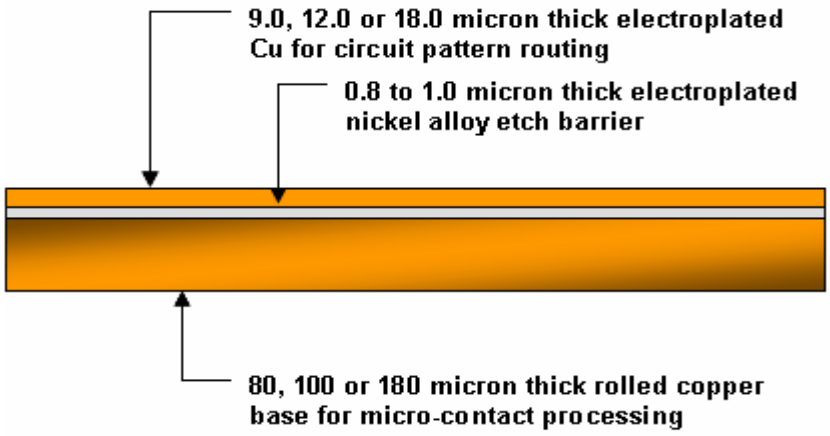

Figure 3. Tri-metal base material for the µPILR™ substrate.

Because the thickness of the base copper can be varied when the foil is initially rolled, the contacts can be designed to have a standoff height from 80 to 180 microns, depending on the application and, although the contact base diameters range from 65 to 375 microns, contact tip diameters will be only 40 to 200 microns in diameter. Figure 3 illustrates the resulting substrate structure.

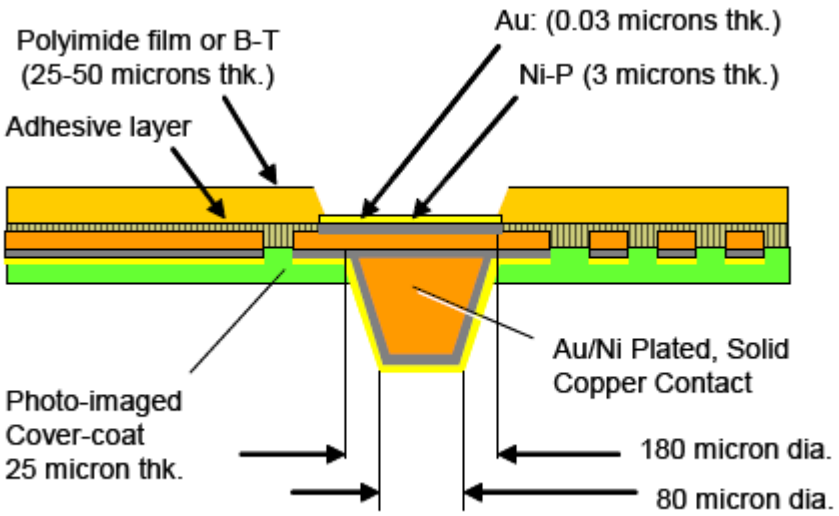

Figure 4. µPILR™ substrate cross-section.

Substrate fabrication sequence:
1. Photo-image and chemical etch Cu circuit pattern
2. Laminated dielectric onto Cu circuit pattern
3. Photo-image and chem.-etch Cu contact features
4. Chemical etch exposed Ni barrier layer
5. Apply, photo-image and develop solder mask
6. Laser ablate interface and wire-bond features
7. Plate Ni/Au finish on exposed copper features

Package-on-Package Development

To date, a number of products have been developed for OEM companies using the µPILR substrate technology and several variations of memory test packages have been manufactured, mounted onto standard IPC test platforms and undergone extensive physical testing and evaluation. A new test vehicle was recently developed within Tessera's laboratories to address the projected requirement for mixed function applications. The test package is a two section, 12 mm square design with two circuit layers on both lower and upper sections. The additional circuit layers have been added to better represent the anticipated in-package interconnect requirements for higher density silicon designs.

Combining logic functions with memory in a single package outline has always proven difficult. The testing and burn-in requirements for memory devices are very different than that required for the logic functions. When companies stack these elements within a single package outline (die-stack), the radically different die sizes and die quality often affect package assembly yields. Separating these functions for assembly and test and later joining package sections (package-on-package) has proven far more practical for both supplier and user companies. The sections can be supplied as separate units and joined together at the board-level assembly stage or furnished as a single package-level product, thoroughly tested and ready for PCB mounting.

If the decision is to join the sections at the board-level assembly, the baser package can be placed onto the board and the memory package placed sequentially onto the mating contact matrix of the base for simultaneous reflow soldering. This alternative has two benefits. It allows the user to specify multiple variations (different memory functions, data rate and so on) as well as accommodating secondary sources of supply.

Test Vehicle Description

The base section of the test vehicle has contact features on both top and bottom surfaces. The top surface was designed to mount a logic die and mate with a second layer package. The bottom surface of the lower substrate section is furnished with Ni-P (3 microns thk.) Au: (0.03 microns thk.) Polyimide film or B-T (25-50 microns thk.) Photo-imaged Cover-coat 25

micron thk. Au/Ni Plated, Solid Copper Contact Adhesive layer 80 micron dia. 180 micron dia. partially depopulated array of 672 I/O µPILR contacts on 0.4mm pitch. The top surface of the lower substrate section has 168 contact lands furnished in two rows of 0.5mm pitch on the package perimeter for interface to the upper level package section as illustrated in Figure 5.

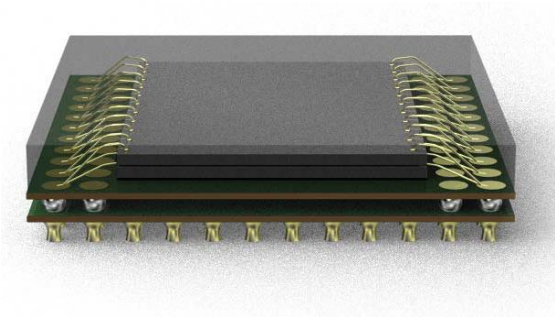

Figure 5. Two section µPLR logic + memory test package ***(Tessera).***

The upper level substrate was designed to accommodate a memory die and is furnished with µPILR contacts in two perimeter rows of the bottom surface to mate with contact lands on top of the lower package substrate.

Mixed Function Package Assembly

Package assembly utilizes an already established µBGA® infrastructure. For efficient assembly processing the substrate is typically furnished in a narrow multiple site strip-array format. Die elements are first attached to the top surface of the substrate with active face up using a low modulus dry film type die attach adhesive. Following die attach, conventional wirebond process are used to complete the die-to-substrate interface. The die are then over-molded and laser marked. To accommodate the stacking process, a fine-grain 'SAC 305' solder paste is printed onto the land patterns on the top surface, reflow-soldered and finally singulated, electrically tested and transferred to a standard JEDEC matrix tray carrier. The actual stacking process is relatively simple. Using commercial pick-and-place assembly systems, the lower package sections are transferred from the carrier tray to a specially configured, multiple cavity fixture (see Figure 6).

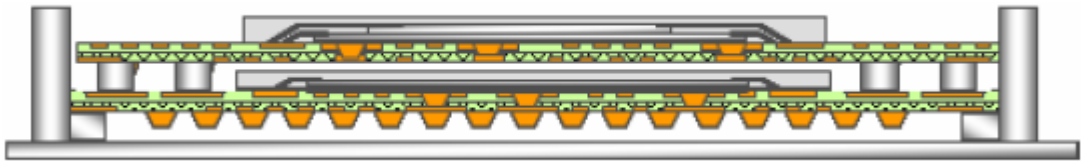

Figure 6. Fixture maintains µPILR package alignment during joining process.

The fixture is designed to align and support the package units without excessive physical loading on the µPILR contacts. The upper package sections are transferred from their respective carrier tray, automatically dipped into a shallow reservoir of flux and placed on top of the pre-soldered contact sites on the lower package sections. When all devices are placed, the fixture is transferred to a conveyor type multiple-zone convection oven for reflow processing, completing the package joining process.

Printed Circuit Test Platform

When developing the circuit board for attaching any surface mount device, the designer must consider the physical conditions that the product will experience during the board-level assembly process. Use of lead-free tin/silver/copper solder alloys is currently in wide use in compliance with European Union (EU) regulations. Both package and PC board may be exposed to multiple cycles of solder reflow temperatures exceeding 235ºC. It is critical that the laminate materials and surface finish selected for the board be compatible with the thermal extremes required for reflow soldering and the number of exposures anticipated in completing the assembly.

The industry has established specifications for variations of glass reinforced-epoxy laminate compositions that are both compliant with RoHS and meet the UL FR-4 requirements. The materials and physical characteristics for each laminate type are detailed within the IPC-4101, a publication developed by a subcommittee of experts representing a number of manufactures and users of the materials. The specification sheets (generally referred to as 'slash sheets') outline the requirements for each product grade and include requirements for physical, electrical, thermal and environmental properties for both laminate and prepreg base materials. All of these FR-4 grade laminates have an epoxy-resin base and use some form of woven glass fiber for reinforcement. The IPC-4101/126 and /129 specifications define a glass transition temperature (Tg)

170ºC and a decomposition temperature (Td) rating of 340ºC, far more robust for lead-free soldering than the other FR-4 laminates.

The PCB developed for the qualification test and evaluation of the logic + memory µPILR package has eight circuit layers and was fabricated using commercial glass reinforced FR-4 laminate. The dimensions and construction of the test board meets the requirements specified in IPC-9701. Each board has 15 device mounting sites equally spaced within the central section of the board outline with a pattern of plated holes located around each mounting site and at opposite ends of the board for hard wire interface during environmental testing.

Test Board Description-
• Outline Dimensions: 77.0 mm x 132 mm
• Circuit Layers: 2-4-2 Build-up Construction
• Finished Board Thickness: 1.0 mm +/- 0.07 mm
• Core Dielectric: FR-4 Multifunctional (Tg > 170ºC)
• Core Dielectric Layers: 6 @ 0.13 mm ea.
• Cap Layer Dielectric: Resin Coated Copper
• Cap Dielectric Layers: 2 @ 0.065 mm
• Solder Mask: Liquid Photo-imaged (IPC-SM-840)
• Surface Finish: Organic Surface Preservative
• OSP Coating Rqmt.: > 5 x Reflow Process

Land patterns are interconnected in a daisy-chain fashion to continue the electrical conductivity of the package units mounted on its surface. The circuit conductor metallization connecting lands are 50 microns. Registration of the solder mask opening around the 0.4mm pitch land patterns is critical. The test boards are fabricated in the conventional 18" x 24" panel format and singulated after all process steps have been completed. Solder mask is applied as one of the final process steps and registration of the mask and land pattern must be very precise. Although some tolerance allowances must be tolerated, there can be no mask overlapping onto the land pattern surface. To achieve the alignment criteria, the fabricator adapted a step and-repeat imaging process that exposed the photo-imageable mask coating at each test board location.

Board Level Assembly
Circuit board assembly is very typical of most surface mount processes beginning with solder paste printing, pick-and-place and reflow soldering. The stencil used for printing is a 100 micron thick stainless steel foil with laser ablated 270 µm square apertures. Because of the very small stencil aperture, the solder paste used for this program was a Type 5, RoHS compliant SAC 305 alloy composition. Precise placement of the 0.4mm pitch components is critical as well. Although the somewhat tapered shape of the 0.4mm pitch µPILR contact narrows down to a diameter as small as 50 microns, placement accuracy should not exceed +/- 20 microns to assure a reasonably uniform solder fillet at all contact sites.

The reflow solder process for the test board's assembly utilized a ten zone convection oven. The overall cycle time for the process for the lead-free alloy used was approximately six minutes, the time above liquidus (220ºC) will generally vary from 60 to 90 seconds (depending on mass) and rising to a peek temperature at or above 235ºC for up to 30 seconds.

Environmental Testing for Package Qualification
A number of industry standard specifications have been selected to develop a comprehensive environmental test process. Many standards associated with the manufacture of this test vehicle are currently being modified by the industry to account for the changes in manufacturing conditions required by the lead-free solder alloys. Modifications have been required to account for the higher second-level manufacturing process temperatures required for Sn-Ag-Cu or other alloys, and the impact that this has on all the materials involved. The test methods adopted for the qualification of the 0.4mm pitch logic + memory package include the following IPC and JEDEC standards:

• IPC/JEDEC J -STD-020 Moisture Sensitivity
• IPC-9701 Temperature Cycle
• JEDEC JESD22 -A104 Thermal Shock
• JEDEC JESD22 -A102 Pressure Cooker Test
• JEDEC JESD22 -A103 High temperature Storage
• JEDEC JESD22 - B111 Drop Test
• JEDEC JESD22 - B113 Bend Test

In determining the specific test method and conditions to be met with the testing, the company considered the effect of the actual environmental conditions and anticipated use of the targeted product category. As noted in the introduction, the primary market for these 3D package applications covers both consumer and high-end electronics that need a greater degree of miniaturization. Reliability test conditions complied with all related industry standards established to qualify an IC package for the commercial market place. The laboratories are equipped to combine materials, mechanical and environmental test labs with a comprehensive failure analysis capability.

Phase I Testing for the 0.40 mm µPILR Package
The first test package developed for with 0.4mm pitch was a 10 x 10 mm single die over-molded device with 529 I/O.

Land patterns are interconnected in a daisy-chain fashion to continue the electrical conductivity of the package units mounted on its surface. The circuit conductor metallization connecting lands are 50 microns. Prior to reliability testing, sample board assemblies are examined visually, cross-sectioned and examined again using optical and X-ray microscopy (see Figure 7).

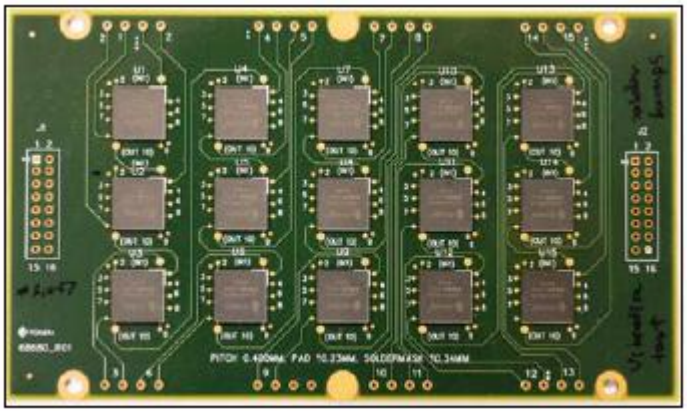

Figure 7. Test board layout for fifteen site 0.40 mm pitch µPILR package evaluation.

All test criteria for the 0.4mm pitch µPILR package were met during package-level testing. The following details the results from the board-level thermal cycle and drop testing.

Board-Level Thermal Cycling IPC-9701 TC3
• **Purpose-** To determine the resistance of packages mounted on test boards to temperature extremes and cycling between those extremes.
• **Test conditions-** Min. temp: -40oC; Max. temp: +125oC. Dwell time 10 minutes. 17 minute ramps. Total cycle time ~54 minutes.
• **Equipment-** Espec ET8-CCW single-zone thermal cycling chamber with resistance monitoring system.
• **Test set-up-** Continuous monitoring of electrical resistance.
• **Failure criteria-** Electrical resistance increase >30% .

Results- 1250 cycles 0 fails/32
Drop Test JEDEC JESD22-B111
• **Purpose-** To determine the resistance of surface-mounted packages to mechanical shock resulting from dropping under gravitational acceleration onto a hard surface.
• **Test conditions-** 1500-*gn* shocks from 0.4 m (approx.)
• **Equipment-** Free-fall drop test apparatus with drop table-mounted accelerometer for calibration.
• **Test set-up-** Parts for test are surface-mounted onto a test board, which is then mounted using stand-offs onto a drop table and secured at the corners. The board is free to flex under shock loading.
• **Failure criteria-** Electrical resistance increase greater than 20% (monitored using high speed DAQ), electrical open, or portions of or whole parts separating from the test boards.

Results- 207 drops/0 failures

Conclusions
The EDC laboratory's conclusions stated that the 0.4mm pitch µPILR package structures appear capable of satisfactory moisture resistance and thermal shock/cycling performance for the intended operating environments. The contact/solder interconnect structure itself appears robust, so long as sufficient solder volume is present and other package structures remain

intact. µPILR packages are intended for surface mounting to PCBs using industry-standard surface mount technology (SMT). The presence of the miniature contacts and the intended use in fine-pitch applications does, however, necessitate modification to SMT processes utilized for standard BGA packages. Specifically, package units are typically assembled to boards using solder paste only, rather than a combination of paste + solder balls, or solder balls + flux. This allows maximum form factor and a finer pitch advantage to be derived from the contact structures.

In the course of developing µPILR package technology, insight was gained into the relevance of various SMT factors to board-level robustness and reliability. One of the benefits of the package substrate structure is the ability to reduce interconnect solder volume and tailor the solder shape to allow for closer spacing of interconnects between package and board, although excessive reduction in solder volume may result in reduced interconnect reliability and strength. Substantially more solder, however, reduces the fine pitch advantage of the miniature contacts.

Acknowledgments
The testing described here was conducted at Tessera's Evaluation & Discovery Center in 2007, providing a first look at the environmental reliability of the 0.4mm pitch µPILR structures and materials. A special thanks to Chris Wade, Daniel Buckminster and Dr. David Baker for contributing technical support and testing data referenced in this paper. Due to the developmental nature of the 0.4mm pitch package program, sample numbers are somewhat limited at this time, however, more extensive testing is planned throughout 2008.

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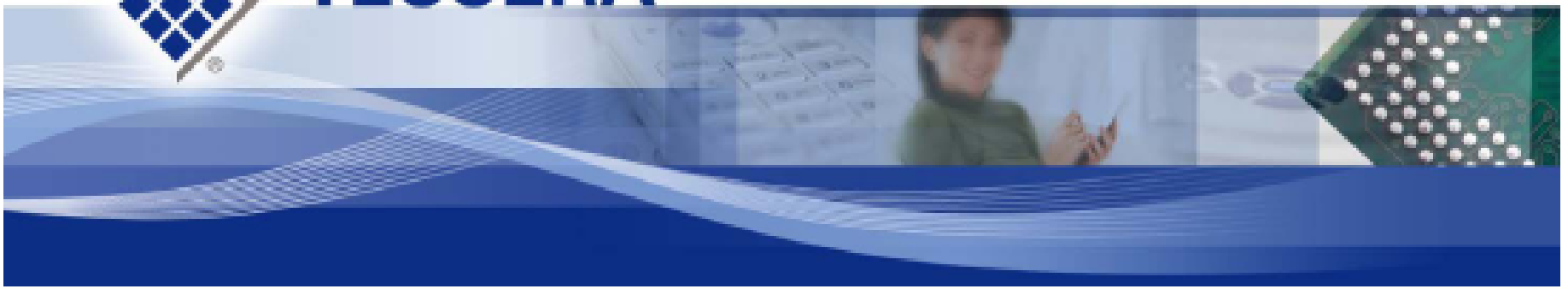

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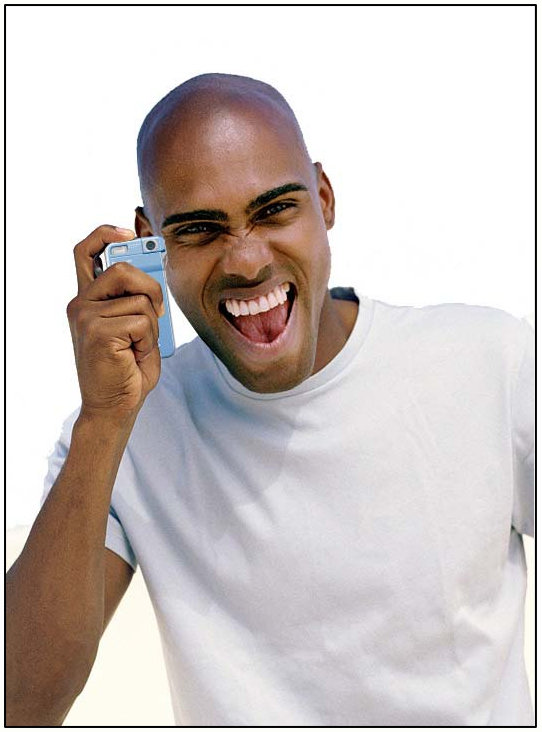
IPC Printed Circuits Expo®, APEX® and the Designers Summit 2008

Presentation overview…

- The presentation will address current expectations for multiple function IC packaging for hand-held and portable electronic applications and consider a number of mixed memory and mixed function variations.

- Information furnished will focus on the product development, performance criteria and qualification test for a unique, vertically configured µPILR package technology for mixed function applications.

Consumer Expectation

Low-Cost	High-Performance	Small Form Factor
		

Addressing Primary Factors for Advanced IC Packaging

- The three primary factors that must be addressed when developing a solution for high density IC packaging-
  - Performance
  - Reliability
  - Cost
- Although each factor carries equal status when assessing the merits of any packaging innovation, cost of the product will always influence adoption of one technology over the other.

Multiple Die Package Concerns

- For a number of applications the stacking of several die within a single package outline provided a reasonably simple solution for a wide range of applications.
- When silicon die having different functions are combined within a single component several issues must be addressed-
  - Managing multiple IC vendors
  - Known good die, test and burn-in
  - Die and wafer availability/uniform quality
  - Compound yield of less mature ICs
  - Accommodating incompatible die shrinks

Markets for 3D IC Packaging

- According to *DataQuest*, “the need for multiple function system like IC packaging has steadily grown and is expected to exceed ten billion units by the year 2010”.
- Primary applications for 3D IC packaging:
  - Consumer- Wireless, entertainment and wearable electronics.
  - Medical- Hand held controllers, wearable monitoring or delivery devices.
  - Military and Aerospace- Wearable, aircraft and spacecraft electronics.

Early Package-on-Package Innovations

- **High Performance Memory and Mixed Function SiP**
  - **Stackable BGA sections enables pre-test and burn-in before joining.**

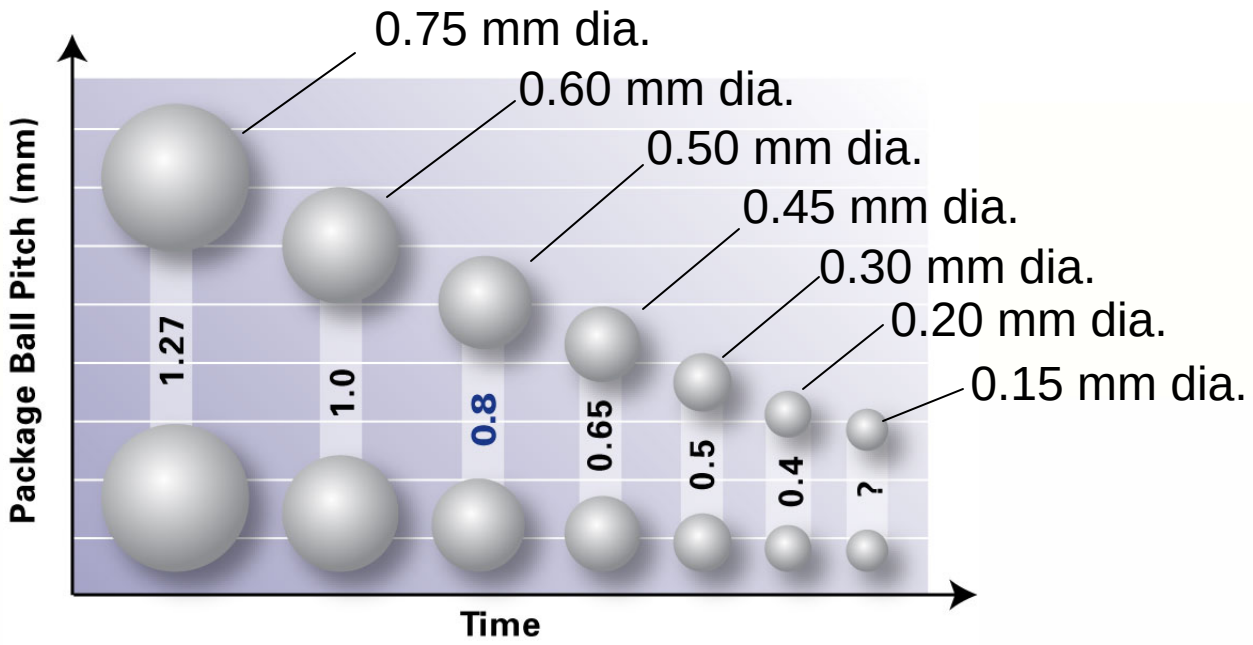
Addressing the Need for Greater Contact Density

- The array package format has already proved to be most versatile method for stacking packaged devices.
  - Although slightly greater in size the largest die in the stack, contacts are arranged in the column and row format established by the industry standards.
- The developers of chip sets for hand held electronics have expressed their goal to develop multiple function packages that have a foot print no greater than 12.0 mm square.

Overcoming the Limiting Factors of BGA Package Technology

- Ball contacts have proved ideal for IC packaging, however, the size (diameter) of the ball contact tends to limit inner-package routing density.
- As I/O increase:
  - Increased difficulty in circuit routing and/or increased package size
  - Increased complexity in test and burn-in sockets (higher cost)
  - Potential limitation in high speed performance

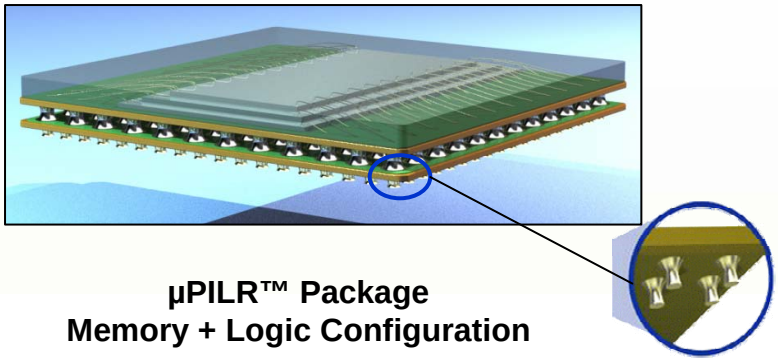
Addressing Projected BGA Contact Pitch and Size Reduction



- Handling and attaching the preformed ≤ 250 micron diameter solder spheres needed for the reduced pitch product has proved to be a challenge.

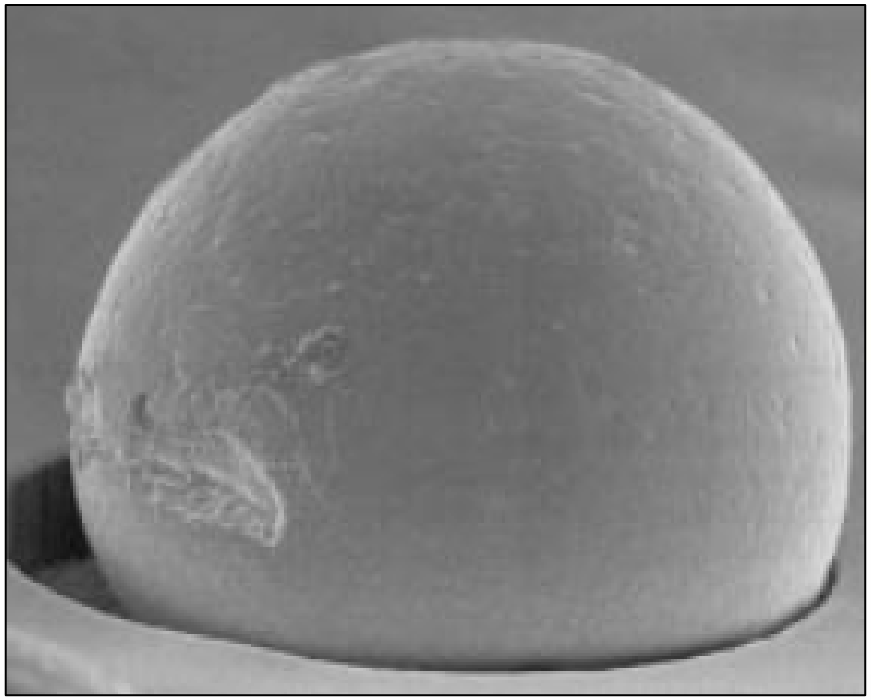
Introducing the µPILR™ Platform for Higher Density IC Packaging

- The µPILR contact enables dramatic improvements in-
  - lowering the package profile
  - reducing contact pitch
  - enabling more efficient package stacking
  - functional performance

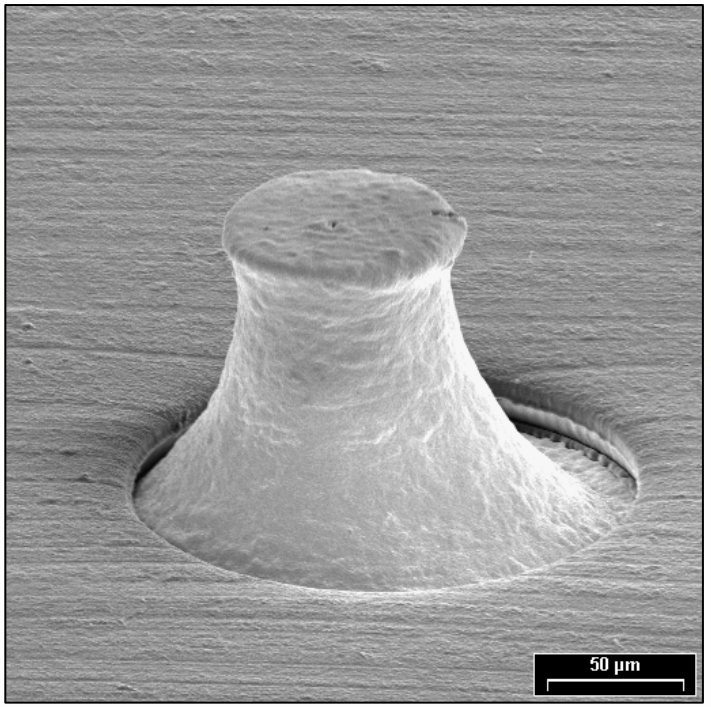


µPILR™ Package
Memory + Logic Configuration

Comparing the Ball Contact to the µPILR™ Contact



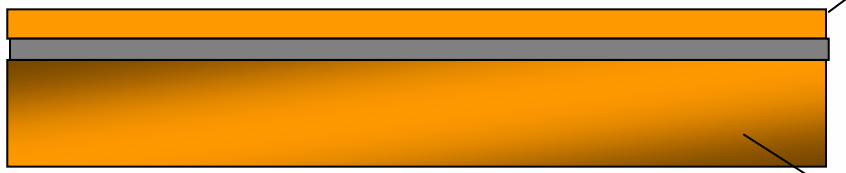
300 micron diameter
ball contact



180 micron base diameter
µPILR contact

Base Material for the µPILR™ Substrate Fabrication

- Contact and Conductor: Tri-metallic *(Cu-Ni-Cu)* composite



Tri-metallic Composite

9.0, 12.0 or 18.0 micron thick electroplated Cu for circuit pattern routing

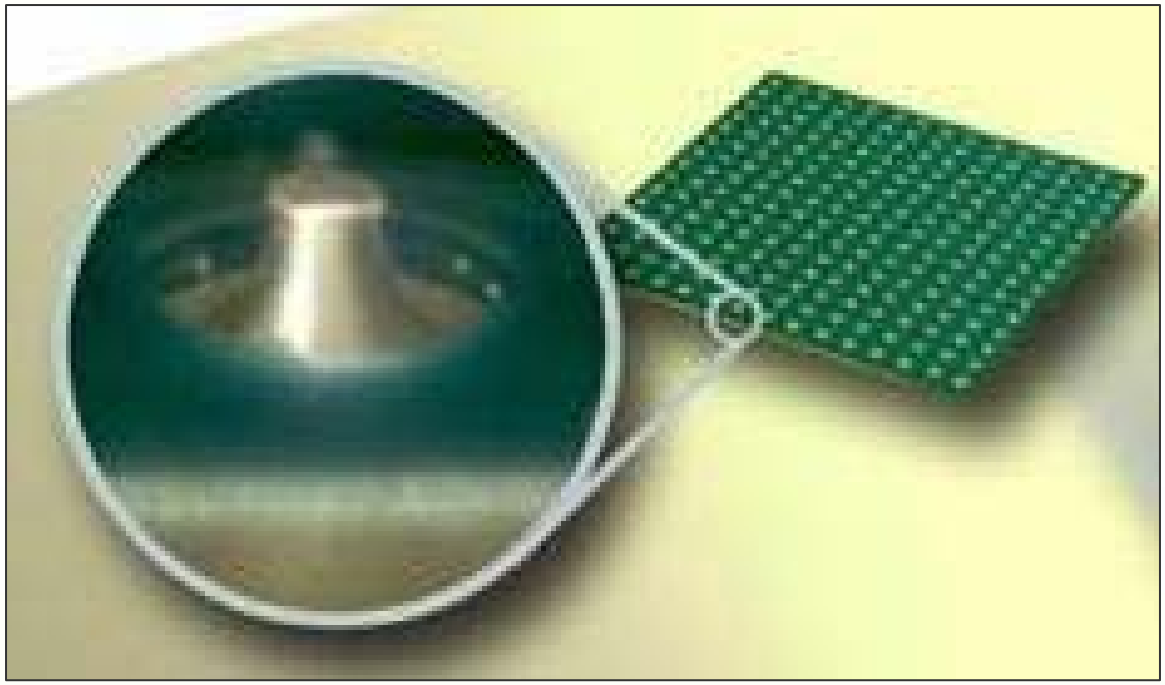
0.8 to 1.0 micron thick electroplated nickel alloy etch barrier

80, 100 or 180 micron thick rolled copper base for micro-contact processing

Not to scale

µPILR™ Substrate Dielectric

- Dielectric: Glass Reinforced B-T Epoxy
- Dielectric Thickness: 50 microns (2 mil)



Substrate Fabrication Process Overview

- Using a two stage subtractive process:
  - Circuit features are pattern printed, chemically etched on the thin copper layer.
  - The B-T epoxy prepreg layer is then bonded over the etched circuit features.
  - The contact features are defined on the thick copper side using a photo-imaged resist.
  - The contact profiles that result from chemical etching will taper from its 180 micron base diameter to just 80 microns at the tip.

Process Flow of Circuits-Out Substrate Fabrication

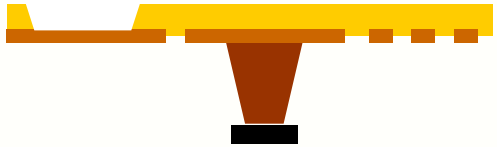
1. Apply and develop resist

2. Chem-etch, remove resist

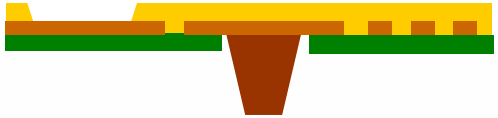
3. Apply B-T dielectric

4. Apply resist and chem-etch contacts

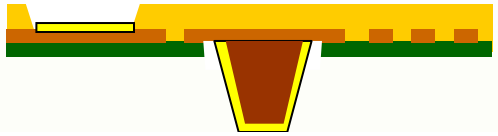
5. Laser ablate bond-site features



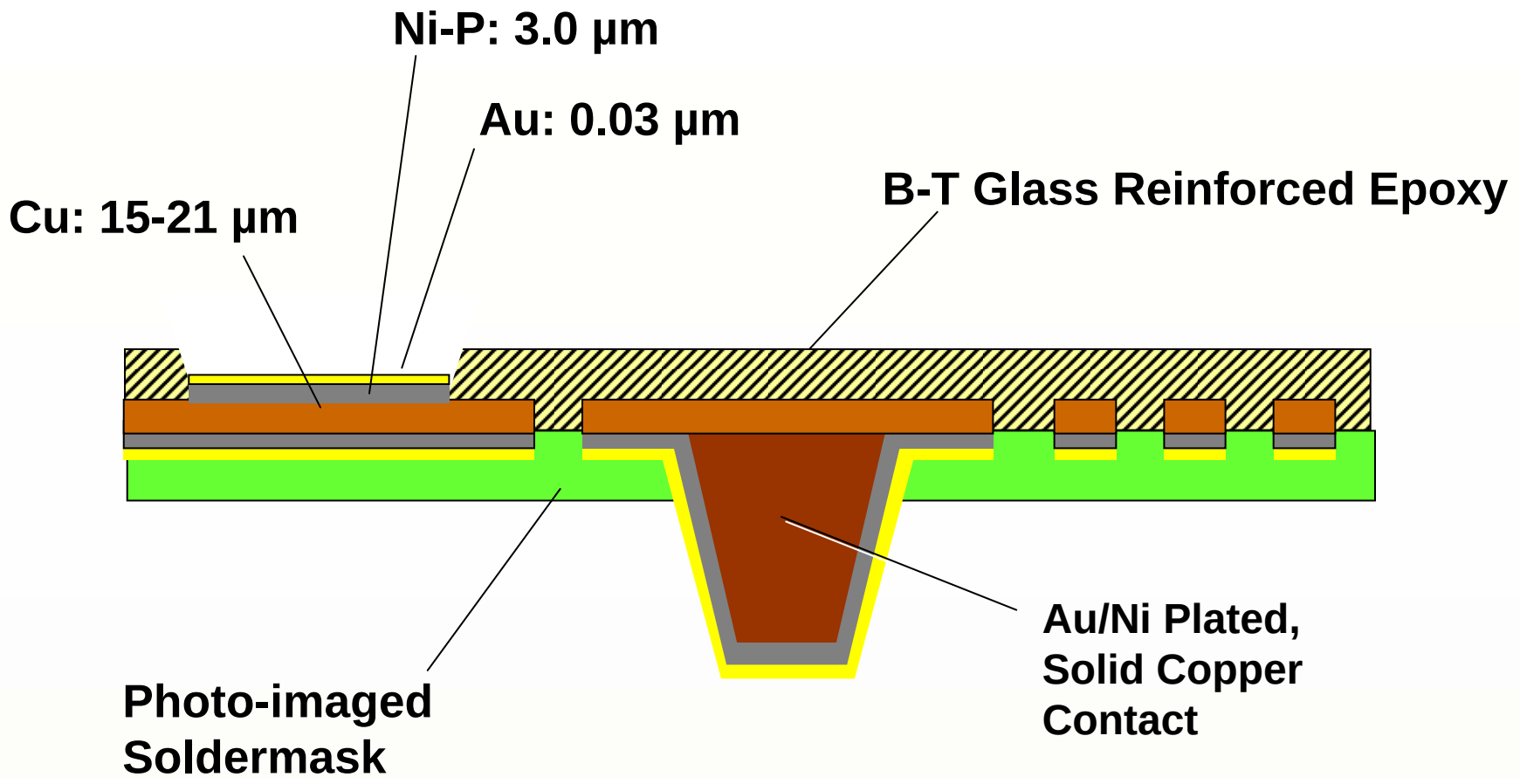
6. Apply solder mask over conductor features



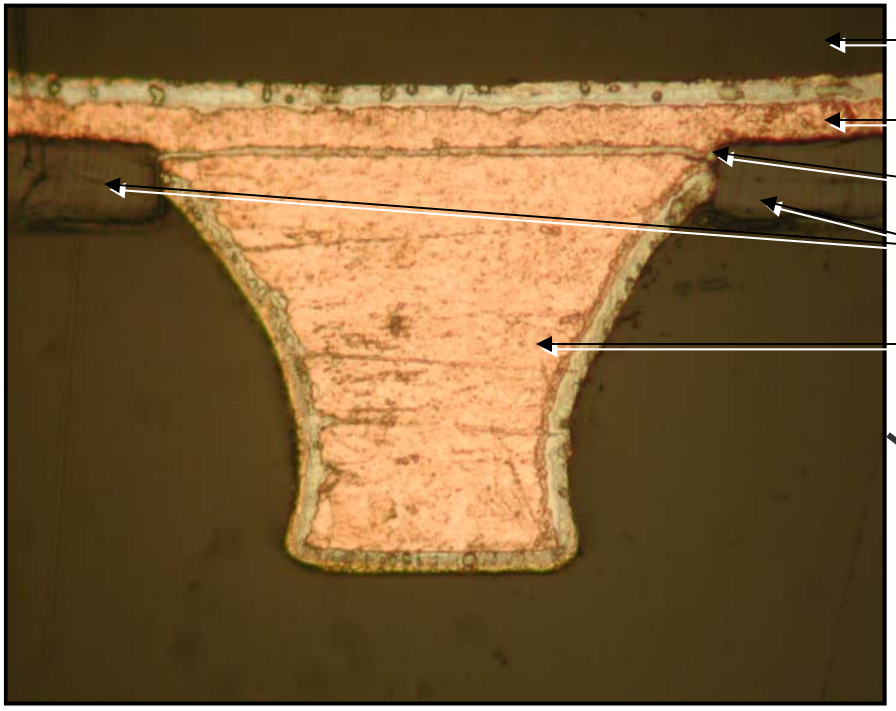
7. Add electroless Ni/Au plating to exposed Cu



Final Form of Circuits-Out µPILR™ Substrate



Finished µPILR™ Contact Detail



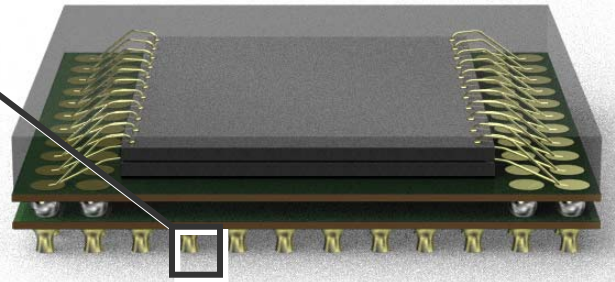
Dielectric layer (50 microns)

Copper layer 1 (12 microns)

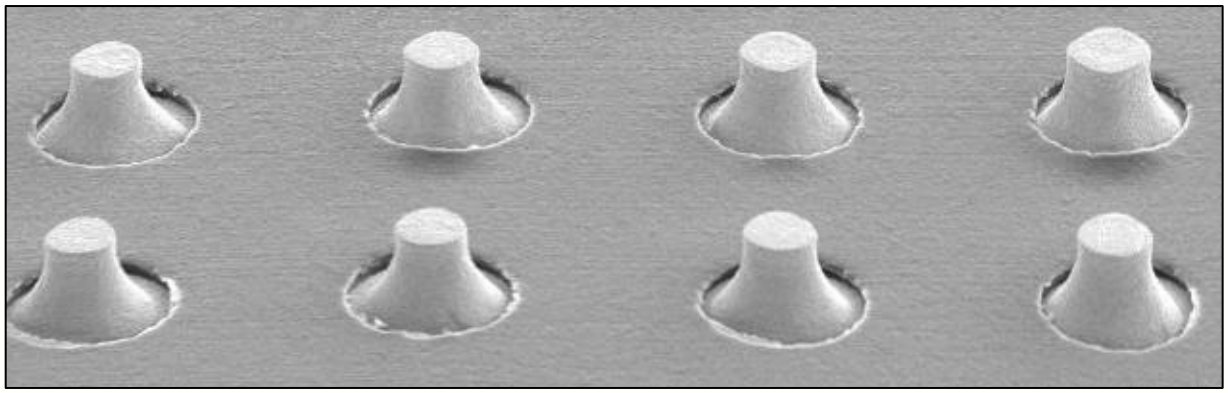
Nickel barrier layer (0.8 microns)

Solder mask (25 microns)

Copper layer 2 (80-125 microns)



µPILR™ Contact Array Example



Because the rolled copper material thickness is very uniform, coplanarity of all contacts on the finished substrate are near perfect.

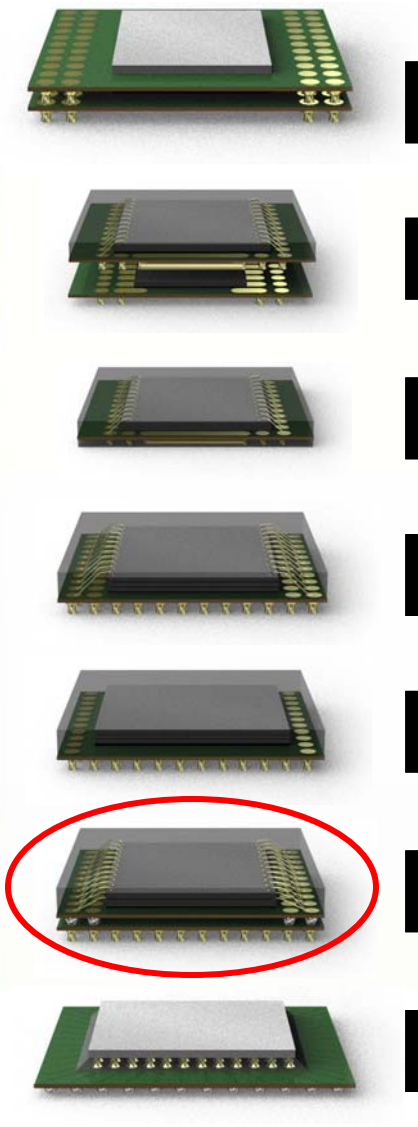
Plating: Au/Ni over solid copper

80 µm tip diameter (typical)

180 µm base diameter (typical)

80-180 µm height (selectable)

µPILR™ PoP/SiP Configurations



Fine pitch, low profile stacked package for high capacity Flash and DRAM

Fine pitch CSP for low-med I/O DSP, RF, Analog and Microcontrollers

High thermal performance CSP for low-med I/O RF, Analog, DSP and Microcontroller ICs

Fine pitch CSP for med-high I/O DSP, Baseband and processor

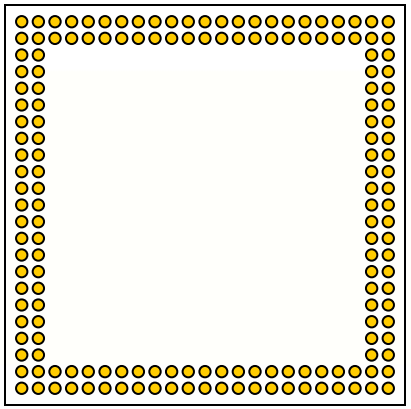
Fine pitch CSP for high I/O DSP, Baseband and processor

Fine pitch, low profile package for stacking memory and logic

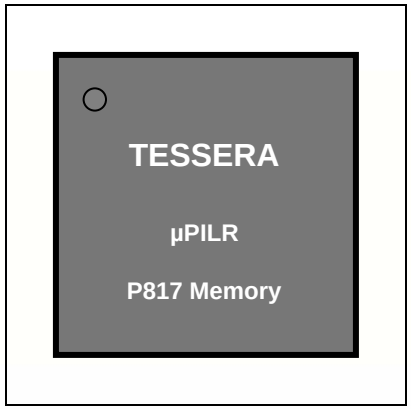
Reduced contact pitch, high I/O count flip-chip packaging

Wireless handsets, notebook computers, Compact Flash, USB Drives and other mobile appliance

µPILR™ Logic-Memory SiP Package-on-Package Test Vehicle

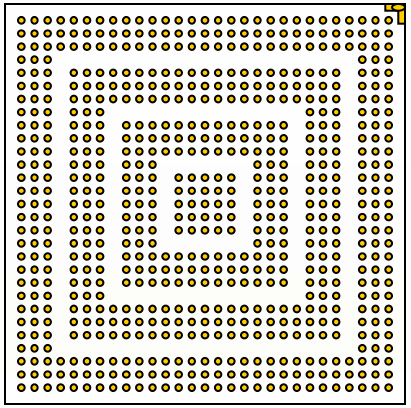


Bottom View
(0.5 mm pitch)

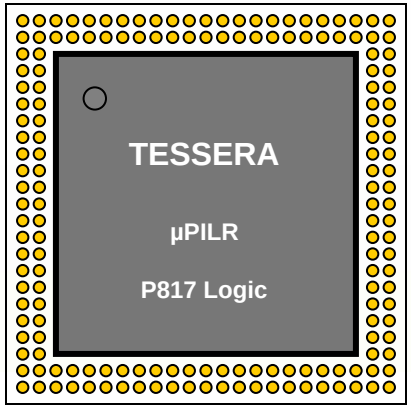


Top View

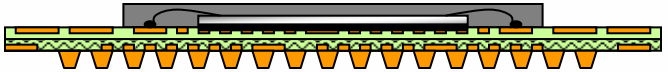
Top Package
- 1-5 memory die (NOR, NAND, DDR)
- Perimeter array contact pitch: 0.5 mm
- Package outline: 10x10 mm to 14x14 mm



Bottom View
(0.4 mm pitch)



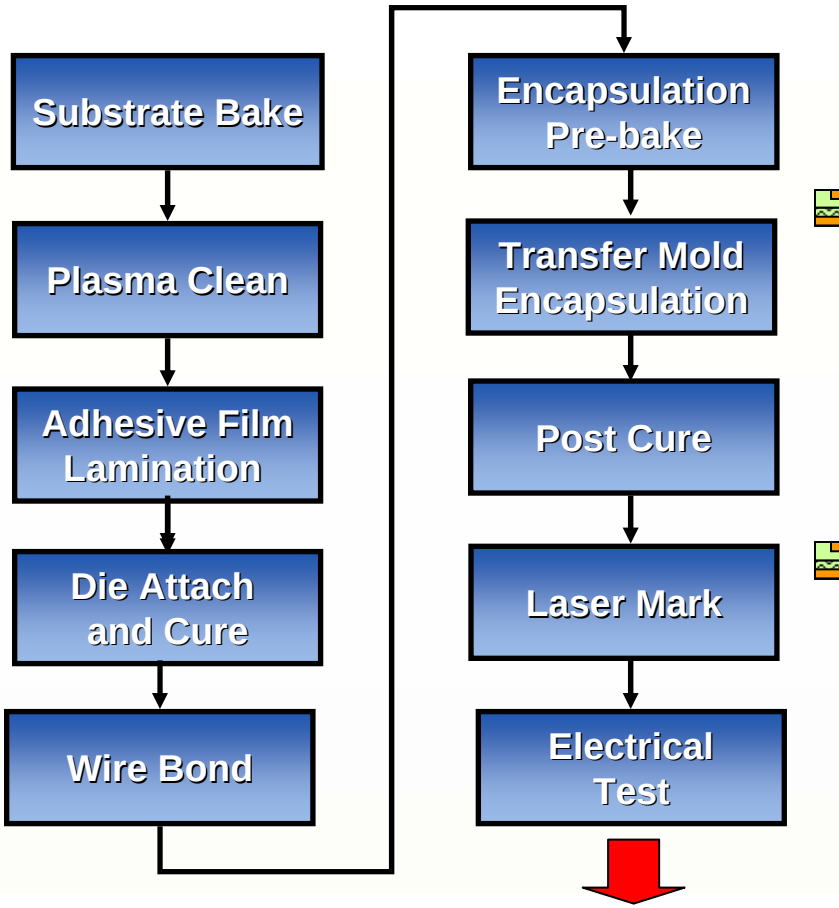
Top View
(0.5 mm pitch)



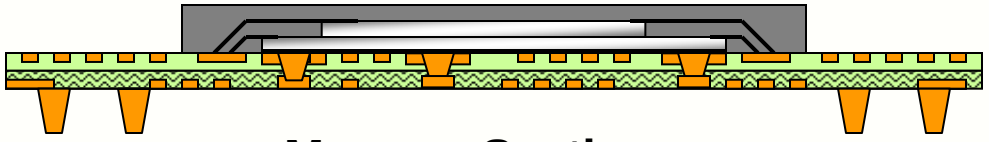
Bottom Package
- 1-2 Logic (apps, Broadband, analog)
- Array contact pitch: 0.4 mm
- Package outline 10x10 mm to 14x14 mm

Package Assembly Process Overview

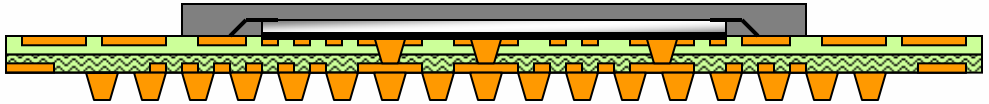
(typical for both sections)



Transfer to package stacking operation



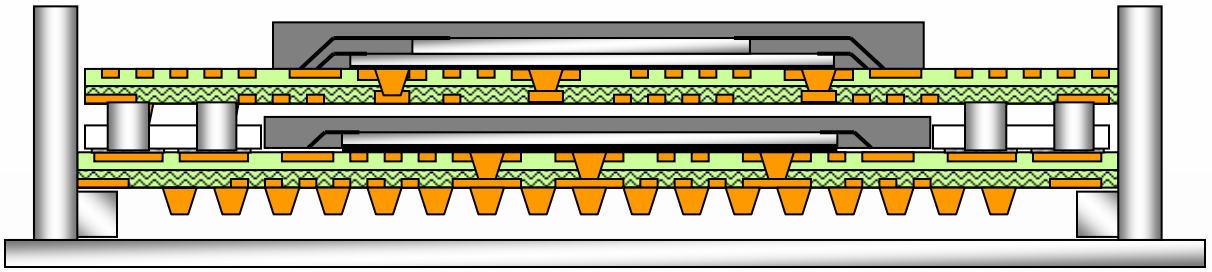
Memory Section
0.50 mm contact pitch



Logic Section
0.40 mm contact pitch

Package Stacking Sequence

1. Deposit solder paste on lands of base (logic) package
2. Place base package section in fixture
3. Sequentially stack upper (memory) section onto base
4. Mass reflow solder to complete joining of sections
5. Remove from fixture, clean and electrically test



Environmental Test Overview

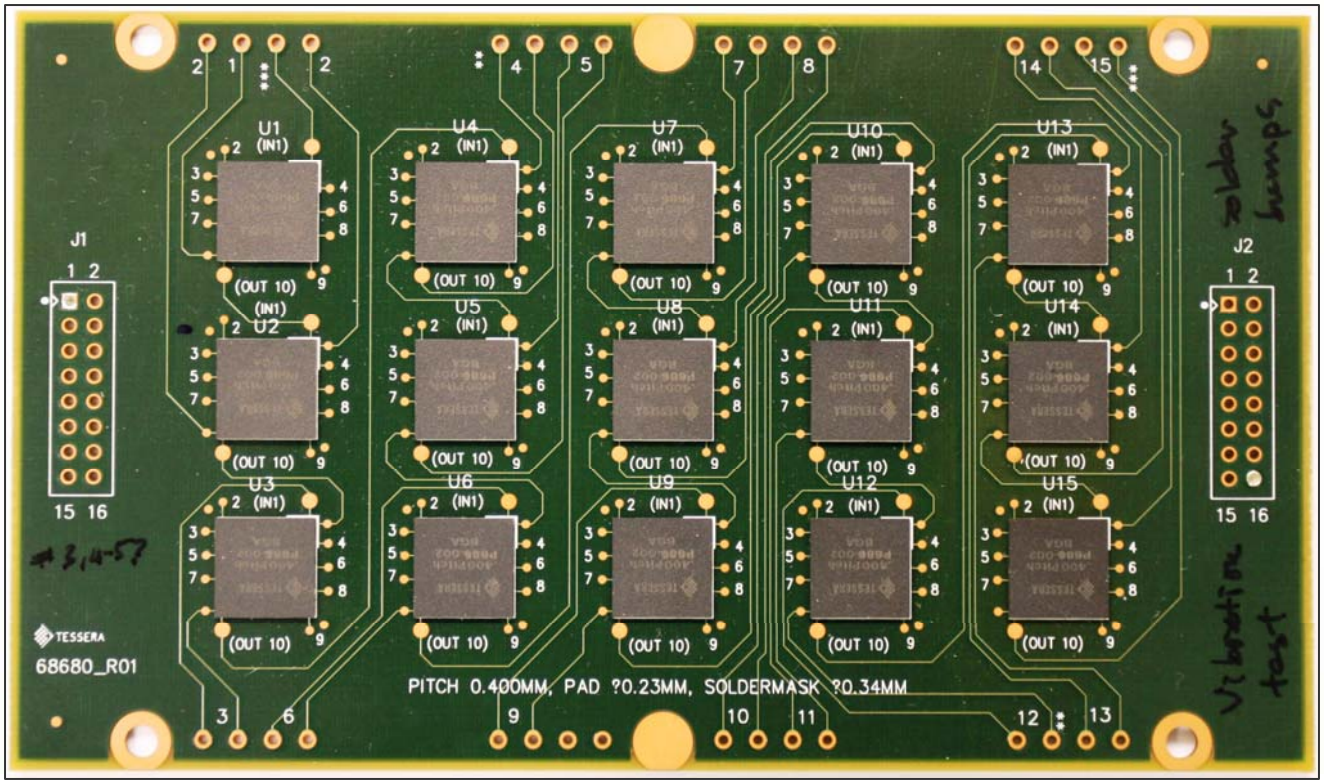
Preconditioning-

- High Temp. Storage:
  - JESD22-A103-C Condition B
- Moisture Sensitivity:
  - J-STD-020 Level 2
- Autoclave:
  - JESD22-A102-A Condition C

Board level-

- Thermal Cycle:
  - IPC 9701 Test Condition 3
- Vibration:
  - JESD22-B103-B
- Drop Test:
  - JESD22-B110A 500g and B111A 1000g

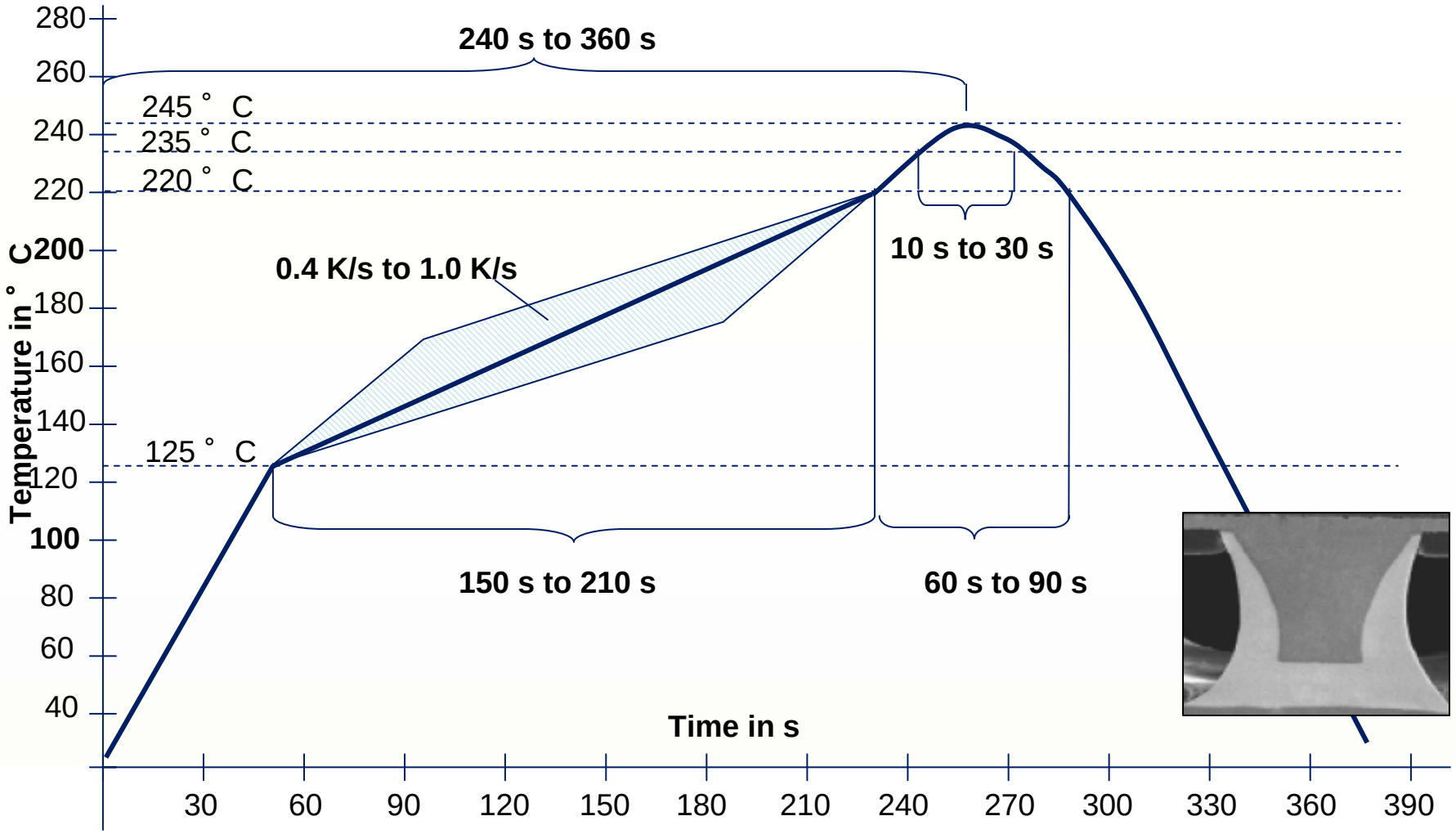
15 Site Test Board Platform for Logic-Memory µPILR™ Package



Size:
80 mm x 132 mm
Material:
IPC-4101/129, FR-4
Ckt Layers:
1-4-1 Buildup
Brd. Thickness:
1.0 mm
Finish:
OSP on Copper
Contact Pitch:
0.5 mm

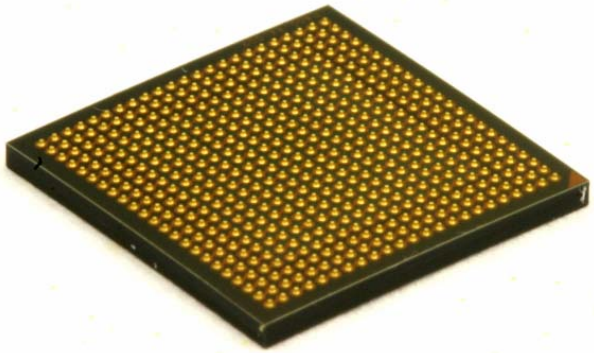
As defined in IPC-7901

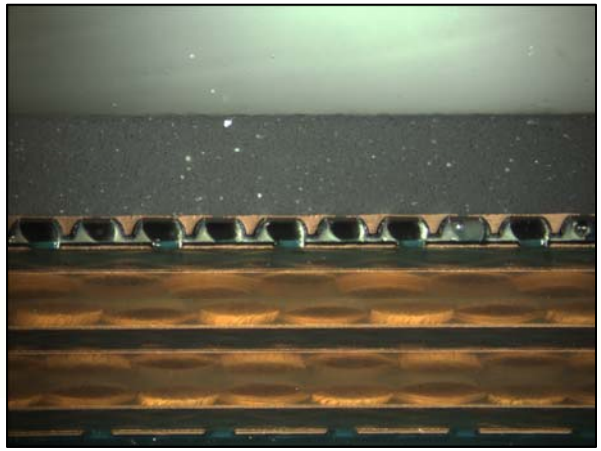
Reflow Solder Profile



Phase 1 Environmental Test Program Overview

- A partial section of the fine-pitch area-array µPILR™ package (P686) is shown below.
- Sn-Ag-Cu (Pb-free) is used for connection to the PCB.
  - Package outline- 10.0 x 10.0 mm x 0.80 mm
  - Die size- 6.5 x 6.5 x 0.15 mm





Contact pitch variations tested;
0.40 mm, 0.50 mm and 0.65 mm

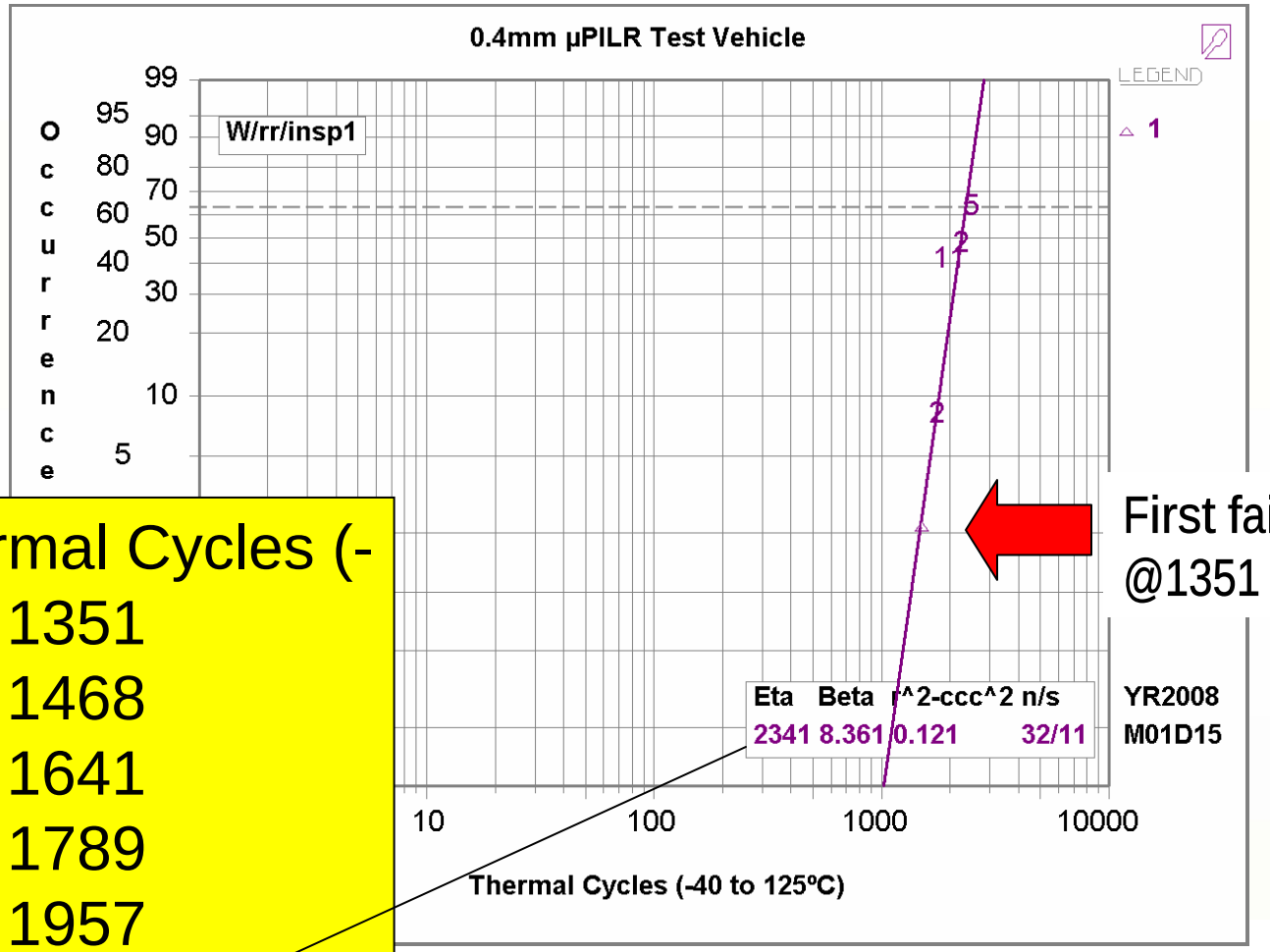
Board Level Thermal Shock Test

(IPC-9701 TC3)

- Purpose- To determine the resistance of packages mounted on test boards to temperature extremes and cycling between those extremes.
- Test conditions- -40ºC; to +125ºC. Dwell time 10 minutes. 17 minute ramps. Total cycle time ~54 minutes.
- Test set-up- Continuous monitoring of electrical resistance.
- Failure criteria- Electrical resistance increase >30% .

Sample size: 32 Units

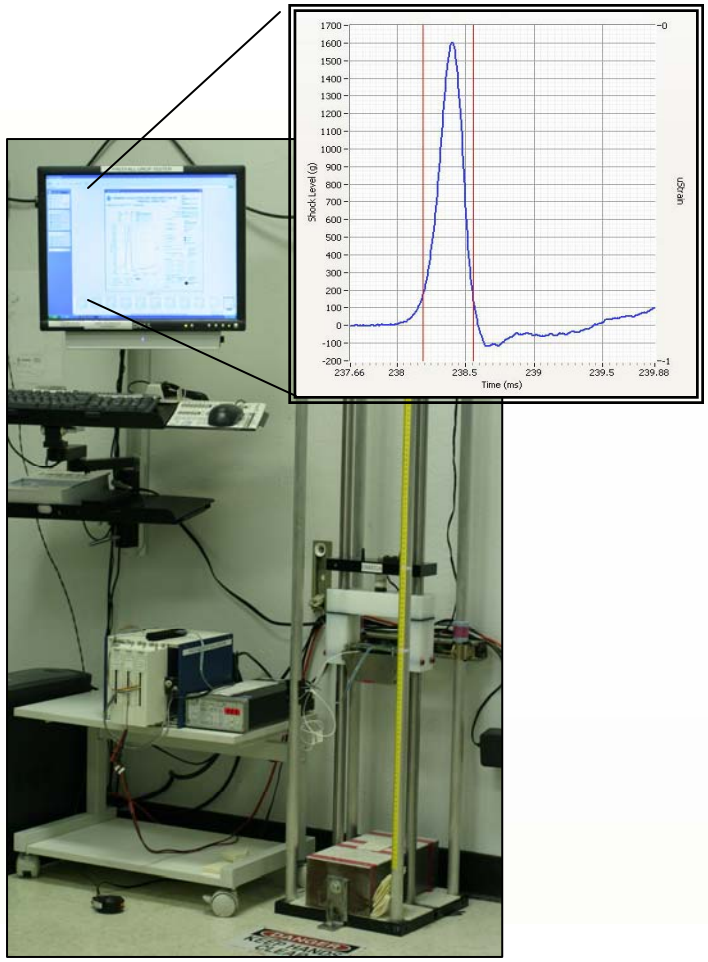
µPILR™ Lead-Free Thermal Shock Test Results



B%	Thermal Cycles (-
1	1351
2	1468
5	1641
10	1789
20	1957
50	2341

First fail @1351 cycles

Stepped Drop Test Results
(JEDEC JESD22-B110/B111)

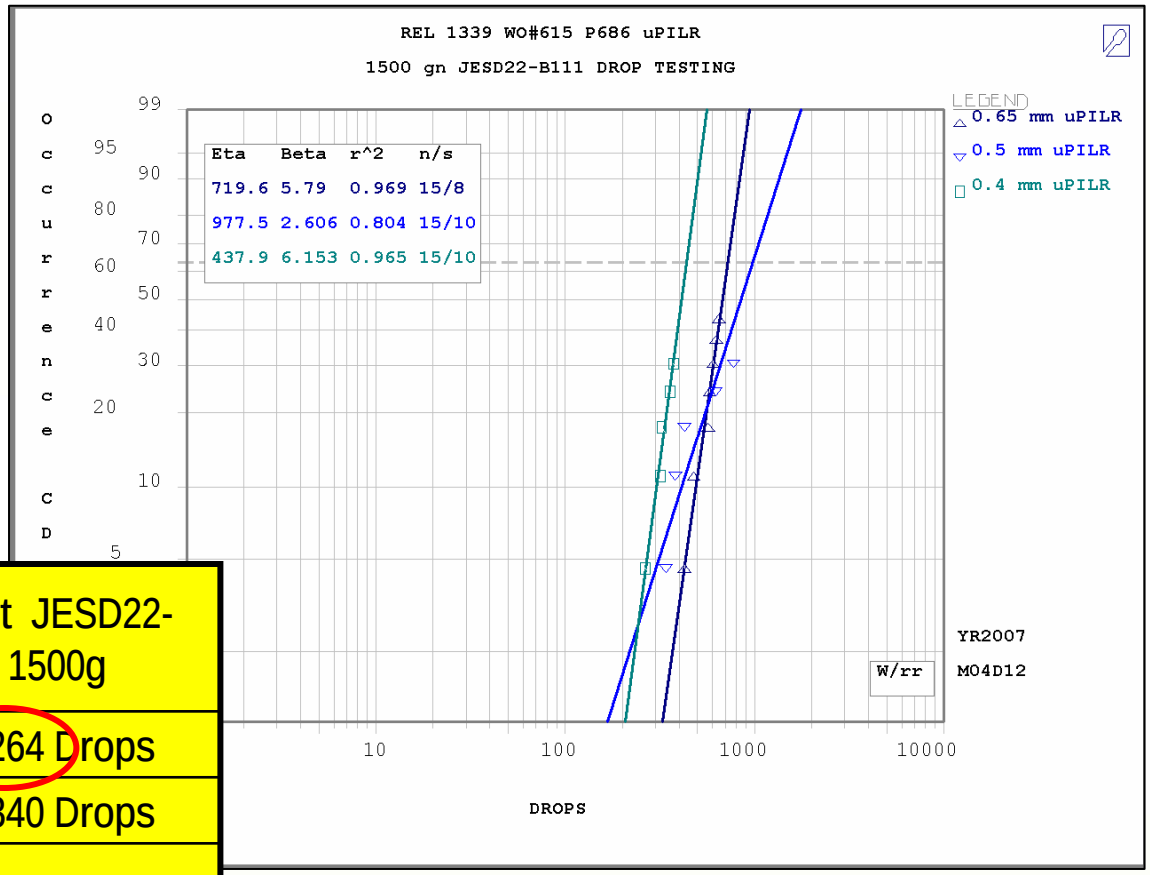


- Purpose- To determine the resistance of surface-mounted packages to mechanical shock resulting from dropping under gravitational acceleration onto a hard surface.
- Test conditions- 1500-*gn* shocks from 0.4 m (approx.)
- Failure criteria- Electrical resistance increase greater than 20% (monitored using high speed DAQ), electrical open, or portions of or whole parts separating from the test boards.

µPILR™ Lead-Free Drop Test Results

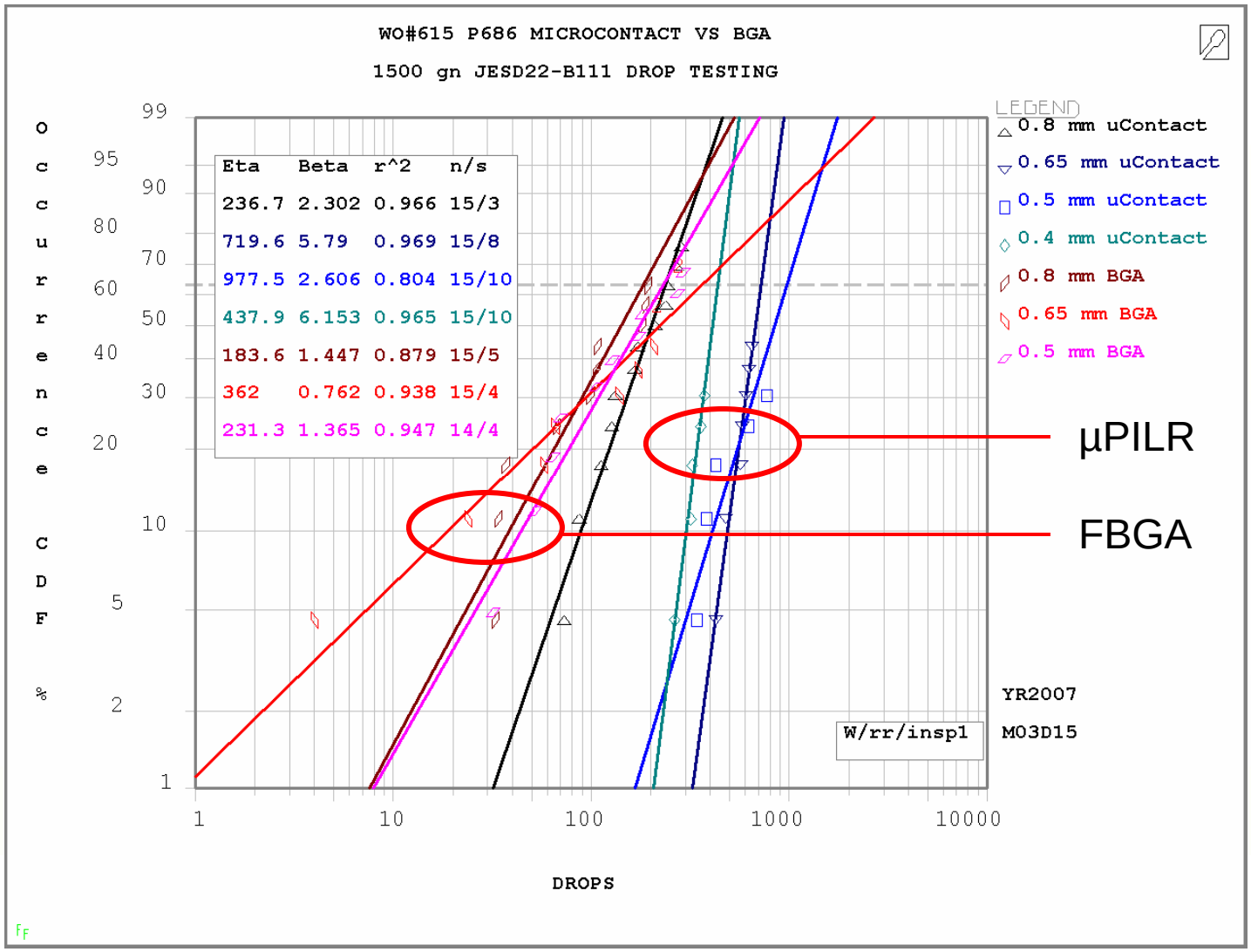
- Test Package Contact Pitches
  - 0.4 mm
  - 0.5 mm
  - 0.65 mm

Note: No underfill was used



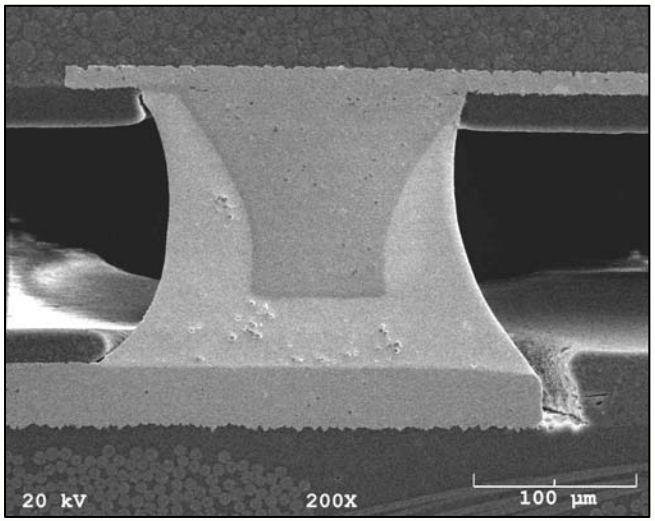
Pitch, I/O	SS	Drop Test JESD22-B111 1500g
0.4 mm, 529	15	1st Fail 264 Drops
0.5 mm, 324	15	1st Fail 340 Drops
0.65 mm, 196	15	1st Fail 426 Drops

µPILR vs FBGA Drop Test Results



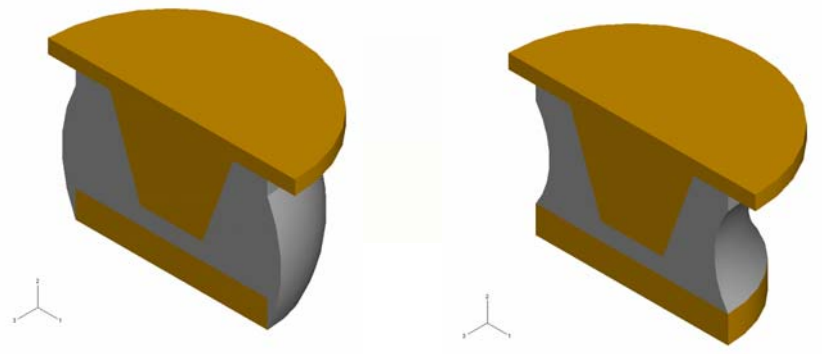
Summary and Conclusions

- The µPILR package structures meet or exceed moisture resistance, thermal shock/cycling performance and drop test criteria for the operating environments for wireless handsets and other portable products.



The contact / solder interconnect structure itself remains robust, so long as sufficient solder volume is present.

- In the course of developing µPILR package technology, insight was gained into the relevance of various SMT factors to board-level robustness and reliability.
- One of the benefits of the package substrate structure is the ability to reduce interconnect solder volume and tailor the solder shape to allow for closer spacing of interconnects between package and board.



µPILR™ Contact Advantage

- The µPILR interconnect technology overcomes many of the existing limitations of the spherical contacts and provides key benefits:
  - Enables closer contact spacing (0.4 mm, 0.3 mm)
  - Thinner, dramatically lowers the package profile
  - Individual package test and burn-in before stacking
  - Enhanced electrical and thermal performance
  - Lighter in weight and rugged construction

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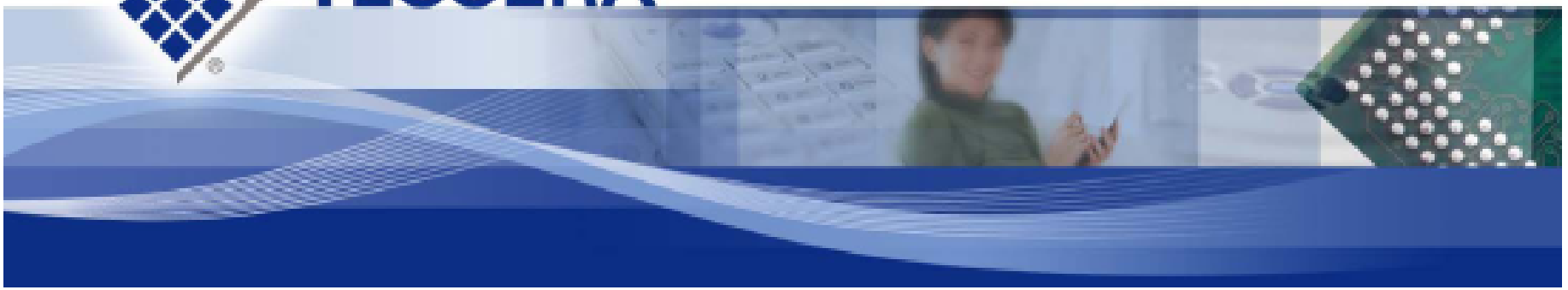

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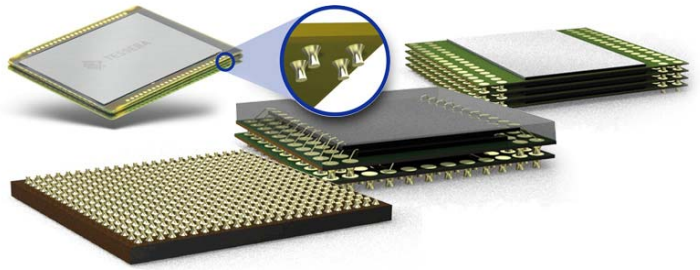

A special thanks to Chris Wade, Daniel Buckminster and Dr. David Baker for contributing technical support and the testing data referenced in this presentation.

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