

The Digital Solder Paste

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Abstract

Since the beginning of Surface Mount Technology over 40 years ago solder paste has been an integral element in electronics assembly. Historically solder paste design and development has been, in a sense, analog in nature. Some users have considered it “black magic”. Formulations were based on previous knowledge bases, honed over the years by tweaking and trial and error science. Paste testing followed suit with virtually all performance tests based on subjective expert inspection and critique. Although statistical design elements have been appending these development methods in recent years, complete digital paste design has been confounded by the lack of quantitative paste tests and the complexity of mixture design technology.

Today we can state that the digital solder paste has been developed by combining “Design for Six Sigma” techniques, quantitative testing methods for all major attributes and specific performance targets derived from a close customer interface. This paper will walk the process of creating this design system, beginning with the building and refining of the “House of Quality” and then coupling this with previously developed quantitative benchmarking techniques, testing and perfecting these techniques for statistical validity, pre-screening potential ingredients, running the mixture Design of Experiments (DOE) and finally verifying the formula. This system has yielded a comprehensive knowledge of interactions for every constituent in the formula, as well as statistically predicted the optimum formula based on desired properties and their relative importance.

There are many obvious benefits to the digital solder paste over its analog predecessors. The design outcome forms a mathematical basis for a chemical formula with the interactive effects on performance attributes for each constituent fully understood. This permits performance simulations of constituent changes, intuitive troubleshooting and other “what if” scenario exercises. Shorter development cycles for formula variations to target key paste attributes are one immediate benefit.

Introduction

SMT assembly has been increasing in complexity due to smaller components, new surface finishes, new component types and more sophisticated automation in the last decade. This has raised both the level of desired solder paste performance for any given attribute as well as the number of desired attributes. Twenty years ago an RMA solder paste that had an abandon time tolerance of 15 to 30 minutes, printed at 1-2 inches per second, soldered to HASL with 50 mil pitch devices with a tin/lead finish using an 8 mil stencil was perfectly acceptable. Today we want an L0 activated solder paste with a minimum 1 hour abandon time tolerance, that prints 2-6 inches per second with excellent solderability to lead free components over an OSP finish to 0.4mm (16mil) pitch QFP and 1.0 mm (40 mil) BGA devices using a 5 mil stencil. We would also like this same formulation to be completely compatible with enclosed print heads such as the *DEK ProFlow* and *MPM Rheopump*, have excellent solderability to Pd flash over nickel terminated components, immersion tin and silver finished PCB's, have a flawless ICT (In Circuit Test) and conformal coating compatible flux residue, be intrusive reflow capable at about 25% of the cost of that solder paste from 20 years ago and still reflow in air.

To meet the challenge presented by these extensive performance requirements, solder paste development had to become more sophisticated and refined. Ideally a mathematical model needed to be developed that predicted the solder pastes performance (y) as shown in Formula 1. To accomplish this, “Design for Six Sigma” (DFSS) techniques were employed. DFSS extends Six Sigma techniques to product design. Traditional Six Sigma techniques focus on removing variation from an existing product or process. DFSS uses statistical modeling tools to develop products inherently free of variation. Of equal importance to these modeling tools are paste performance attribute testing or benchmarking tools. Without quantitative benchmarking tools, the linking of formulation and the specific paste performance interactions would not be possible.

Formula 1: $y = f(x)_{\text{resin}} + f(x)_{\text{solvent}} + f(x)_{\text{activator}} + f(x)_{\text{acid}} + f(x)_{\dots}$

Benchmarking Tools

Although there are specific IPC and JIS paste attribute tests available, most of these are either qualitative or lack the sensitivity to discriminate between small formulation differences in a mixture DOE. Benchmarking tools should emulate the manufacturing environment with enough contrast to differentiate significant variations in formulations. Benchmarking tools must be objective and ideally automated. The individual attribute test areas in the design should have a large enough range or

bandwidth so that no formulation can ever exceed the test capabilities¹. The test board used in this DFSS program has evolved over the last ten years from numerous other board designs. Each previous design had a specialty; there was no one comprehensive design. This generated extra work to benchmark a formulation or process. An effort to combine and upgrade these tests into a single integrated economic test board has resulted in the design as seen below in Figure 1. Major attention went into developing printability and wetting tests with additional emphasis on X-ray voiding, pin testability (ICT), abandon time and enclosed head compatibility. Test parallax was another design objective. Much in the same way the separation of two eyes by some distance aids in the perception of three dimensions, multiple tests gauging the same attribute add depth to the measurement of that attribute. For this purpose, there are four wetting gauges and three printing gauges that were used in the DFSS program on this board.

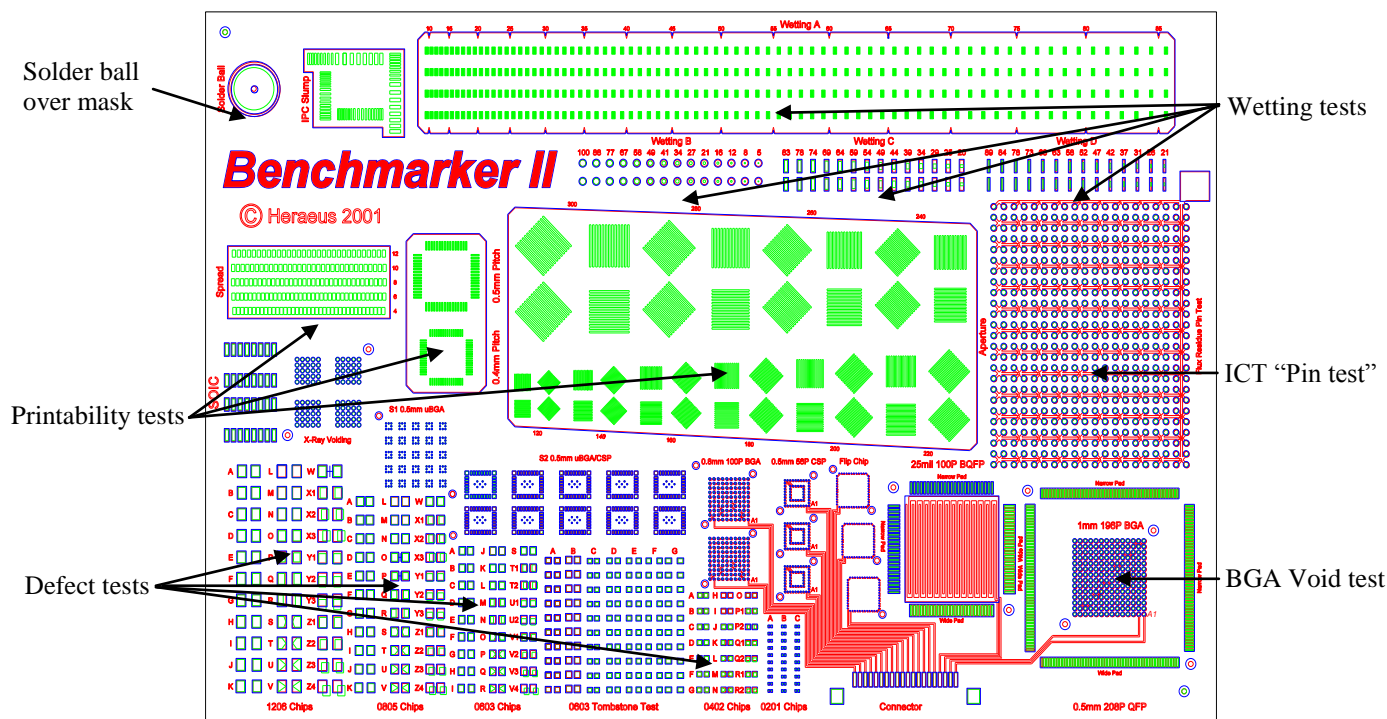


Figure 1 Test Board

Printability Tests

Although there have been five paste printability tests developed on this board, three have been utilized extensively in the DFSS program. A test sequence that captured both print directions and the effects of under stencil wiping involves inspecting the 2nd, 5th, 9th, 10th and 15th print with a wet-vac-dry wipe after the 10th print was central to the printability testing. Since fast squeegee speed was one of the most important goals of this new paste, the speed printing of each paste was vetted with the following process:

1. Load 375g of material on the stencil (15g per cm of squeegee length)
2. Starting Point - 150mm/sec @ 15 kg pressure (3/4 of maximum pressure)
 - a. *If clean wipe*: cut back pressure until minimum pressure is achieved for clean wipe and record.
 - b. *If not clean wipe*: cut back speed, with 15 kg pressure, until maximum speed is achieved for clean wipe and record.
3. Generate print, reflow defect, ICT pin test, X-ray voiding, hot slump and wetting test boards.

With this screening process not only the printing but the total paste performance was gauged at the maximum printing speed that the formulation under test could achieve.

The first test is the Aperture Test, which is the inspection of 10 different pitch areas, which vary from 120μ lines and spaces to 300μ lines and spaces, as in the central portion of the design in Figure 1. For each pitch there are 4 groupings of 13 lines and 12 spaces with one grouping horizontal, one vertical and two oriented at 45° to the print direction. For each of the 5 saved prints (2nd, 5th, 9th, 10th & 15th), each pitch and each group orientation, print defects are inspected for and noted. A defect is defined as any bridge of spaces with as little as 2 particles of solder powder touching (Figure 2) or any gap in any of the lines indicating hang-up in the stencil (Figure 3). The pitch (aperture width times 2) at which there were no more than one defect in any of the five prints is considered its aperture rating, expressed in microns.

This test is also used in quantifying hot slump by inspecting a print before and after heating to 150C. This test basically quantifies a pastes ability to resolve fine lines.

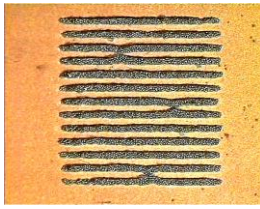


Figure 2 Bridge

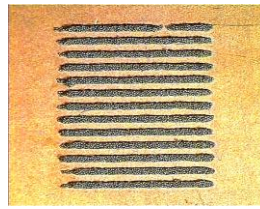


Figure 3 Gap

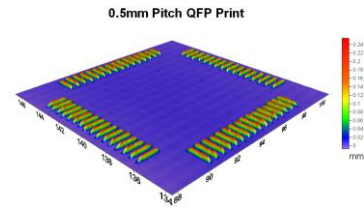


Figure 4 Solder Volume

The second test is the Spread Test that gauges printability from a slightly different viewpoint. It is often referred to as cold slump, but differs in that it occurs *during* the printing process as opposed to *after* the printing process due to time. This test basically quantifies a paste's ability to resolve fine spaces. Relatively large pads, such as SOIC pads, placed very close to one another have been effective in generating spread in as little as 2 prints in most formulations². Large pads with narrow spacing manifest this printability trait more effectively than fine pitch pads as are used in the previously discussed test. There were originally only 5 rows of relatively wide pads (0.025") with small gaps between them, the gaps varied from 4 mils to 12 mils in 2 mil increments. This test underwent considerable Gauge R&R testing during the DFSS program as did all of the other tests described in this paper. The resolution of this test was considerably increased by adding 5, 7 and 9 mil gaps and dropping the 12 mil gap. The old design is shown in Figure 1 just below the test vehicle name. Although the very fine gaps in the first two rows of the test pattern are not typical, it does provide a spectrum of worst-case design scenarios that simulates the effects of poor stencil gasketing. For each of the five saved prints (2nd, 5th, 9th, 10th & 15th), defects are inspected for and noted. A defect is defined as any bridge of the gap between the pads with as little as two particles of solder powder touching. The total number of defects is calculated with less is better. This test is also used in quantifying hot slump by inspecting a print before and after heating to 150C.

The third test utilized is the Solder Volume test. One of the more important goals of this development program was to gauge the change in printed solder volume over time with less is best. Initially the 0.5mm pitch QFP printed area (between Spread and Apertures test areas in Figure 1) was measured on the 2nd and 15th saved prints with a high resolution confocal measuring system as shown in Figure 4. Since there was statistically very little contrast between formulations on the 2nd print, only the 15th print was used to gauge this attribute. The average pad volume and standard deviation were used as data points.

Wetting Tests

The other major area of test emphasis is with wetting or solderability testing. There are 4 wetting areas (A, B, C & D) in the design as can be seen in Figure 5. In Area A the gap between each adjacent pad is increased by 1 mil rendering the difficulty of creating a bridge between printed pads of solder paste progressively more difficult as the gap increases, essentially creating a horizontal wetting thermometer. Gaps range from 10 to 85 mils. Areas B, C & D gauge pad wettability by printing varying coverage's of solder paste onto round BGA, wide rectangular SOIC and narrow rectangular fine pitch pads for areas B, C & D respectively. These areas are inspected for which pads the reflowed solder was able to extend to the pad ends (Figure 6). The smaller the coverage the more distance the solder has to wet to reach the pad end and the more difficult a pad wetting scenario, essentially creating 3 different pad geometry wetting "thermometers". Results are reported in wetting points based on the paste coverage as in Figure 7, with more points is better. These wetting tests are another example of parallax in this test board design. It has been shown that if a paste exhibits some hot slump as measured by the spread test, the wetting in area A is higher than expected based on observed results in the other 3 areas.

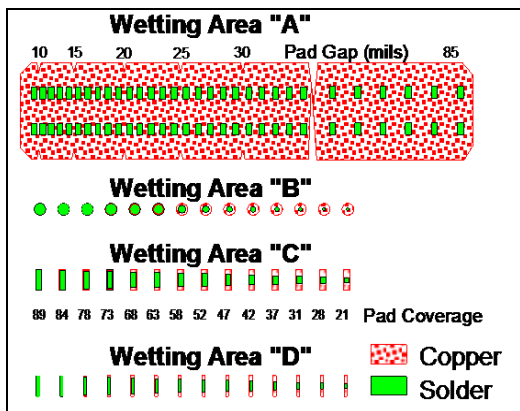


Figure 5 Wetting "Thermometers"



Figure 6 Wetting C

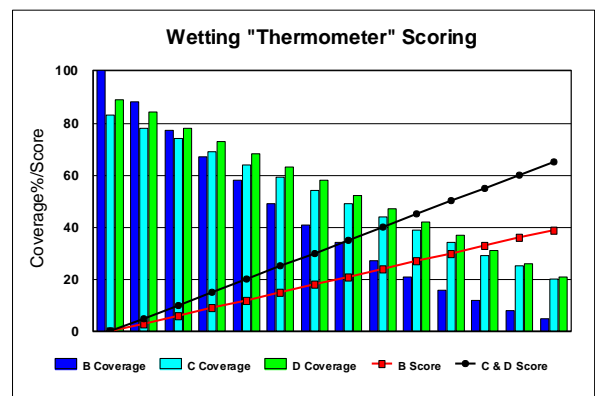


Figure 7 Greater Pad Wetting = Higher Score

These gauges were not only valuable in screening DOE (Design of Experiment) measurement but in the full mixture design phases of the project. Quantitative reliable gauging is critical to get meaningful results in any DOE. Figure 7 illustrates the wetting gauges used to study the effects of the ratio of an acid and a solvent to obtain maximum wetting.

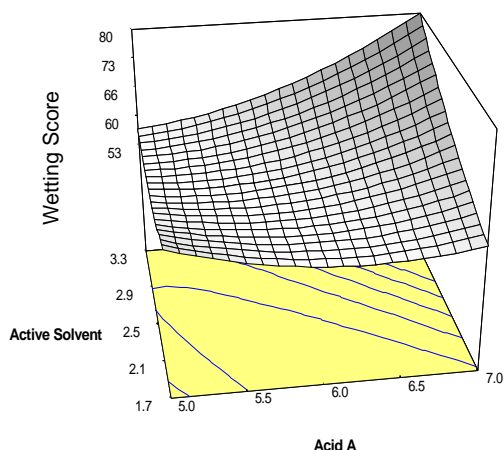


Figure 7 Formula Concentrations Vs Wetting

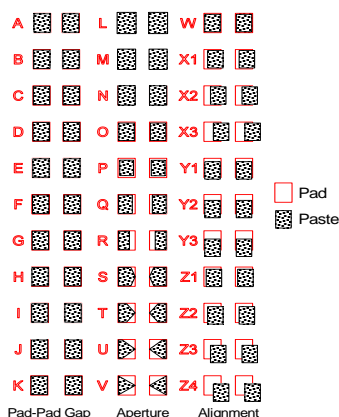


Figure 8 Chip Defect Stress Test

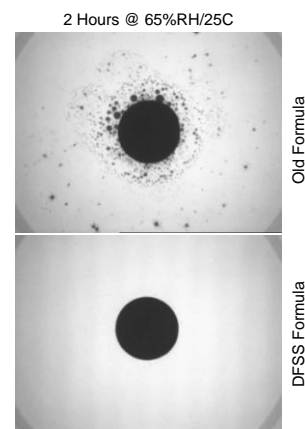


Figure 9 X-ray Count of SBOM

Solder Defect Testing

There are 4 sections (1206, 0805, 0603 and 0402 chips) on the test board designed with a series of chip pads varying the gap between the pads to the full range recommended by the IPC³ and then some. Figure 8 is a graphic of section 1; the other three test areas employ similar design logic. Various stencil aperture designs that can be found on customer designs and induced aperture misalignment are also included. These design features are intended to push formulations to generate solder beads, balls and occasionally tombstones. The number of chips with as little as one bead, solder ball or tombstone are recorded.

Another test area that proved strategic was the Solder Ball over Mask test area (SBOM) that can be seen in the upper left hand corner in Figure 1. One other very important desired paste performance attribute was the tolerance of a high humidity factory exposure after printing. To test this, all pastes under test were tested for SBOM, wetting, solder defects and BGA voiding at zero hour (immediate populate and air reflow after printing) and two hour exposure in 65%RH/25C after print and before populate and air reflow. As can be seen in Figure 9, the X-ray was used to automate solder ball counting.

DFSS Tools⁴

The DFSS process began with establishing the “House of Quality” (HOQ) from the “Voice of the Customer” (VOC). Measurement Systems Evaluations (MSE) defined variability in testing and helped refine existing tests to yield the most statistically significant data. Process Maps (PMAP) and Failure Mode and Effects Analysis (FMEA) defined variability in process. Mixture Design of Experiments (DOE) was used because solder paste has a constraint formula. DOE regression analysis determined the formulation model. Finally Response Optimization shows the performance of each raw material on each critical test attribute and establishing the model $y = f(X)$.

House of Quality

Houses of Quality (Figure 10) are used to create a customer-driven environment by including the VOC in product and process design. This systematic process translates customer requirements into product design requirements; the product design requirements are then translated into part, process, and production requirements. By defining the requirements early in the design process, design cycle time and cost are reduced by enhancing communication and reducing the number of design iterations. HOQ bridges the gap between the customer’s needs and the supplier’s process capability.

HOQ1 is the first matrix created; the purpose of creating this matrix is to gather and translate the customer’s needs and expectations (the WHAT’s) into functional requirements (the HOW’s). With knowledge of the customer attributes, the functional requirements (functional characteristics, targets, specifications) are defined. The DFSS team identified five (5) customer requirements and seventeen (17) functional requirements. The output of this analysis is the conceptual design.

For this DFSS project there was one major OEM that defined the customer attributes and their paste supplier. Together, the OEM and their supplier defined the paste functional requirements. The strong partnership between the two organizations resulted in a high-performance team that was able to overcome translation issues regarding customer needs, importance rankings, and specification definition. Approximately 50% of the DFSS project time was spent on HOQ planning and ingredient screening experiments and 50% was spent on Mixture DOE execution, analysis and response optimization.

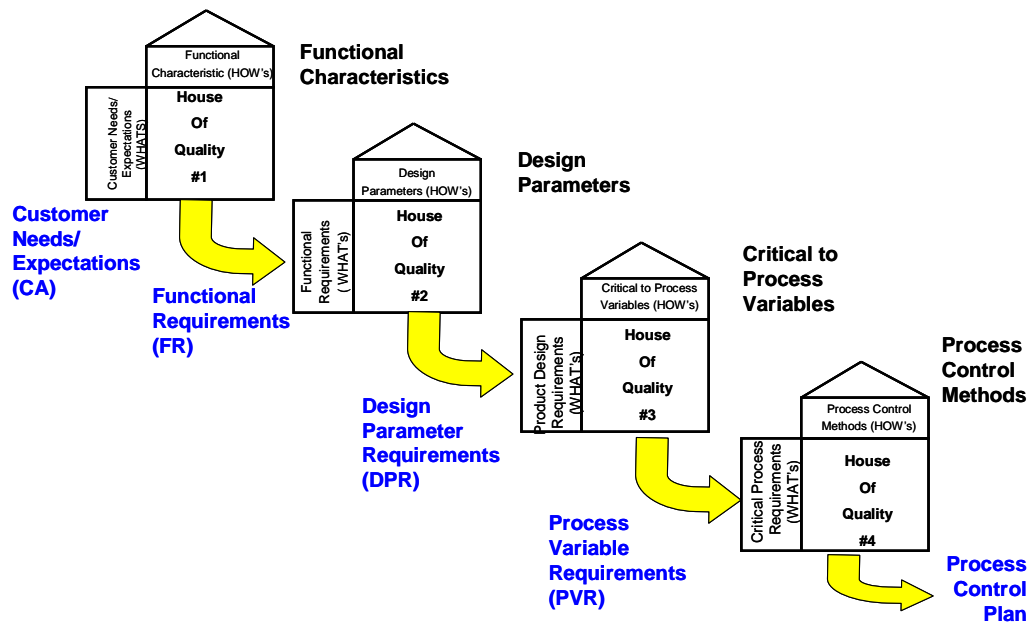


Figure 10 The House of Quality Process Distills the Requirements and Their Relative Importance

The second House of Quality (HOQ2) defined and evaluated the design parameters required to meet the functional requirements established in the HOQ1. As with HOQ1, importance values were established and applied to the design parameters as they related to the functional requirements. The team defined eleven (11) design parameters (inputs or X's) to optimize the 27 functional requirements (outputs or Y's). The design parameters were the switches that could be adjusted to make the trade-offs necessary to balance all customer requirements.

Measurement Systems Evaluations (MSE)

The DFSS MSE determined whether the *full* measurement system was adequate to serve the purposes of the project. The MSE design should consider the operators, equipment, set-up, and other aspects of the measurement process. A good measurement system will have good stability, repeatability, and reproducibility with adequate discrimination between parts along with little equipment or operator bias. The X-ray solder ball counting method showed good part to part variation with minimum variation due to the measurement system (gage) and was therefore suitable for the needs of this project. The spread test showed a lack of resolution in the 7 to 9 mil gap region of the test. A new design was created as previously described, retested and qualified for the project. Every test was essentially tested to ensure statistically significant results would be available for the project.

Mixture Design

During the planning stages for the evaluation, the team had to make a decision, based on the data available, about what type of experimental approach to use. The choices were either a factorial experiment or a less familiar mixture experiment⁴. The mixture design was chosen simply because it models the product under design best since solder paste is a mixture of flux and powder metal and flux is a mixture of multiple components. Unfortunately the flux application takes mixture design beyond four dimensions. A four component mixture (pyramid) is the most complex mixture that can be drawn. The need to visualize the design as well as the number of trials gave the team a very strong incentive to try and minimize the number of factors in the experiment. The formulation was complex and necessitated an extreme vertices design (Figure 11). Contour and surface plots (Figures 12 and 13) provided help to define and optimize sub-mixtures. With the ability to do selective data “blocking” plus the use of this sub-mixture concept, the software program (*Minitab*) was able to be effective with this 7 component mixture design.

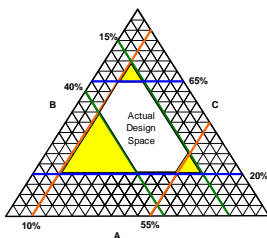


Figure 11 Extreme Vertices Example



Figure 12 Contour Plot

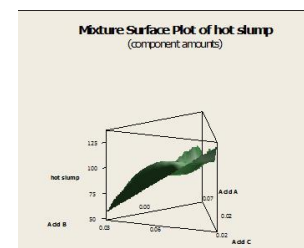


Figure 13 Surface Plot

Response Optimization

Response Optimization shows the effect of seven components on 15 significant performance properties of the paste. It utilizes the importance and target values from the HOQ to establish the product desirability. It can be modified to suggest a different formulation if the balance of property desirability's (responses) is changed. For instance, if faster print speed becomes most important, the new formulation can be predicted with any other performance tradeoffs suggested by the model. In essence it is a mathematical model for a flux formulation. This system has essentially designed a *digital* solder paste. Figure 14 shows a small portion of the optimal formula of seven components and the responses of 15 significant paste properties.

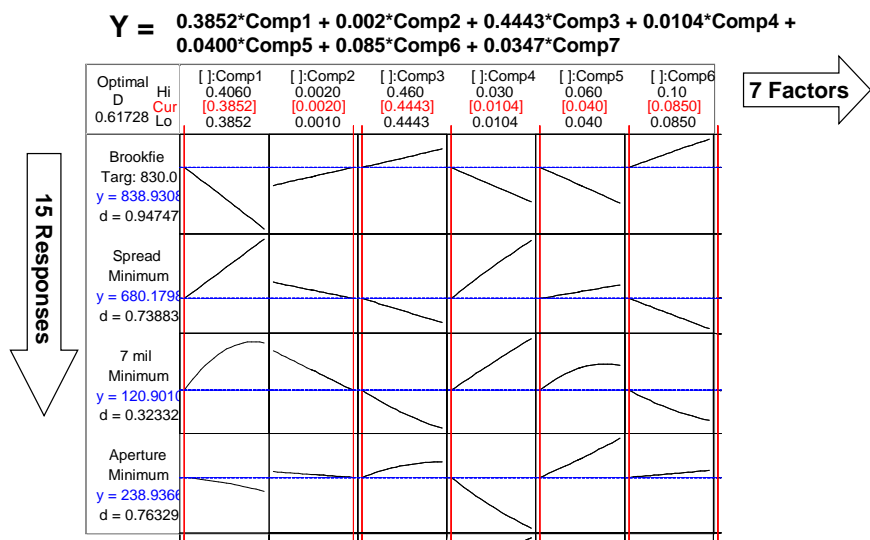


Figure 14 Response Optimization⁵

Verification

The last step is to verify that the desired paste improvements have been met or exceeded. In Figure 15 a stacked bar chart shows the old and new DFSS formulation in comparison to the other supplier's material at the OEM. Throughout scale up the material is also benchmarked to verify consistency. Final verification occurs on the customer's lines with normal process variables added in controlled experiments to verify the bandwidth of the final formulation. Minor variations in the formula, viscosity and/or solids can be included.

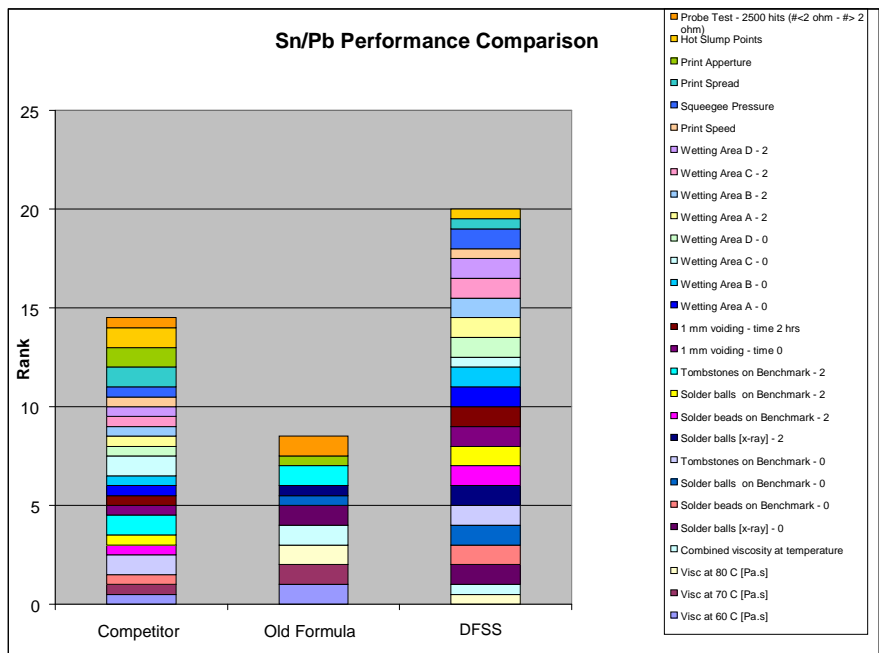


Figure 15 Verification

Selective Tests

The tests covered earlier in the paper were done on the entire 200+ pastes that were created during this project. When there was a significant change in chemistry, the corners of a DOE or at the discretion of the R&D team, additional tests were done on selective pastes to verify performance in either less important attributes or time-intensive tests.

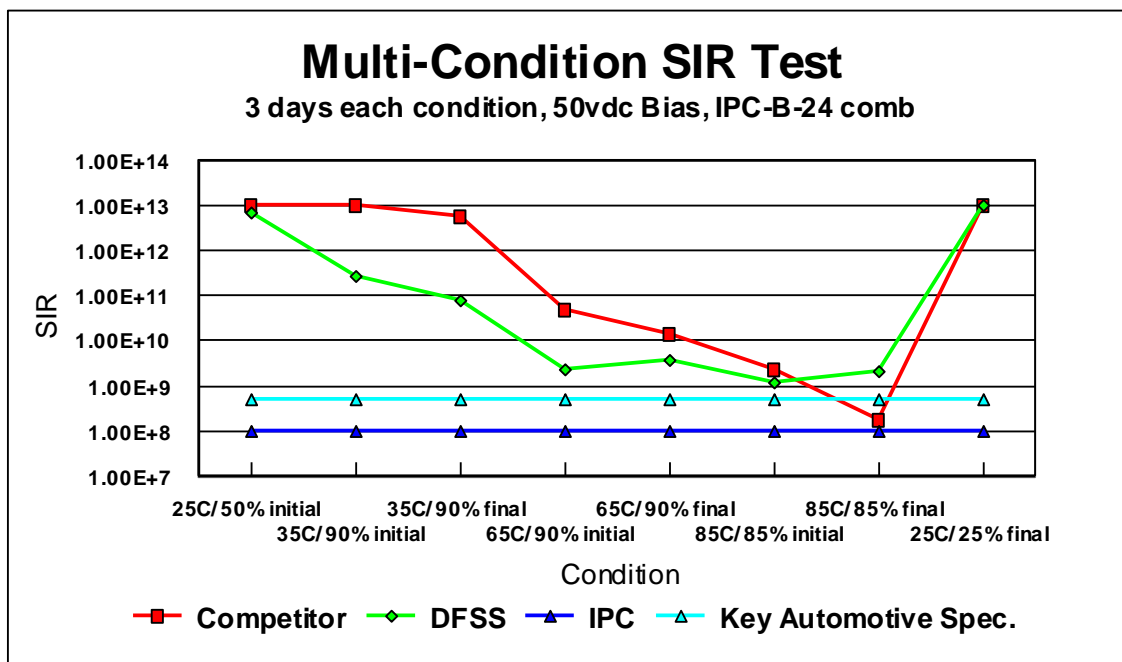


Figure 16 10 Day SIR Test

One time-intensive test was a SIR test that had three days at three different conditions (Figure 16). With setup and data analysis it ended up taking 10 days to complete.

Other selective tests were, ICT pin test, IPC tack and tack life tests, 1 hour abandon time test, intrusive reflow compatibility, conformal coat compatibility, BGA “Ball in Cup” defect sensitivity testing, storage stability and enclosed print head “compaction” compatibility. The “compaction” test was another important but time intensive test in that it involved a whole day of lab time. In this test a ProFlow head is filled with material to be tested and a 15 print test is done initially. This is a fourth type of print test where over 20 aperture locations on the test vehicle (Figure 17) are inspected for coverage by the printer’s 2D camera. The values of every aperture are stored in a data file and decoded to coverage charts in a spreadsheet. The stencil is replaced with a no aperture stencil and the print head is cycled in simulated printing for a minimum of 2000 prints. The head is removed, a trough of paste is removed on the printing side of the head, the stencil is re-installed and another 15 print 2D inspect test is performed without “priming” the head. If material is compacted in any portion of the head the print coverage recovery will either be slow (> 5 prints) or non existent. Figure 18 shows the results of a successful post compaction cycle 2D print test.

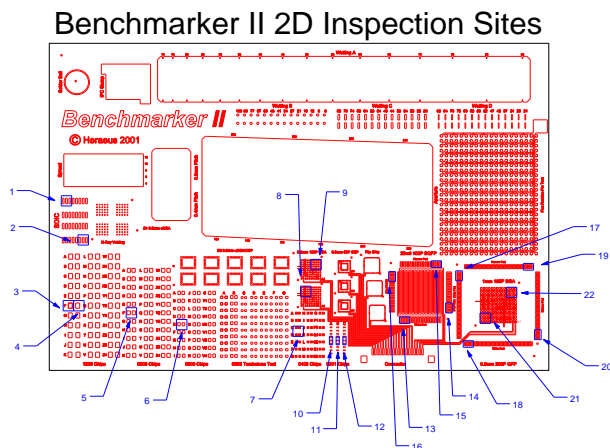


Figure 17 Compaction 2D Print Test

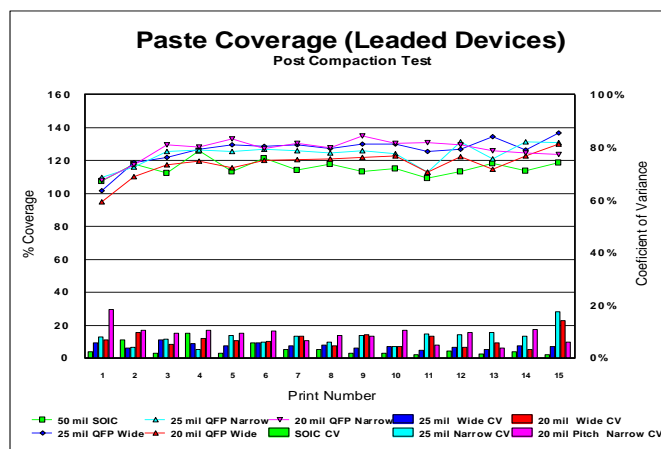


Figure 18 Post Compaction 2D Inspection Results

Conclusions

By using a series of defined measurable tests, selected for relevance and used in DOE's, it is possible to develop a solder paste tailored to specific needs. The result is a formula that is more stable over raw material lots, time, process and environmental variations. This method was applied to a no clean Sn/Pb paste and resulted in the first reformulated paste of this type in the 21st century. Factors in this success include:

- Only with quantitative paste attribute tests that are repeatable and reveal formulation performance contrast can a DFSS solder paste development project be successful.
- The OEM and its solder paste supplier have developed a more synergistic relationship with a greater level of solder paste formulation comprehension as a direct result of applying the DFSS tool set.
- In the application of the DFSS methods, Applications benchmark testing has been both improved and verified. The knowledge and skills have facilitated a new lead free DFSS project which is currently underway.
- Analog trial and error development methods have been replaced by DFSS tools. Qualitative perception based testing methods have been replaced by statistically significant quantitative ones. The merging of both of these improvements is required to develop the truly digital solder paste.

Acknowledgements

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- Steve Fritzinger and Derrick Moyer for their tireless testing support of 200+ pastes and over 2500 tests to support this project.
- Mike Skrzat for his project leadership, consistent customer communication and persistence towards a black belt certification.
- Research and Development for their chemical knowledge, leadership and the construction of over 200 pastes to support this project.

References

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THE DIGITAL SOLDER PASTE

RICK LATHROP

Paste Requirements

1989

- RMA
- Squeegee (2ips max)
- HASL
- Tin/ lead components
- 15 min Abandon time
- 50 mil pitch QFP
- 8 mil stencil
- $\approx 24 \text{ ¢/g}$

2009

- No Clean L0
- Squeegee (6ips max)
- LF HASL, OSP, ENIG, Imm Ag, Imm Sn
- 100% tin, Pd flash components
- 1 hr Abandon time
- 0.4/0.5mm pitch QFP & BGA
- 5-6 mil stencil
- $\approx 8 \text{ ¢/g}$
- ICT compatible residue
- Conformal coat compatible
- Intrusive reflow compatible
- Enclosed print head compatible

Solder Paste Development

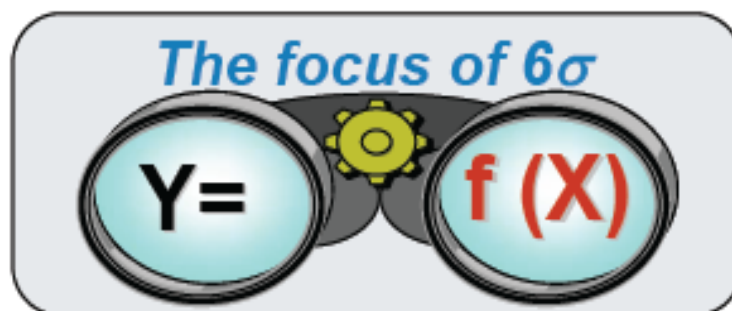
1989

- **Tweaking previous formulations**
- **Trial and error science**
- **Subjective measurements by “experts eyes”**
- **Qualitative testing**
- **Trial by fire at customer**

2009

- **DFSS**
 - **House of Quality distilled from customers requirements**
 - **Mixture design of experiments**
 - **Response optimization to balance paste property desirability's**
- **Quantitative Testing**
 - **Test “parallax” for major properties**
 - **Measurement Systems Evaluations to ensure good test methods**
 - **Non-subjective test methods**

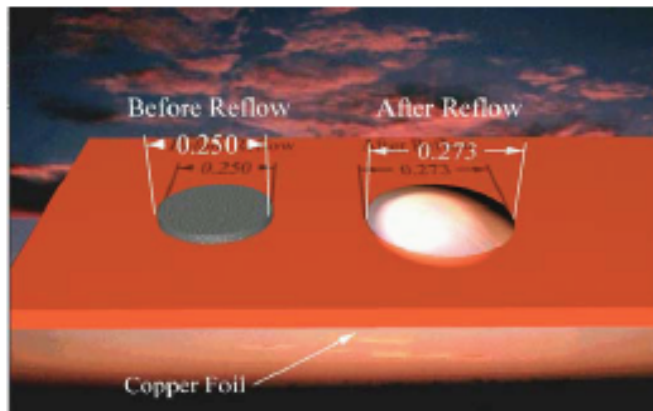
Main Goal of DFSS Program



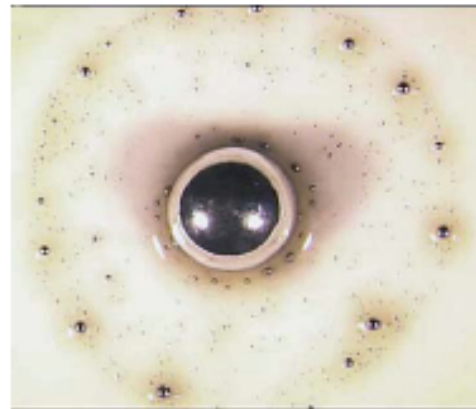
$$y = f(x)\text{resin} + f(x)\text{solvent} + f(x)\text{activator} + f(\text{acid}) + f(x)\dots$$

A mathematical model for a flux formulation

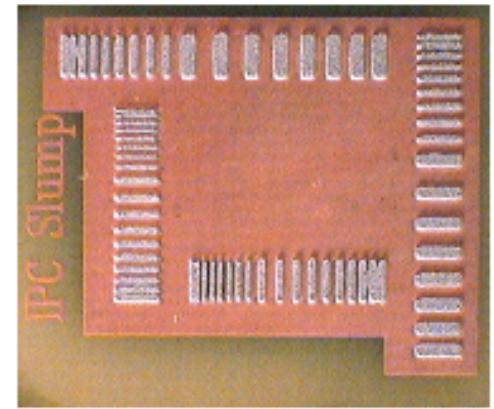
Historical Paste Tests



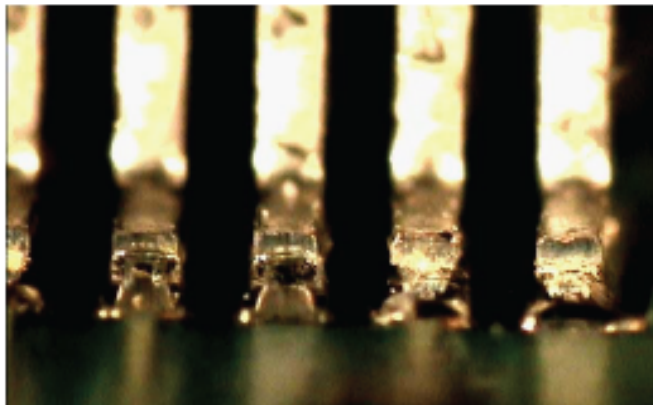
IPC Wetting



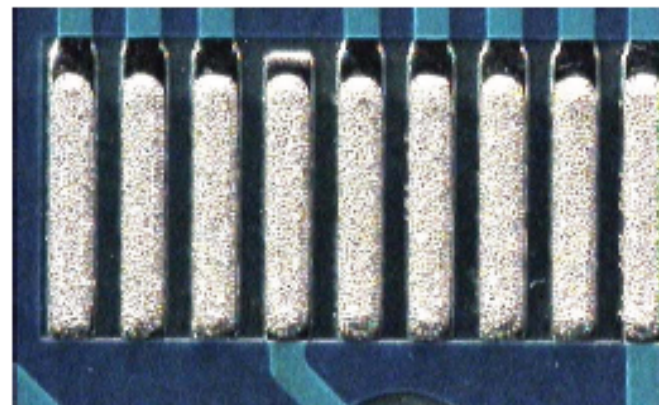
IPC Solder Ball



IPC Slump

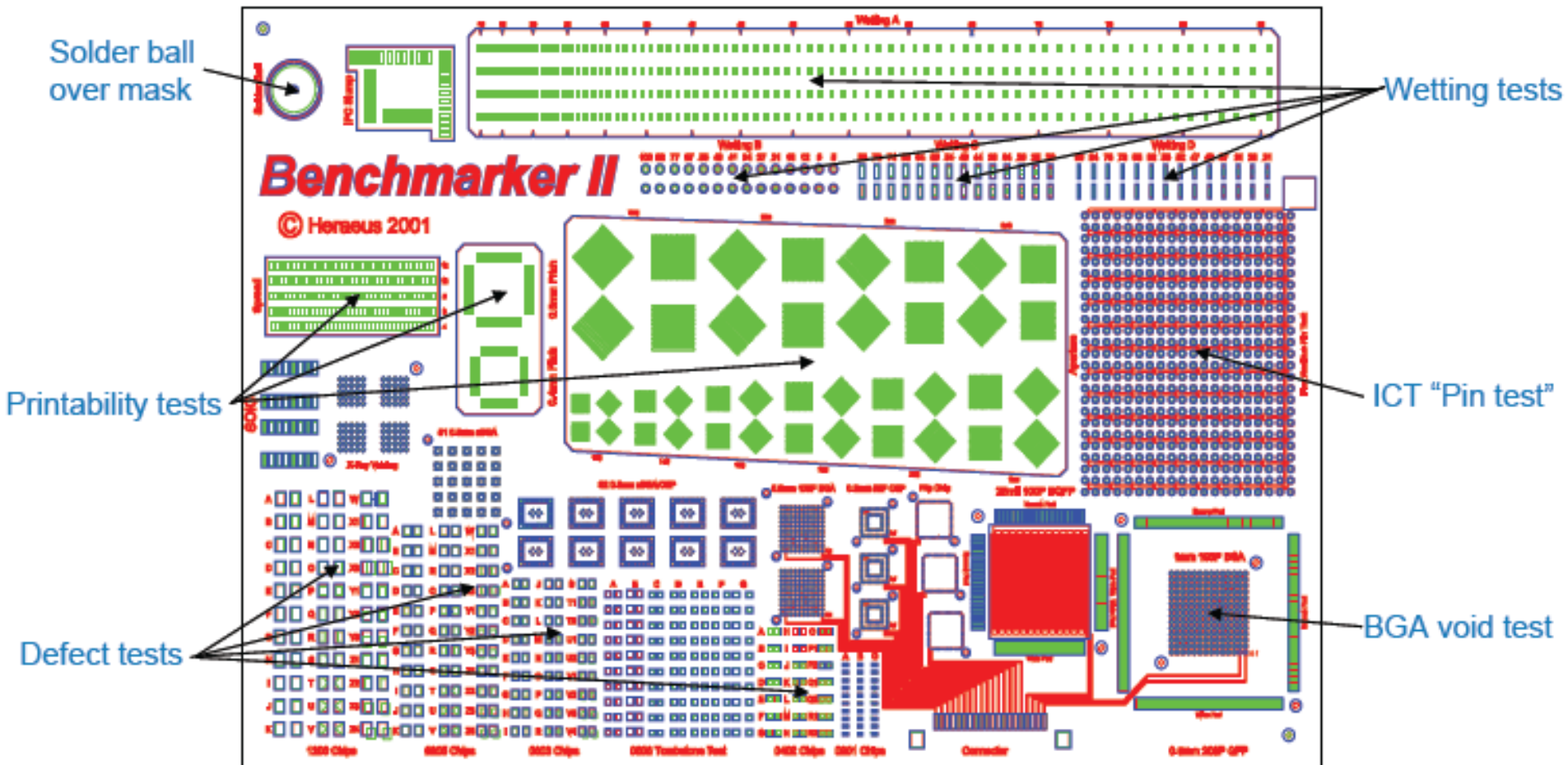


Visual Wetting (toe fillets)



Visual Printing (fine pitch)

Quantitative Performance Tests



A Printability Test Protocol that Vet Pastes for Speed

— Start @ 6ips and 15kg

- If clean wipe, lower pressure to find minimum
- If smeared wipe, lower speed to find maximum
- Run screen clean and begin 15 print test

1. Print →

2. **Print ← inspect *Spread* and *Aperture***

3. Print →

4. Print ←

5. **Print → inspect *Spread* and *Aperture* then re-inspect after heating for *Hot Slump***

6. Print ←

7. Print →

8. Print ←

9. **Print → inspect *Spread* and *Aperture* then store @ 25oC/65% RH for 2 Hours**

10. **Print ← inspect *Spread* and *Aperture* then populate and reflow**

Clean screen (wet - vac - dry)

11. **Print → populate and reflow**

12. **Print ← store @ 25oC/65% RH for 2 Hours**

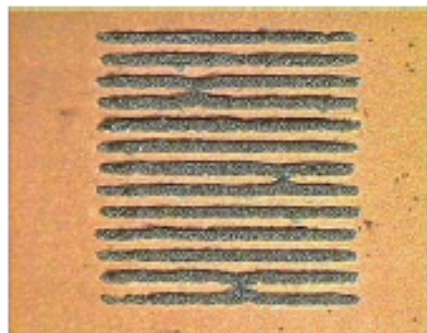
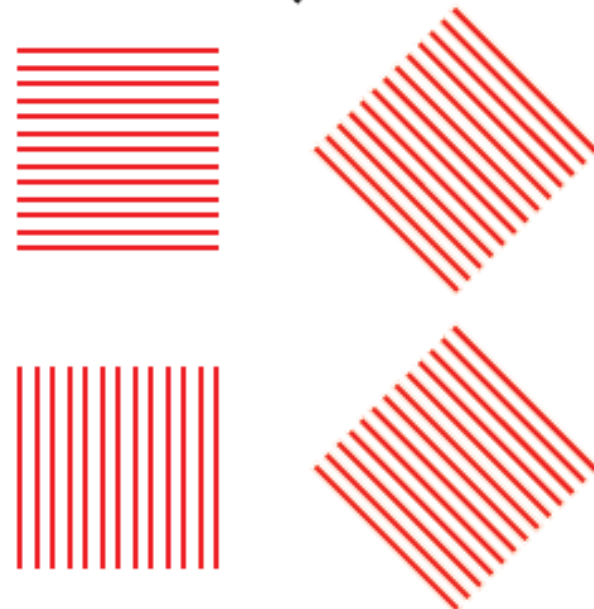
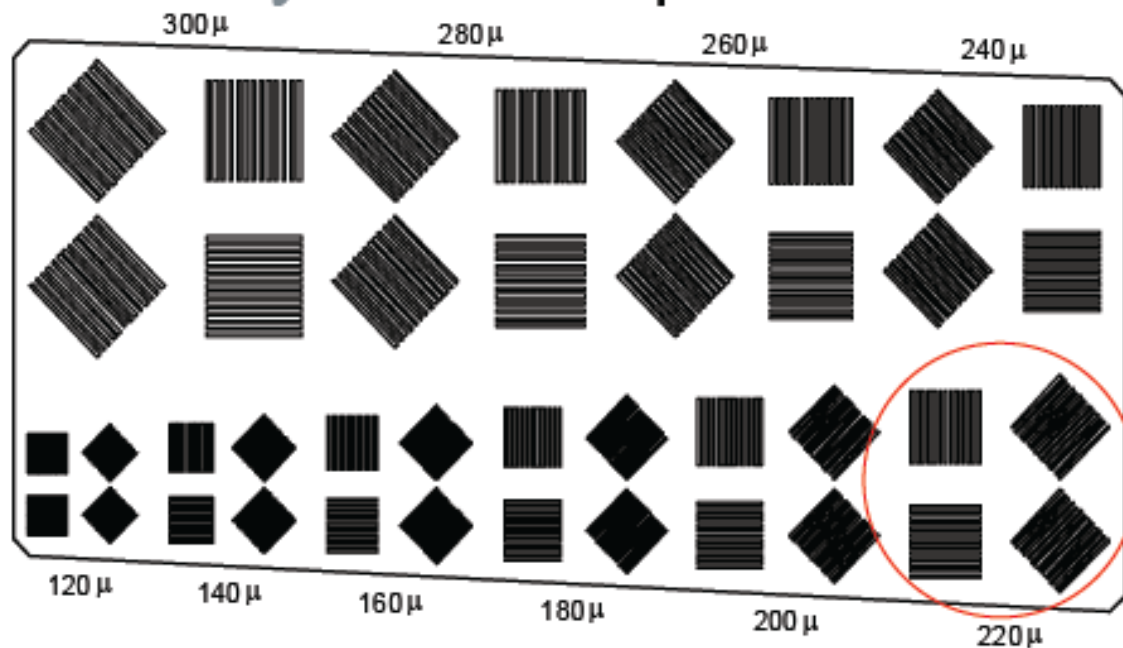
13. Print →

14. Print ←

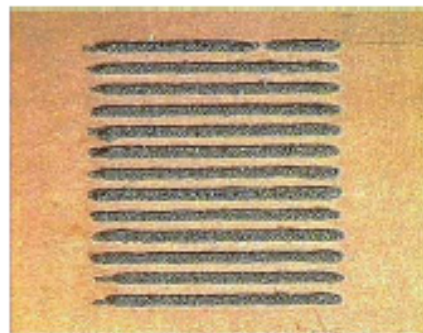
15. **Print → inspect *Spread* and *Aperture* then measure *Solder Volume***

Populate and reflow prints 9 & 12

Printability Test 1 - Aperture Test



Shorts



Line Opens

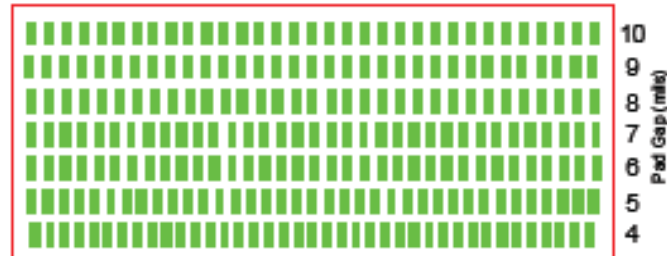
Printability Test 2 - Spread Test (Improved by DFSS)

Original Design

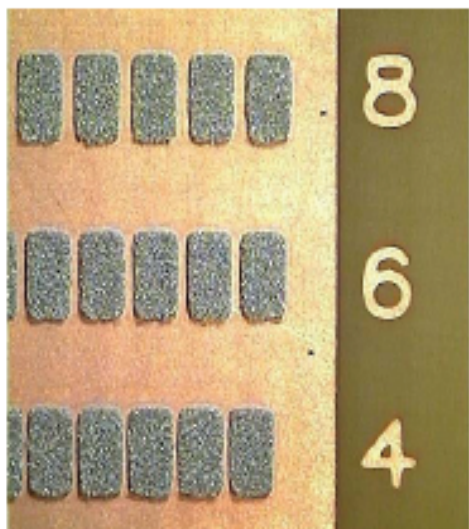


MSE showed
most of data
in this range

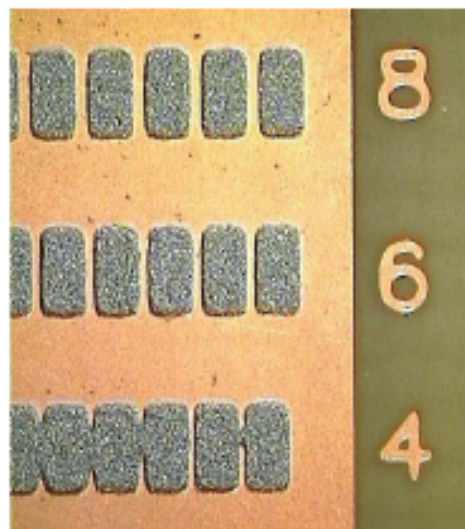
New Design



No
Spread



Slight
Spread

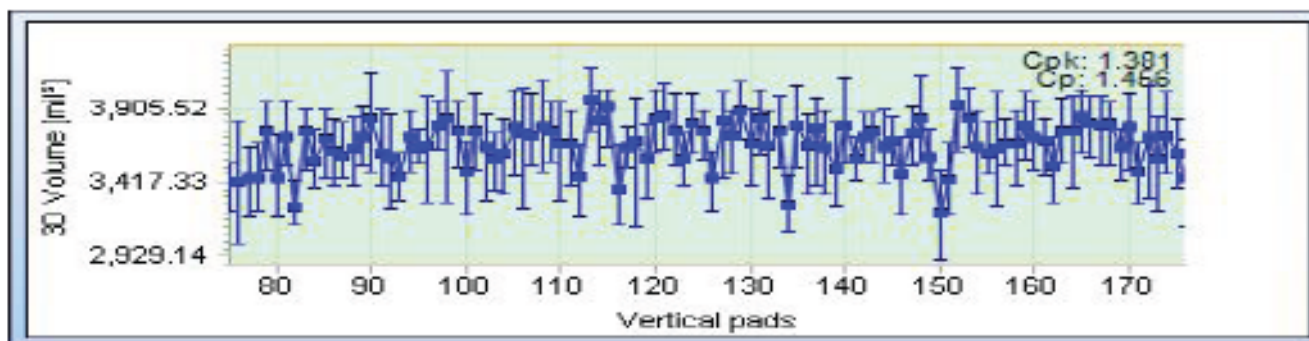
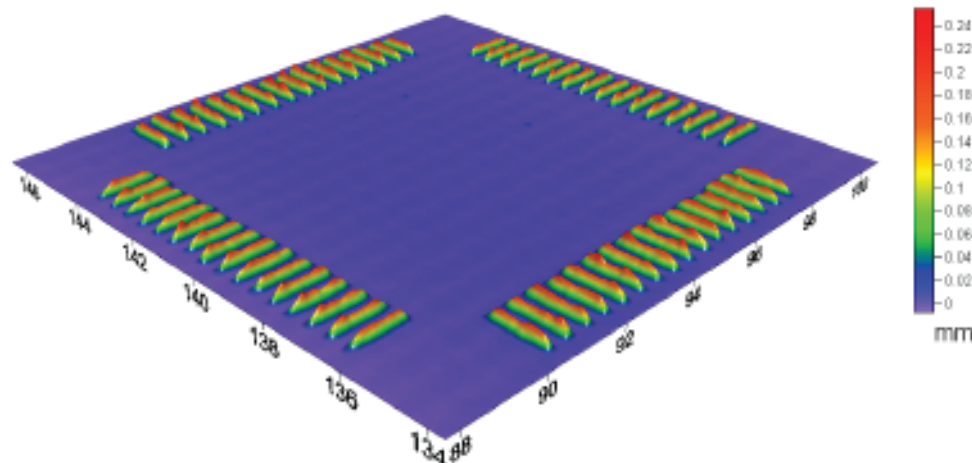


Printability Test 3 – Solder Volume over Time

0.5mm Pitch QFP Print

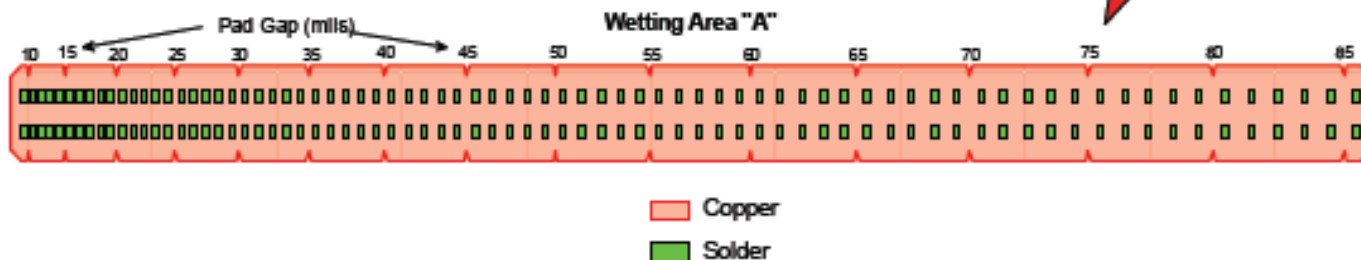
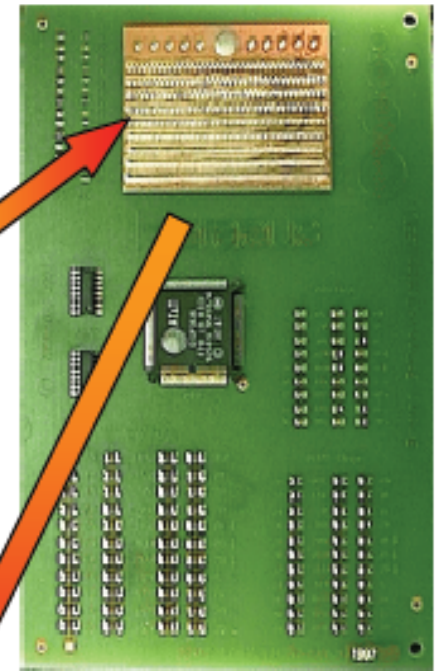
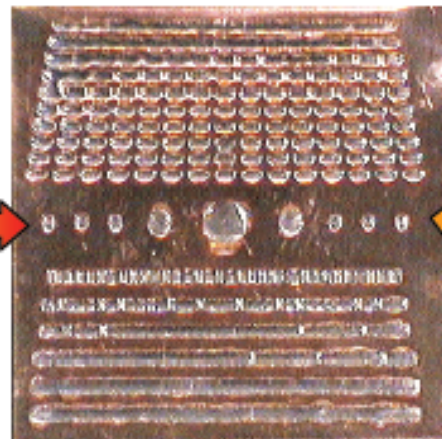
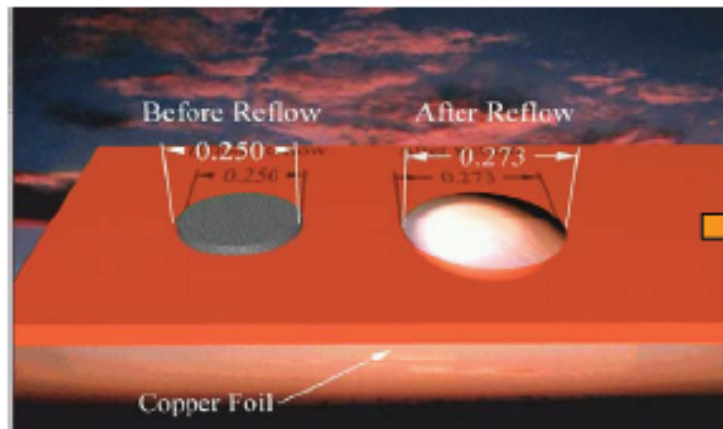
Print # 15 measured

- Initially print #2 and #15 measured
- Measurement of print #2 dropped since only #15 varied by formulation
- Average volume and STD

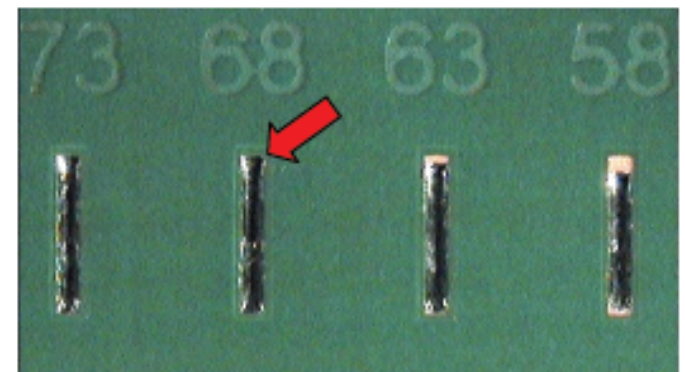
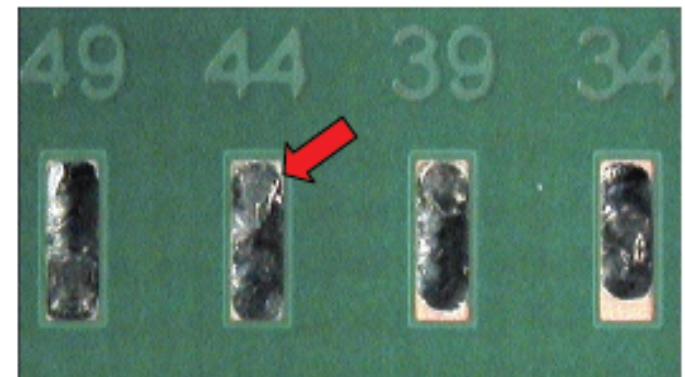
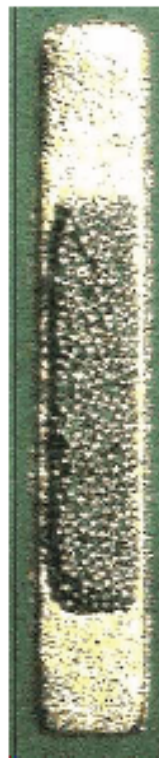
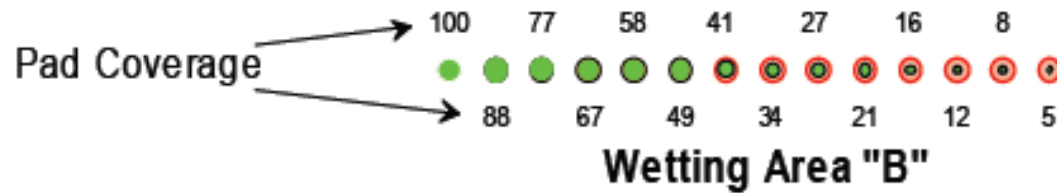


15th Print QFP Volume Data

Wetting Tests - Area A Development History

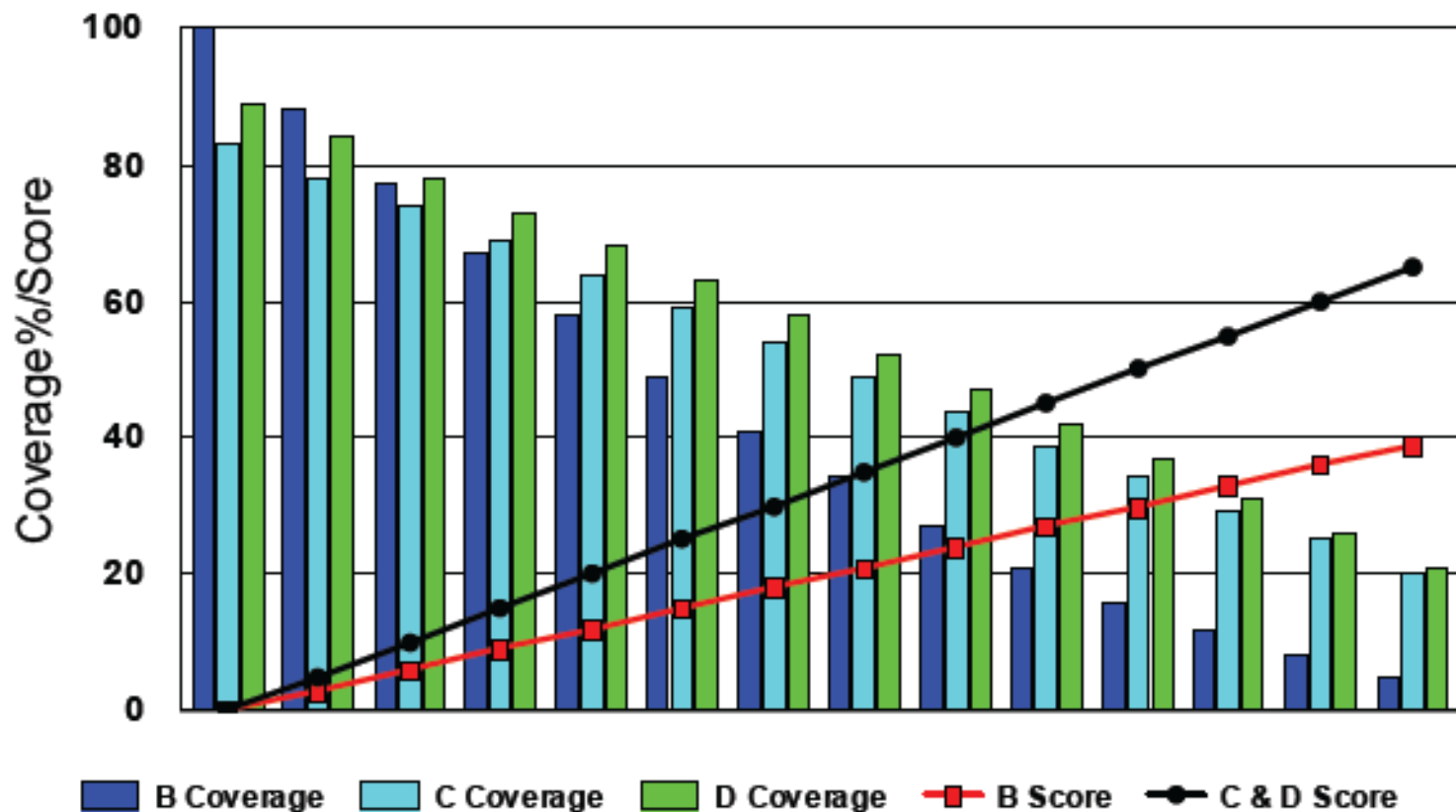


Wetting Tests - Areas B,C&D

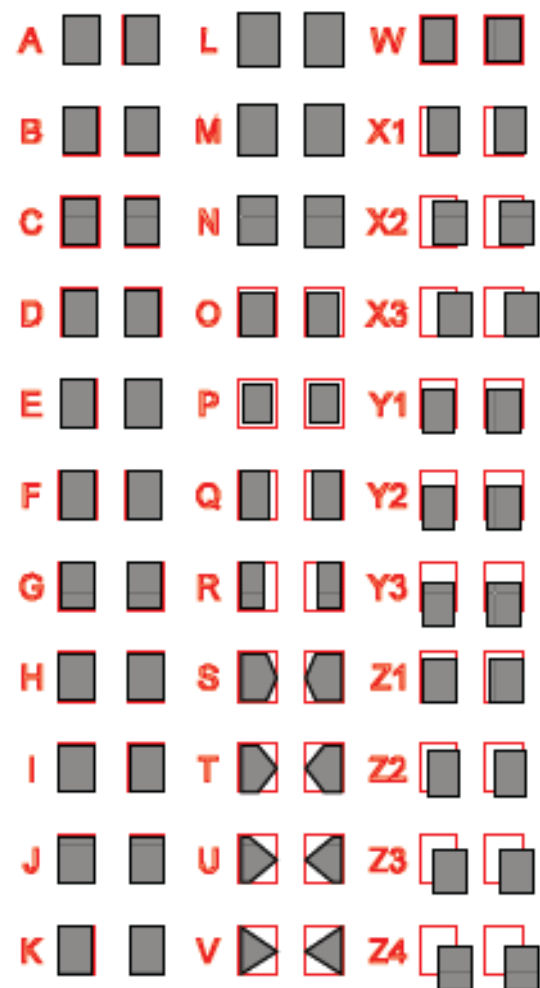


Wetting Tests - Scoring Results

Wetting "Thermometer" Scoring



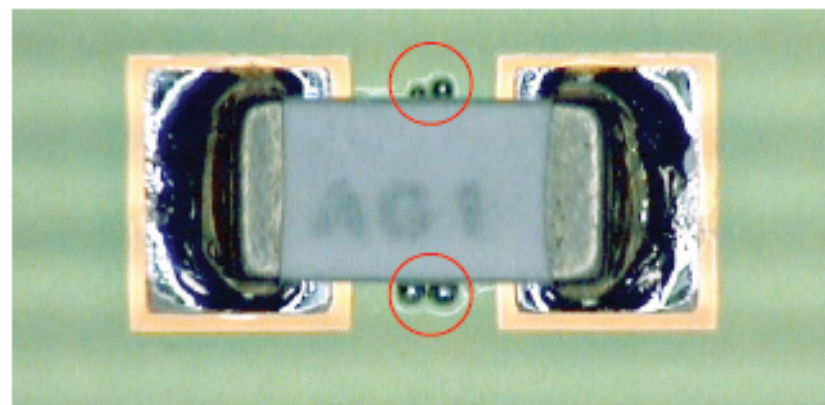
Reflow Defect Testing – Passive Components



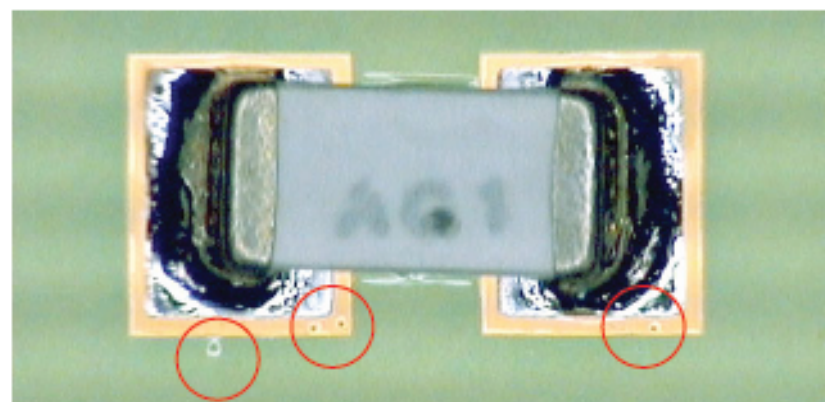
 Pad
 Paste

Pad-Pad Gap Aperture Alignment

1206, 0805, 0603, 0402



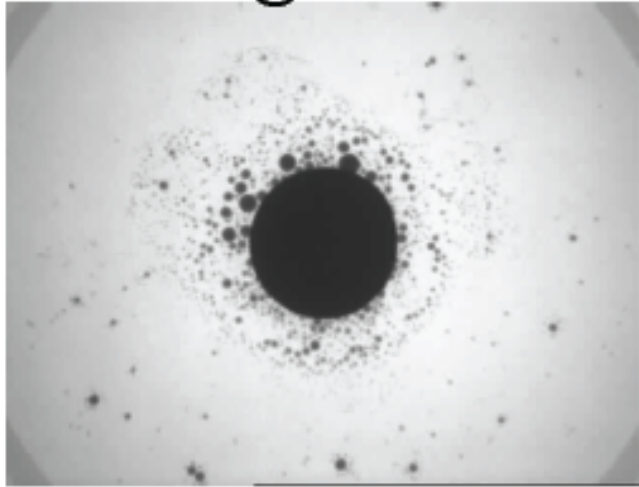
Solder Beads



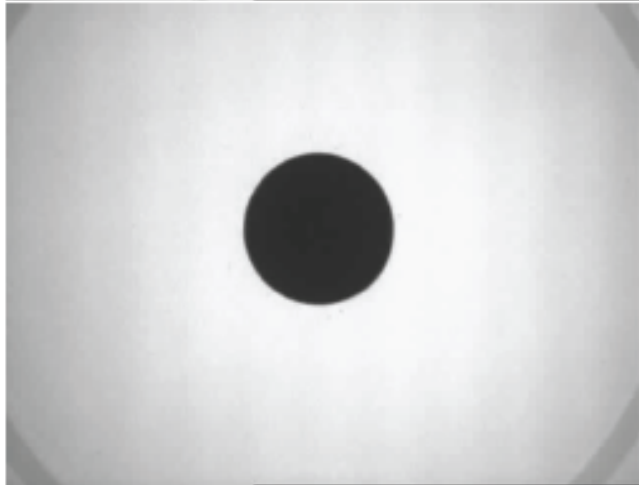
Solder Balls

Reflow Defect Testing – Solder Ball over Mask

2 Hours @ 65%RH/25C



Old
Formula



DFSS
Formula



Selective Tests

— More time consuming tests

- Compaction – 2000 prints
- SIR – 10 days
- Print After Wait – 3 hours
- Pin Tests – 2500 probes

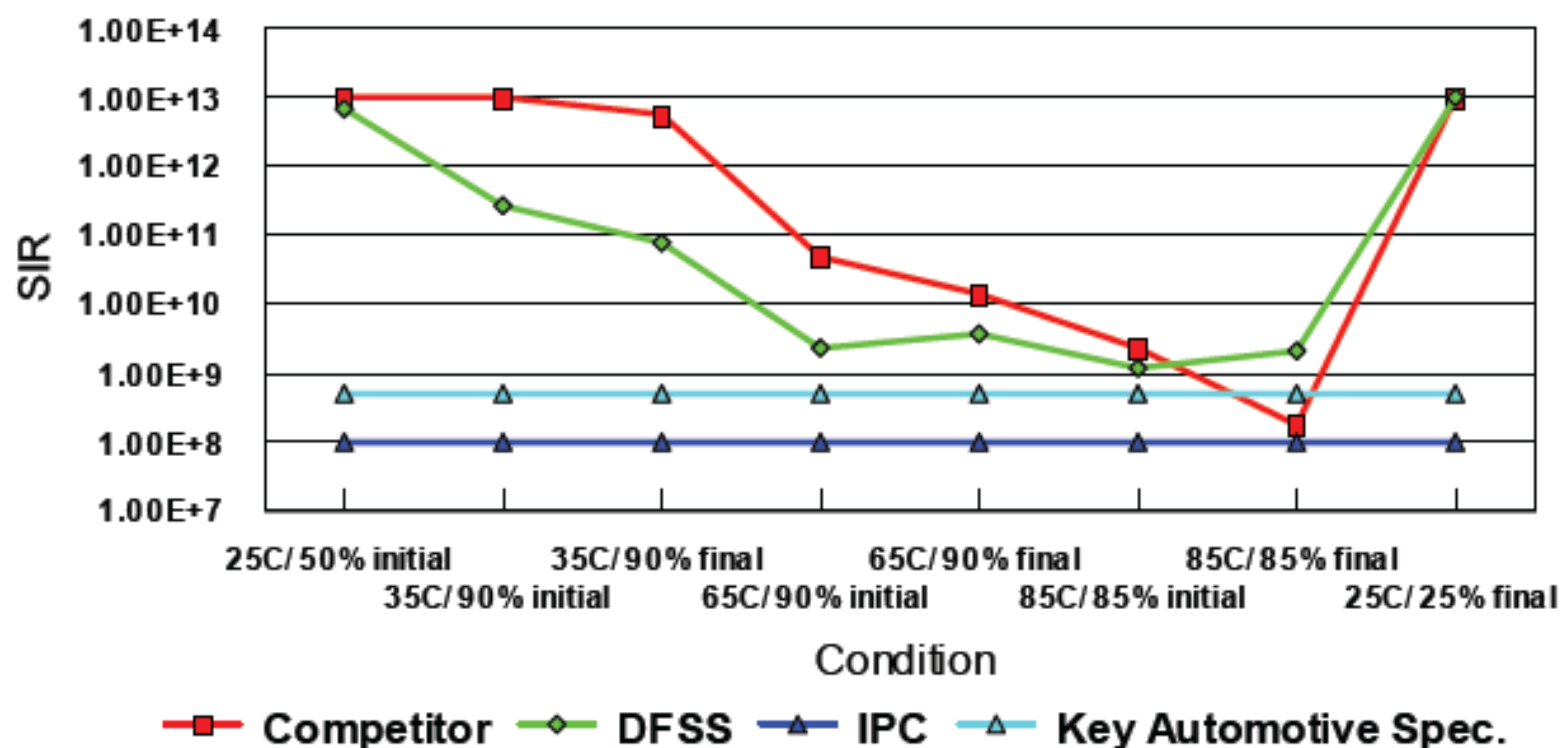
— Done on “Chemical Extremes”

- Corners of DOE's (ingredient concentration extremes)
- New ingredients
- Screening Experiments
- Final formulas in Verification stage

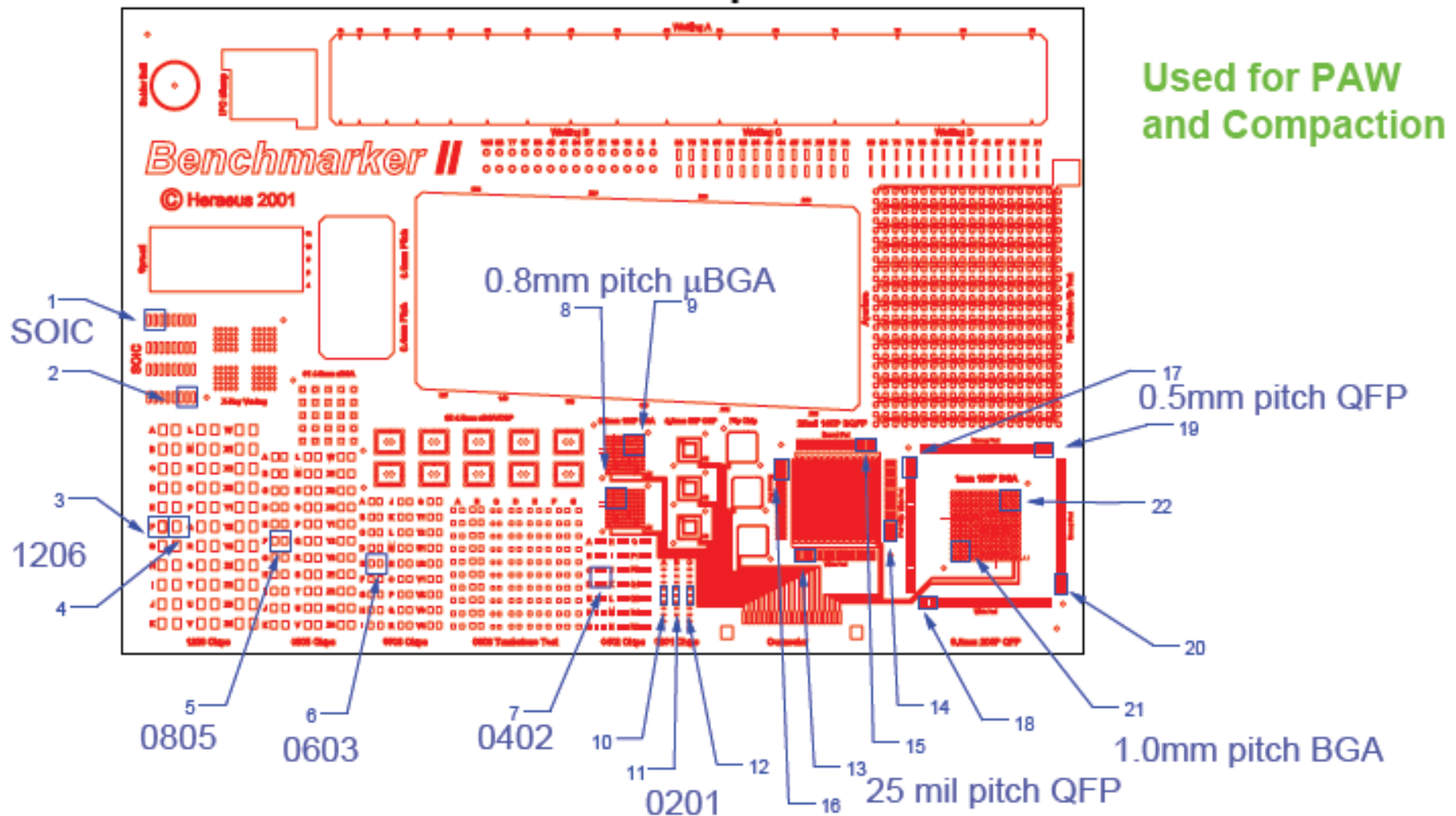
Selective Tests: Surface Insulation Resistance

Multi-Condition SIR Test

3 days each condition, 50vdc Bias, IPC-B-24 comb

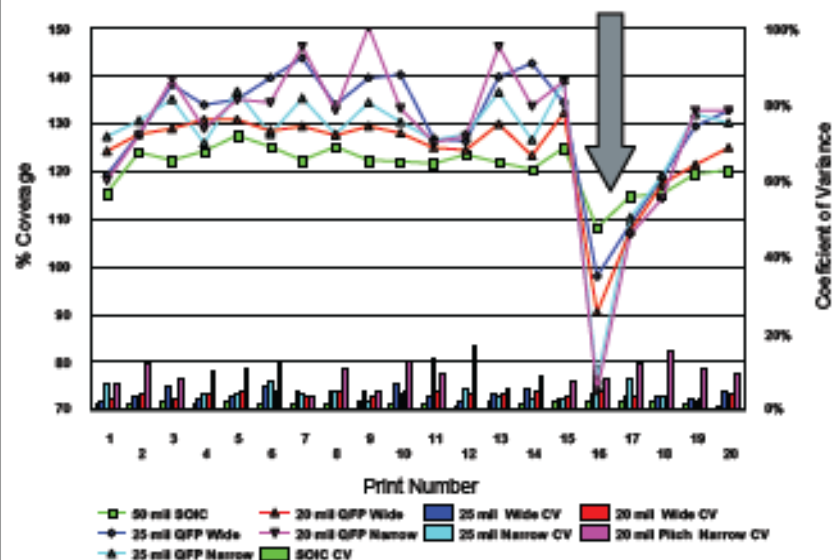


Selective Printability Tests - 2D Inspection Test



Selective Printability Tests – Print After 1hr Wait (PAW)

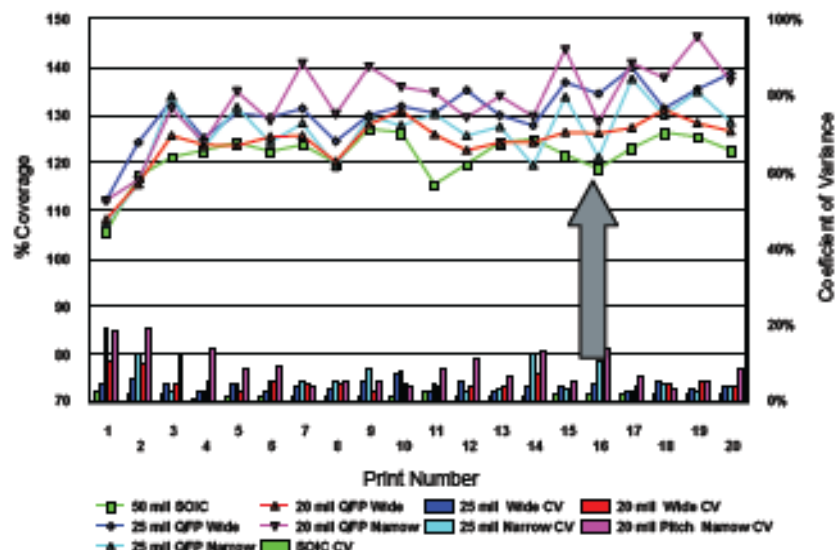
Paste Coverage (Leaded Devices)



PAW Index = 96

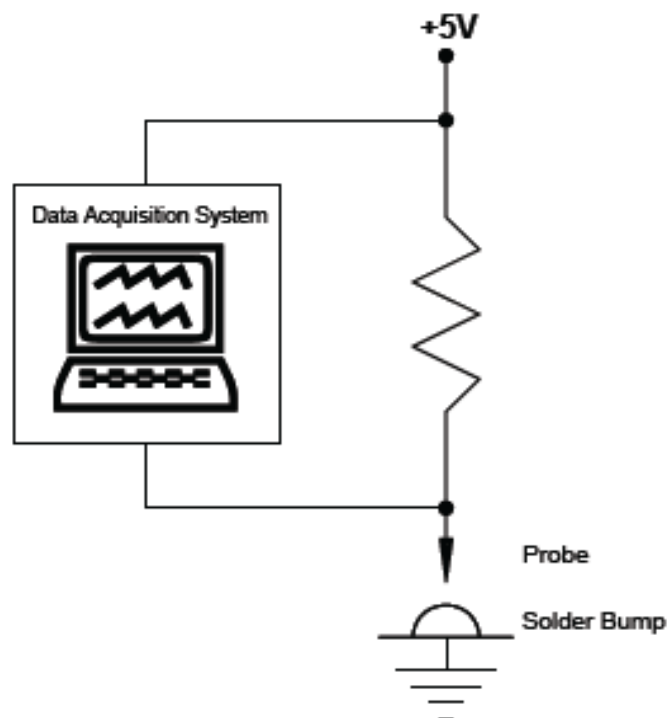
PAW Index = avg coverage reduction (15th – 16th prints) + avg blockage increase (15th – 16th prints) for sites 15 & 16 (25mil pitch narrow pads)

Paste Coverage (Leaded Devices)

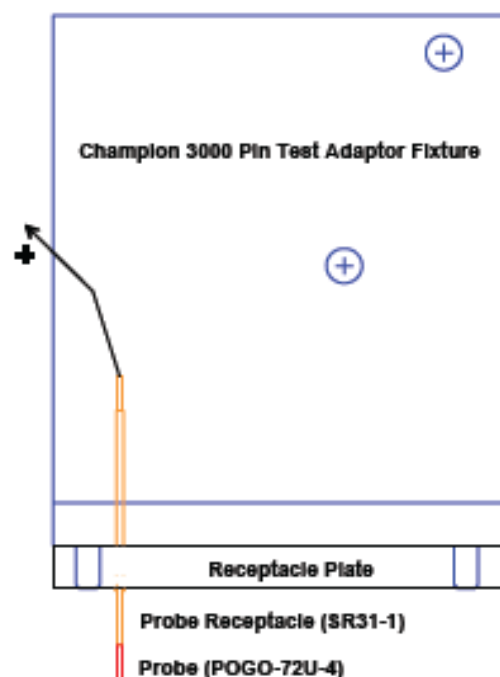


PAW Index = 18

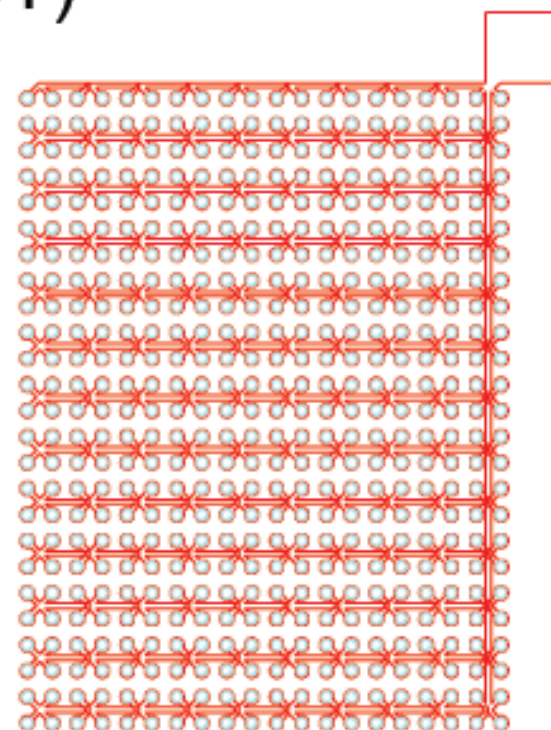
Selective Testing - Pin Testability (ICT)



Schematic



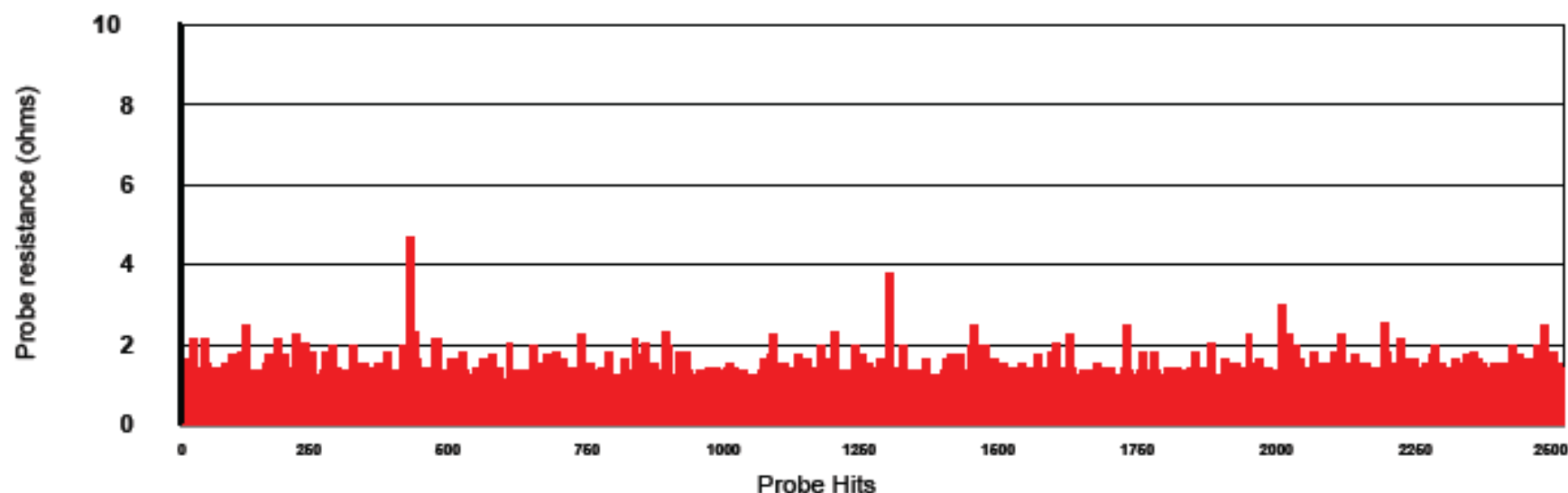
Probe Fixture



500 Pad Array

Pin Testability – Raw Data

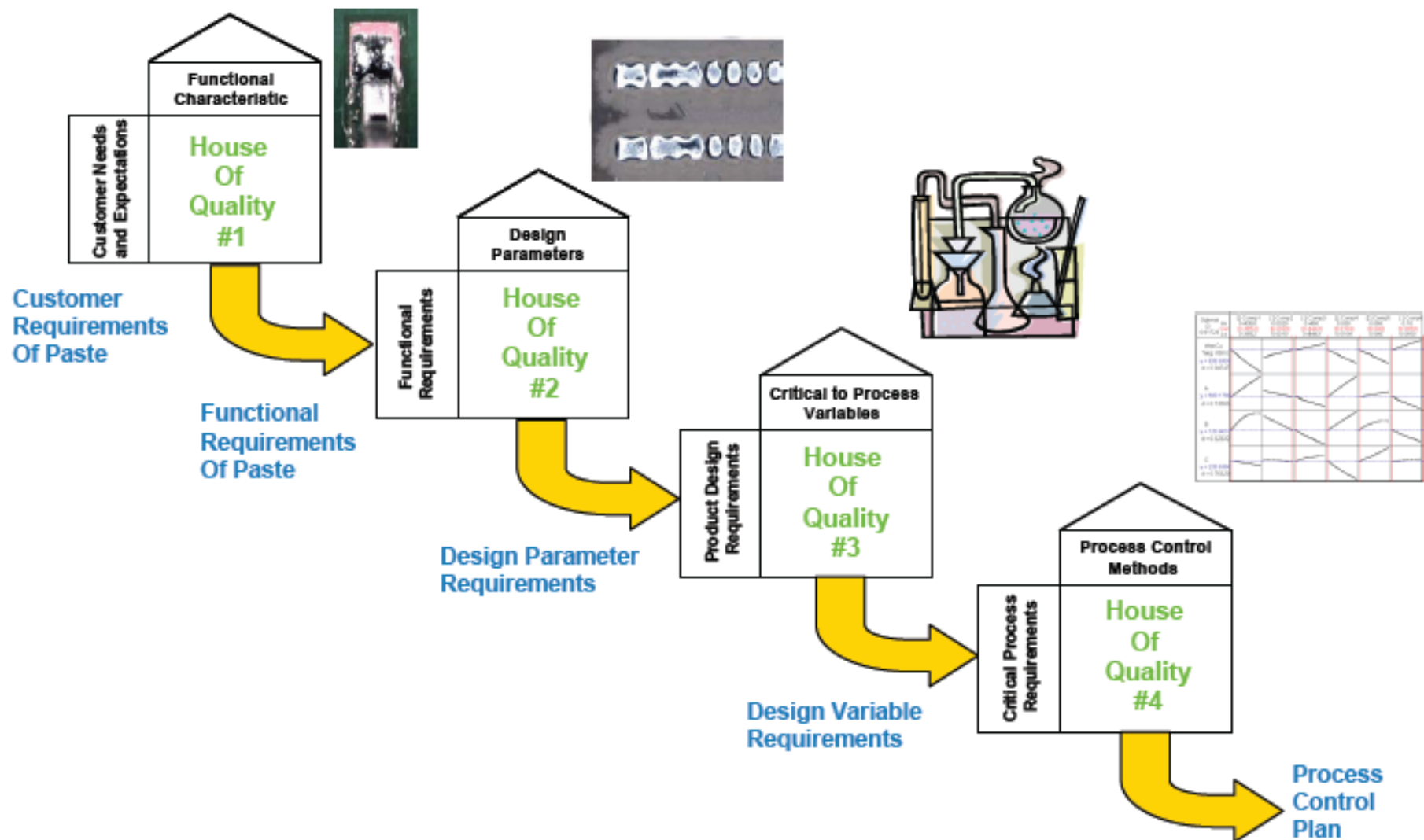
Simulated In-circuit Test



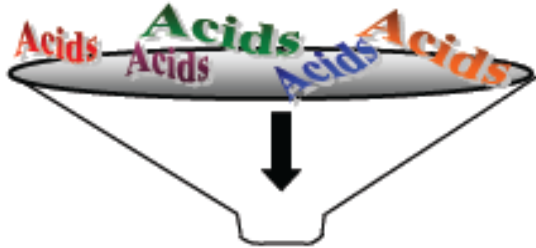
DFSS Tool Box

- **House of Quality (HOQ)** to establish Voice of Customer (VOC)
- **Measurement Systems Evaluations (MSE)** define variability in testing
- **Process Maps (PMAP)** and **Failure Mode and Effects Analysis (FMEA)** define variability in process
- **Mixture Design of Experiments (DOE)** because solder paste has a constraint formula
- **DOE Regression Analysis** determines the formulation model
- **Response Optimization** shows the performance of each raw material

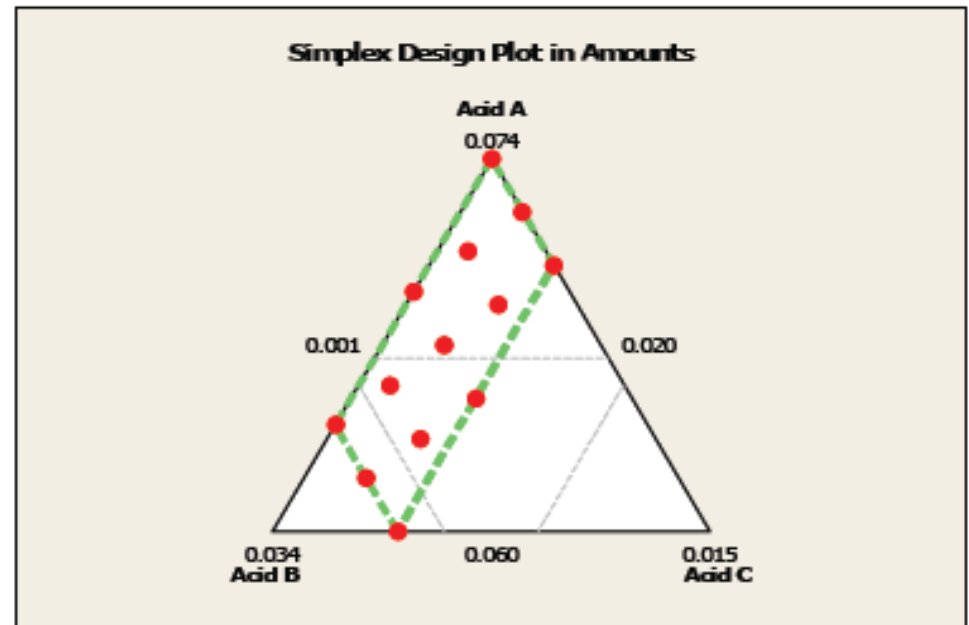
House of Quality Concept



Design Simplification



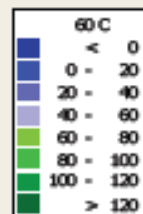
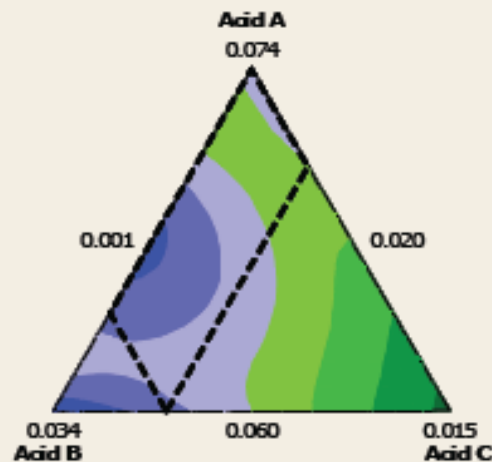
- Screening designs for continued raw material selection
- Separate experiments according to functionality
 - Resins
 - Activators



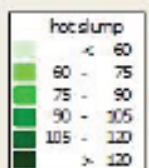
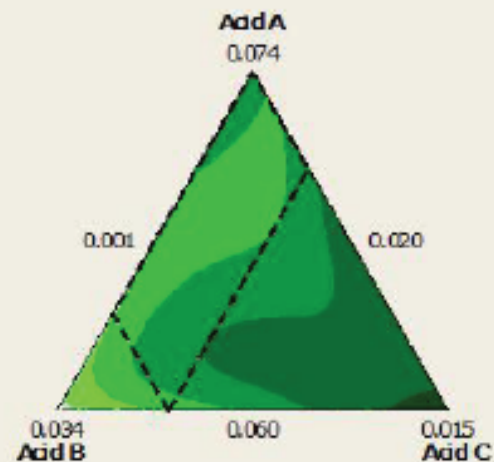
Screened six different acids of various functionality. Selected three to continue in the design above.

Analysis tools

Mixture Contour Plot of 60 C
(component amounts)



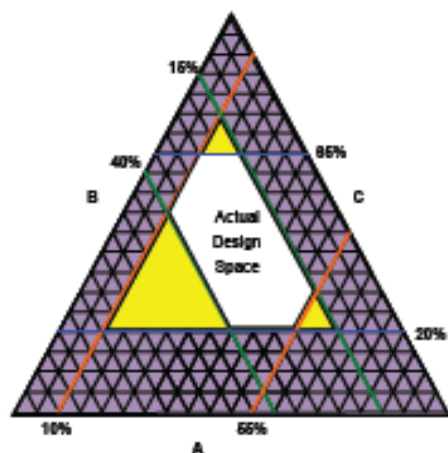
Mixture Contour Plot of hot slump
(component amounts)



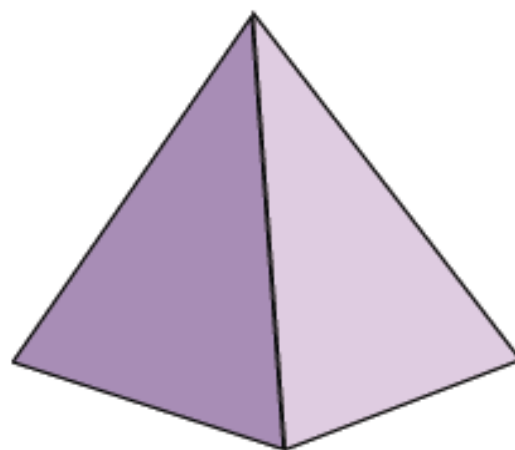
Contour and surface plots graphically show the performance within the inference space

Mixture Modeling Dilemma (11)

Basic models

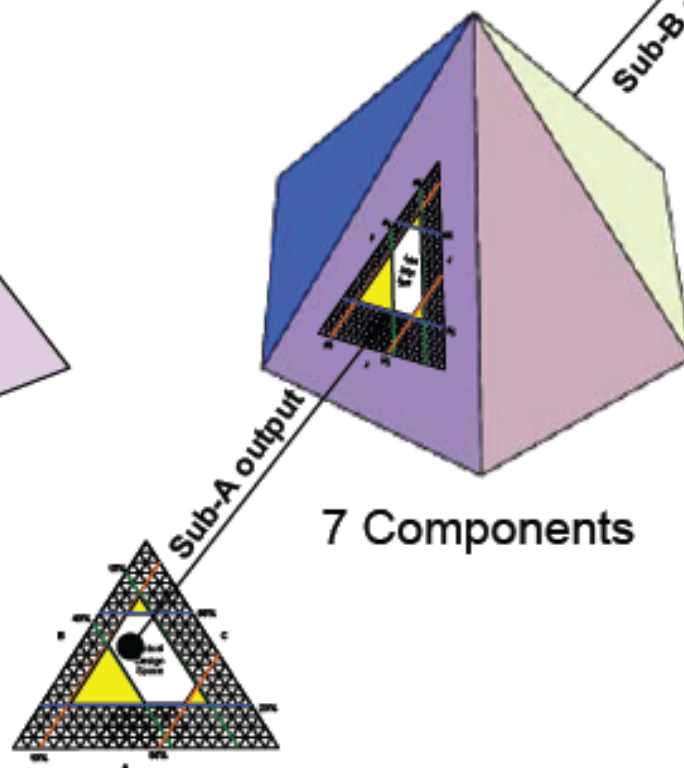


3 Components

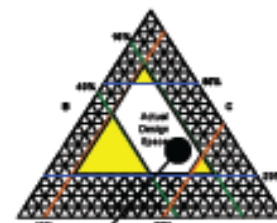


4 Components

Solution: Sub-mixtures + data blocking

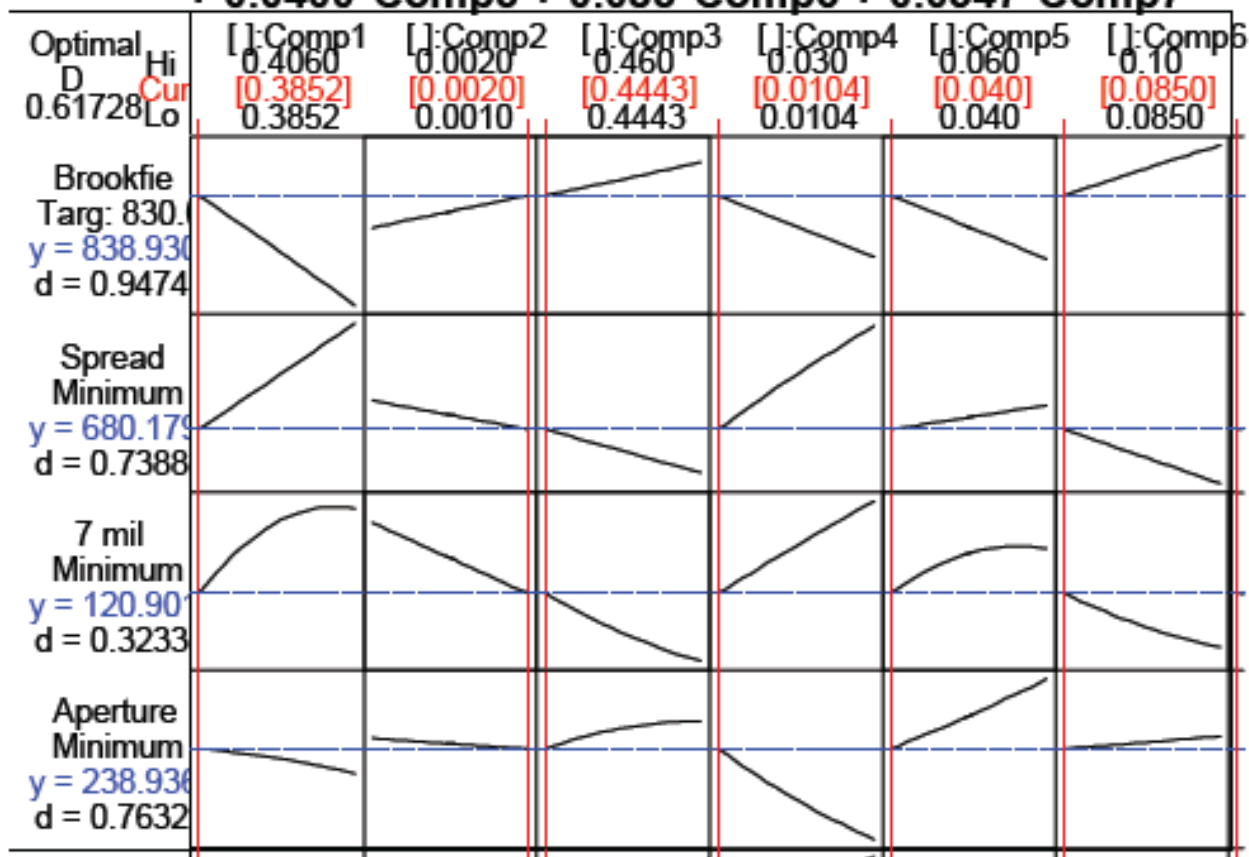


7 Components



Response Optimization

$$Y = 0.3852 \cdot \text{Comp1} + 0.002 \cdot \text{Comp2} + 0.4443 \cdot \text{Comp3} + 0.0104 \cdot \text{Comp4} + 0.0400 \cdot \text{Comp5} + 0.085 \cdot \text{Comp6} + 0.0347 \cdot \text{Comp7}$$



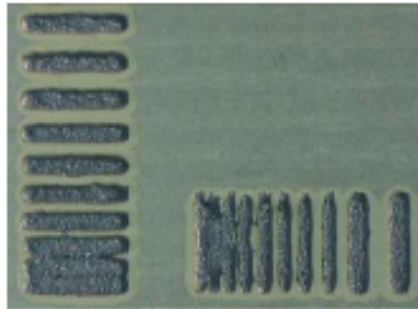
7 Factors

15 Responses

Verification - Fast Printing

Old Formulation

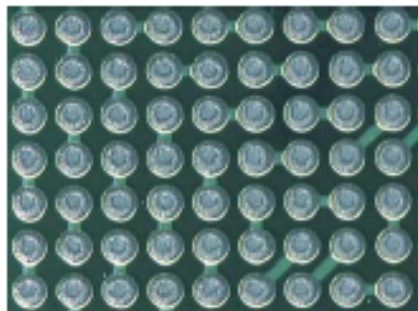
15kg squeegee pressure



IPC Slump



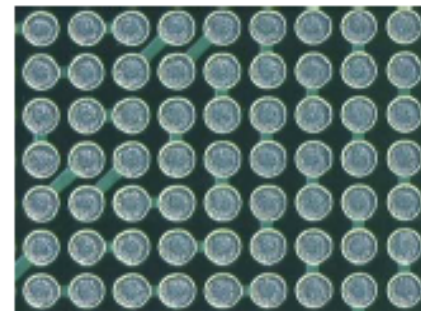
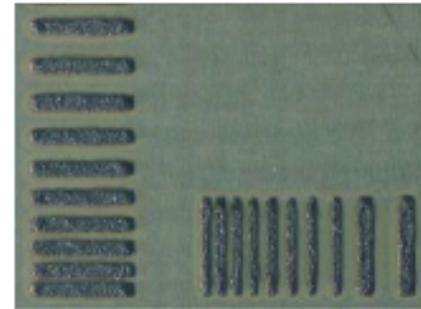
25 & 20 mil pitch



1mm pitch BGA

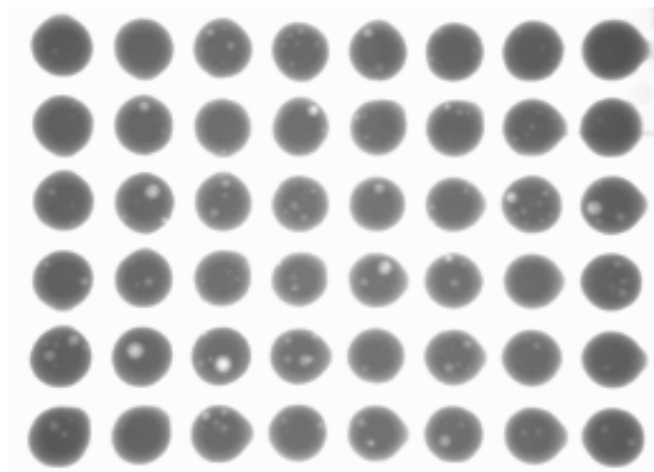
DFSS Formulation

10kg squeegee pressure

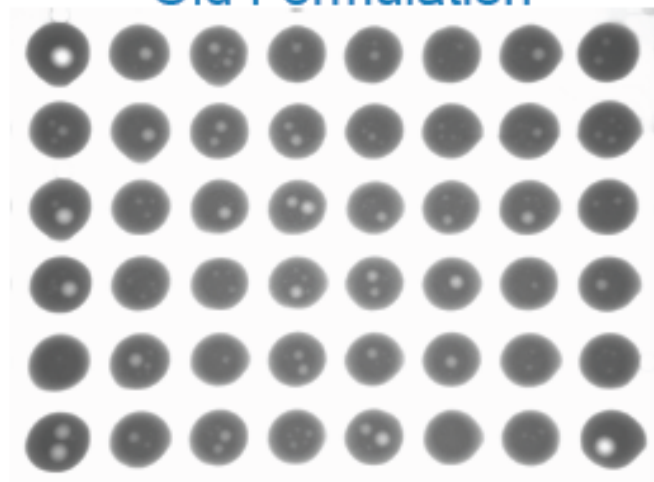


Example: 100mm/s print speed, type 3 powder

Verification - Low Voiding (X-ray of BGA)

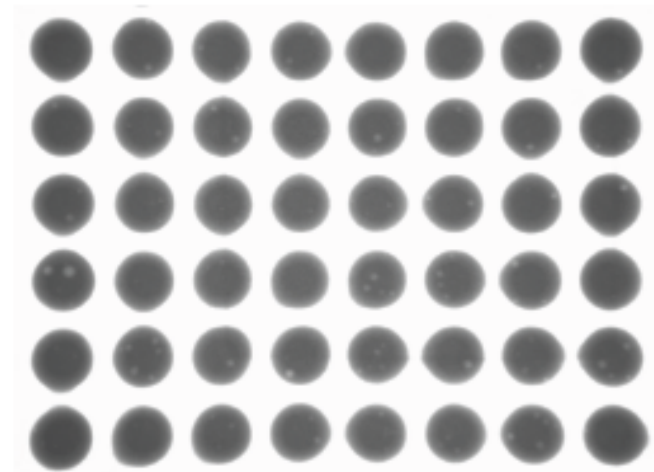


Old Formulation

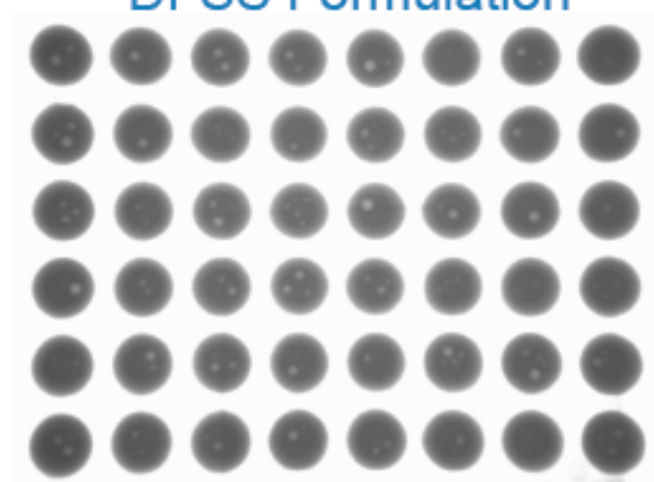


OSP

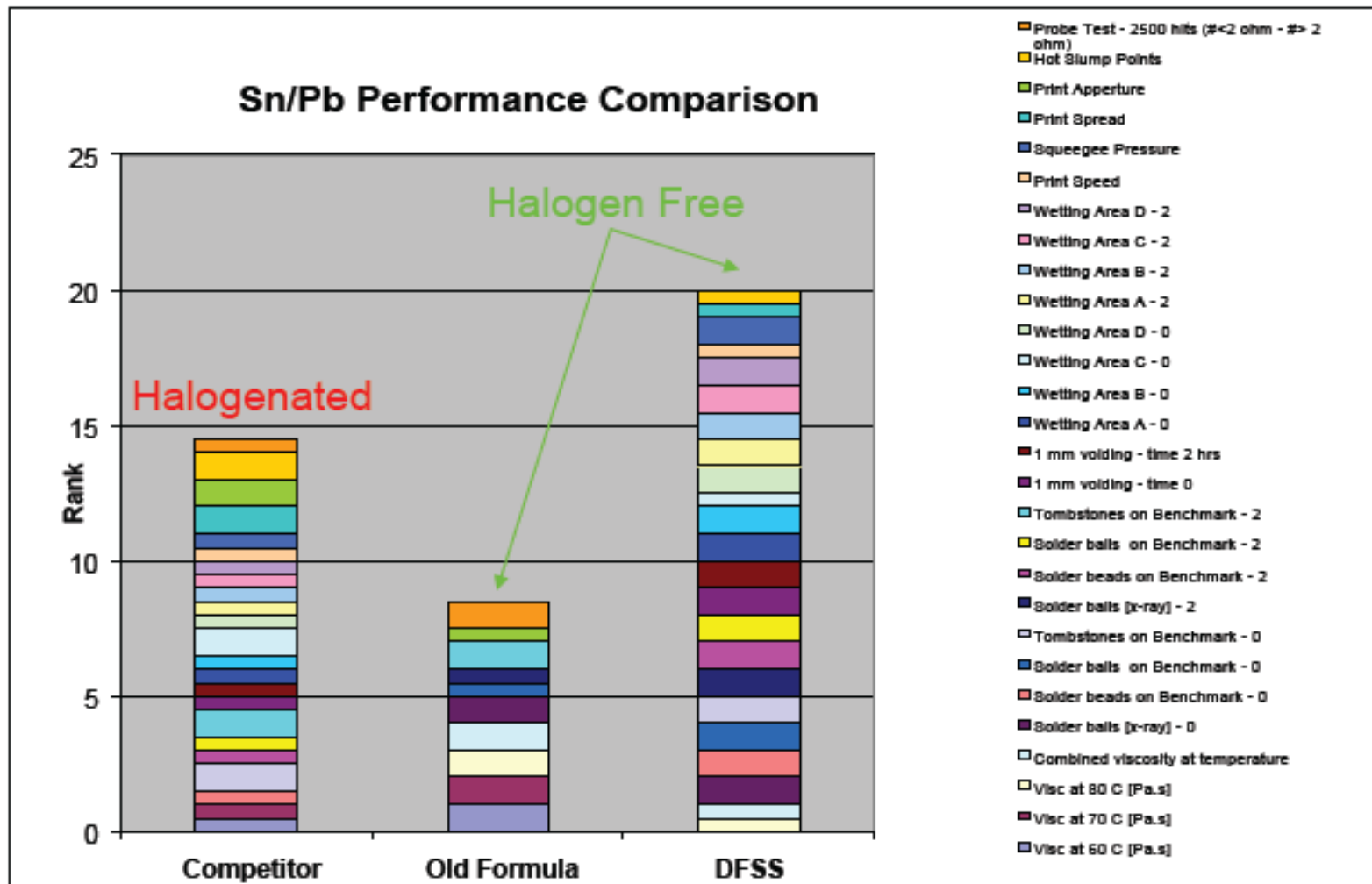
ENIG



DFSS Formulation



DFSS Verification – All Responses



Conclusions

- **By using a series of defined measurable tests, selected for relevance and used in DOE's, it is possible to develop a solder paste tailored to specific needs.**
- **Only with quantitative paste attribute tests that are repeatable and reveal formulation performance contrast can a DFSS solder paste development project be successful.**
- **In the application of the DFSS methods, benchmark testing has been both improved and verified.**
- **Analog trial and error development methods have been replaced by DFSS tools. Qualitative perception based testing methods have been replaced by statistically significant quantitative ones. The merging of both of these improvements is required to develop the truly digital solder paste.**

Acknowledgements

- **Hank Sanftleben and Kris Stark of Delphi Electronics Group** for their DFSS method and analysis expertise, coaching and support.
- **Steve Fritzinger and Derrick Moyer** for their tireless testing support of 200+ pastes and over 2500 tests to support this project.
- **Mike Skrzat** for his project leadership, consistent customer communication and persistence towards a black belt certification.
- **Research and Development** for their chemical knowledge, leadership and the construction of over 200 pastes to support this project.