

# Comparative Assessment of Electrochemical Migration on Printed Circuit Boards with Lead-Free and Tin-Lead Solders

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## Abstract

Current leakage on a printed circuit board (PCB) can occur due to a reduction in surface insulation resistance (SIR) between adjacent conductors. This is frequently caused by electrochemical migration (ECM), which is the growth of conductive metal filaments, or dendrites, on a PCB through an electrolyte solution under the influence of a DC voltage bias.<sup>1</sup> Since the mechanism of ECM involves the electrodisolution and migration of metal, the metallic species present on the PCB surface represent an important factor which can influence ECM time-to-failure. Despite the widespread adoption of tin-silver-copper solder alloys in response to RoHS requirements, there have been relatively few reported assessments of their propensity for ECM in temperature-humidity bias conditions.

This paper presents results of temperature-humidity-bias (THB) testing of over 1500 hours duration at 65°C, 88% relative humidity for comparative evaluation of ECM on circuit boards processed with Sn-3.0Ag-0.5Cu solder versus Sn-37Pb solder. *In situ* monitoring of SIR was performed throughout these tests. In addition to assessing the effects of solder alloy, several other factors were investigated: solder assembly process (wave versus reflow), board finish (organic solderability preservative, or OSP, versus hot air solder leveling, or HASL), spacing (25 mil versus 12.5 mil) and voltage (40V versus 5V bias). Measurements of SIR were combined with observations from optical and electron microscopy to determine the effect of each factor on ECM. Results revealed significant differences in current leakage and metal migration behavior between SAC 305 and eutectic tin-lead assemblies. Furthermore, in some cases, short-term trends in SIR were not maintained over the longer duration of these tests, showing the value of extended test durations for reliability testing of long-life products.

## Keywords

Electrochemical migration, dendrite, current leakage, surface insulation resistance

## 1. Introduction

Electrochemical migration (ECM) is a failure mechanism which can affect printed circuit board (PCB) reliability in electronic products. This phenomenon is characterized by the growth of conductive metal filaments, or dendrites, on a PCB through an electrolyte solution under the influence of a DC voltage bias,<sup>1</sup> causing a drop in surface insulation resistance (SIR). The resulting current leakage can lead to intermittent or permanent failures. The occurrence of ECM requires an electrolyte and a voltage drop across two metallic electrodes. The electrolyte comprises dissolved ions and a liquid medium, which is typically either ambient moisture adsorbed onto the substrate or condensed droplets of water. In order for the electrolyte to dissolve contaminants and transport ions it must have at least three monolayers of adsorbed moisture,<sup>2</sup> with twenty monolayers considered sufficient to promote ECM.<sup>3</sup> The electrodes which provide the migrating metallic species may be copper traces or pads on the PCB, board finishes such as immersion tin or silver, or solder.

The ECM process consists of the following sequence of steps: path formation, electrodisolution, ion transport, electrodeposition, and filament growth.<sup>4</sup> Path formation is the creation of a preferential path, including establishment of a

medium consisting of an electrolyte layer, through which metal ions migrate. This step is dependent on the PCB material composition, board surface topography, concentration and distribution of contaminants, and environmental conditions. For example, within the temperature range of 40°C~85°C polyimide has been found to absorb about twice as much moisture as that absorbed by FR-4, cyanate ester and bismaleimide triazine laminates, which have similar moisture absorption.<sup>5</sup> Pores, scratches, and cavities on the surface, which have higher surface energy than a smooth surface, are more likely to adsorb thicker water layers from the environment. The presence of certain types of contamination, such as flux residues or fibers, on the board surface further enhances the adsorption of moisture.

Electrodisolution involves the oxidation of metals to become cations at the anode (positive electrode). Dissolved ionic contamination, such as halides, can promote this step of the process. Metal cations are driven by the DC bias voltage to the cathode (ion transport), where they are reduced into neutral metal and deposit onto the cathode (electrodeposition). Filament growth occurs when more and more metal deposits onto the cathode and a dendritic structure grows from the cathode toward the anode.

As the metallic dendrites grow the SIR decreases. Once the dendrites fully span the gap between adjacent conductors and touch the anode a short may occur. The current flowing through a dendrite may burn out part of the dendrite due to Joule heating. This phenomenon can lead to intermittent failures, which can be recurrent if re-growth and fusing occur in a cyclical fashion. If the dendrites are thick enough to withstand the current, a permanent short may result.

Typical accelerated test conditions for ECM on printed circuit boards and assemblies involve exposure of test specimens to elevated temperature, humidity, and voltage bias (THB) levels, which are intended to reduce the time-to-failure without inducing condensation. The contributions of various material and processing factors to ECM in THB conditions, including conformal coating, flux, conductor spacing, and voltage bias, have been reported previously.<sup>4</sup> Over the past several years, SnAgCu solder alloys have been widely introduced as a replacement for the traditional eutectic tin-lead solder. Although some studies have been published of the relative risk of ECM with select lead-free solder alloys and finishes,<sup>6,7</sup> there are few reported results of THB tests comparing tin-lead and SnAgCu solder alloys.<sup>8</sup>

## **2. Experimental Setup**

A comparative test was designed to determine the contributions of the relevant factors to ECM, including solder type, soldering process, finish, and conductor spacing, as shown in Table 1. Sn-37Pb (SnPb) and Sn-3.0Ag-0.5Cu (SAC305) solder, wave and reflow soldering, OSP and HASL finishes, and 0.32 mm (12.5 mil) and 0.64 mm (25 mil) conductor spacings were investigated using a full factorial experimental design. At a single bias voltage, this gave 16 combinations. For each combination, 3 identical test specimens were tested, so in total 48 specimens were tested at each of two voltages.

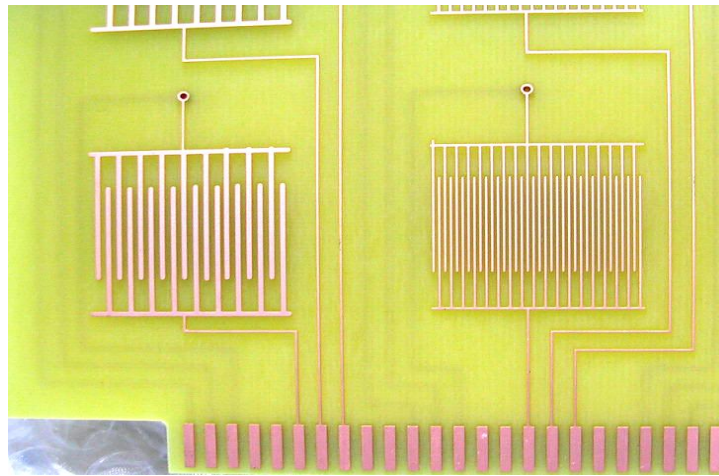
No-clean fluxes and processing were used for all boards. Following the notation for solder fluxes given in IPC-J-STD-004,<sup>9</sup> ROL0 was used for lead-free wave processing with SAC305 and ORL0 for SnPb wave. ROL0 was used in the SAC reflow solder paste, and REL1 in the SnPb reflow solder paste. The test specimens in this experiment were modified IPC-B-24 comb patterns on FR-4 substrates, as shown in Figure 1. 12.5 and 25 mil spacings were assessed to cover the current spacings in fine-pitched electronic packaging.

Surface insulation system (SIR) test systems are used on PCB boards to detect leakage current. SIR represents both surface and bulk conduction paths, but when conductive filament formation (CFF) does not occur, 99.9% of the leakage current takes a surface path.<sup>10</sup>

The SIR test system comprises a computer, a high resistance meter, low noise switches, a temperature-humidity chamber, a DC power supply, triax cabling, and test boards. The Agilent 4349B high resistance meter had an accuracy of 2.5%~3.1% over the resistance range ( $10^6 \sim 10^{10}$  Ohms) used in these tests. The Agilent E5252A low noise switches provided the ability to multiplex 48 channels to the resistance meter, allowing an SIR measurement to be collected once every 3.6 minutes for each comb pattern. A 1-megohm current limiting resistor was placed in series with each comb pattern in order to minimize the fusing of dendrites in the event of a drop in SIR, while still providing the opportunity to observe SIR behavior over about 4 orders of magnitude in resistance.

**Table 1 THB test board characteristics and process factors**

Solder alloy	Sn-37Pb (SnPb), Sn-3.0Ag-0.5Cu (SAC305)
Process	Wave, Reflow
Board Finish	Organic Solderability Preservative (OSP), lead-free HASL
Conductor Spacing	0.32 mm (12.5 mil), 0.64 mm (25 mil)
Voltage bias	5V, 40V
Flux (no clean)	ROL0 for SAC305 wave, ORL0 for SnPb wave ROL0 for SAC305 reflow, REL1 for SnPb reflow
Substrate	FR-4 (170 °C Tg)
Replicates	3
Environment	65°C/88%RH (non-condensing)
Duration	1653 hours for 40V, 1550 hours for 5V



**Figure 1: Image of test board containing comb structures based on an IPC-B-24 pattern, with 0.64 mm (25 mil; left) and 0.32 mm (12.5 mil; right) conductor spacings**

The temperature and humidity conditions (65°C/88%RH) were consistent with the IPC standard for ECM testing IPC-TM-650 method 2.6.14.1,<sup>11</sup> as well as prior studies<sup>4</sup> showing that testing at higher temperatures (such as 85°C) can cause the weak organic acids in no-clean fluxes to be volatilized. This can adversely affect the applicability of such tests to field conditions, which typically involve lower temperatures. While the IPC standard calls for a 500 hour test duration, longer test times were selected for this study. In contrast to qualifying a candidate process to a minimum requirement, the

objective was to provide insights that would be of general relevance to electronic products, including those with an expected life of more than just a few years. Thus, the actual test durations were 1653 hours for the 40V test and 1550 hours for the 5V test. The failure criterion for SIR was chosen to be 100 MOhms.

### 3. Results and Discussion

The SIR data collected during each of the THB tests (40V and 5V) were analyzed to identify trends and times-to-failure associated with each combination of experimental factors. In this section, individual factors are evaluated independently of other factors whenever possible. Interactions with other factors are discussed when independent analysis was not appropriate.

#### 3.1 Effect of Solder Alloy: SnPb vs. SAC

The solder alloy and soldering process are two critical factors that act together to determine susceptibility to ECM. The clearest distinctions in performance for the two solder alloys can be drawn for reflow processed samples. Considering only reflow processed boards, SnPb solder showed better reliability overall than SAC solder. This was observed in the results of both the 40V and 5V THB tests. For example, during the 40V test all 6 SnPb reflowed samples with 25-mil spacings survived the test, while 5 out of 6 SAC samples failed. Of the 12.5 mil reflowed samples tested at 40V, all 6 SAC samples failed after around 100 hours, while 2 out of 6 SnPb samples survived for more than 1000 hours and the remainder failed before 200 hours.

The differences between the SnPb and SAC soldered boards tested at 5V were consistent with those tested at 40V. For example, all 6 SnPb samples with 25 mil spacing that were reflow soldered survived the entire 1550 hours of testing, while only 4 out of 6 SAC samples survived. For the 12.5-mil samples, 5 out of 6 SnPb samples survived the test, while all 6 SAC samples failed between 270 and 540 hours.

The differences in SIR trend between reflow-soldered SnPb and SAC samples were pronounced. The SIR of the SnPb samples that were reflow soldered showed an initially increasing trend followed by a leveling off, as illustrated in Figure 2. The SIR of the SAC samples showed a generally decreasing trend, which is evident in Figure 3 **Error! Reference source not found.** This phenomenon was true for all SnPb and SAC reflow-soldered samples in both the 40V and 5V THB tests, regardless of which type of finishes and spacings were used.

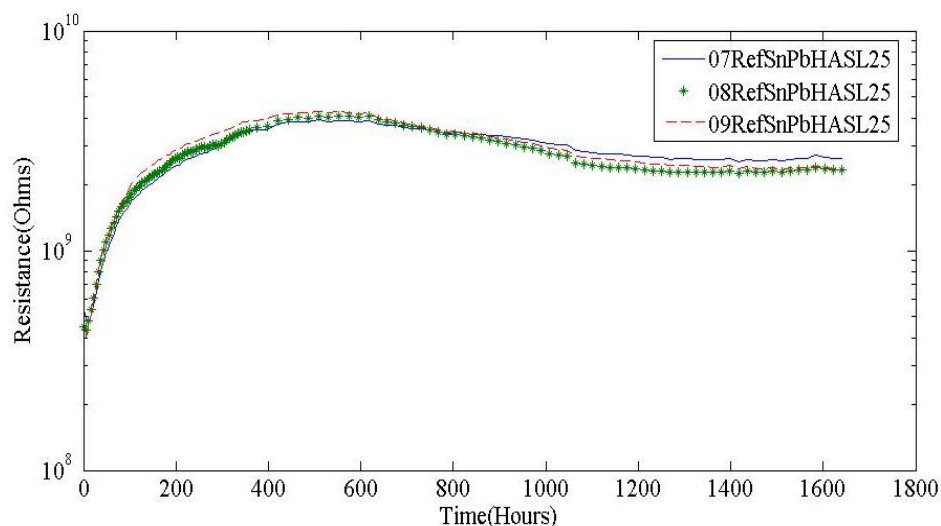
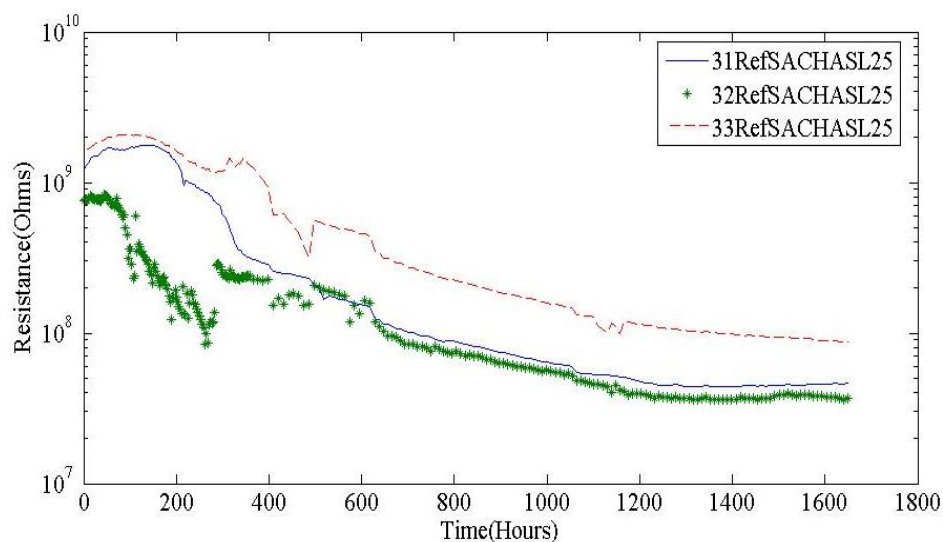


Figure 2: 40V SIR of 3 comb structures on board with reflow soldered SnPb, HASL finish, and 25-mil spacing

Figure 2 and Figure 3~~Error! Reference source not found.~~ show the SIR results for 25 mil comb structures with SnPb solder and SAC solder, respectively, with reflow processing, HASL finish, and 40V bias voltage. After 200 hours, the SnPb-soldered boards rose to a nearly stable SIR value, while the SAC-soldered boards manifested a deteriorating trend over an extended period. During the first 150 hours, the SIR of the SAC-soldered boards showed a stable or increasing trend, although this was followed by a long term gradual decrease. The 5V test showed similar trends. Thus, if only the initial 200 hours performance is taken into account, as is commonplace during testing to certain qualification standards that may only require 1 week of testing, (such as IPC-TM-650, Method 2.6.3.3<sup>12</sup>) the observations cannot be extrapolated to longer durations. Such tests may not be valid for products with expected lifetimes longer than the equivalent of a few hundred hours at these accelerated conditions. Based on the SIR results on SnPb and SAC boards with reflow processing obtained over a duration of 1650 hours at 40V and 1550 hours at 5V, SnPb-soldered boards demonstrated a better long-term behavior and thus higher reliability than SAC-soldered boards.



**Figure 3: 40V SIR of board 6 with SAC solder, reflow soldering, HASL finish, and 25-mil spacing**

### 3.2 Effect of Processing Method: Wave vs. Reflow

During the 40V test all of the wave-processed samples using SnPb solder failed right after the test started (after the chamber stabilization period ended), while 8 out of 12 reflow processed samples using SnPb solder lasted longer than 1000 hours. During the 5V test, more than half (7 out of 12) of the wave-processed samples using SnPb solder failed right after the test started, and the remainder survived the entire test. The characteristic Weibull life for the 5V samples was 2.3 hours. In the same 5V test, most (11 out of 12) of the reflow-processed samples using SnPb solder survived the test, with a characteristic Weibull life of  $2.3 \times 10^5$  hours. Thus, in general reflow-processed SnPb samples showed higher reliability than wave-processed SnPb samples. Initial SIR measurements taken prior to THB testing indicated somewhat lower resistance for the wave-processed SnPb specimens, as well as the wave-processed SAC specimens with HASL finish, but still above the failure threshold. Failure analyses revealed that dendritic growth, rather than solder bridging, was responsible for the failures of the wave-processed specimens which failed at the start of the test

One contributor to these differences may have been the use of different types of flux for the SnPb reflow and wave processes. The reflow-processed SnPb samples used REL1 flux, which used resin as a vehicle and had halide content of up to 0.5% of flux residue, based on the nomenclature of IPC J-STD 004.<sup>9</sup> It should be noted that analysis of board extracts using ion chromatography showed reflow-processed SnPb boards with HASL finish had about twice the concentration of chloride ions

as any of the other boards. Nevertheless, the absolute concentration which was found,  $12.8 \mu\text{g}/\text{in}^2$ , did not represent a drastic elevation above generally accepted levels, and does not appear to have adversely affected the reliability of these boards. The wave-processed SnPb samples used alcohol-based ORL0 flux, which had a halide content below 0.05% of flux residue, and was free of resin or rosin. Optical inspection showed a larger amount of flux residues on the reflow-processed SnPb samples than on the wave-processed SnPb samples. Although REL1 left more flux residues on the board, the resinous/rosinous residue may have served a protective function, inhibiting the adsorption of moisture,<sup>13,14</sup> thus reducing the potential for ECM failure. Further, it has been observed<sup>14</sup> that rosin residues are hydrophobic. The hydrophobic nature of these rosin residues appears to be inconsistent, however, since during this experiment one area containing rosin flux residues seemed to have contributed to the growth of dendrites, as shown in Figure 4 and Figure 5. Rosin or resin residues may not be as hygroscopic as polyglycol or polyglycol surfactants, which are a constituent of water soluble fluxes.<sup>15</sup> ORL0 fluxes can be either aqueous-based or alcohol-based. Aqueous-based ORL0 flux uses deionized water as a solvent, but alcohol-based ORL0 fluxes usually use low molecular weight alcohol such as isopropanol as a solvent.<sup>13</sup> While the present study suggests that alcohol based ORL0 flux may be more susceptible to ECM than REL1 flux, aqueous-based ORL0 flux has been reported elsewhere to be less susceptible to ECM than rosin-based ROM0 flux, which has a higher content of weak organic acid and thus more corrosive flux residues.<sup>16</sup> In addition, an elevated amount of nitrate ions was found on wave-processed SnPb boards, using ion chromatography of board extracts. Since lead (II) nitrate is soluble in water, the dissolution of lead nitrate in absorbed moisture can generate significant quantities of lead ions available to migrate, which may have contributed to the rapid failures of wave-processed SnPb boards.

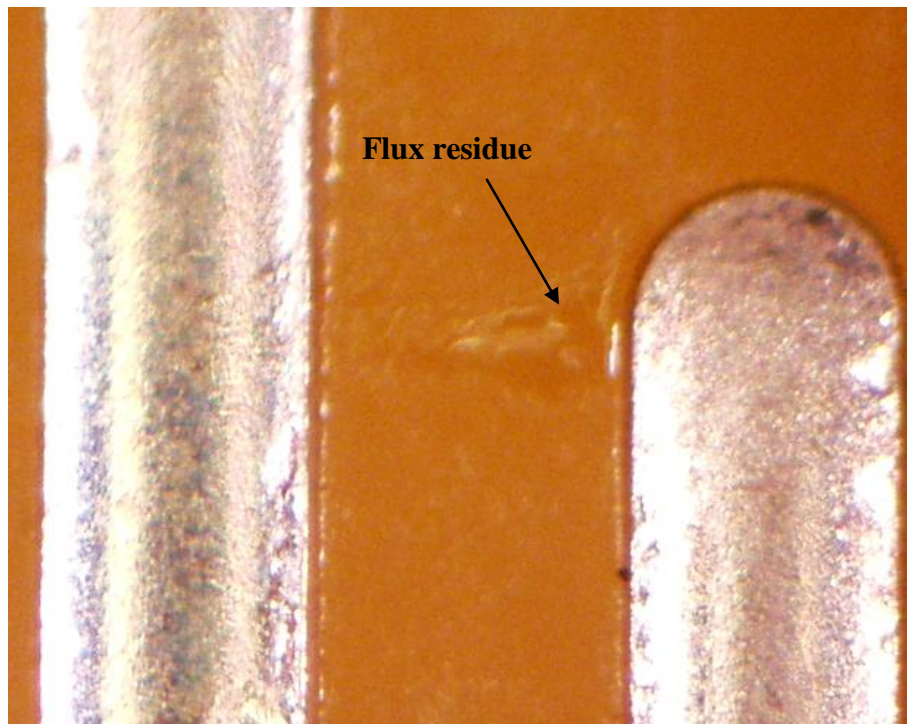
On both the 40V and 5V test boards using SAC solder, wave-processed specimens showed higher reliability than reflow-processed specimens. Figure 6 presents a Weibull analysis of the results for wave-processed SAC boards and reflow-processed SAC boards including both 40V and 5V test results. Wave-processed SAC samples had a characteristic Weibull life of  $1.2 \times 10^5$  hours, much longer than that of reflow-processed SAC samples (715 hours). In addition, wave-processed SAC samples showed a decreasing hazard rate ( $\beta=0.24$ ), while reflow-processed SAC samples showed an increasing hazard rate ( $\beta=1.19$ ). ROL0 flux was used for both wave-processed and reflow-processed SAC samples, although the amount of flux residues on wave-processed SAC samples was much less than that on the reflow-processed SAC samples based on optical inspection. This may be one reason why wave-processed SAC samples had better reliability than the reflow-processed SAC samples.

### 3.3 Effect of Board Finish: OSP vs. HASL

Finishes are used to retard oxidation of bare copper on PCBs so as to maintain the solderability of the metal surface. Organic solderability preservative (OSP) is an organic layer evenly deposited onto the exposed copper metallization. Early formulations of OSP, based on benzotriazole and typically 5~15 nm thick, were easily broken and susceptible to physical damage during handling. Benzimidazole, an OSP formulation introduced in the mid-1990s, can be 200~500 nm thick and is more durable.<sup>17,18</sup> Hot air solder leveling (HASL) involves passing boards over molten solder and blowing off excess molten solder by a hot air knife, thus leaving a thin solder layer over the exposed copper metallization. Compared to OSP, HASL layer thickness is harder to control, HASL produces more brittle intermetallics, and it is a more expensive process. HASL thickness can vary by up to several hundred micrometers, even with a single manufacturer and HASL process.<sup>18</sup> As a result of the higher heating and cooling rates associated with the HASL process, the intermetallics on HASL finished boards tend to be thicker, more irregular, and may have higher void content, while the intermetallics on OSP finished boards are thinner, more uniform and have fewer voids. Thus the fracture toughness of the intermetallics on HASL boards is reported to be lower than that on OSP boards.<sup>18</sup> In addition, HASL processing can cost almost three times more than OSP

processing.<sup>19</sup> The potential disadvantages of OSP are that the finish is more prone to physical damage during PCB handling, and it can partially dissolve in solvents like water,<sup>17</sup> which may be constituents of fluxes used during soldering.

In the present study, OSP and HASL finishes did not noticeably differ in their influence on ECM, with the exception of the SnPb wave-processed boards in the 5V test. This may be observed from the Weibull analysis shown in Figure 7. The similarity exhibited in the contribution of board finishes under most circumstances suggests a relatively passive role of the board finish in characteristics affecting ECM. This may be due to the evaporation of OSP during soldering and the dissolution of HASL into the solder during the reflow and wave soldering process. A notable exception was found during the 5V test, in which the wave-processed SnPb samples with HASL finish showed much higher reliability than those with OSP finish. Table 2 compares the times-to-failure for these samples with the corresponding samples finished with OSP.



**Figure 4: Optical micrograph of 0.64 mm (25 mil) wave-processed SAC sample using OSP finish and ROL0 flux, obtained prior to 40V THB test**



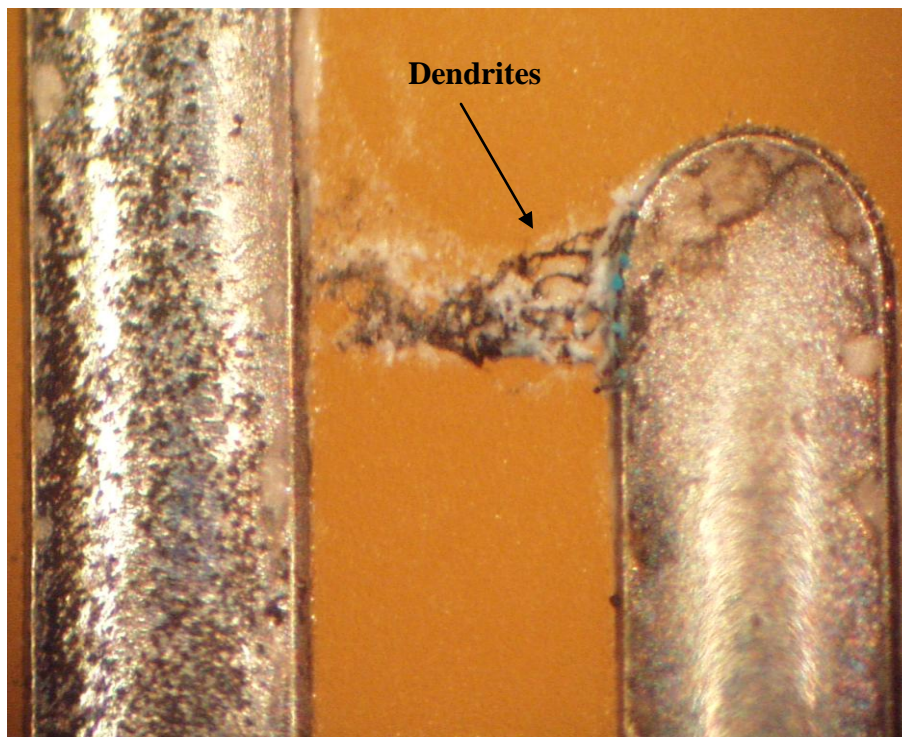


Figure 5: Optical micrograph of 0.64 mm (25 mil) wave-processed SAC sample using OSP finish and ROL0 flux, after 1653 hours at 65°C, 88% RH and 40V

Table 2 Times to failure of 5V THB test of wave-processed SnPb soldered boards

OSP finish, 25 mil	0	0	0
OSP finish, 12.5 mil	0	0	0
HASL finish, 25 mil	Survived	Survived	Survived
HASL finish, 12.5 mil	0	Survived	Survived

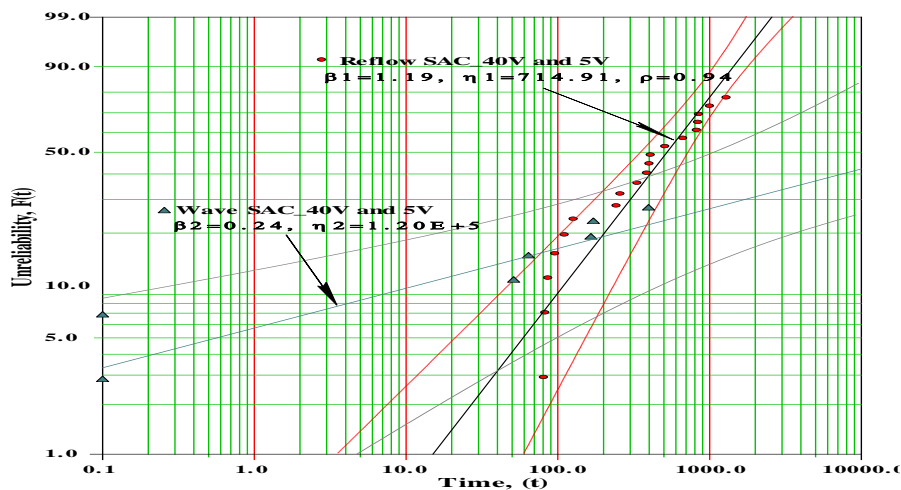


Figure 6: Weibull analysis of 40V and 5V test boards using SAC solder with wave and reflow processing. The figure provides the results of a Weibull two-parameter fit plus the 90% confidence interval. Surviving samples are not shown.



### 3.4 Effect of Voltage: 40V vs. 5V

The electrostatic force,  $F$ , on a charged particle is given by

$$F=qE=qU/d \quad (1)$$

where  $q$  is the charge carried by ions,  $d$  is the spacing, and  $E$  is the electrical field. This expression shows that the electrostatic force is proportional to the ionic charge and applied voltage. Given a constant spacing, the higher the voltage, the larger the electrostatic force. In the present study, 40V and 5V voltage biases were applied to the samples. Figure 8 shows the differences between all the samples tested at 40V and 5V, except the wave-processed samples using SnPb solder. Excluding the wave-processed SnPb samples, for which the results of the voltage comparison were inconclusive, the samples tested at 5V showed longer times-to-failure and thus better reliability than those tested at 40V. This result is consistent with the hypothesis that a weaker driving force resulting from a lower voltage (given the same spacing) can lengthen the characteristic life.

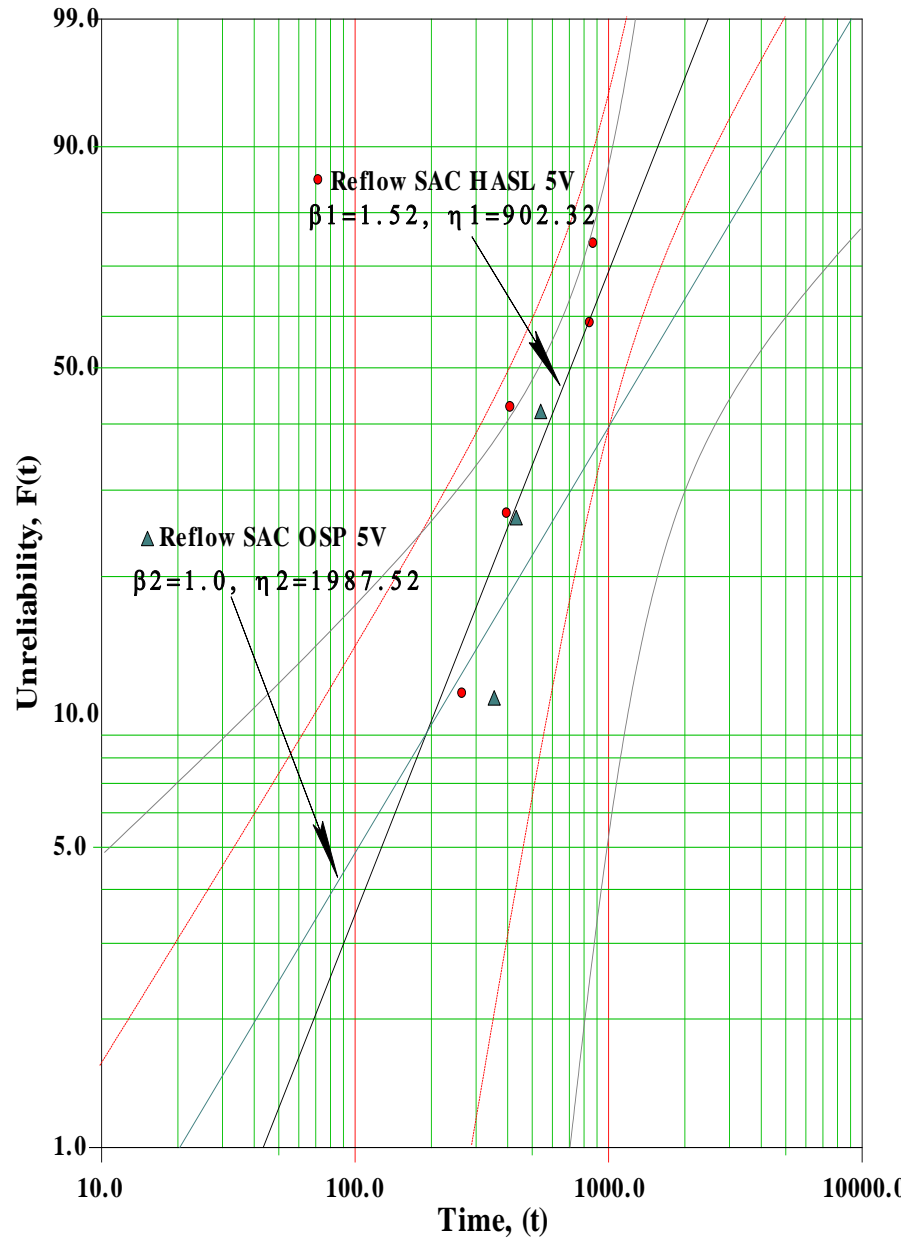
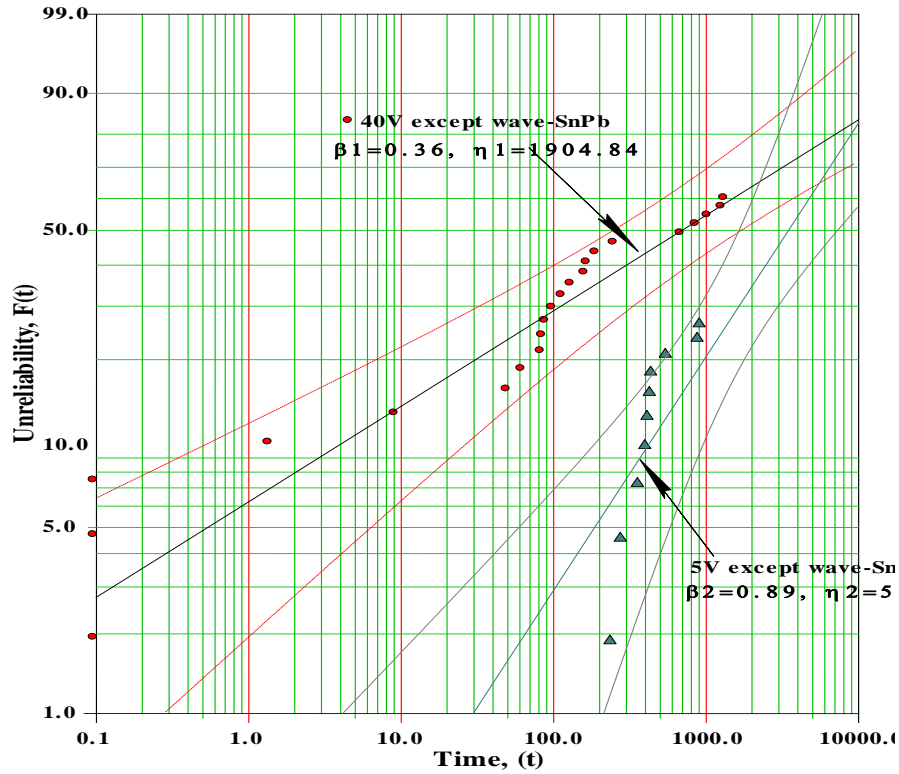
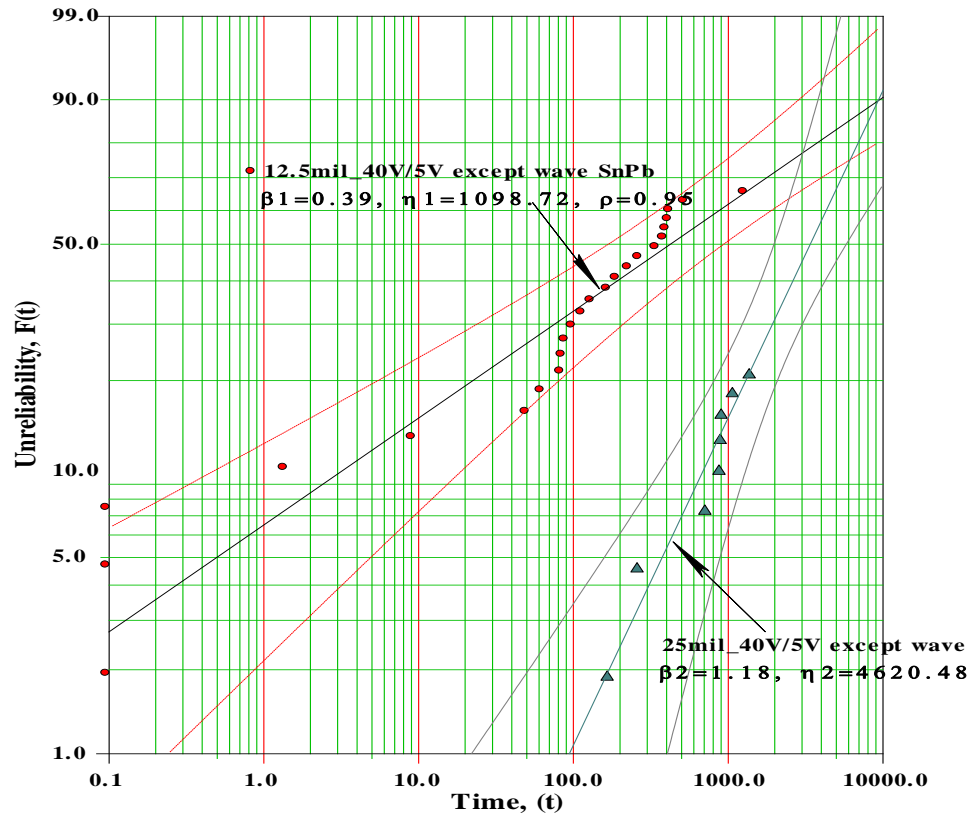


Figure 7. Weibull plot comparing reflow-processed SAC samples with OSP and HASL finishes from 5V THB test



**Figure 8. Weibull plot comparing all samples tested at 40V and 5V except wave-processed SnPb samples**  
**3.5 The Effect of Conductor Spacing: 0.64 mm (25 mil) vs. 0.32 mm (12.5 mil)**

The spacing of the conductors, which are the electrodes in an electrochemical migration process, affects both the ion migration time and the incubation time. Migration refers to the movement of metal ions from anode to cathode within the electrolyte layer on the board surface. Thus, a larger spacing requires that ions travel a longer distance, which contributes to a longer time-to-failure. As shown in Equation 1, a larger spacing also results in a lower electrostatic force on the ions, reducing the driving force for migration. Incubation time refers to the period required for path formation prior to electrodisolution, as well as the period needed for free ions to accumulate within the electrolyte solution prior to migration. Therefore, a smaller spacing increases the probability that flux residues or surface contamination will be sufficient to bridge all or most of the gap between electrodes, allowing moisture to adsorb and form the continuous electrolyte medium required for ECM. The results of both the 40V and 5V THB tests exhibit a general trend: the times-to-failure of samples with larger spacings are longer than those of samples with smaller spacings, as shown in Figure 9. This clearly indicates that the industry trend towards higher density board designs is associated with an increased risk of ECM, which must be mitigated through appropriate selection of other design and process factors.



**Figure 9. Comparison between all 25 mil samples and 12.5 mil samples under 40V and 5V THB test except wave-processed SnPb samples**

#### 4. Conclusions

One of the most significant outcomes of the present study is the difference of long term behavior between reflow-processed boards with SnPb solder and SAC solder. The SIR of reflow-processed samples with SnPb solder generally showed an initially increasing trend followed by a gradual stabilization. In contrast, the SIR of reflow-processed samples with SAC solder showed a stable or increasing trend in the first couple of hundred hours, but this was followed by a prolonged decline. This slow deterioration of reflowed SAC solder may represent a long term reliability risk, especially to long life products, and thus warrants further study using long duration THB tests. This failure mechanism should be carefully evaluated when selecting SAC solder alloys for reflow processing of boards which may encounter high humidity field conditions for extended periods. Wave-processed SAC solder samples showed longer characteristic lives than reflow-processed SAC solder ones.

Flux residues on a printed circuit board can potentially either inhibit or boost moisture adsorption, depending on the composition and thickness of the residues. Rapid and extensive dendrite growth occurred on wave-processed boards with SnPb solder using an alcohol-based ORL0 flux, whereas it did not occur on reflow-processed boards with SnPb solder using REL1 flux or with SAC solder using ROL0 flux. These rapid failures require further investigation to determine if the solvent system (alcohol or aqueous) of the ORL0 flux is important, or if different behavior would be observed using a similar flux in a reflow process.

SIR results on boards finished with OSP and HASL were not significantly different in most cases. The sole exception was the higher reliability observed for wave-processed SnPb samples with HASL finish, compared with those finished with OSP, in the 5V test.

Voltage and conductor spacing were both found to exert a significant influence on time-to-failure by ECM. The applied voltage is directly related to the driving force for ion migration. Conductor spacing also affects the driving force for migration as well as determining the distance over which ions must travel in order to reach the cathode and form dendrites. The spacing also affects path formation, which can be the rate-limiting step for ECM under many circumstances. For all samples for which the voltage comparison was conclusive, the samples tested at 5V showed longer times-to-failure and thus better reliability than those tested at 40V. A similarly general conclusion is possible regarding spacing, since the times-to-failure of samples with larger spacings were clearly longer than those of samples with smaller spacings. Higher applied voltage and smaller spacing showed worse reliability, respectively. Thus, applications involving voltages smaller than 5V may offer the board designer more latitude in the choice of conductor spacing.

Overall, the best reliability was found for SnPb samples reflow-processed using an OSP finish and SAC samples wave-processed using a HASL finish, when tested at 5V. For these combinations of factors, all samples survived the entire duration of the THB test, independent of the conductor spacing.

### Acknowledgement

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# Comparative Assessment of Electrochemical Migration on PCBs with Lead-Free and Tin-Lead Solders

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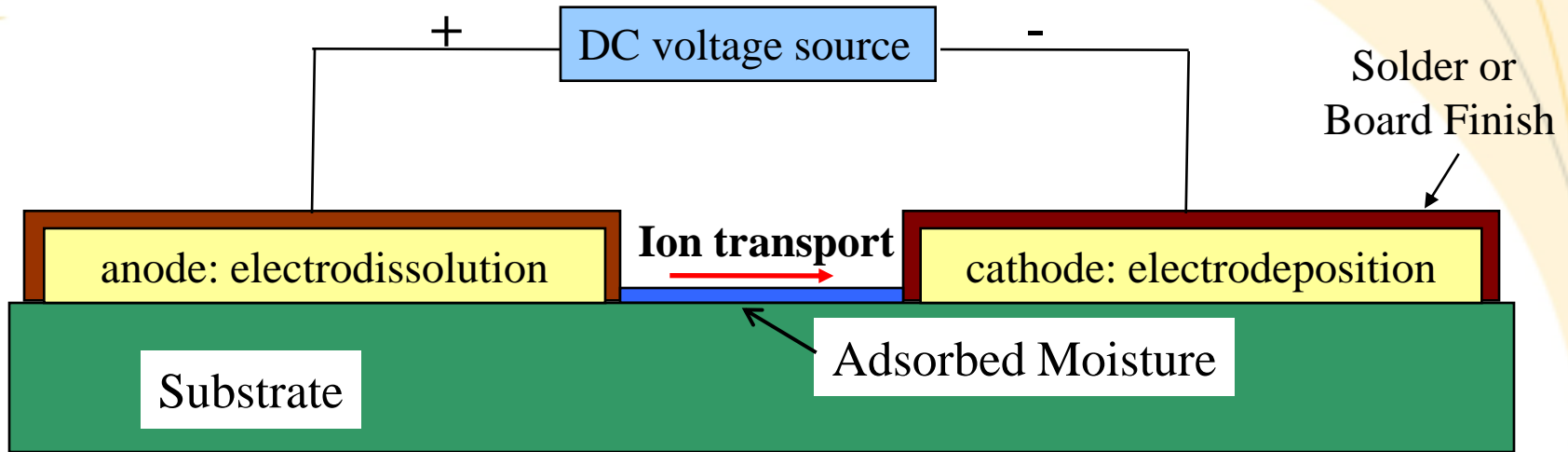
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# Electrochemical Migration



Electrochemical Migration (ECM) is the growth of conductive metal dendrites through an electrolyte solution under the influence of a DC voltage bias [1].

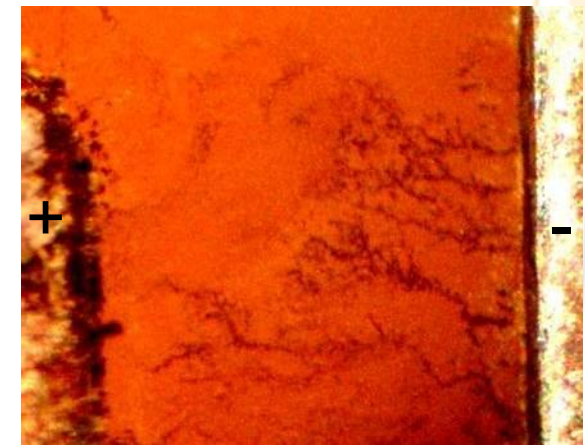
at anode:



at cathode:



ECM mechanism steps: path formation, electro-dissolution, ion transportation, electro-deposition, and filament formation (dendrite growth) [2].



Dendrite growth direction

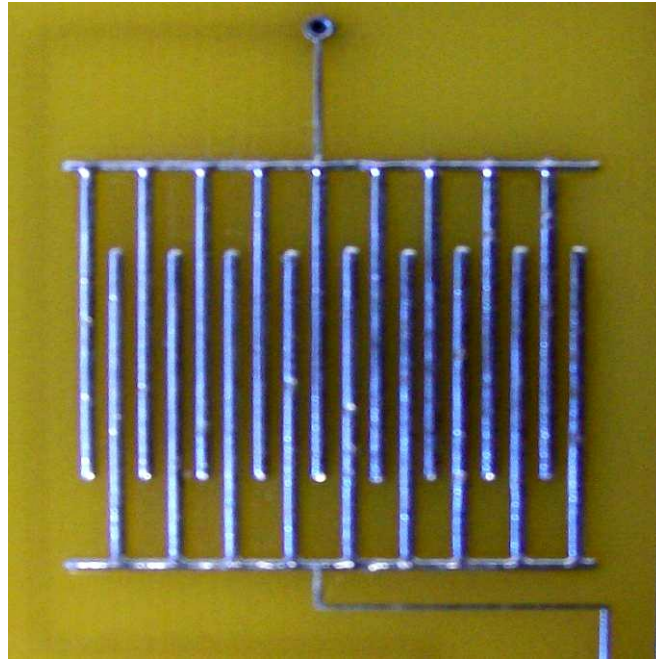
# Introduction

- The widespread use of lead-free solders calls for a comparison between the reliability of lead-free and tin-lead solder in temperature-humidity-bias (THB) conditions.
- Other material and design factors can interact with the solder alloy to affect the risk of ECM. This study addresses the influences of several different factors including solder alloy, soldering process, board finishes, conductor spacing, and applied voltage.
- Most published studies on ECM of lead-free circuit boards either report results of water drop testing or THB tests lasting only a few hundred hours. Extended duration THB tests are needed to address applications involving long expected life, long durations in high humidity conditions, or high criticality.

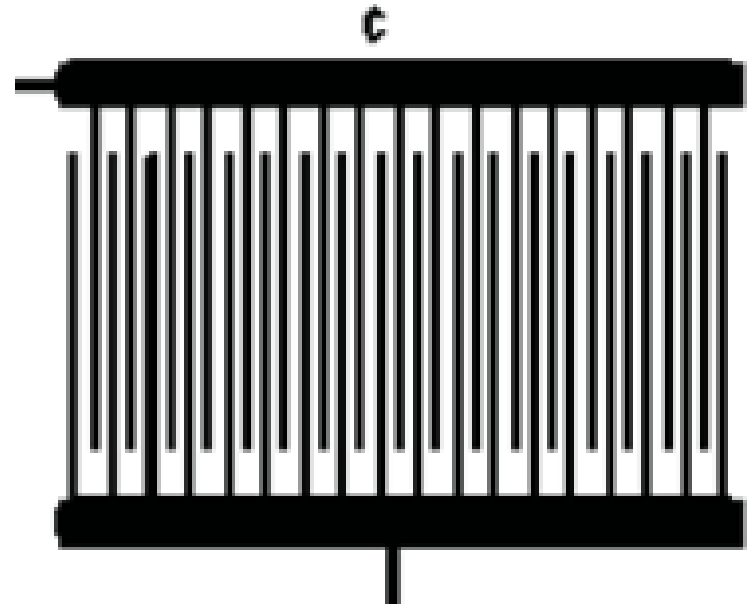
# Experimental Factors Used in THB Tests

<b>Solder Alloy</b>	Sn-37Pb (SnPb), Sn-3.0Ag-Cu0.5 (SAC)
<b>Process</b>	Wave, Reflow
<b>Board Finish</b>	Organic Solderability Preservative (OSP); or SnPb HASL for SnPb solder, Pb-free HASL for SAC solder
<b>Wave Flux</b>	No clean; ORL0 for SnPb, ROL0 for SAC
<b>Solder Paste Flux</b>	No clean; REL1 for SnPb, ROL0 for SAC
<b>Voltage Bias</b>	40 VDC, 5 VDC
<b>Conductor Spacing</b>	0.64 mm (25mil), 0.32 mm (12.5 mil)
<b>Substrate</b>	FR-4 (170 °C Tg ) no solder mask
<b>Replicates</b>	3 identical samples for each set of factors
<b>Environment</b>	65°C/88%RH (non-condensing)
<b>Test Time</b>	1653 hours for 40V test, 1550 hours for 5V test

# Test Structure Used in THB Tests



**THB Test Structure**



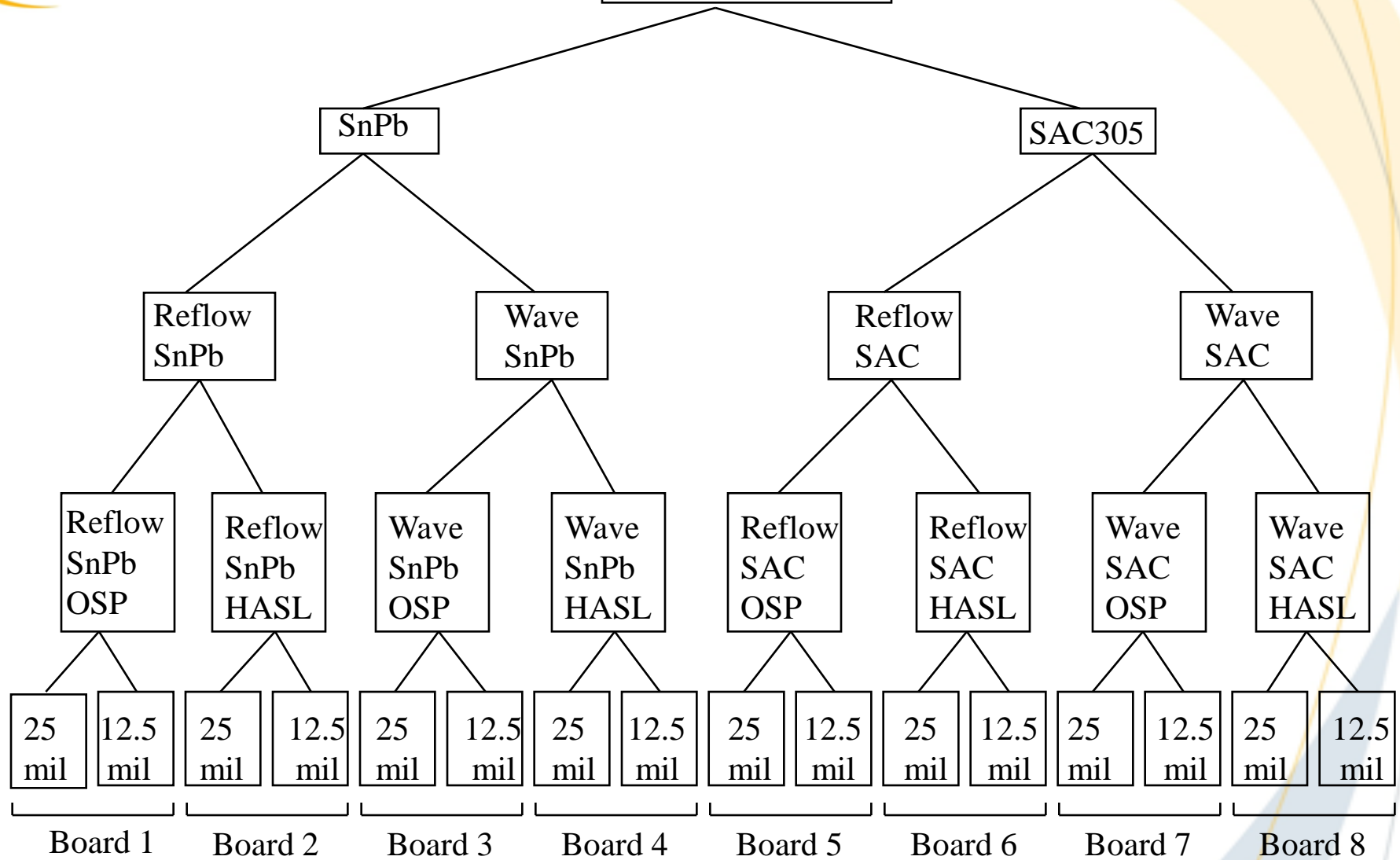
**IPC-B-24 Comb Pattern**

THB test structure: modified IPC-B-24 comb pattern, from IPC-9201[3].  
SIR was measured once every 3.6 minutes for each comb pattern.  
1-megohm current limiting resistor in series with each comb pattern.

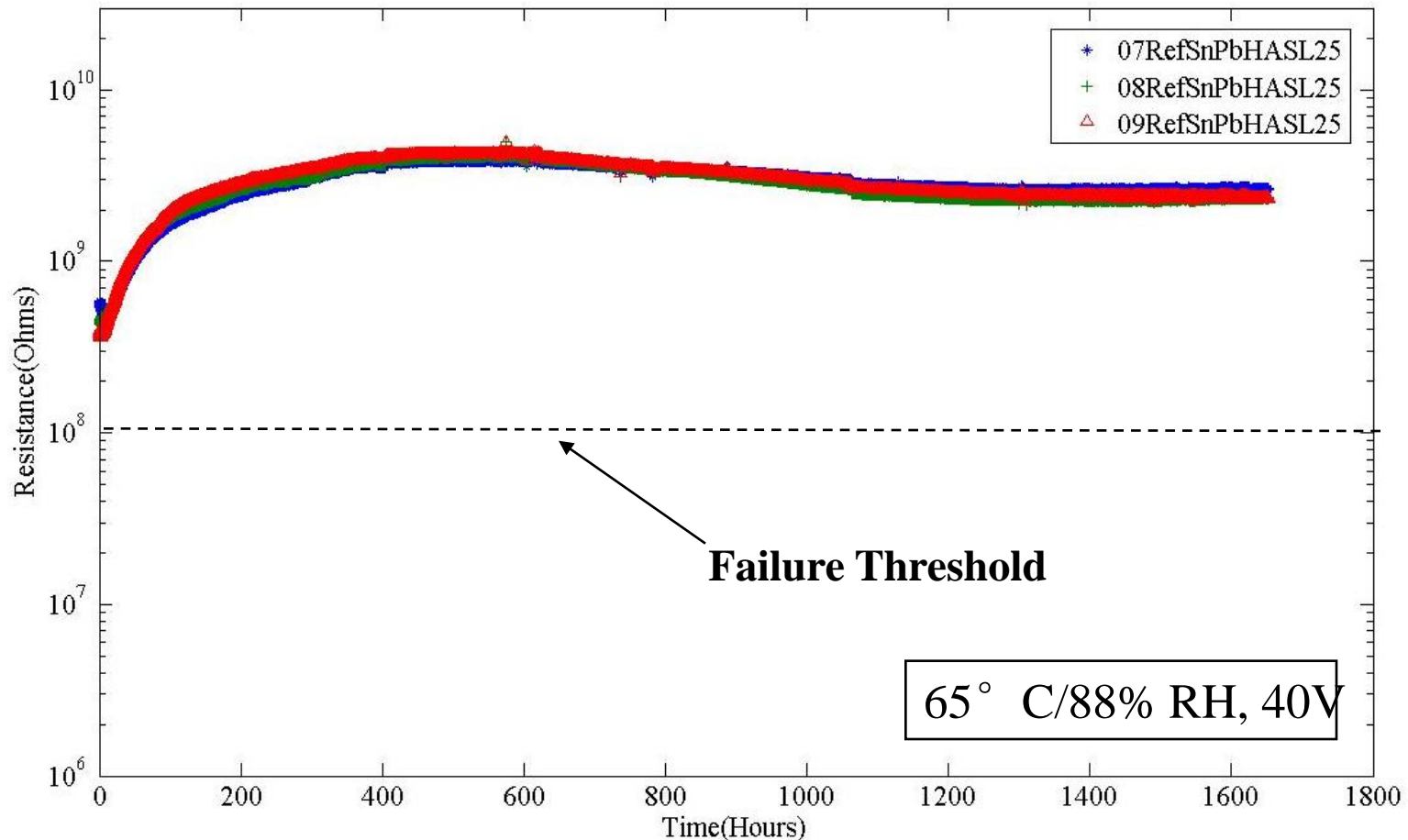
**Failure criterion:**  $SIR < 1 \times 10^8$  Ohms

# Test Matrix

40V/5V THB Test



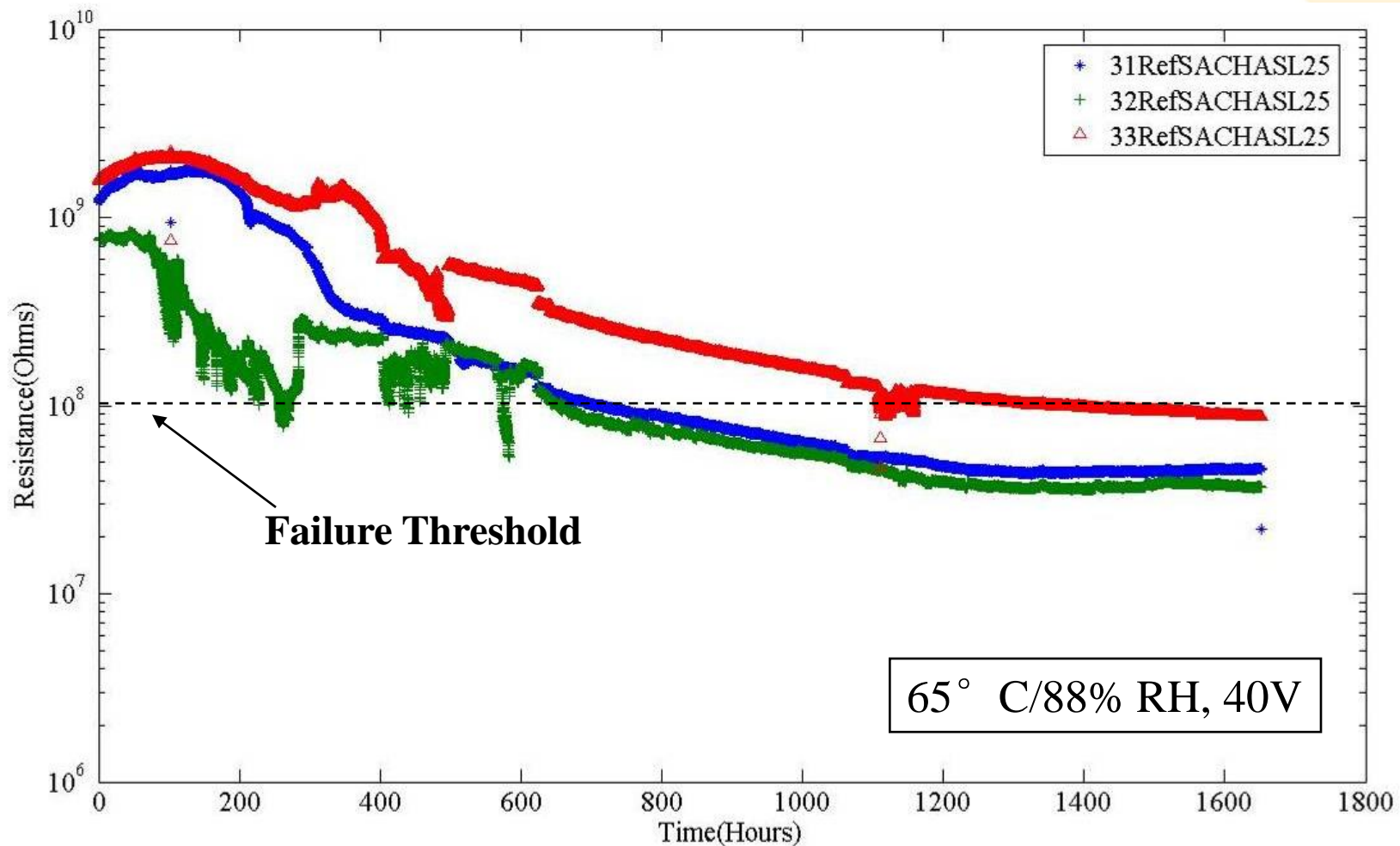
# 40V SIR Data of 25 mil Structures with Reflow-Soldered SnPb



SIR of 25 mil test structures with reflow-soldered SnPb and HASL finish. It shows an initial increase followed by stabilization. 5V SIR results followed a similar trend.

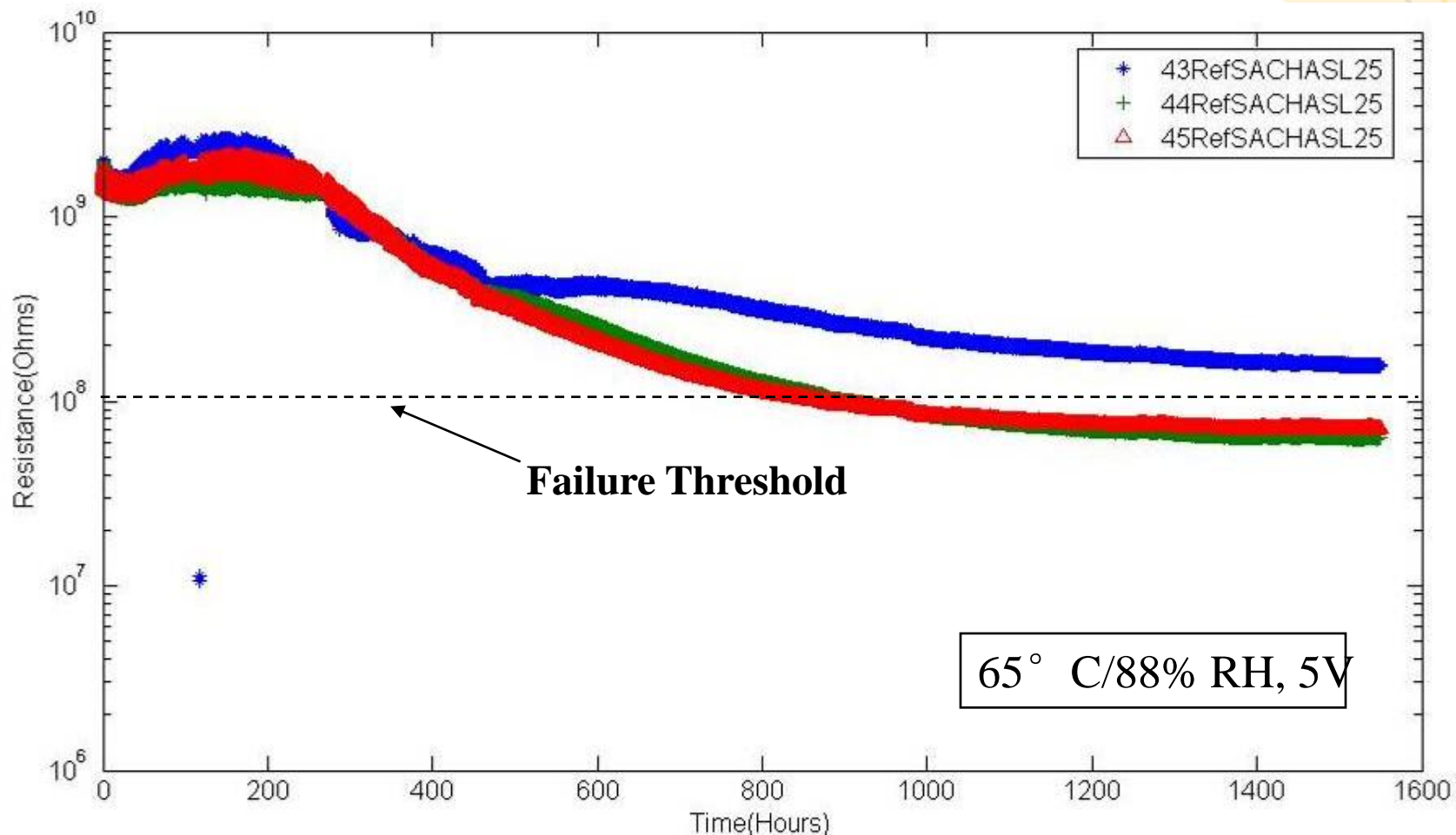


# 40V SIR Data of 25 mil Structures with Reflow-Soldered SAC305



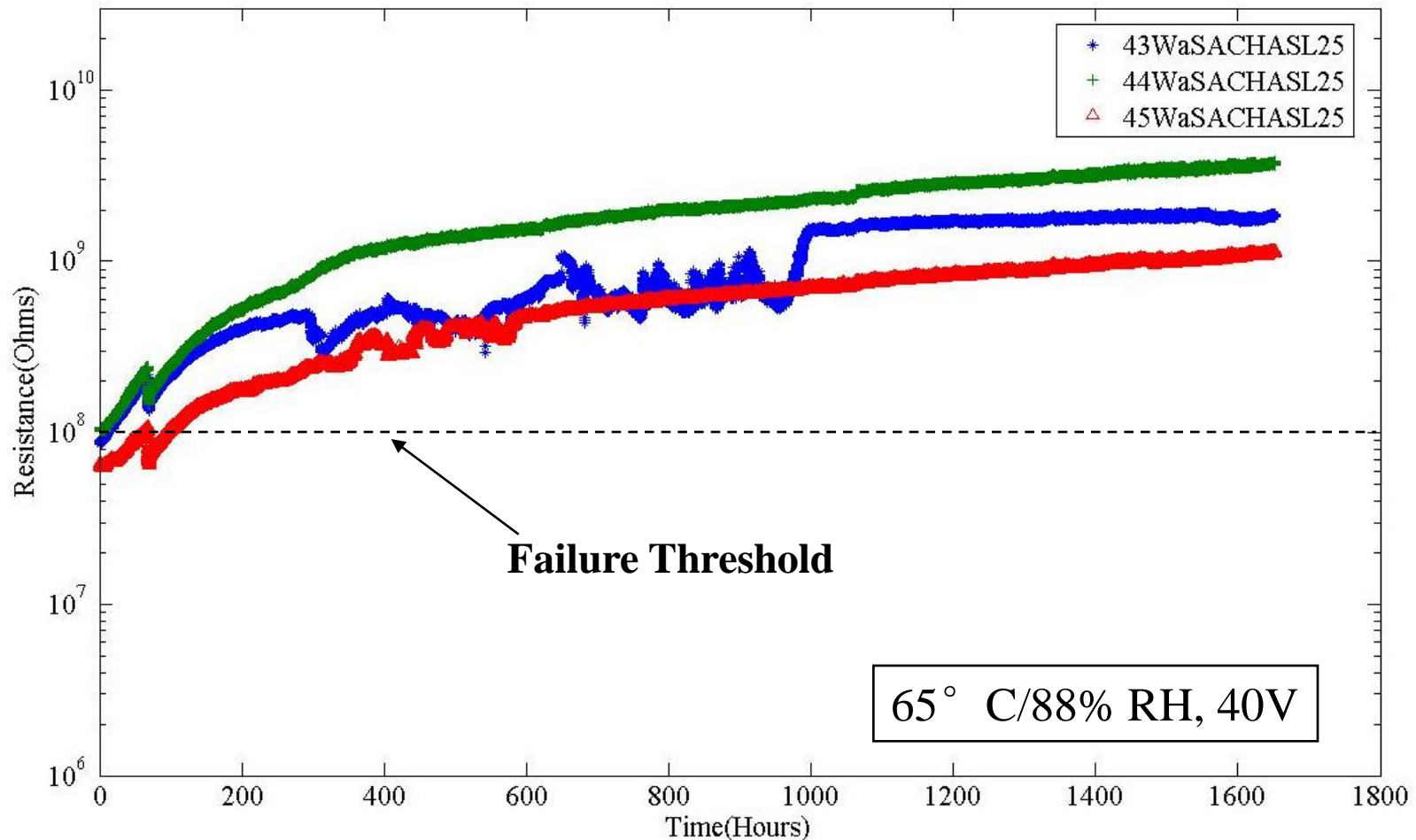
SIR of 25 mil test structures with reflow-soldered SAC and HASL finish. It shows an initial increase followed by a long decline.

# 5V SIR Data of 25 mil Structures with Reflow-Soldered SAC305



SIR of 25 mil test structures with reflow-soldered SAC and HASL finish. It shows an initial increase followed by a long decline.

# 40V SIR Data of 25 mil Structures with Wave-Soldered SAC305



SIR of 25 mil test structures with wave-soldered SAC and HASL finish. It increases gradually over a long time.

# THB Results for Reflowed Solder (SnPb vs. SAC)

- Samples which were reflowed with SnPb solder had fewer failures than those reflowed with SAC305 solder in both 5V and 40V tests.

	5V Reflow	
	SnPb (OSP and HASL, 25 and 12.5 mil)	SAC305 (OSP and HASL, 25 and 12.5 mil)
Number of failed samples after 1000 hrs	1	8
Number of failed samples after 1550 hrs	1	8
Total number of samples	12	12

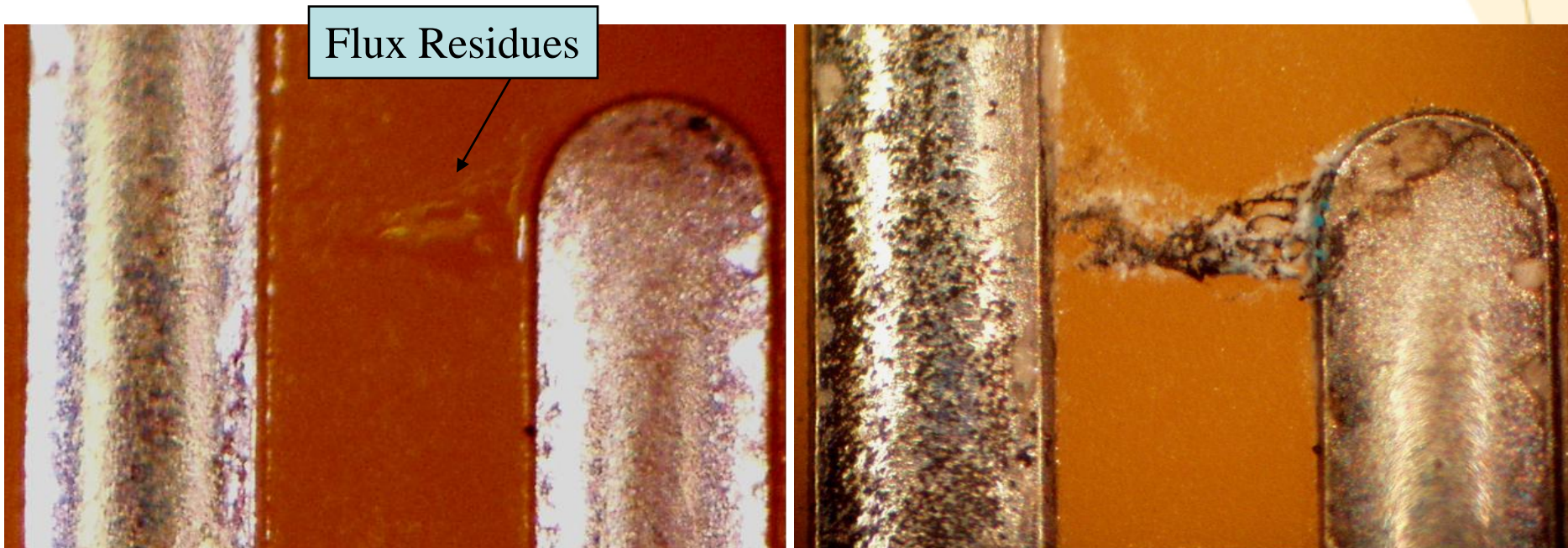
	40V Reflow	
	SnPb (OSP and HASL, 25 and 12.5 mil)	SAC305 (OSP and HASL, 25 and 12.5 mil)
Number of failed samples after 1000 hrs	4	9
Number of failed samples after 1653 hrs	5	11
Total number of samples	12	12



# Role of Flux Residues on Dendrite Growth

Prior to 40V THB test

After 40V THB test



0.64 mm (25 mil) wave-processed SAC305  
sample using OSP finish and ROL0 flux.

# THB Results for SAC Solder (Reflow vs. Wave)

- SAC305 samples which were wave processed showed higher reliability than those which were reflowed.

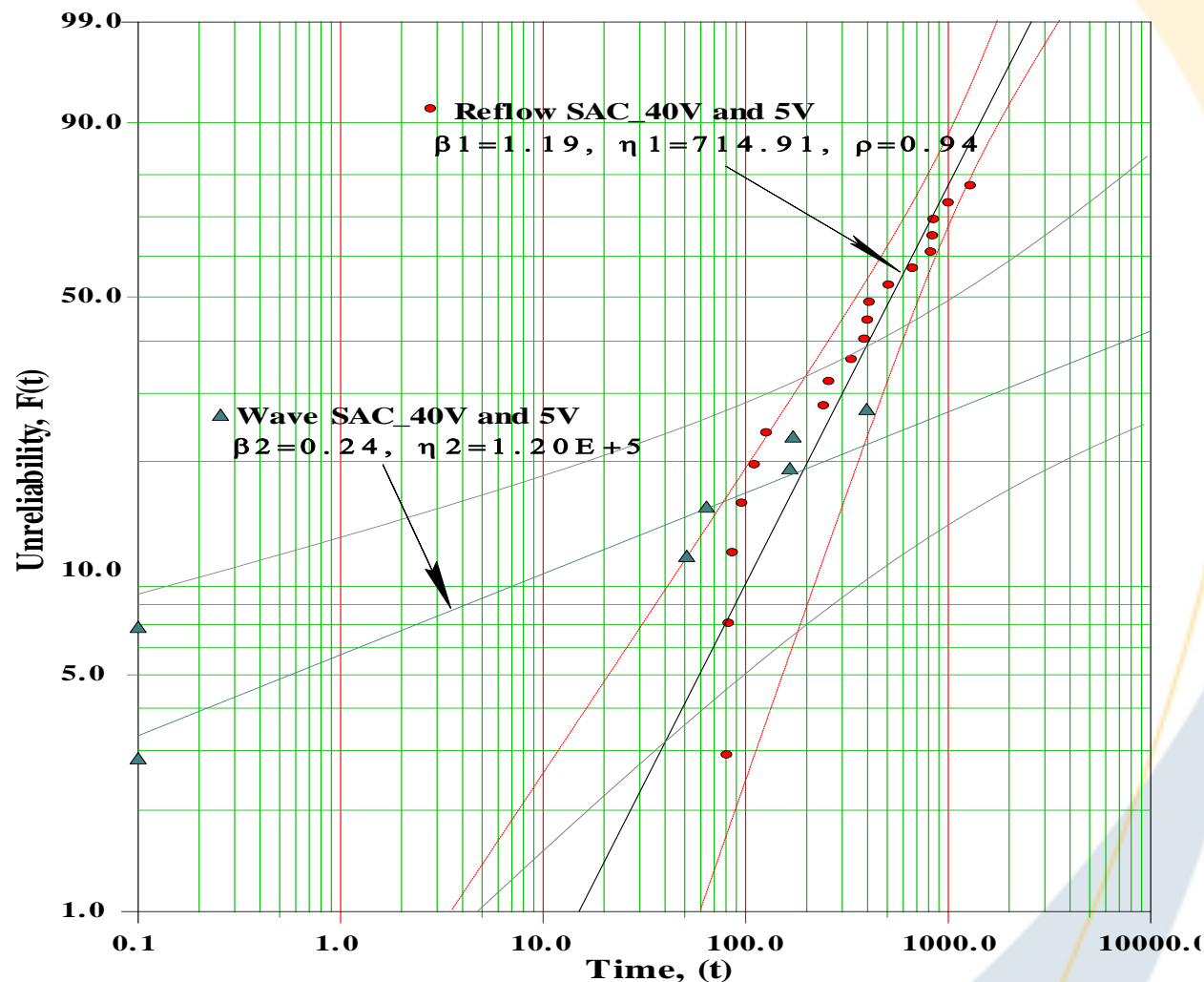
	<b>5V SAC305</b>	
	<b>Wave (OSP and HASL, 25 and 12.5 mil)</b>	<b>Reflow (OSP and HASL, 25 and 12.5 mil)</b>
Number of failed samples after 1000 hrs	1	8
Number of failed samples after 1550 hrs	1	8
Total number of samples	12	12

	<b>40V SAC305</b>	
	<b>Wave (OSP and HASL, 25 and 12.5 mil)</b>	<b>Reflow (OSP and HASL, 25 and 12.5 mil)</b>
Number of failed samples after 1000 hrs	6	9
Number of failed samples after 1653 hrs	6	11
Total number of samples	12	12



# Weibull Analysis of Test Results using SAC305 Solder Comparing Wave vs. Reflow Processing

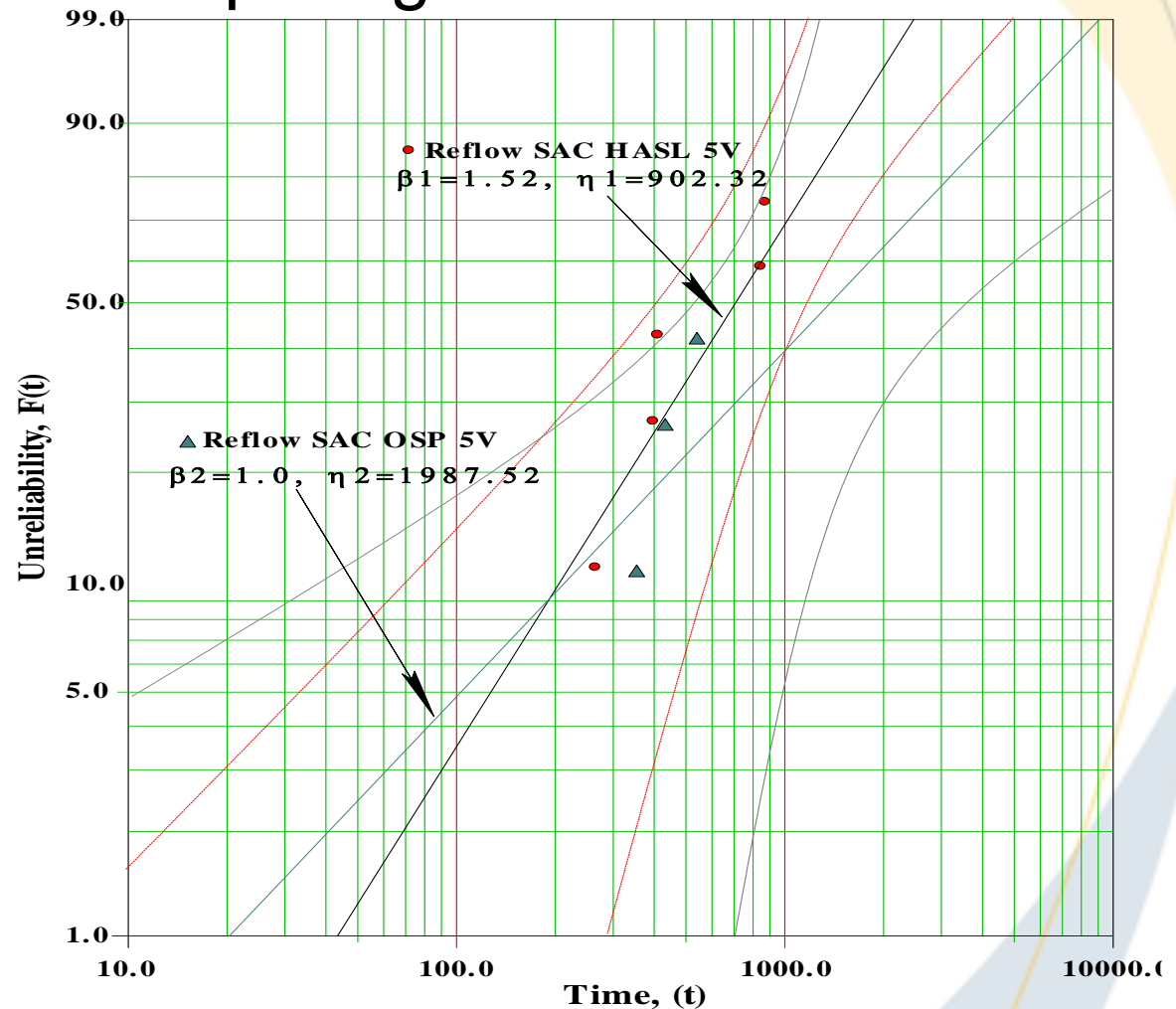
Wave-processed SAC samples showed longer characteristic life than reflow-processed SAC samples



Weibull two parameter fit with 90% confidence intervals

# Weibull Analysis of 5V Test Results using Reflowed SAC305 Comparing OSP vs. HASL

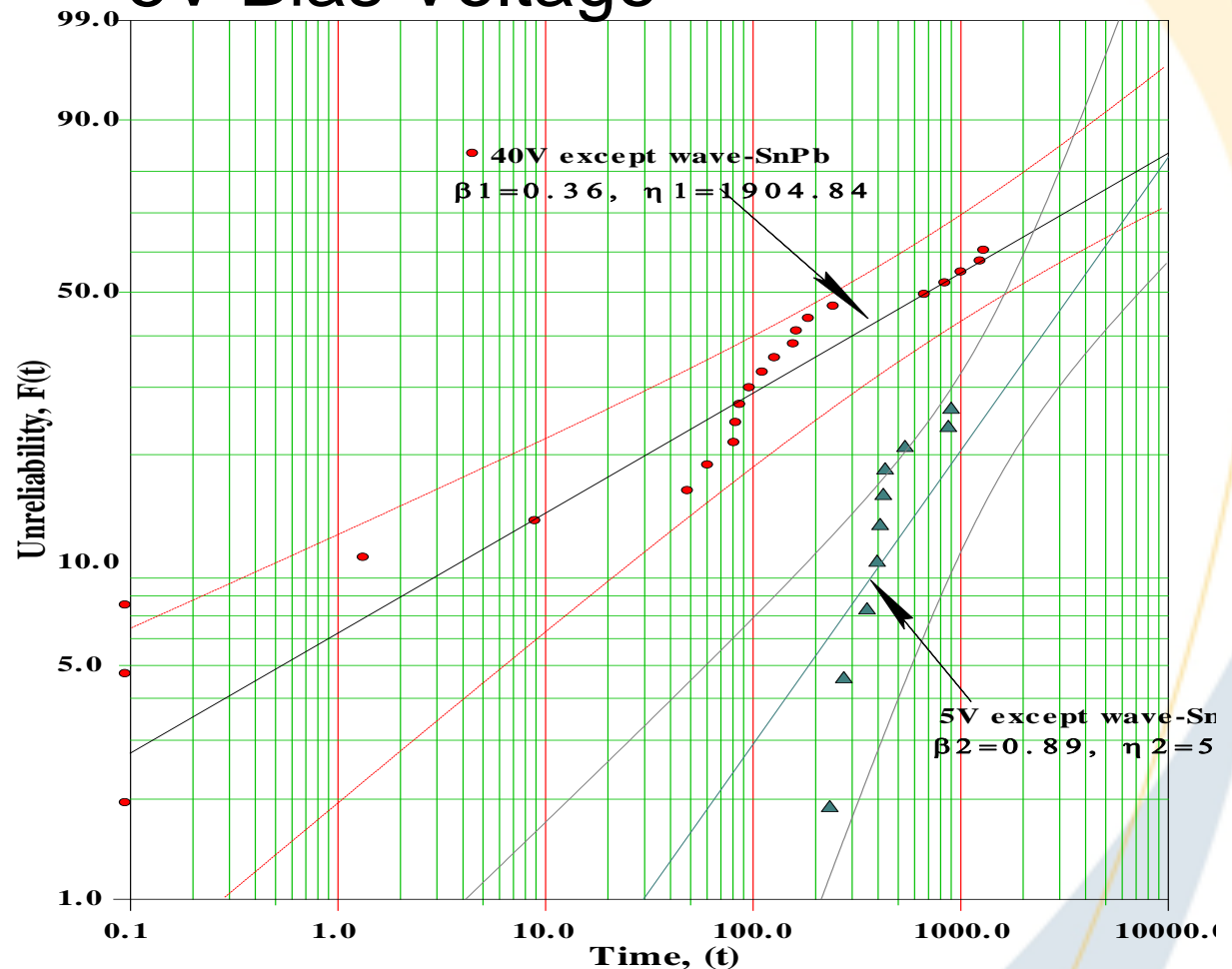
For reflow-processed solders (both SAC and SnPb), OSP and HASL finishes produced similar failure distributions (90% confidence intervals showed considerable overlap).



Weibull two parameter fit with 90% confidence intervals

# Weibull Analysis of Test Results Comparing 40V vs. 5V Bias Voltage

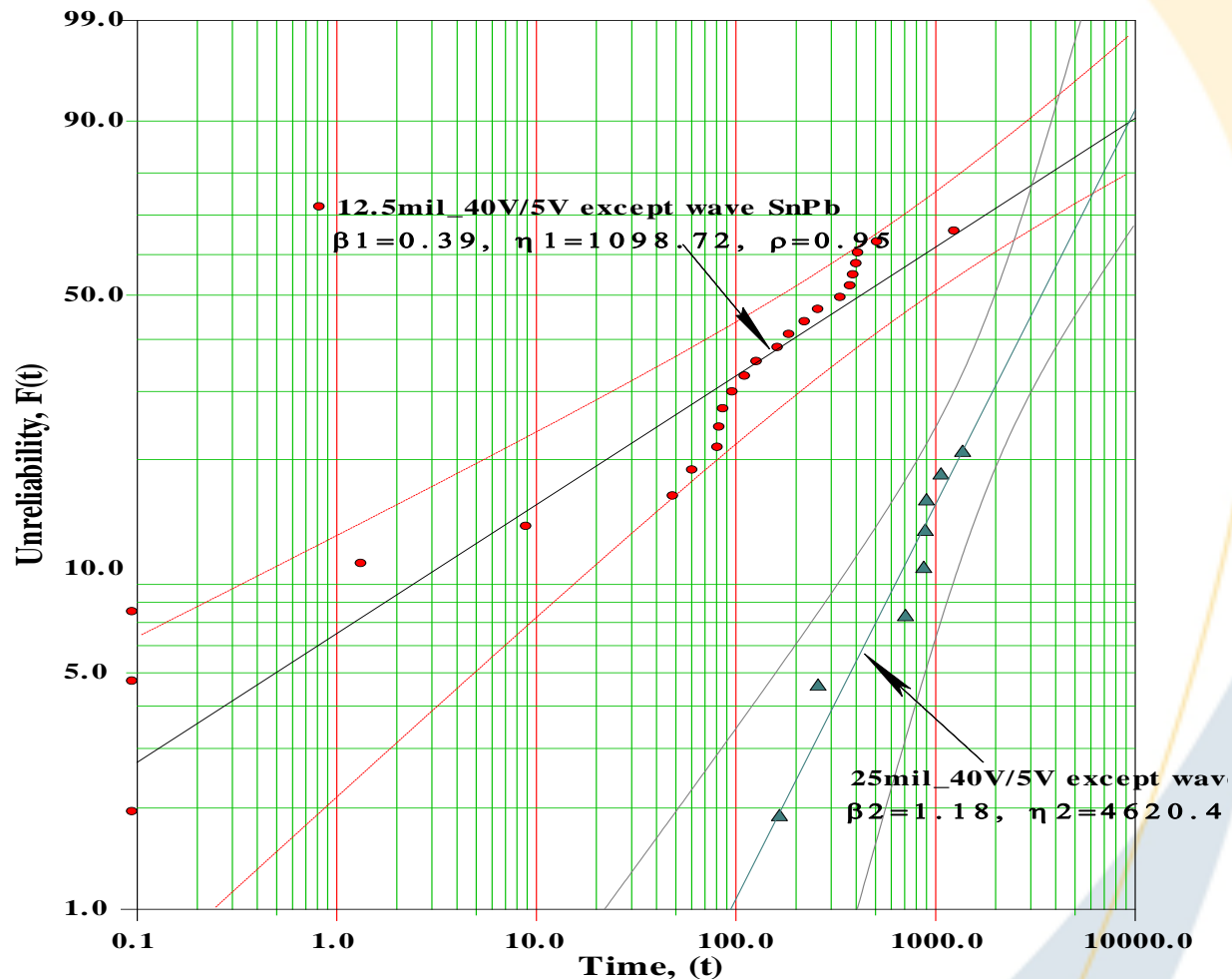
Samples tested at 5V showed longer times-to-failure than those tested at 40V (excluding the wave-processed SnPb samples, for which the results of the voltage comparison were inconclusive).



Weibull two parameter fit with 90% confidence intervals

# Weibull Analysis of Test Results Comparing 25 mil vs. 12.5 mil Conductor Spacings

Samples with 25 mil (0.64 mm) spacings showed longer times-to-failure than those with 12.5 mil (0.32 mm) spacings (excluding the wave-processed SnPb samples, for which the results of the spacing comparison were inconclusive).



Weibull two parameter fit with 90% confidence intervals

# Summary and Conclusions

- Reflow-processed SnPb samples showed longer characteristic life than reflow-processed SAC305 samples
  - SIR of reflow-processed SAC samples showed a stable or increasing trend in the first couple of hundred hours, followed by a prolonged decline. This represents a potential risk to long-life products, and warrants further study.
- Wave-processed SAC samples showed longer characteristic life than reflow-processed SAC samples.
- SIR results on boards finished with OSP and HASL were not significantly different in most cases.
- Higher voltage and smaller conductor spacing both led to shorter characteristic life.
- Short term SIR trends do not consistently predict the relative risk of electrochemical migration over longer periods of THB.

# References and Acknowledgement

- [1] IPC Publication IPC-TR-476A, "Electrochemical Migration: Electrically Induced Failures in Printed Wiring Assemblies," Northbrook, IL, May 1997.
- [2] S. Zhan, M. H. Azarian, and M.G. Pecht, "Surface Insulation Resistance of Conformally Coated Printed Circuit Boards Processed With No-Clean Flux," IEEE Transactions on Electronics Packaging Manufacturing, Vol.29, No.3. July 2006, pp. 217-223.
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