

# Assessment of Moisture Content Measurement Methods for Printed Circuit Boards

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## ABSTRACT

Using embedded structures in printed circuit boards, changes in moisture content have been monitored using route-impulse-energy measurement, capacitance measurement and weight gain. All three methods showed good correlation for different prepregs with similar structures.

Two designs of capacitor plate, a solid plate and a multi slotted plate, showed significantly larger percentage increases in capacitance values (10%) than the corresponding mass increases (0.35%) from moisture ingress effects. A good correlation was also obtained between the RIE measurement results and the board mass changes. The RIE values showed significantly larger percentage increases (20%) than the corresponding mass increases (0.35%) over a similar timeframe.

Although some results indicated a slightly greater moisture take-up for the 2116 prepreg samples compared to the 7628 prepreg samples, the majority of measurements did not show significant performance differences between the two prepreg types.

Both the RIE measurement and capacitance methods show promise in evaluating the moisture content of printed circuit boards. Capacitance measurements using capacitors of a solid plate design, have the disadvantage of inhibiting the take up of moisture if the plates are near the surface of the PCB. RIE coupons have an aspect ratio which enables them to be relatively easily incorporated into the break-off panel that commonly occurs around the outside of many PCB designs during manufacture. Provided that similar coupons had been characterised in the dry condition previously, and that the PCB has the same build characteristics, both types of coupon could be interrogated immediately prior to assembly, to determine the current level of moisture content.

## INTRODUCTION

Recently introduced European RoHS legislation (Reference 1) has removed lead-based solder alloys from a wide range of electronics manufacturing. While beneficial to the environment, it has had a negative impact for printed circuit board manufacturers, assemblers and end-users, who have reported a significant increase in multilayer printed circuit board (PCB) defects associated with the higher soldering temperatures of the replacement alloys (References 2 and 3). Most notably these problems include delamination within the PCB structure, which may lead to premature electrical failure. The cause of delamination is thought to be the more rapid vaporisation of residual moisture at the higher processing temperatures. IPC are already addressing this issue by preparing handling and storage guidelines (References 4 and 5).

Currently there is no simple inspection method to detect delamination. The only available detection method (micro-sectioning) is expensive, time-consuming and destructive. The aim of this project was to develop a new instrumental approach that will allow PCB manufacturers and assemblers to quickly differentiate between good and poor quality product. Moreover, it will enable better selection of PCB materials and the optimisation of processing conditions by PCB assemblers (e.g. pre-baking temperature/time) to minimise electrical failure increasing manufacturing yield, while saving costs, time and energy.

Three novel solutions to the measurement challenge are considered. The first of these uses electrical impedance measurements as a rapid non-destructive test for moisture content. The benefits of measuring moisture content within PCBs using high frequency reflected wave techniques such as time domain reflectometry (TDR) and route impulse energy (RIE) are explored using test features designed into PCBs with impedance characteristics uniquely sensitive to defects. These test patterns could be incorporated onto the supporting window frame located around PCBs, which is typically removed after soldering. Capacitance measurements are also assessed utilising conductive planes incorporated in the multilayer structure in the PCB. Increases in moisture levels of the epoxy-glass between the plates will change the dielectric constant of the material and thus there is the potential for a measurable capacitance change.

CAPACITANCE CHANGES DUE TO MOISTURE INGRESSION

Capacitance Measurement Methodology

Capacitance measurements of two different capacitor designs incorporated in PCBs, were undertaken periodically after conditioning PCBs in a damp environment to increase the moisture content. The mass of the test structures was also monitored to give an indication of moisture take-up.

Design of Capacitance Test Structure

A four layer PCB was designed incorporating capacitor designs using solid plates and multi-slotted plates. The multi-slotted plate, on one layer is actually an interdigitated SIR comb pattern, where the two halves on that layer have been connected together. The solid plate capacitors of three differing areas are shown in Figure 1 and detailed in Table 1. The slotted plate capacitors are shown in Figure 2. These utilised SIR comb patterns of 200 micron tracks on a 400 micron pitch. The patterns on layers 2 and 3 were interconnected to form upper and lower plates of a capacitor.

Table 1: Details of solid plate capacitors

Pattern	Area (mm <sup>2</sup> )	Layers incorporating plates
A	1000	1, 2, 3 & 4
B	1000	2 & 3
C	2000	1, 2, 3 & 4
D	2000	2 & 3
E	4000	1, 2, 3 & 4
F	4000	2 & 3

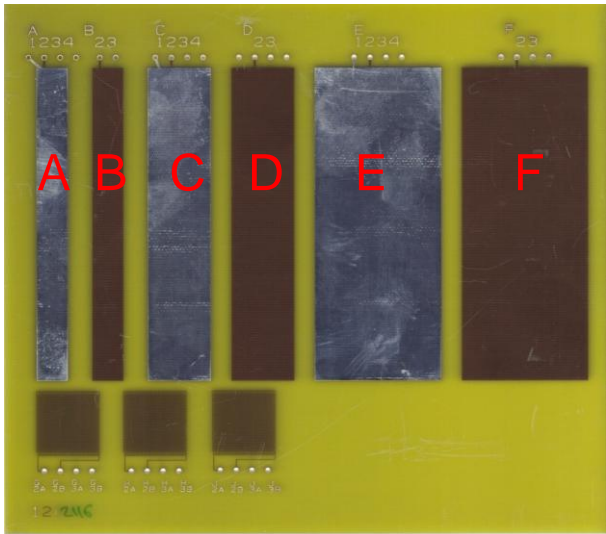
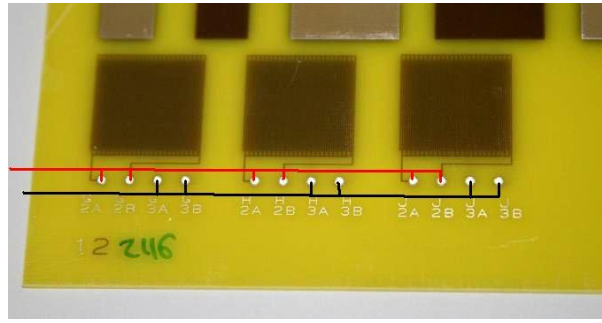


Figure 1: Parallel plate capacitors (A-F)



**Figure 2: Interdigitated capacitors, with electrical connections indicated**

### Fabrication of Capacitance Test Structure

Four layer, 1.6mm thick PCBs were fabricated using two different lay-ups. Samples designated 2116 were fabricated using copper foils on two layers of 2116 prepreg (pre-impregnated composite fibres) either side of a 1mm copper clad core. Samples designated 7628 were fabricated using a single 7628 prepreg layer either side of a 1mm core. The major differences in the two prepregs is given in Table 2. The 2116 prepreg has a slightly higher resin content, and a greater number of smaller diameter fibres.

**Table 2: Details of pre-preg types used**

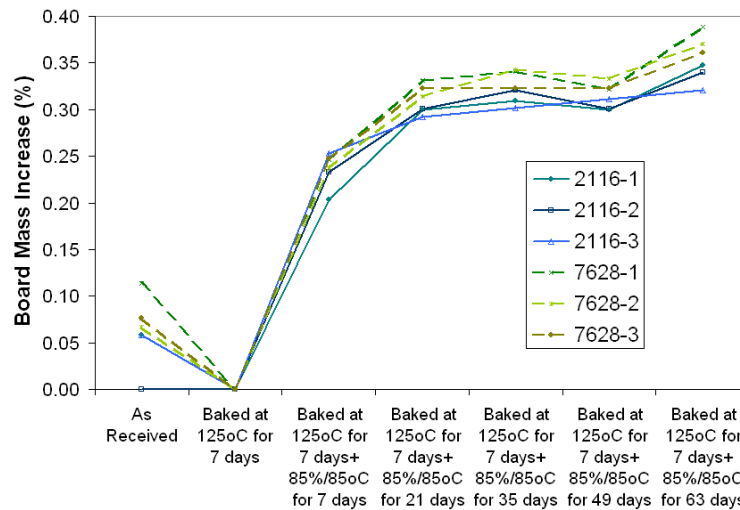
Prepreg Type	2116	7628
Resin Content	53%+3%	51%+3%
Fibre Thickness (mm)	0.094	0.173
Fabric Count (warp x fill, per cm)	23.6x22.8	17.3x12.2

### Capacitance Measurement

The capacitance of the solid plate capacitors were measured at 10 kHz and 100 kHz. The slotted capacitors were measured at 100 kHz.

### Conditioning

Test boards were initially baked at 125°C for 7 days to remove any residual moisture. Subsequent conditioning was undertaken at 85°C/85%RH.



**Figure 3: Increase in board mass for solid plate capacitor test structures during damp heat conditioning**

### Results for board mass of solid plate capacitor PCBs

The percentage increase in solid plate test board mass during damp heat conditioning is shown in Figure 3, with three samples for each material type. All samples showed an increase in board mass when subjected to the damp environment. The samples using 7628 prepreg showed a slightly greater increase in board mass compared to those fabricated with 2116 prepreg. Peak levels of moisture ingress were achieved at around 21 days of exposure to 85°C/85%RH.

### Results for capacitance measurements of solid plate capacitor PCBs

The percentage increase in parallel plate test board capacitance during damp heat conditioning is shown in Figure 4 for the 2116 samples and in Figure 5 for the 7628 samples. The numbering system for each capacitor indicates on which layers the capacitance is being measured, for example A12, indicates pattern A, and measure between layers 1 and 2. All samples showed an increase in capacitance of up to 12% when subjected to the damp environment. The samples using 2116 prepreg generally showed a greater increase in capacitance compared to those fabricated with 7628 prepreg. Also the smaller sized plates (A&B) showed greater capacitance increases compared to the larger C and D plates which in turn, showed greater increases than the largest plates (E & F). Maximum take-up of moisture occurred at around 49 days when subjected to an 85°C/85%RH environment.

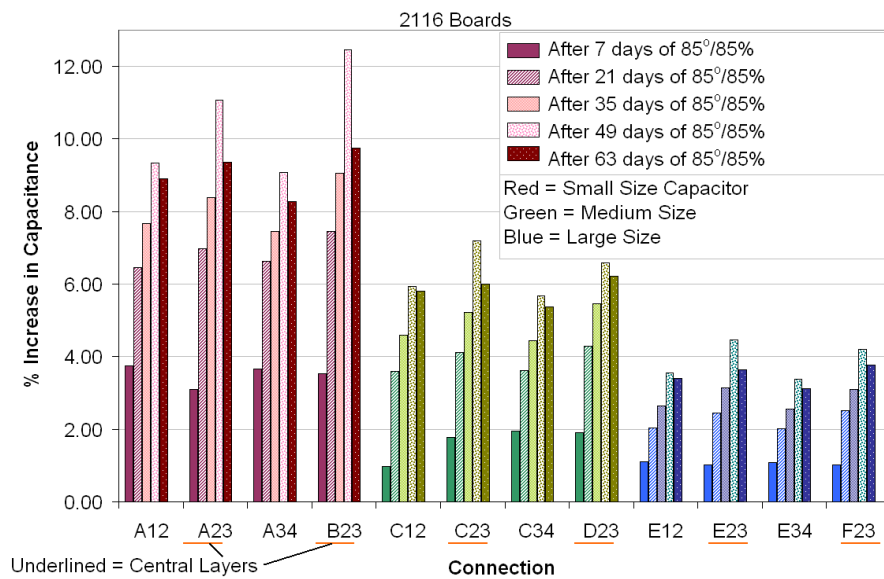


Figure 4: Changes in solid plate capacitance for 2116 samples during damp heat conditioning

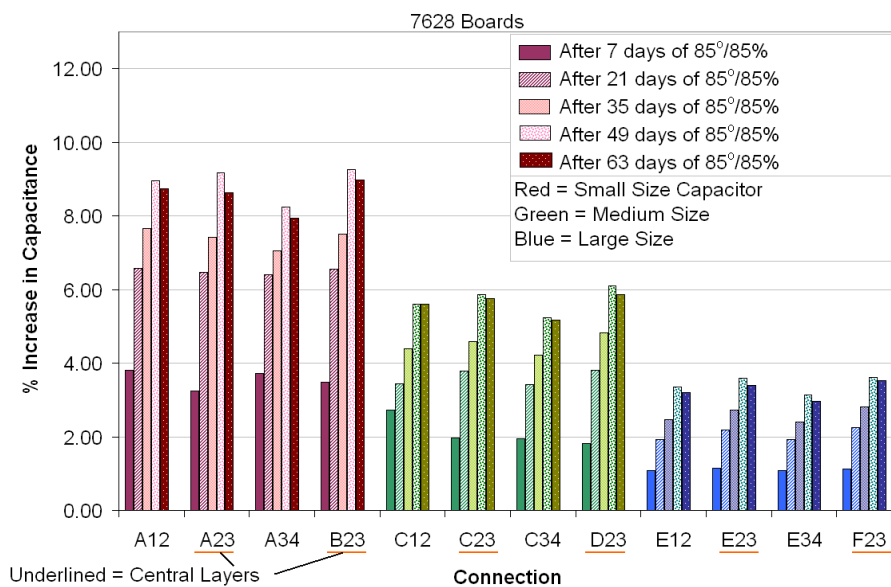
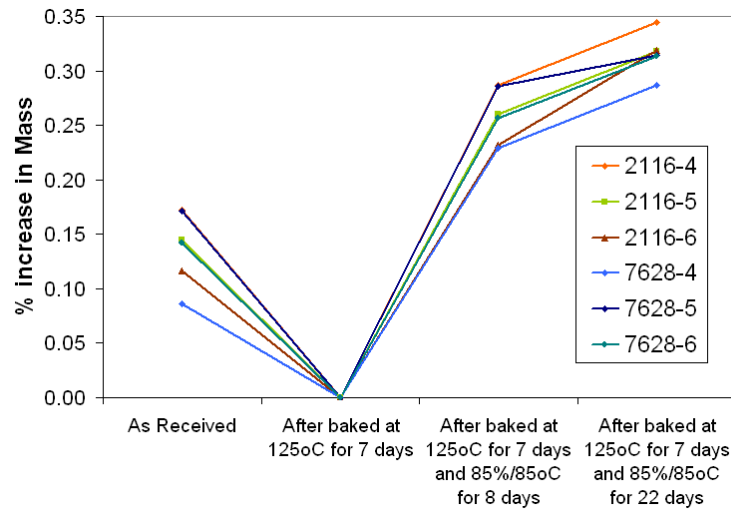


Figure 5: Changes in parallel plate capacitance for 7628 samples during damp heat conditioning

### Results for board mass changes for slotted capacitors

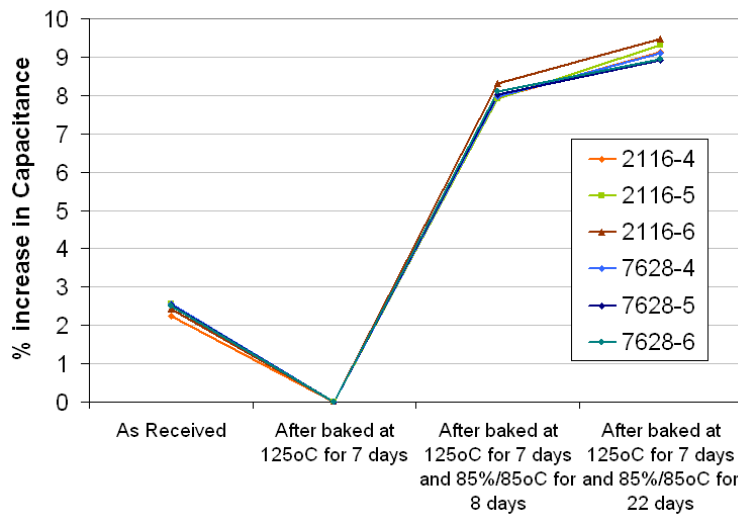
The percentage increases in inter-digitated capacitor test board mass during damp heat conditioning is shown in Figure 6. All samples showed an increase in board mass when subjected to the damp environment with no discernable differences between 7628 and 2116 prepreg samples.



**Figure 6: Increase in board mass for slotted capacitor test structures during damp heat conditioning**

### Results for capacitance measurements of slotted capacitor PCBs

The percentage increase in parallel plate test board capacitance during damp heat conditioning of both 2116 and 7628 samples is shown in Figure 7. All samples showed an increase in capacitance of up to 9% when subjected to the damp environment for 22 days. No differences between the two pre-preg types were apparent.



**Figure 7: Changes in solid plate capacitance for 2116 and 7628 samples during damp heat conditioning**

### Capacitance Discussion

Both types of capacitor (solid and slotted plate) showed significantly larger percentage increases in capacitance values than the corresponding mass increases due to moisture ingress. Increases in board mass were up to 0.35% over a three week exposure period whereas capacitance increases approached 10% over a similar timeframe.

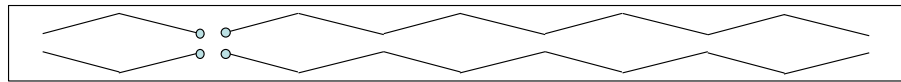
Comparing the different sizes of the solid plate capacitors, it is clear that the larger area capacitors show significantly less capacitance change over the duration of the damp heat conditioning. This is because the copper plates of the capacitors prevent moisture ingress from the surface of the test boards. Moisture is only able to penetrate from the edges of the plates and thus the distances required for the moisture to travel are significantly greater and longer periods of time are required to gain similar levels of moisture between the plates. This is further borne out by the data from the slotted plates where moisture is able to permeate between the copper tracks and thus has significantly less distance to travel to saturate the region between the plates. With these samples, capacitance increases of 8% are achieved with eight days of damp heat conditioning, whereas the solid plate samples require 35 days to reach similar levels and then only on the smaller plate sizes.

The results from the solid plate capacitor samples indicate a slightly greater moisture take-up and capacitance change for the 2116 prepreg samples compared to the 7628 prepreg samples. This may be due to the slightly higher resin content of this prepreg. However, the slotted capacitance samples did not show significant differences.

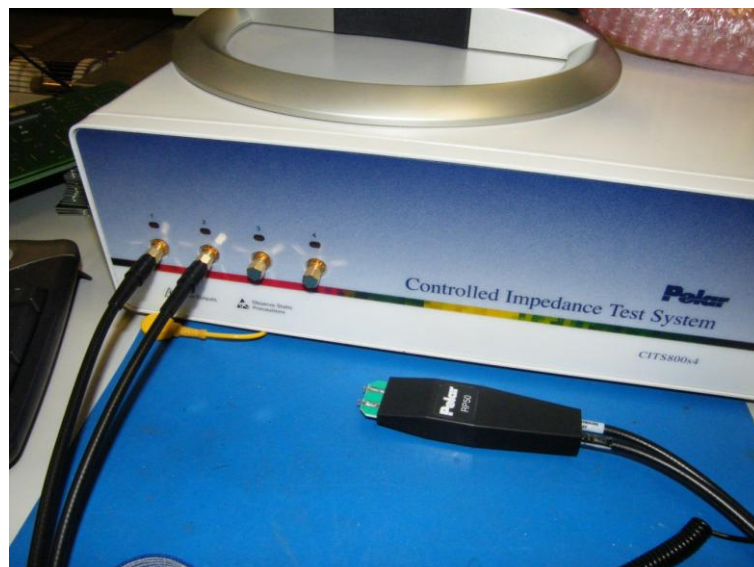
## **ROUTE IMPULSE ENERGY (RIE)**

### **Methodology**

Route impulse energy (RIE) measurements use time domain reflectometry (TDR) to measure the difference in losses between two identically constructed PCB transmission lines of different lengths. These lines are a short reference line and a longer test line, both with far ends that are open circuited. Further details of the RIE techniques can be found in references 6 and 7. A schematic of the test coupon is shown in Figure 8. The lines are meandered to reduce potential differences associated with the weft and warp of the reinforcing fibres in the PCB. Identical step pulses are injected into each line and reflected step pulses captured. The ratio between the energies contained in reflected step pulses is proportional to extra loss introduced by additional length of test line. If the moisture content of the PCB increases, this causes an increase in the PCB materials dielectric constant which will lead to increases in signal losses. The test equipment and probes used are shown in Figure 9. The technique uses additional software running on readily available PCB impedance measurement equipment.



**Figure 8: Schematics of the RIE test coupon**



**Figure 9: RIE test equipment (software modified controlled impedance test system) and test probes**

## **Test Coupon Design**

A 1.6mm thick, six layer multilayer test coupon design was produced (345mm x 25mm), utilising ground planes on layers 3 & 4, with the one set of reference and test lines on layer 2 and another set on layer 5. The outer layers (1 and 6) contained no copper. Coupons were fabricated using 2116 and 7628 prepregs.

### Conditioning

Test boards were initially baked at 125°C for 7 days to remove any residual moisture. Subsequent conditioning was undertaken at 85°C/85%RH. After 23 days damp heat ageing samples were subjected to single LF reflow profile (peak reflow temperature~ 260°C)

### Results for board mass of RIE test coupon weight gain

The percentage increases in RIE test coupon mass during damp heat conditioning is shown in Figure 10. All samples showed an increase in board mass of around 0.35% when subjected to the damp environment with no discernable differences between 7628 and 2116 prepreg samples.

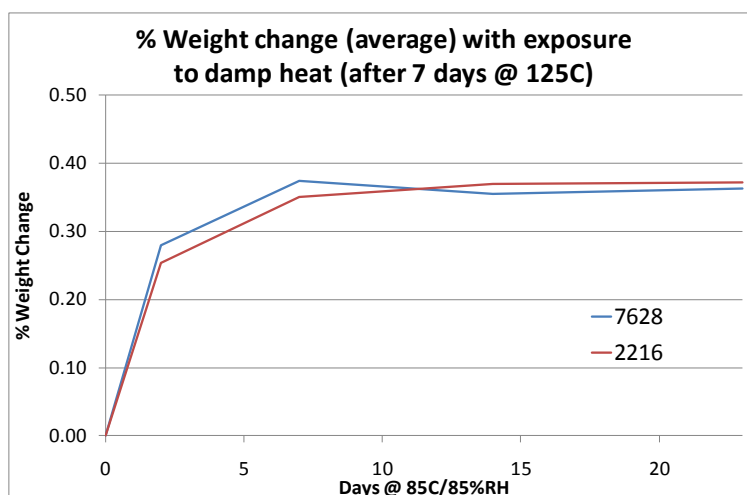


Figure 10: Increase in board mass for RIE test structures during damp heat conditioning

### Results for RIE measurement

The percentage increase in RIE values for the test coupons during damp heat conditioning of the 2116 samples are shown in Figure 11 and 7628 samples in Figure 12. All samples showed an increase in RIE values of typically up to 20% when subjected to the damp environment for 22 days. No differences between the two prepreg types were apparent.

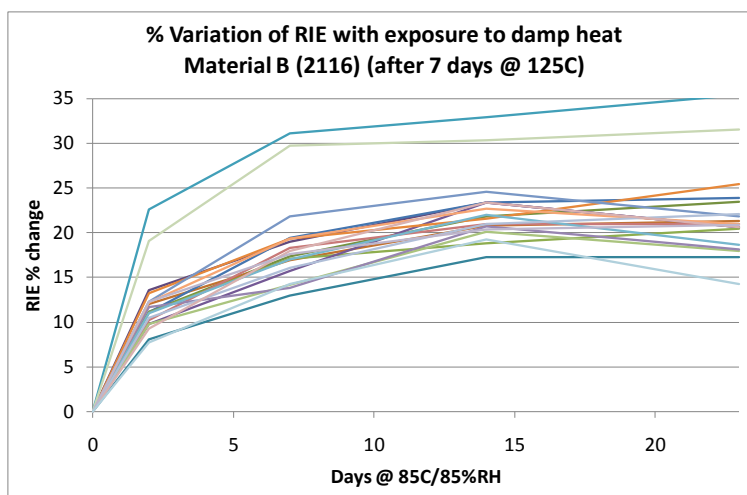
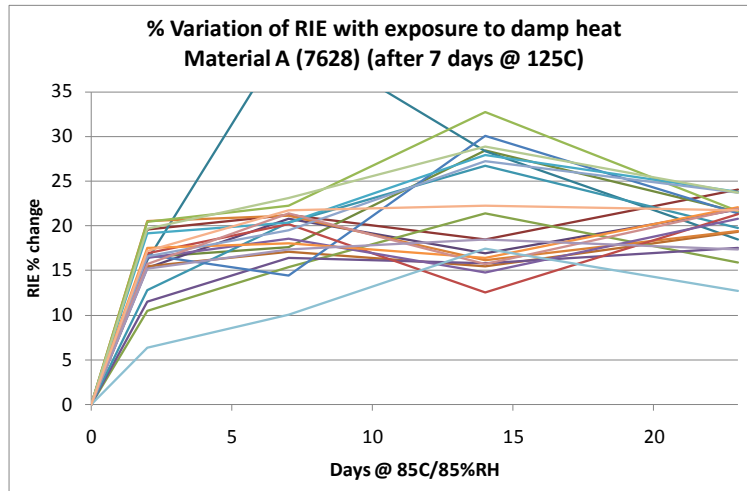


Figure 11: Changes in RIE values for 2116 samples during damp heat conditioning



**Figure 12: Changes in RIE values for 7628 samples during damp heat conditioning**

#### Results: Post Conditioning Reflow

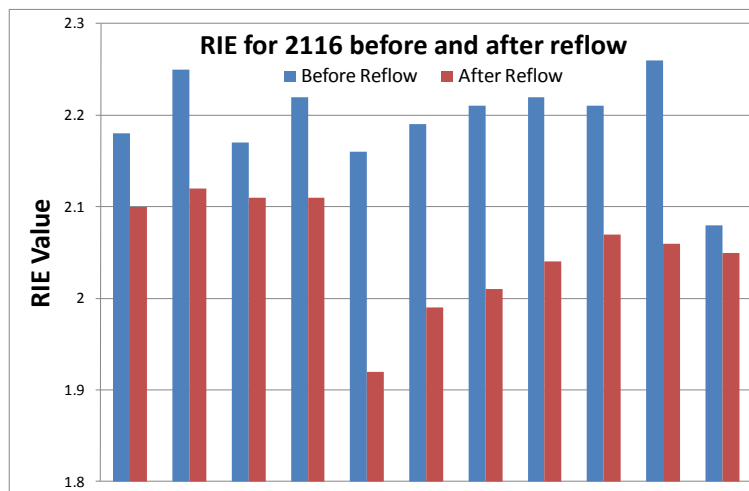
The change in RIE values due to reflow soldering is shown for 2116 in Figure 13 and in

Figure 14 for 7628 samples for 12 samples of each type. After reflow, the RIE values are significantly lower. A summary of the average RIE values before and after reflow is given in

Table 3. The difference in the values corresponds to moisture loss from the PCBs during reflow. Visual inspection of the samples showed significantly greater amounts of delamination in the 2116 samples compared to the 7628 samples.

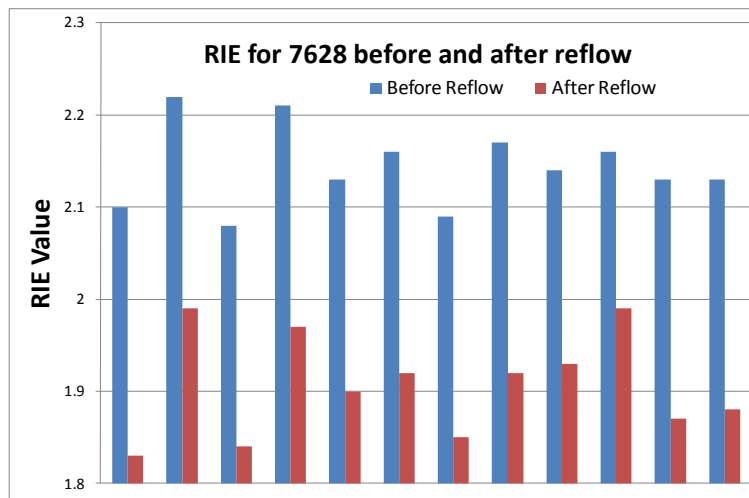
**Table 3: Comparison of average RIE values before and after reflow soldering**

	Average before conditioning	RIE DH	Average before reflow	RIE	Average RIE after reflow
2116	1.81		2.20		2.05
7628	1.78		2.14		1.91



**Figure 13: Comparison of RIE values before and after soldering for 2116 samples**





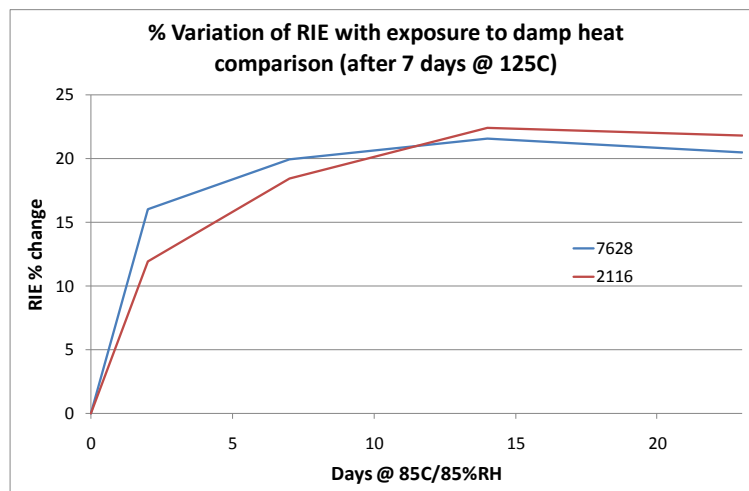
**Figure 14: Comparison of RIE values before and after soldering for 7628 samples**

### Discussion of RIE measurement results

The RIE measurement results and the board mass changes (Figure 15 and

Figure 10) show good correlation between the increases in RIE values and the mass increase due to moisture ingress. The RIE values showed significantly larger percentage increases than the corresponding mass increases due to moisture ingress. Increases in board mass were up to 0.35% over a three week exposure period whereas RIE value increases approached 20% over a similar timeframe.

It should also be noted that the moisture take-up occurs within 10 days as there are no external ground planes to inhibit moisture ingress from the surface of the coupons. Such a coupon could be incorporated into the break-off panel that commonly occurs around the outside of PCBs during manufacture. Provided that similar coupons had been characterised in the dry condition previously, and that the PCB has the same build characteristics, such a coupon could be interrogated immediately prior to assembly, to determine the current level of moisture content.



**Figure 15: Comparison of average RIE values during damp heat conditioning**

### DISCUSSION

Using embedded structures in printed circuit boards, changes in moisture content have been monitored using route-impulse-energy measurement, capacitance measurement and weight gain. All three methods showed good correlation for similar structures using different prepreps during fabrication.

Two designs of capacitor, solid and slotted plates, showed significantly larger percentage increases in capacitance values than the corresponding mass increases due to moisture ingress. Increases in board mass were up to 0.35% over a three week exposure period whereas capacitance increases approached 10% over a similar timeframe. The solid plate capacitors indicated a slower moisture take up because the design utilised uninterrupted ground planes of copper which prevented moisture ingress from the top and bottom surfaces of the PCBs, only allowing moisture ingress in the plane of the PCB. Larger designs of solid plate capacitors showed significantly less capacitance change over the duration of the damp heat conditioning for similar reasons. It should be noted that whilst uninterrupted ground planes near the surfaces of PCBs would inhibit the ingress of moisture, it is also likely that they would lengthen drying times. This is further borne out by the data from the slotted patterns, where moisture was able to permeate between the copper tracks and thus had significantly less distance to travel to saturate the board. With these samples, capacitance increases of 8% are achieved with eight days of damp heat conditioning, whereas the solid plate samples require 35 days to reach similar levels and then only on the smaller plate sizes.

Good correlation was also obtained between the RIE measurement results and the board mass changes. The RIE values showed significantly larger percentage increases (20%) than the corresponding mass increases (0.35%) over a similar timeframe. Again with the RIE samples with no external ground planes, moisture take-up was shown to occur relatively rapidly.

Although some results indicated a slightly greater moisture take-up for the 2116 prepreg samples compared to the 7628 prepreg samples, the majority of measurements did not show significant performance differences between the two prepreg types.

Both the RIE measurement and capacitance methods show promise in evaluating the moisture content of printed circuit boards. Capacitance measurements using capacitors of a parallel plate design, have the disadvantage of inhibiting the take up of moisture if the plates are near the surface of the PCB. However, if this is the normal position of the ground planes in the PCBs design under investigation, this may be considered a benefit. If the PCB design already incorporates such ground planes, it may be possible to utilise these existing structures for capacitance measurement.

RIE coupons have an aspect ratio which enables them to be relatively easily incorporated into the break-off panel that commonly occurs around the outside of many PCB designs during manufacture. Provided that similar coupons had been characterised in the dry condition previously, and that the PCB has the same build characteristics, such a coupon could be interrogated immediately prior to assembly, to determine the current level of moisture content.

## CONCLUSION

- Both RIE and capacitance measurements are sensitive to changes in moisture content in the PCB, giving good single data that can discriminate the moisture level in the board. The effect of one reflow is easily seen on drying a saturated board.
- RIE patterns have a geometry that facilitates easy inclusion into the break-off panel.
- Design of capacitance pattern is critical, and large solid plates act as excellent moisture barriers. A slotted design allows significantly faster moisture uptake and drying.
- Two prepreg styles were tested, 2116 and 7628, these did not show any significant difference in moisture uptake and drying.

## REFERENCES

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5. IPC-1601 Printed board handling and storage guide; Working Draft – Dec. 2009

6. Gore, B., Mellitz R., Loyer J., Gaudion M., Burnikell J., and Carré P.; Toward a PCB Production Floor Metric for Go/No Go Testing of Lossy High-Speed Transmission Lines; 2008 IPC Printed Circuits Expo
7. Harper M., Ridler N. and Salter M.; Comparison between root-impulse-energy and vector network analyzer methods for measuring loss on printed circuit boards; 72nd ARFTG Microwave Measurement Conference Digest, Portland, OR, USA, 9-12 December 2008, 20-25

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Aero Engine Controls  
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BAe Systems  
European Space Research and Technology Centre  
GE Fanuc Intelligent Platforms  
MBDA (UK) Ltd  
Polar Instruments  
Rolls Royce Marine  
Selex S&AS UK

# Assessment of Moisture Content Measurement Methods for Printed Circuit Boards

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- Aero Engine Controls
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- BAe Systems
- Estec
- GE Fanuc
- MBDA
- Hansatech
- Polar Instruments
- Rolls Royce
- Selex

UK government Depart of Business Innovation and Skills

# LF and PCB Integrity

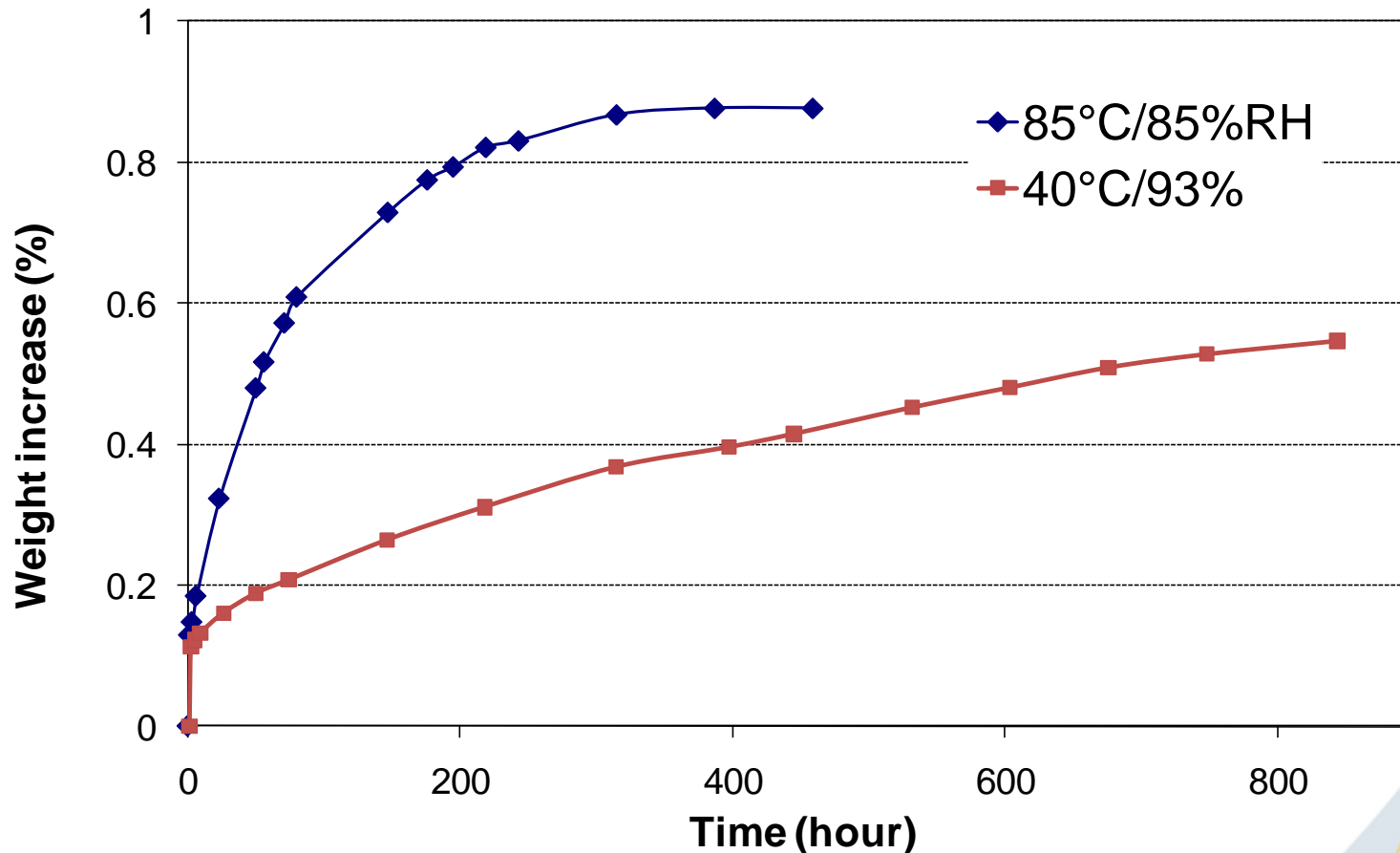
- End-users are reporting a increase in integrity defects for printed circuit boards after lead-free assembly.
- Delamination of multilayer printed circuit boards (PCBs), primarily caused by the moisture ingress into the PCBs, which ruptures apart the multilayer construction during soldering and rework operations

# Project Aims

- This project will review the applicability of a range of non-destructive techniques to determine the degree of delamination and in particular, develop a test method, based on impedance measurements between PCB inner layers.
  - Ideally to provide go/no-go preassembly PCB check
  - High frequency reflected wave techniques such as route impulse energy (RIE)
- This project will also provide industry with a best practice guide on how to minimise the effects on boards of the solder profile

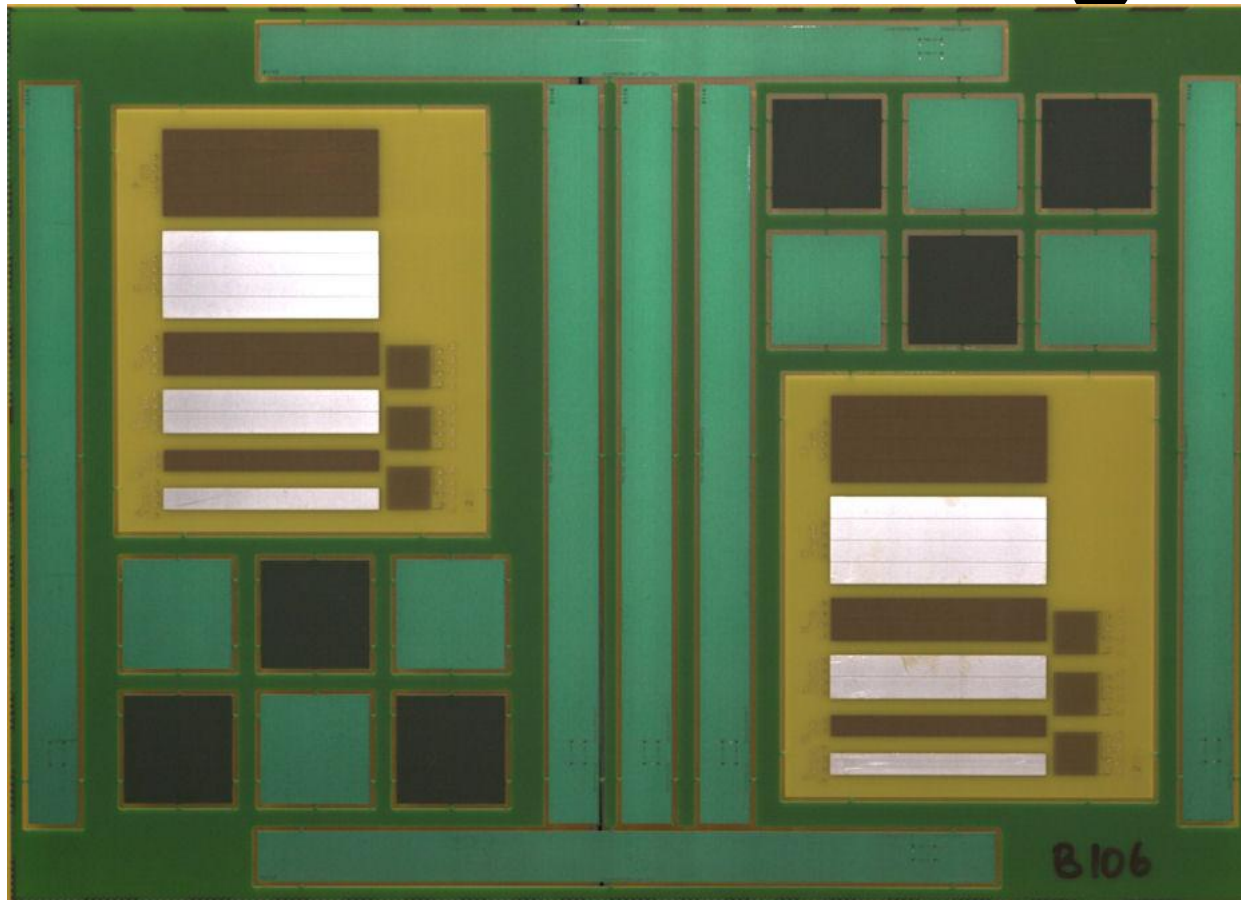
# Accelerated Moisture uptake in FR4

Weight gain in FR4 blanks after drying





# Phase 2 Board Designs



Big thank you to Artetch and Polar

# 7628/2116 Comparison

- Resin content

- 2116     53%+/-3%

- 7628     51%+/-3%

**2116**

Slightly higher resin content

Smaller diameter fibres

Greater no. of fibres

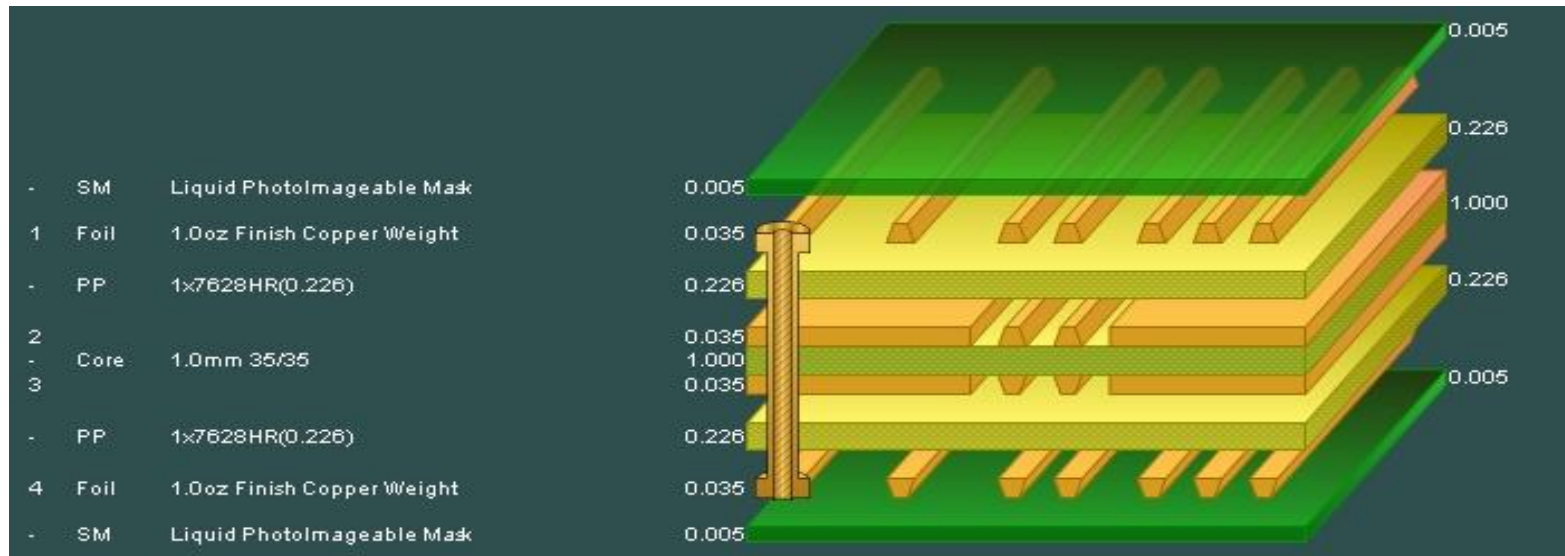
Style	Fabric Count Warp x Fill (Per cm)	Yarn (SI)	Thickness (mm) (Reference Only)	Nominal Weight (g/m <sup>2</sup> )	Weight Tolerance (g/m <sup>2</sup> )
2116	23.6x22.8 (60x58 per inch)	7 22 1x0 7 22 1x0	0.094	103.8	100.7-106.8 1
7628	17.3x12.2 (44x31 per inch)	9 68 1x0 9 68 1x0	0.173	203.4	198.0-208.9 1

Yarn	Nominal Length per Unit Weight (m/kg)
7 22 1x0	45,358
9 68 1x0	14,716

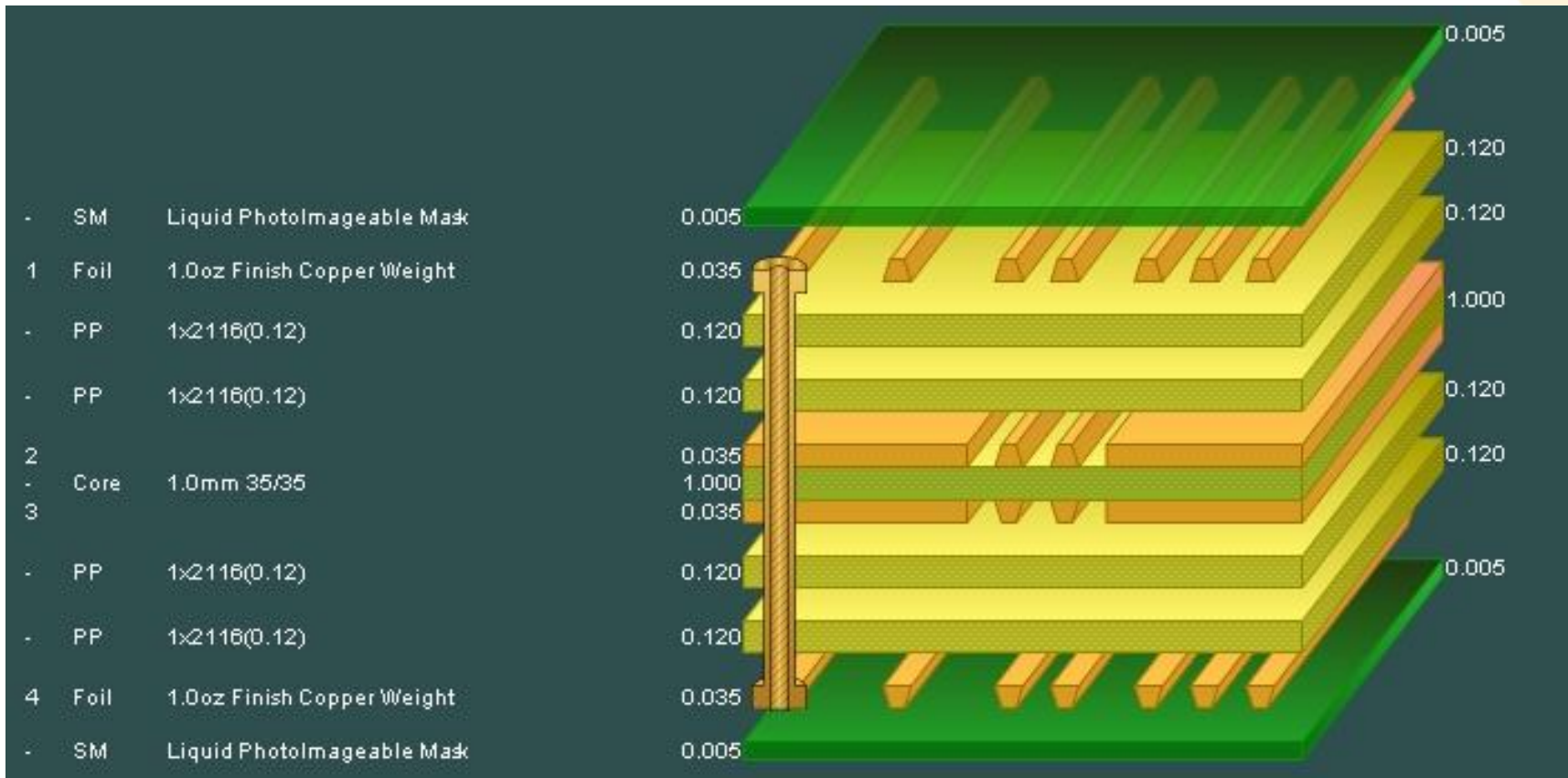
1x0 = Single yarn which has not been combined.

Source: IPC 4412A

# Build 1: 7628, 1.6mm, 4 layer

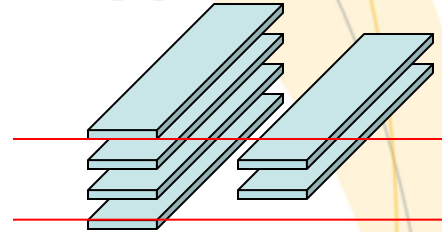


# Build 2: 2 x 2116, 1.6mm, 4 layer

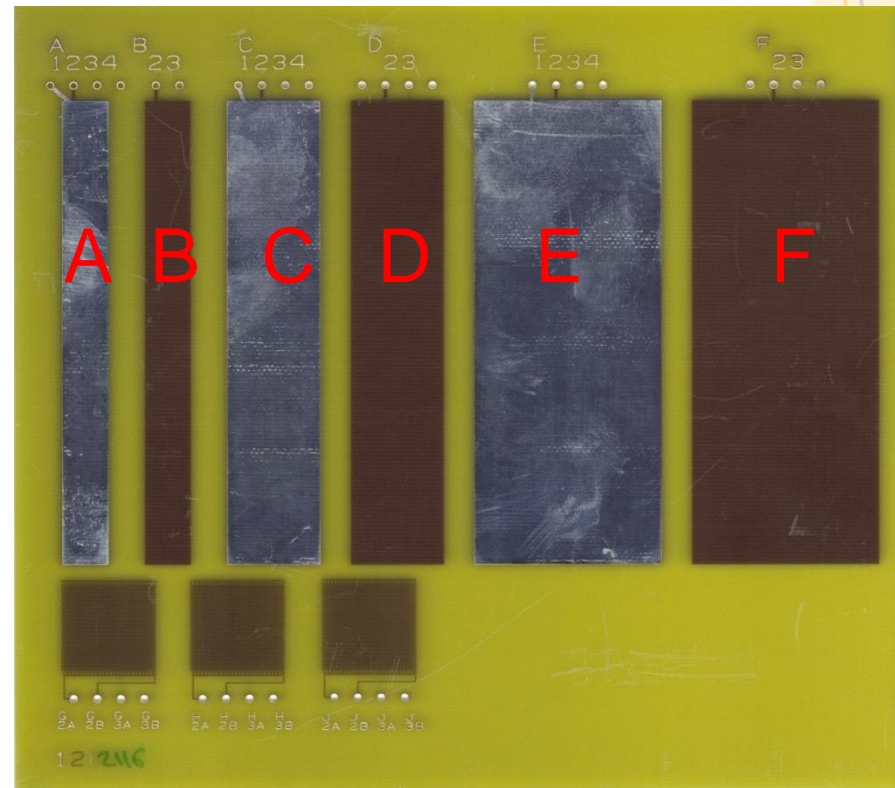


# Capacitance Measurement (I)

- (Parallel) Plate Capacitors
- Cp measured at 10 kHz and 100 kHz
- Four layer construction
- 2116 & 7628



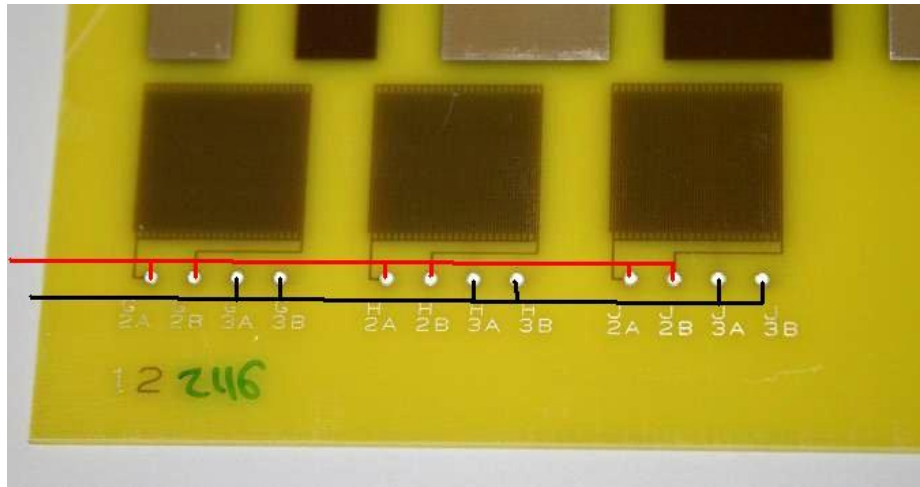
Pattern	Area (mm <sup>2</sup> )	Layers
A	1000	1, 2, 3 & 4
B	1000	2 & 3
C	2000	1, 2, 3 & 4
D	2000	2 & 3
E	4000	1, 2, 3 & 4
F	4000	2 & 3



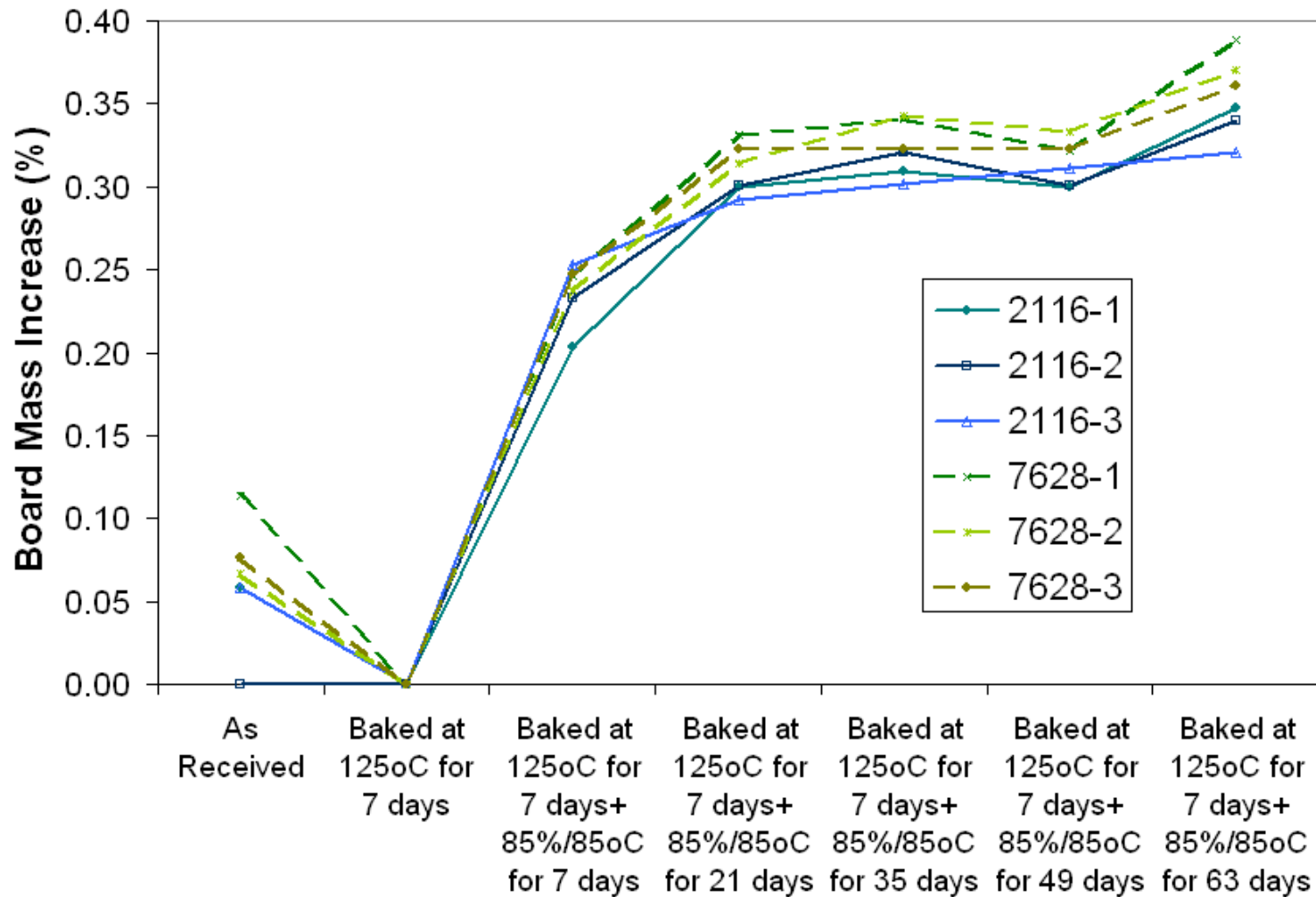


# Capacitance Measurement (II)

- Interdigitated Plate Capacitors
  - 2 board types, 3 boards of each tested
  - $C_p$  measured at 100 kHz only.

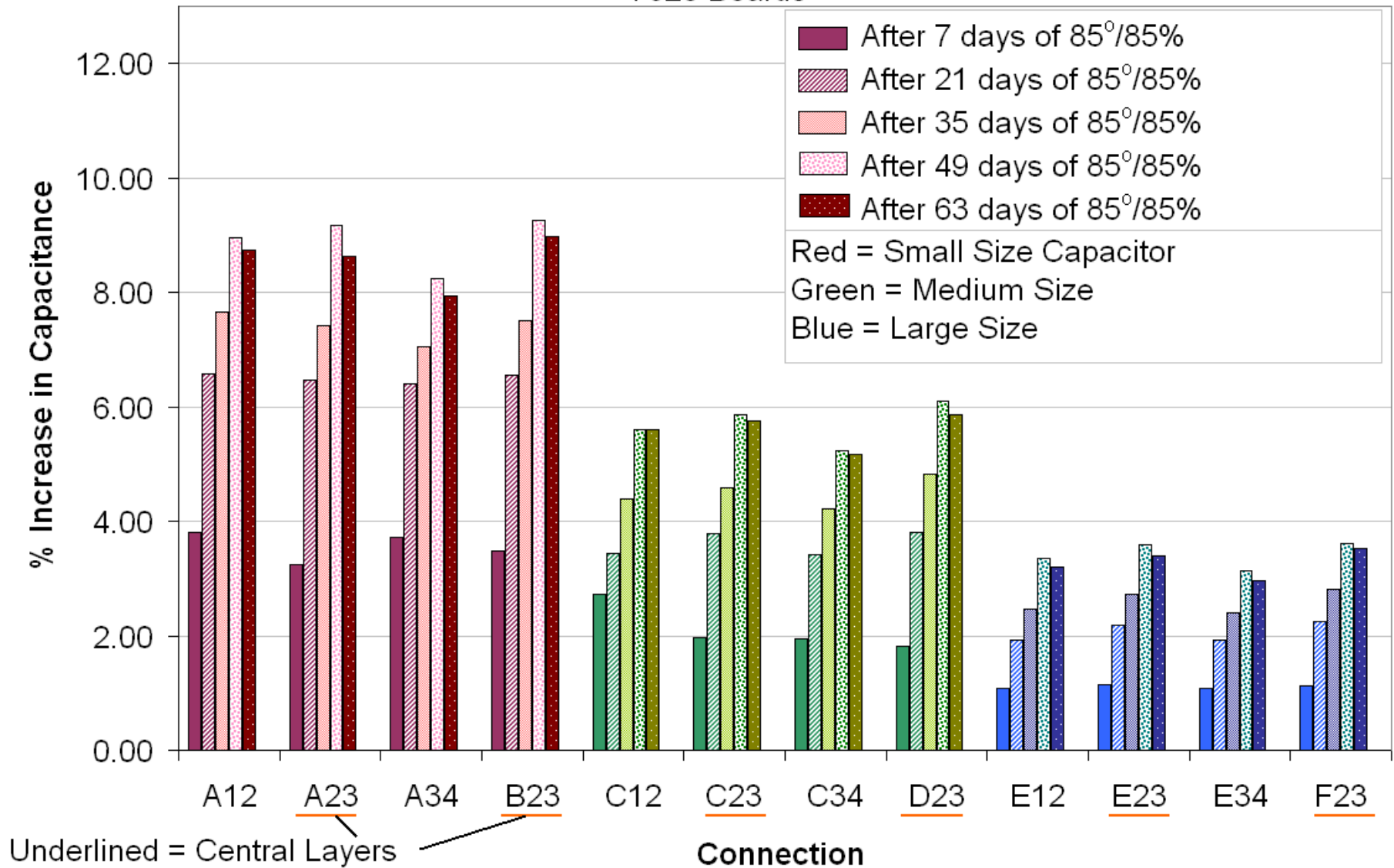


# Plate Capacitors – Board Mass



# Plate Capacitors – Capacitance of 7628

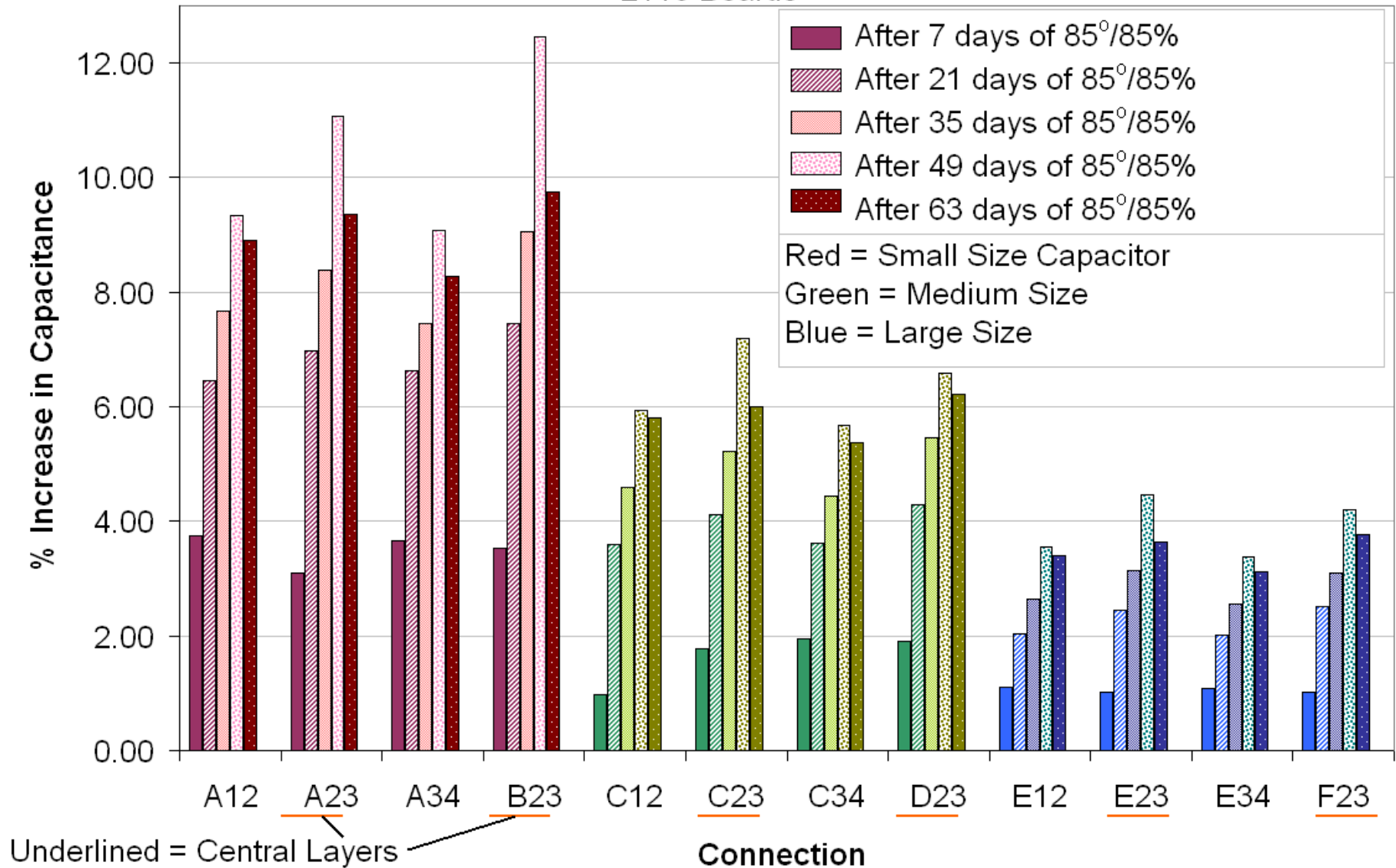
7628 Boards





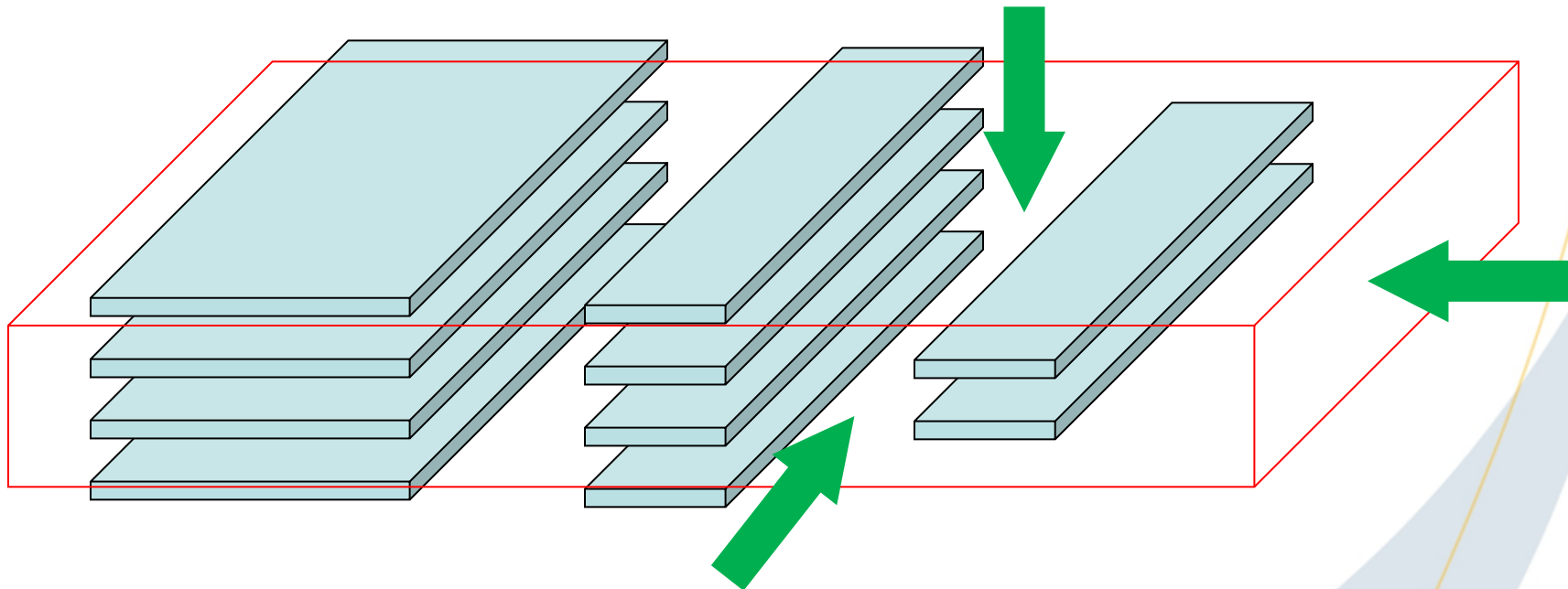
# Plate Capacitors – Capacitance of 2116

2116 Boards

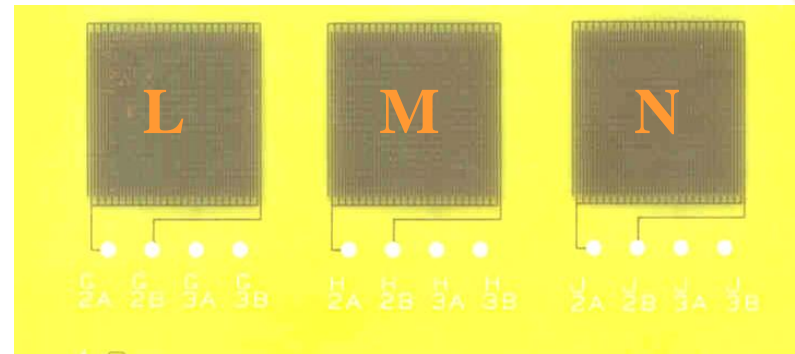
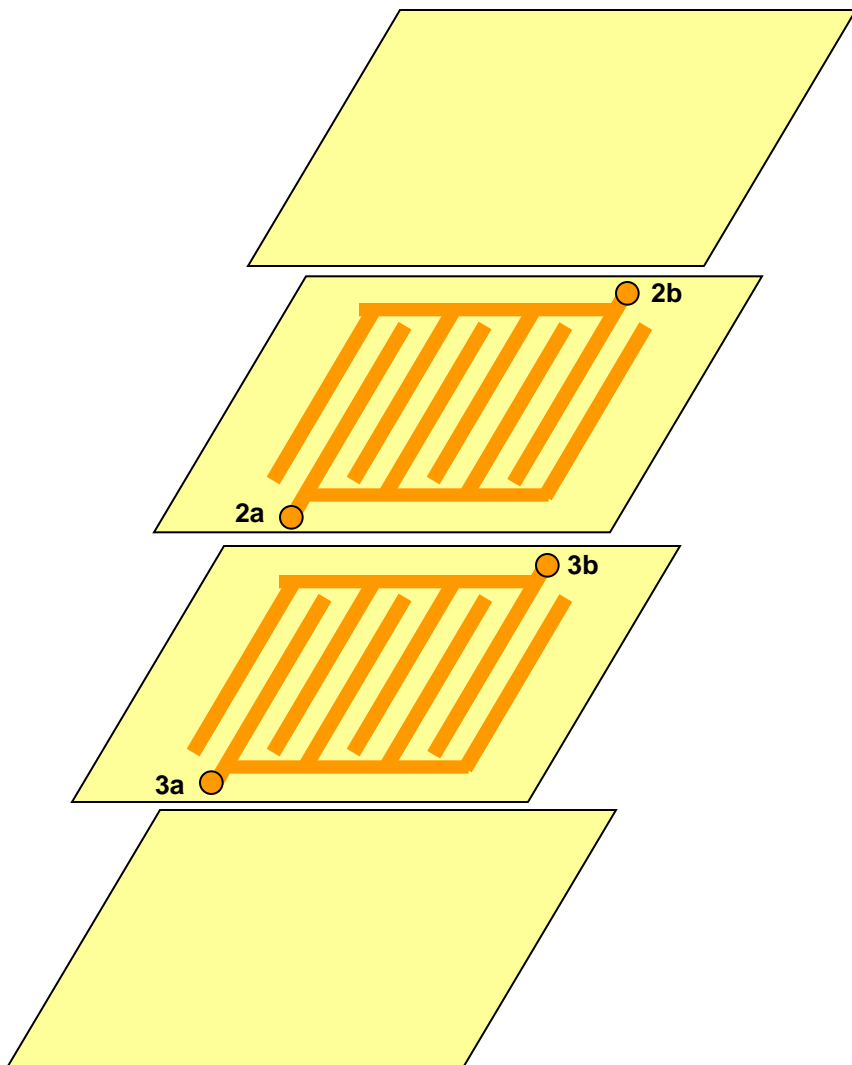


# Capacitance Conclusions

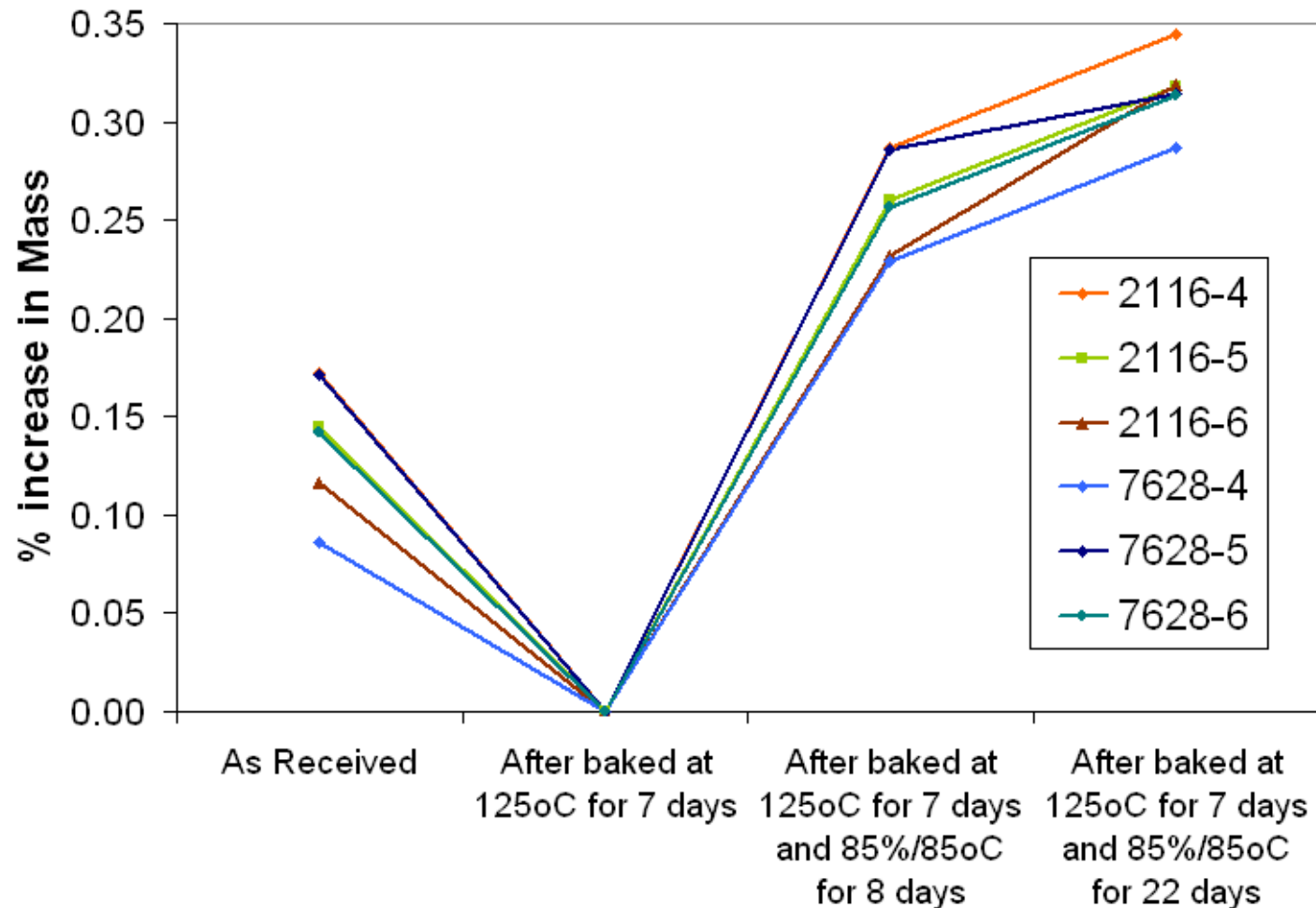
- Larger area cap show less change
  - Lower penetration of moisture



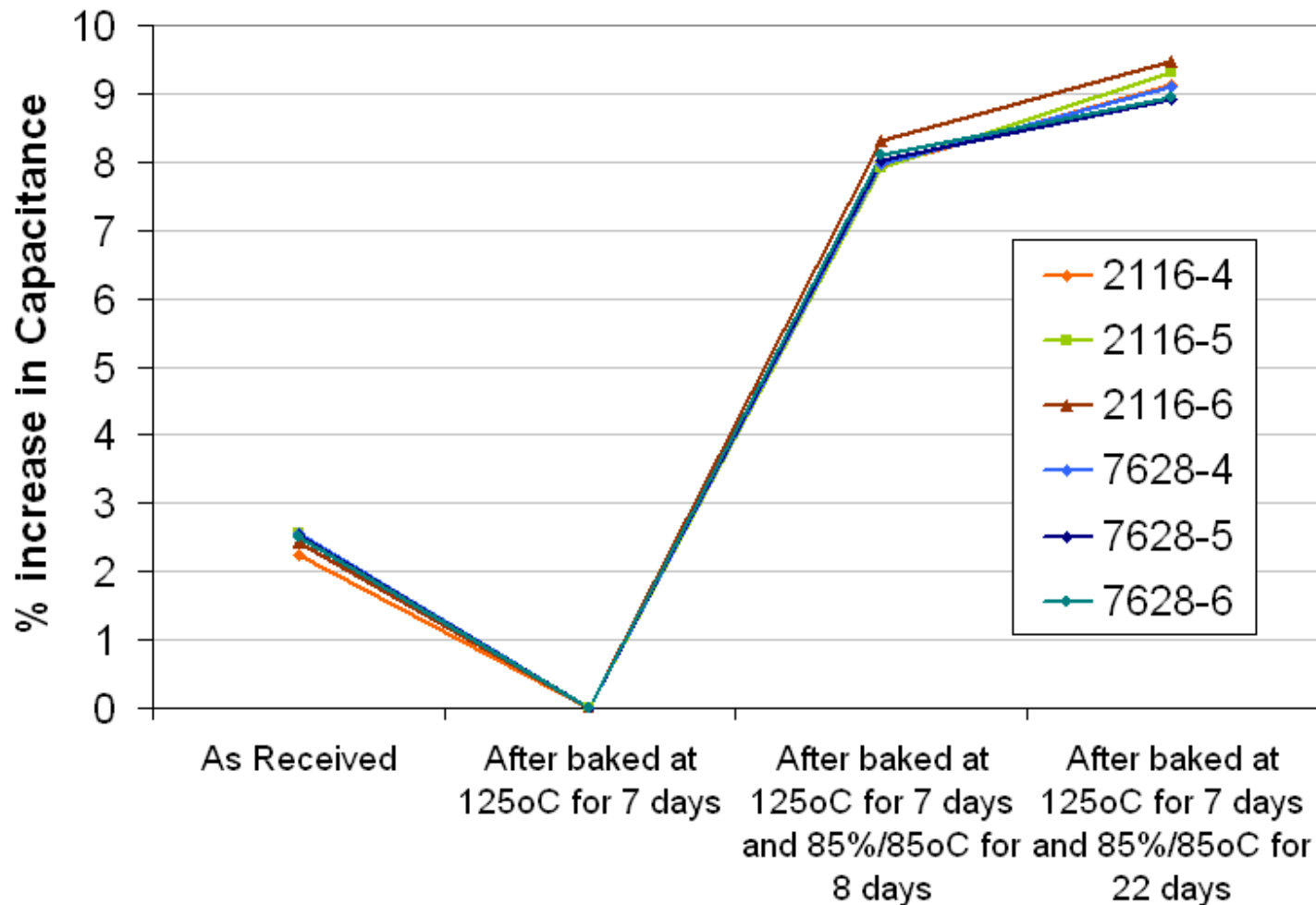
# Four layers PCB



# Interdigitated Plate Capacitors – Board Mass



# Interdigitated Plate Capacitors – $C_p@100\text{kHz}$



# Summary

- Increase in board mass of up to 0.35% over 3 weeks. Negligible change afterwards
- Capacitance increase approaches 10%.
- Larger area plate capacitors have less capacitance change – due to water ingress affecting the edge of capacitors only.
- Capacitance measurement shows no obvious distinction between board types.
- Capacitance increase much faster in interdigitated plate capacitors

# Route Impulse Energy Measurement

# RIE Measurement

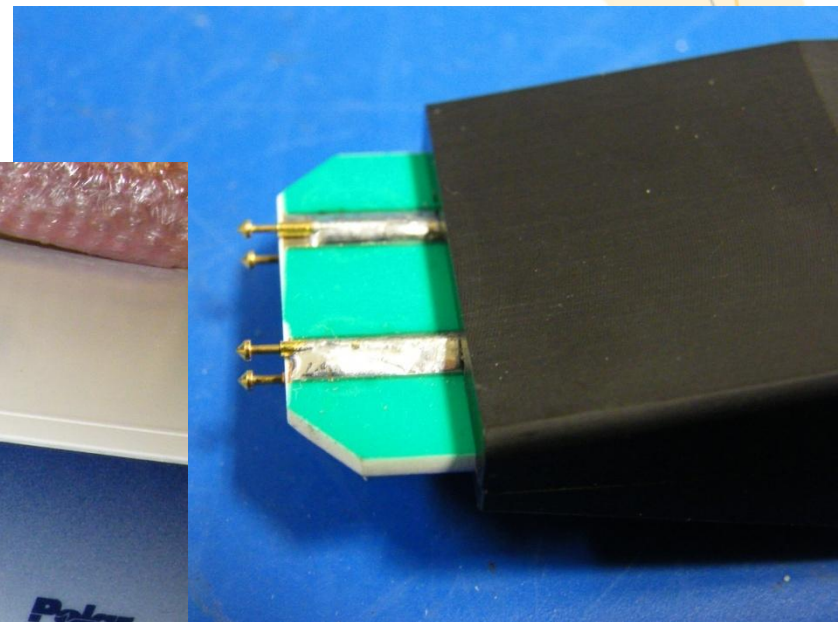
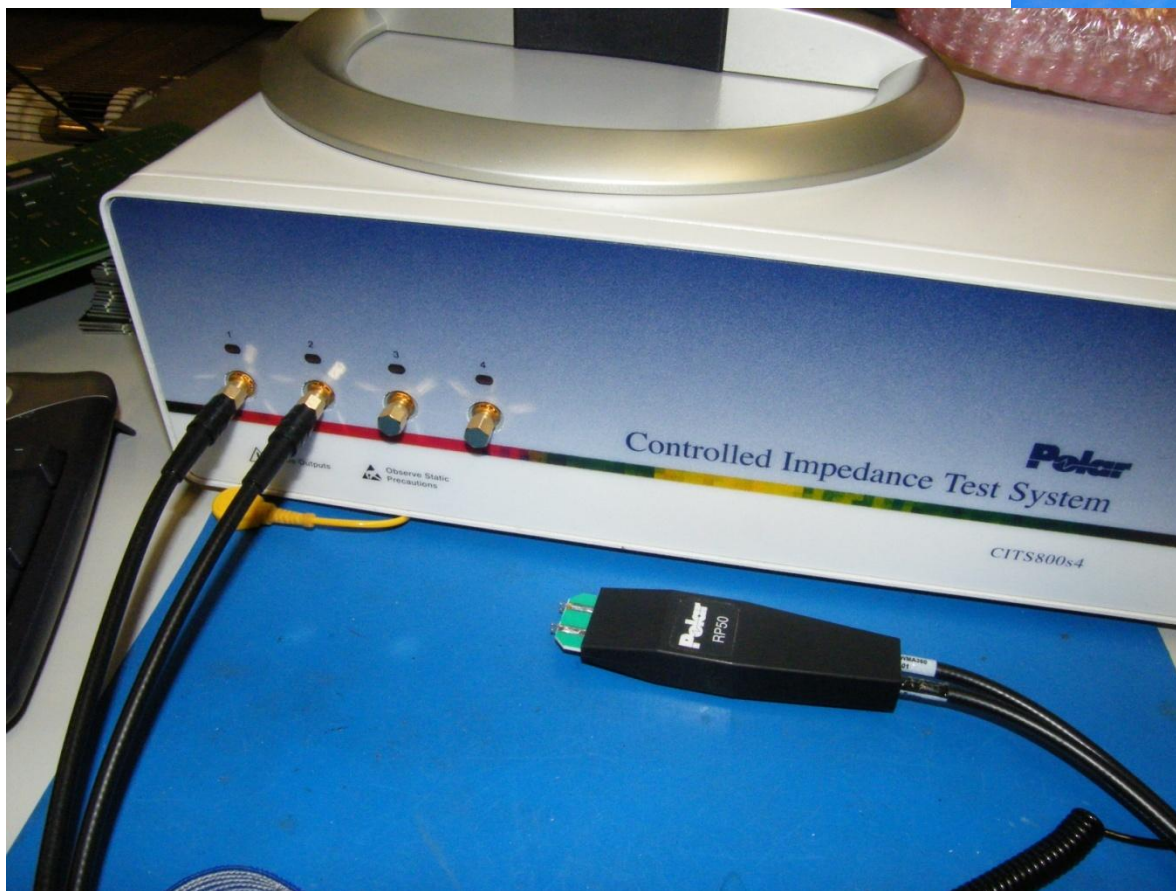
- Route Impulse Energy
  - Uses Time Domain Reflectometry (TDR) to measure the difference in loss between two identically constructed PCB transmission lines of different lengths
  - Longer test line & shorter reference line, both with far ends open circuited
  - Identical step pulses are injected into each line and reflected step pulses captured
  - Ratio between the energies contained in reflected step pulses is proportional to extra loss introduced by additional length of test line



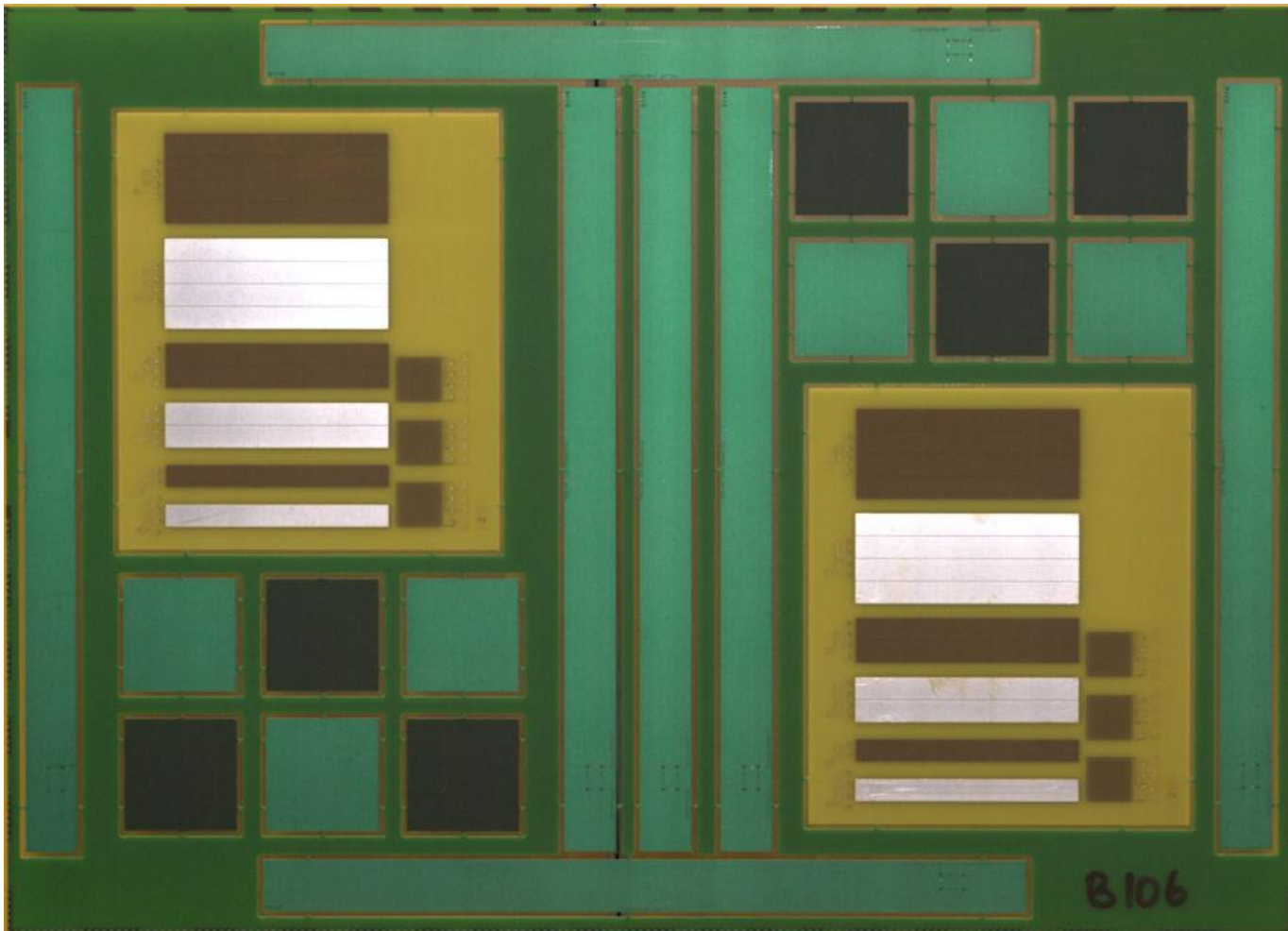
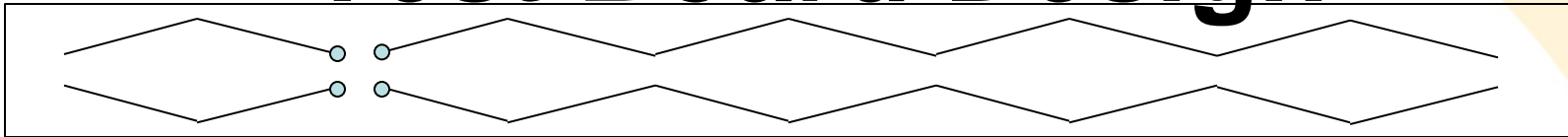
# RIE Measurement

- Increased moisture content of PCB causes increase in dielectric constant
- Increase dielectric constant causes in increases in signal losses
- Using existing PCB impedance measurement equipment with additional software

# RIE Equipment

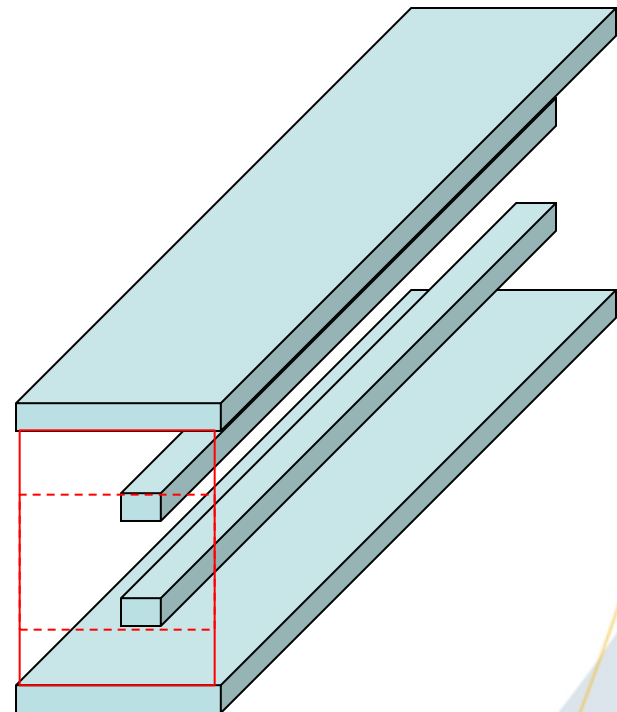


# Test Board Design

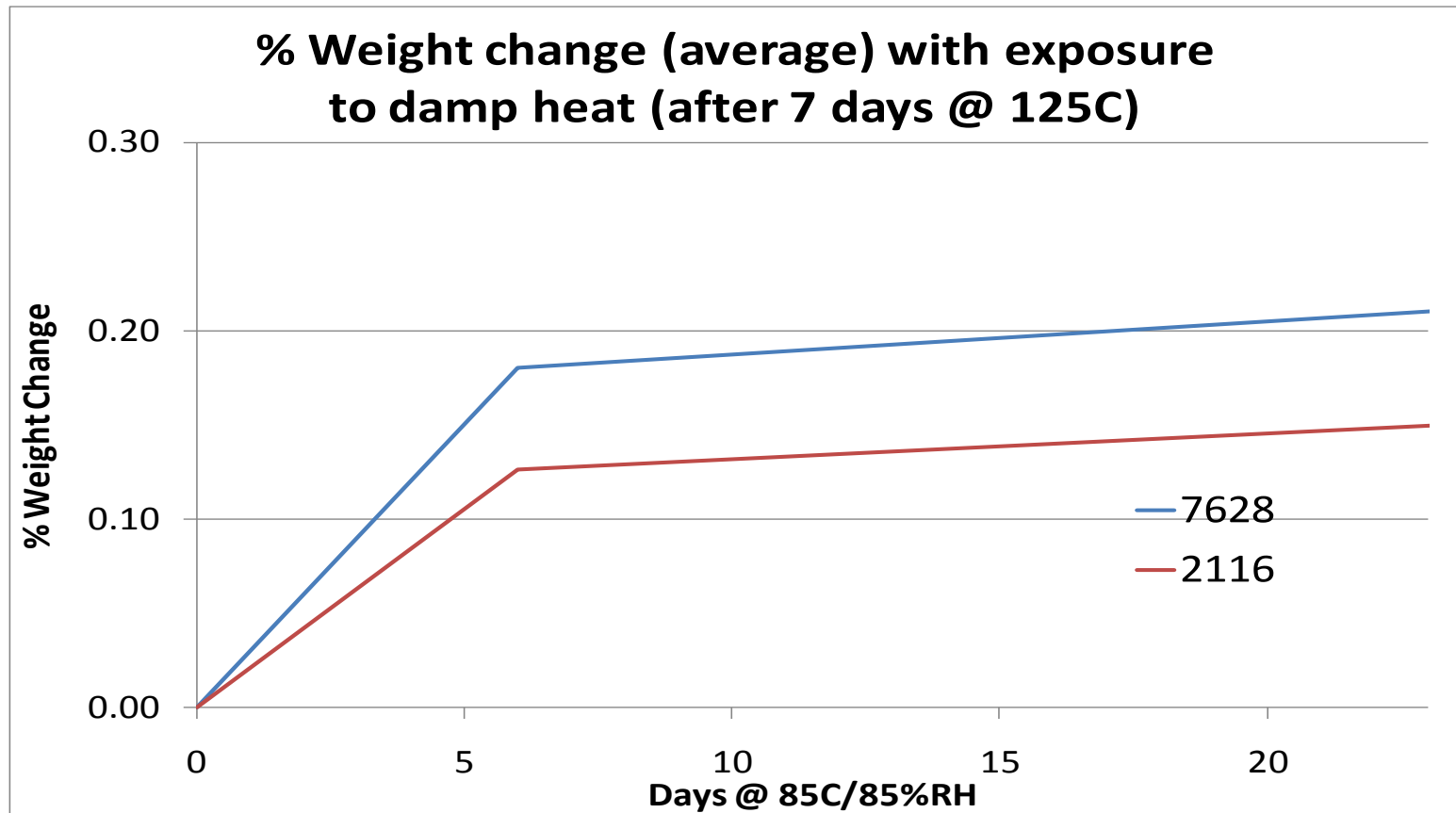


# RIE Phase 1 Measurement

- 4 layer test pattern
- Copper on outer layers
- Solder resist on top

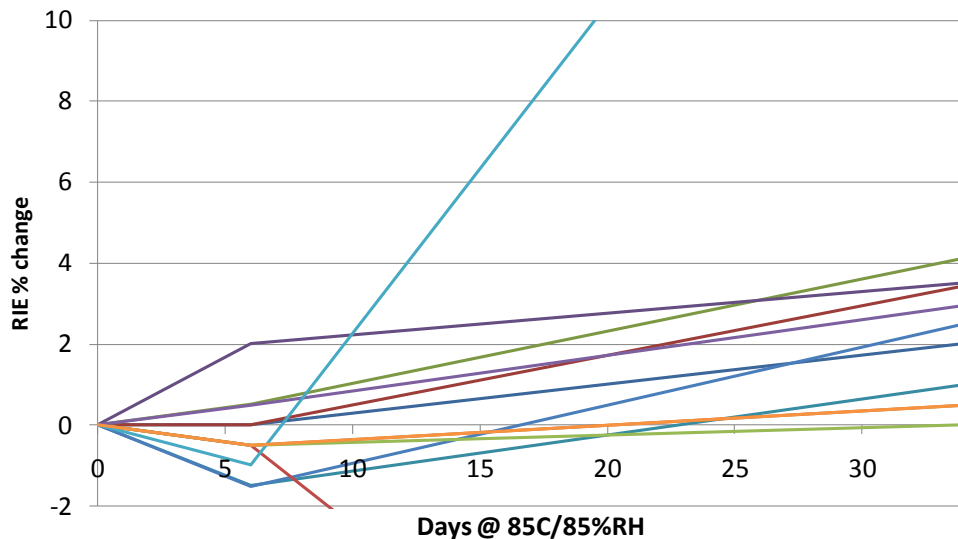


# Phase 1 Weight Gain

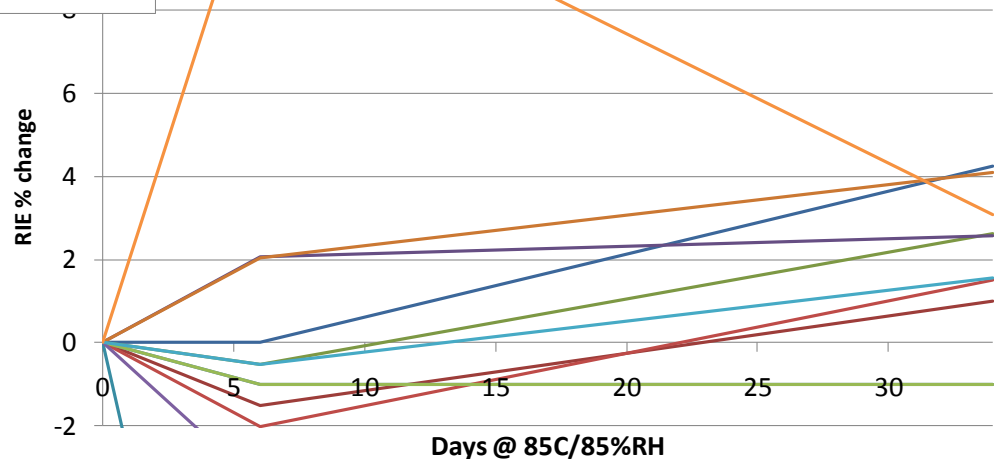


# Phase 1 RIE Comparison

% Variation of RIE with exposure to damp heat  
Material A (7628) (after 7 days @ 125C)



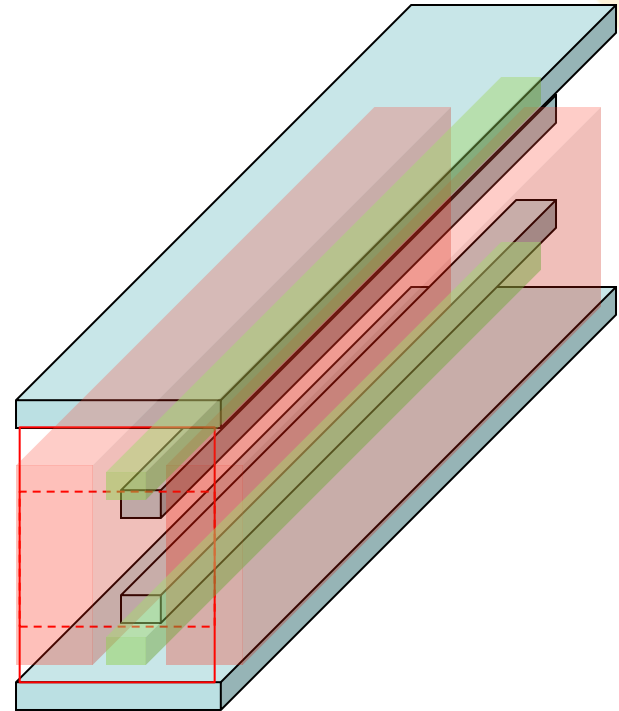
% Variation of RIE with exposure to damp heat  
Material B (2116) (after 7 days @ 125C)





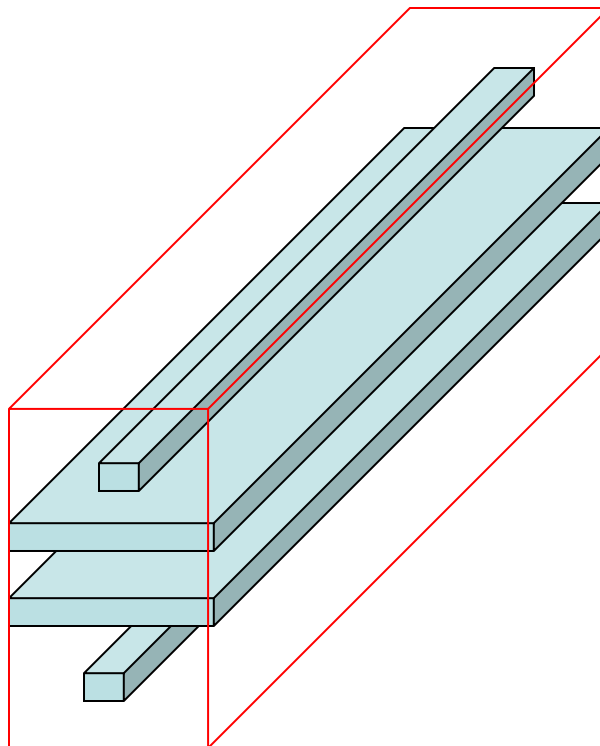
# RIE Phase 1 Measurement

- Moisture ingress occurring to side of signal lines, not between signal lines and ground planes



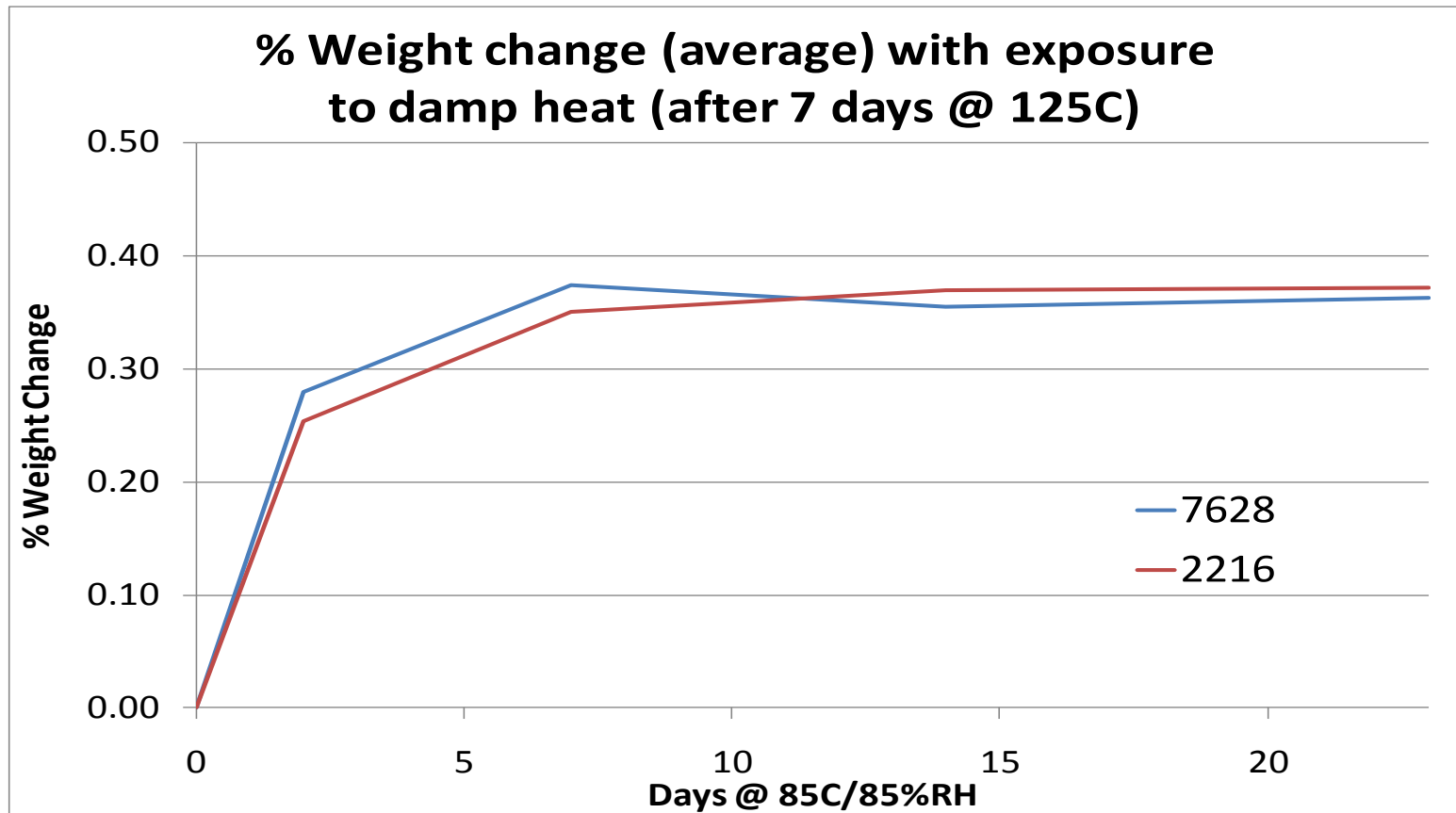
# Revised Test Board Design

- 6 Layer

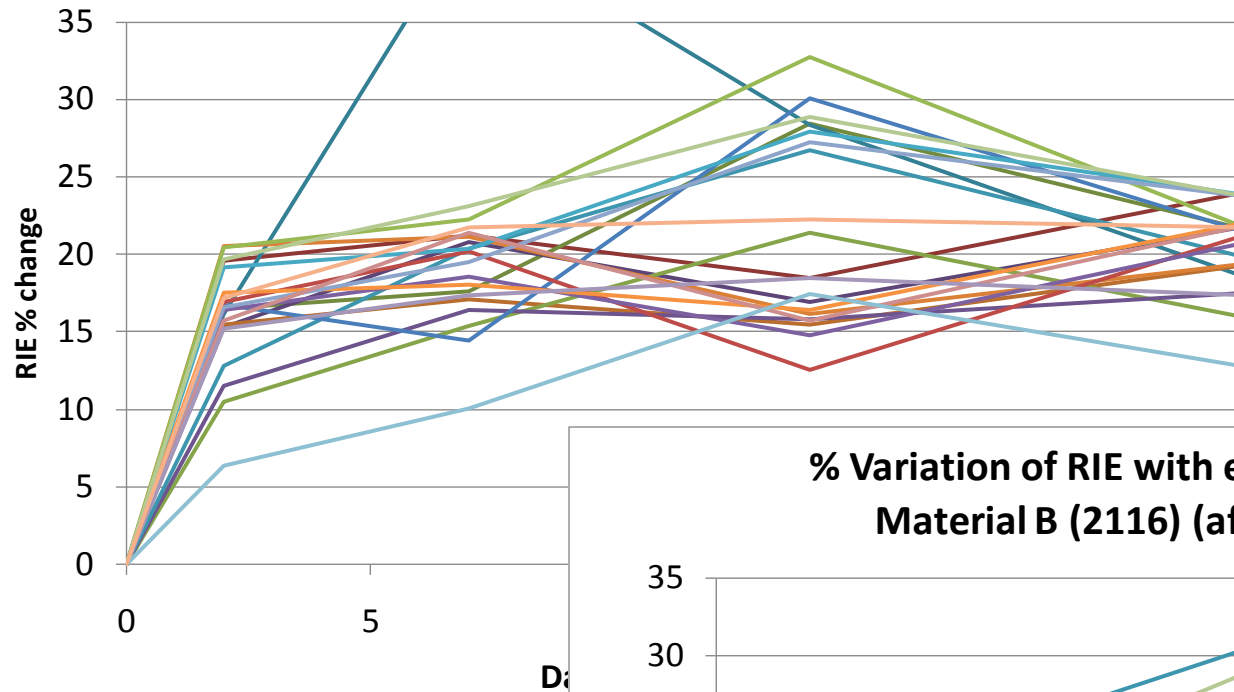




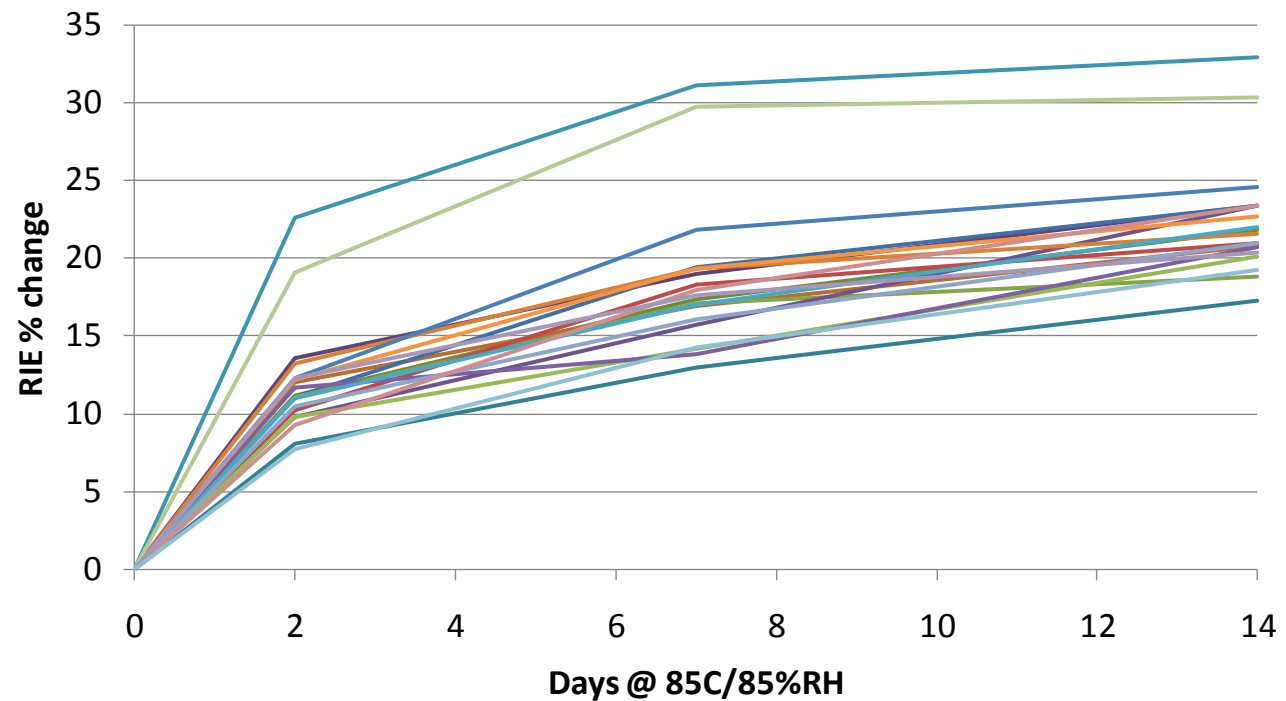
# P2A Moisture uptake



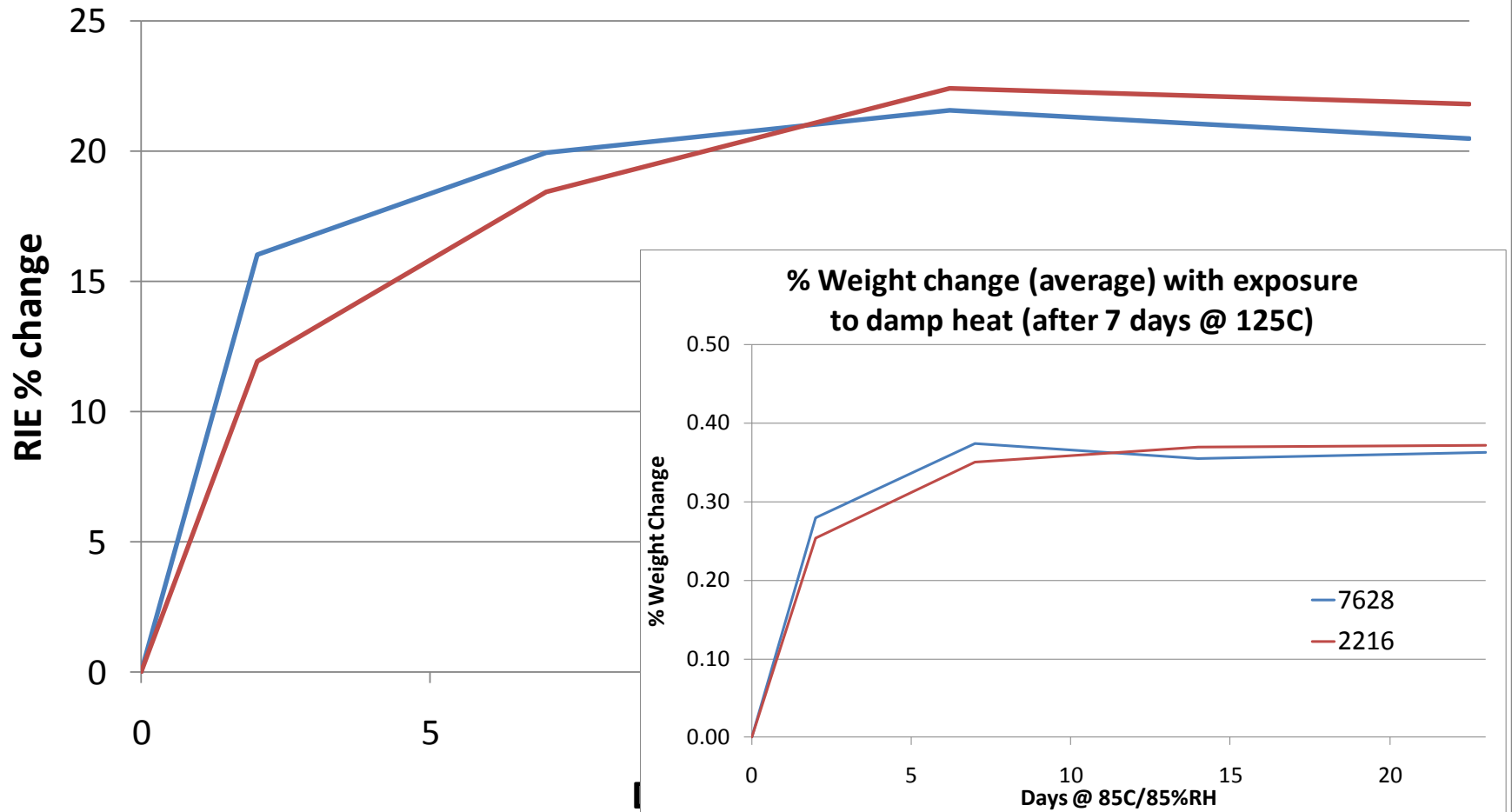
**% Variation of RIE with exposure to damp heat  
Material A (7628) (after 7 days @ 125C)**



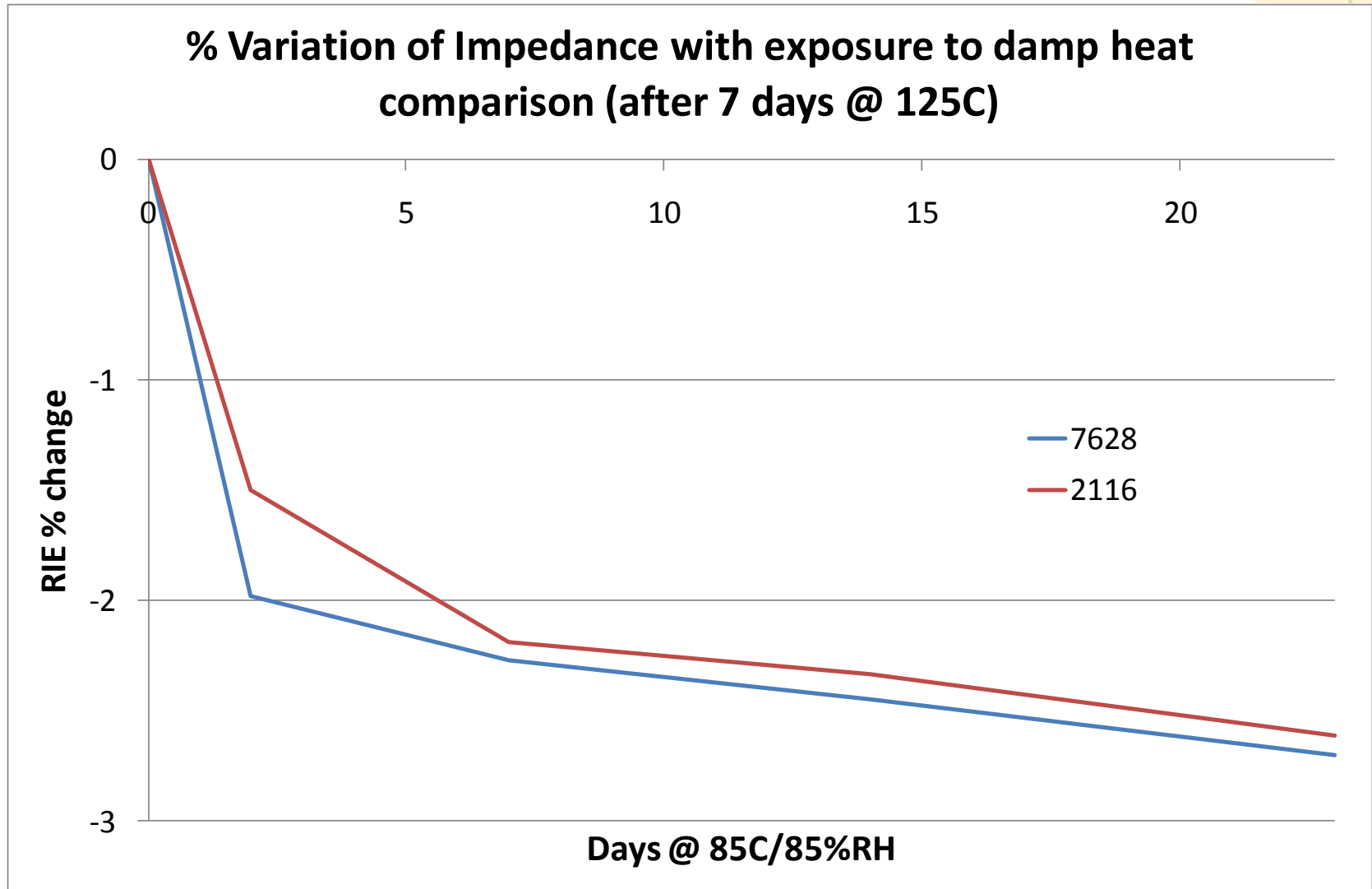
**% Variation of RIE with exposure to damp heat  
Material B (2116) (after 7 days @ 125C)**



## % Variation of RIE with exposure to damp heat comparison (after 7 days @ 125C)

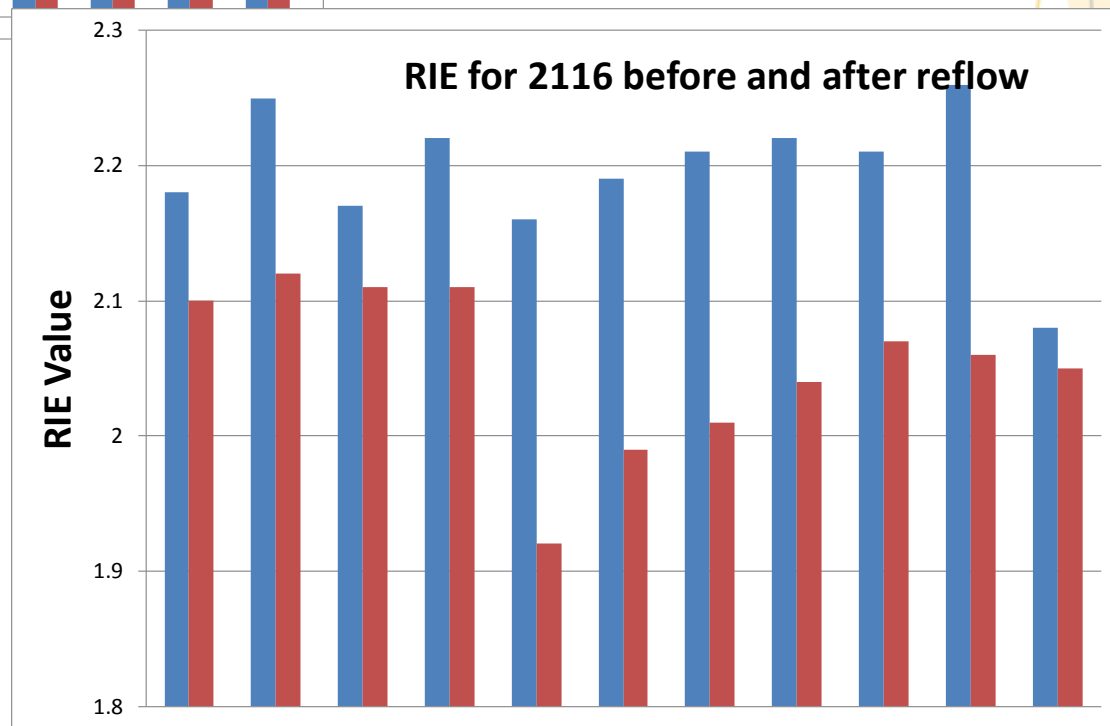
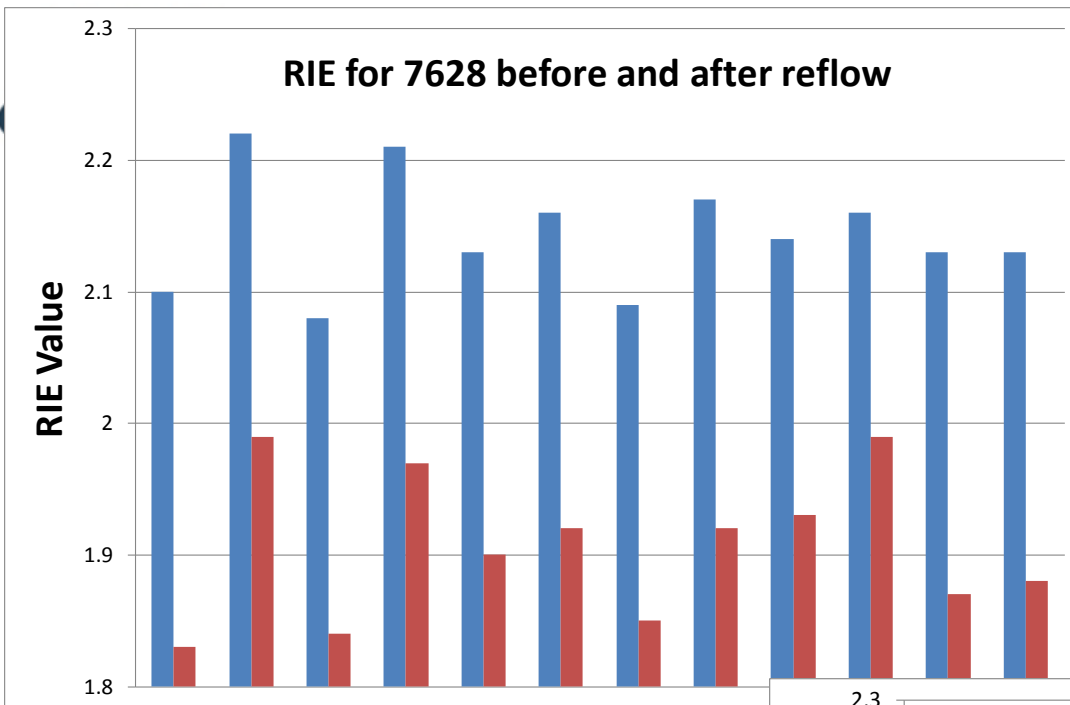


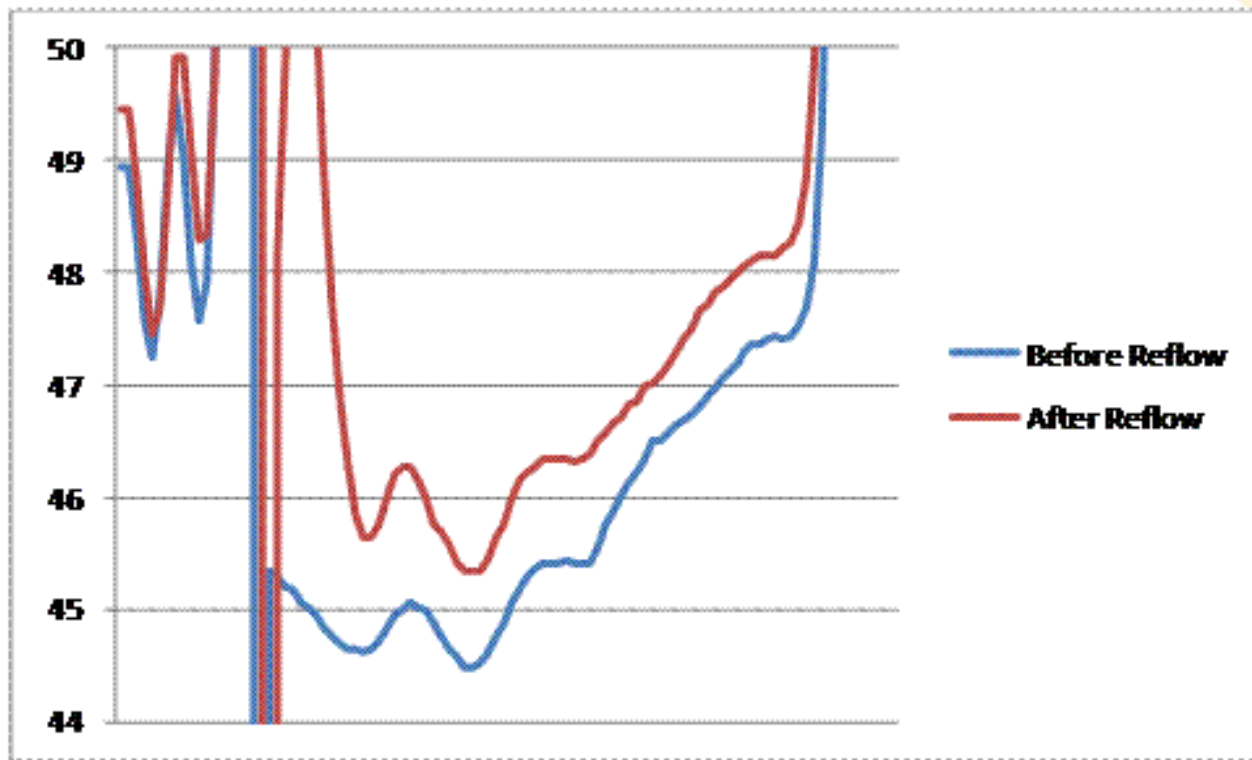
# Impedance

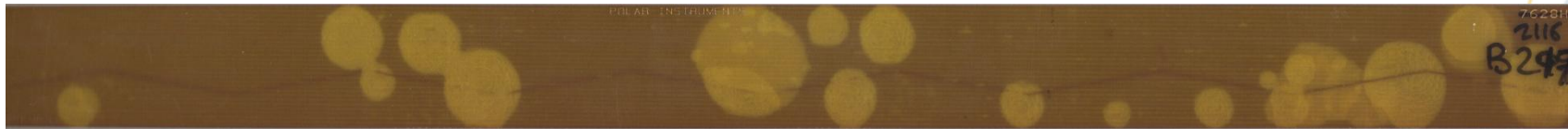
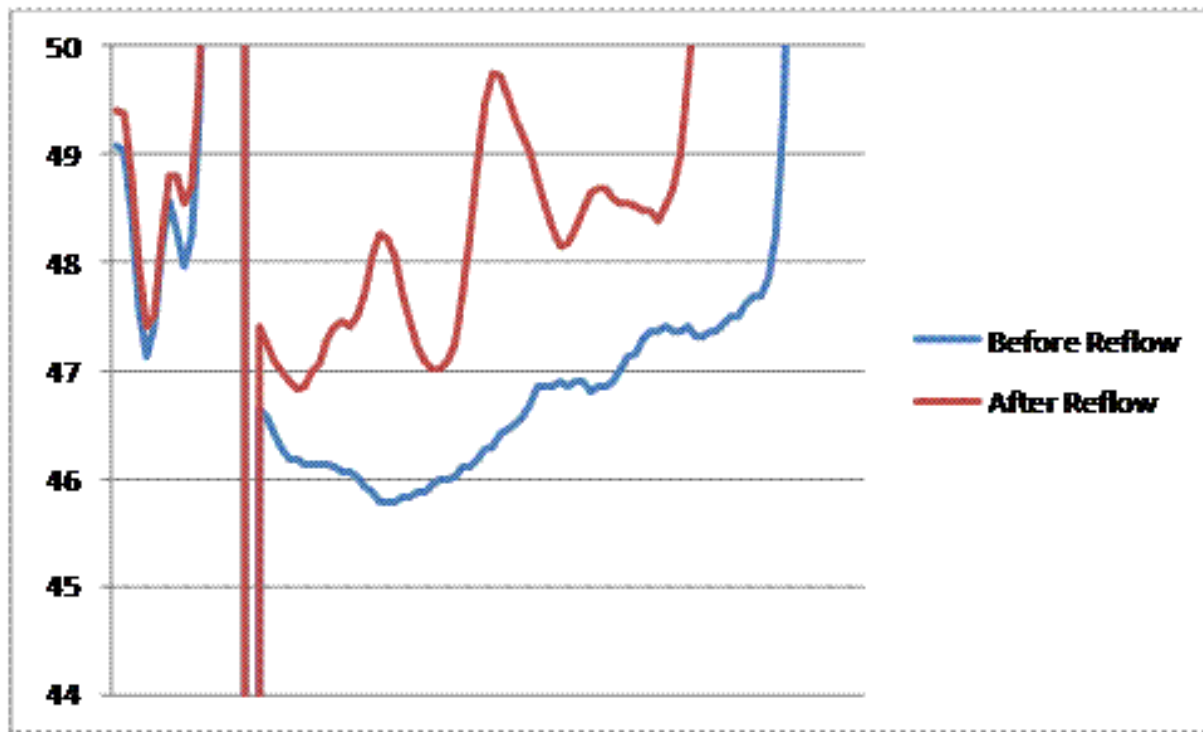


# Change in RIE after Reflow

- After 23 days damp heat ageing samples were subjected to single LF reflow profile (peak ~ 260°C)
- Some samples showed delamination
  - Visually worse for 2116
  - RIE values lower
    - PCBs now drier (corresponding weight loss)
  - Some correlation between delaminated areas and peaks in reflected signal









# RIE Summary

- Results show good correlation between RIE and moisture ingress
- Test pattern relatively large
  - Opportunities for size reduction?
  - Use of existing structures within PCB?
- Possible use for delamination measurement if delam occurs between signal line and ground plane

# Conclusions

- Both RIE and capacitance measurements are sensitive to changes in moisture content in the PCB, giving good single that can discriminate the moisture level in the board. The effect of one reflow is easily seen on drying a saturated board.
- RIE patterns have a geometry that facilitates easy inclusion into the break-off panel.
- Design of capacitance pattern is critical, and large solid plates act as excellent moisture barriers. A slotted design allows significantly faster moisture uptake and drying.
- Two prepreg styles were tested, 2116 and 7628, these did not show any significant difference in moisture uptake and drying.