

Thermal Effects on PCB Laminate Material Dielectric Constant and Dissipation Factor

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Abstract

Values for printed circuit board (PCB) laminate dielectric constant (Dk) and dissipation factor (Df) used in circuit design and signal integrity (SI) modeling are typically those presented on laminate maker datasheets. In most cases, these values are derived from measurements on samples which have not been exposed to thermal stresses representative of the printed circuit board (PCB) assembly process. This paper discusses the changes in Dk and Df values for a variety of laminate materials following simulated assembly thermal exposure of test vehicles to six SMT cycles at 260°C (Pb-free) or 225°C (SnPb eutectic). An additional concern arises around an effect of operating temperatures upon the effective Dk and Df of PCB materials. Due to thermal radiation from active IC devices, power supplies, etc., the operating temperature of PCBs within a network equipment chassis is typically higher than the 23-25°C value at which Dk and Df are measured and reported. This paper also describes the changes in Dk and Df observed when the test samples were measured at temperatures of 50°C and 75°C.

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3. Assembly Thermal Simulation and Dk/Df Effects
4. Elevated Operating Temperature and Dk/Df Effects

Introduction and Background

The dielectric constant (Dk) and dissipation factor (Df) of printed circuit board (PCB) laminate materials are affected by the proportions of certain raw materials (resin, fiberglass, and optionally, filler) present in the finished product [1-7]. During the production process at the material maker's factory, these components are exposed several times to elevated temperatures during the manufacturing process which yields finished pre-preg. Those pre-pregs, which are subsequently laminated into copper-clad core materials, are exposed to another thermal cycle in the laminating press, during which the resin component becomes cured.

In a PCB fabrication shop, the inner-layer circuit patterns are first imaged and etched onto core materials, and the etched cores and prepregs are stacked in the appropriate layer order. Then the fabrication shops use their own laminating press to cure the prepreg layers and yield a laminated multilayer panel. The lamination press temperatures, at both the material manufacturer and the board shop, are typically in the range of 180-185°C for FR4-class materials, and somewhat higher (185-215°C) for non-FR4 resin systems with low Dk and Df.

Industry-standard test methods for Dk and Df may be performed on either of two general classes of test vehicle: a) an individual copper-clad or unclad sheet of core material, or b) a finished bare printed circuit board. Test vehicles of either or both types are measured by the laminate maker, and the corresponding Dk and Df values are reported on the maker's product data sheets. In either case, the maximum temperature to which the test vehicle is exposed during manufacturing up to the time of test does not exceed the upper ranges (185°C to 215°C) noted above.

At the board shop, after the formation of the external circuit pattern, the panel undergoes an additional thermal excursion when coated with solder mask and cured in an oven. However, the maximum temperature in this process typically reaches 135-150°C, and thus does not approach the ranges already experienced during the lamination cycles. The board will be exposed to a higher temperature (250-260°C), if Hot Air Solder Level (HASL) surface finish is applied, but the duration of this excursion is quite short (a few seconds).

An actual PCB onto which components are soldered will be exposed to further thermal excursions during the assembly process. These temperatures may exceed those previously experienced by the PCB, reaching as high as 225°C for SnPb (eutectic) or

260°C (Pb-free) soldering processes. It is reasonable to assume that the fiberglass and inorganic filler components of the PCB base material will not be affected by these higher temperatures. However, the same assumption cannot be made regarding the organic resin components. While gross thermal degradation of mechanical properties may not occur, some slight degradation may be observable in the form of Dk and/or Df deviation from the initial values at room temperature.

With precise values of Dk and Df critical to optimal signal integrity (SI) in high-speed digital circuit designs [8], any deviation in Dk and/or Df from the planned values could lead to undesirable loss of SI margin and compromised performance. It is thus of interest to the high speed PCB/SI designer to know whether the Dk and/or Df of an assembled PCB may change as a result of the soldering process, so that the “real-life” values may be used during the simulation and modeling phase.

Test Vehicle and Dk/Df Extraction Method

A new algorithm for extracting Dk and Df from a single-ended balanced-stripline printed circuit board test vehicle by means of S-parameter measurements up to 20 GHz using a vector network analyzer (VNA) has been described in our previous papers [9, 10]. This technique is further referred to as the *Stripline S-parameter Sweep* (S3) test method.

A PCB under study should be at least a three-layer plane-signal-plane configuration, since it must contain a balanced-stripline signal layer. In the test vehicle under study, Layer 5 is the signal layer, as shown in Figure 1. The PCB may also contain an analogous structure, in which single-ended traces are replaced by differential pairs located on Layer 2. Therefore the actual test vehicle PCB in our work is a six-layer board with identical ground planes on Layers 1, 3, 4, and 6; single-ended traces on Layer 5 (impedance-tuned for 48, 50 and 52 Ω nominal); and differential pairs (96, 100 and 104 Ω nominal) on Layer 2. The length of the traces under test is 406 mm. To minimize stub lengths, connectors are mounted on Layer 1 when Layer 5 traces are to be tested, and on Layer 6 when Layer 2 traces are to be tested.

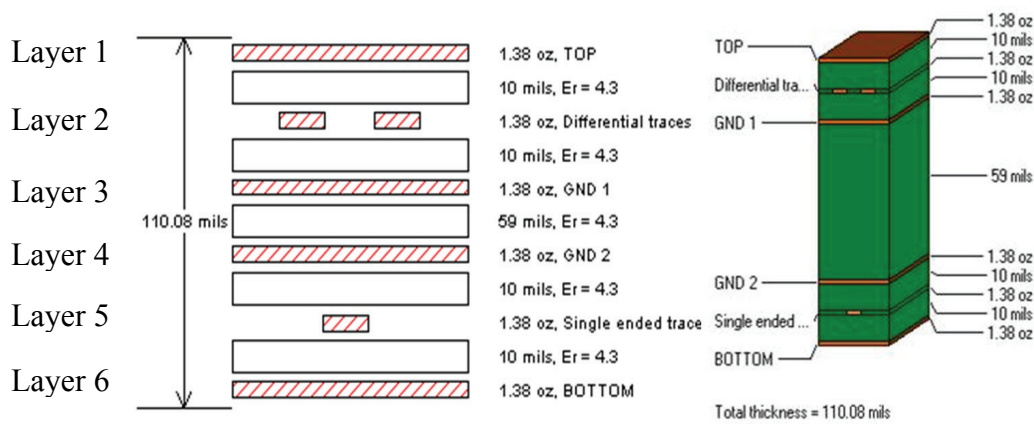


Figure 1
Generic stackup of the test PCB

The dielectrics between Layers 1-2 and 5-6 are prepregs chosen to target 50% finished resin content. As some prepreg resin is squeezed out of the panel during lamination, the resin content of the raw prepreg (as called out by the material maker) must be chosen at a slightly higher value. The typical material used is two plies of 2116 glass style with a 53-55% RC.

Copper-clad cores comprise Layers 2-3 and 4-5, chosen again to be as close as possible to 50% finished resin content, and with a glass ply stackup that matches the prepreg layers whenever possible.

The dielectric between Layers 3-4 consists of dummy prepreg material, whose thickness is chosen to build up the total thickness to 2.4 mm nominal, thus providing mechanical rigidity to the finished board. The type, number, and resin content of these prepregs may be chosen for best convenience and lowest cost, as they have no influence on the function of the traces under test.

The test vehicle PCB is finished in Electroless Nickel – Immersion Gold (ENIG) to provide a low surface contact resistance that will not degrade over time due to oxidation. The board is configured to accept press-fit SMA connectors which are mechanically mounted (not soldered) to the board. Alternatively, contact may be made directly to the SMA footprints using a microprobe station in a G-S-G configuration.

An advantage of the S3 test method is that it largely de-embeds the effect of conductor loss resulting from surface roughness of the stripline traces [9-11]. In this method, it is not mandatory to construct the sample from any specific type of copper foil. However, it is important to specify the foil type (Standard, VLP, RTF, etc.) clearly during procurement, so that the typical

values of surface roughness on the actual traces under test may be known or estimated in order to effectively separate conductor and dielectric loss. These values can be found by microsectioning one or more of the test boards (identical to those under investigation) and measuring the surface roughness using an optical or scanning electron microscope (SEM), as shown in Figure 2. Industry-standard terms defining copper roughness levels are specified in [1, 12].

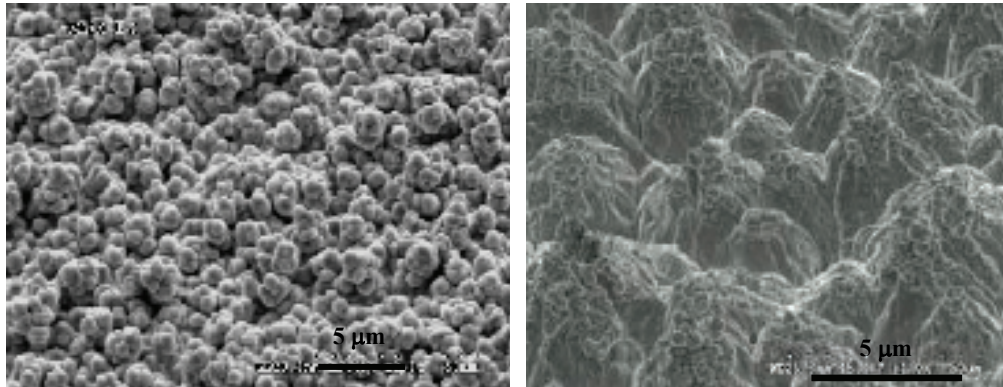


Figure 2
SEM image of typical Standard (right) and Low-profile (left) foil surfaces
(Courtesy Nanya CCL)

The VNA used in the S3 test method must be capable of obtaining the output S-parameters in Touchstone format (.s2p), and preferably has a maximum frequency capability 10% higher than the highest frequency of interest. The same requirement also applies to signal cables, SMA connectors, and a probe station, if used.

The test vehicle is designed with 50Ω-tuned calibration traces on layer 2 to permit use of the TRL (Through-Reflect-Line) calibration technique [10, 13]. If a given VNA does not support this calibration method, the conventional SOLT (Short-Open-Line-Thru) calibration technique may be used instead, requiring external reference standard loads (electronic calibration module, or a 50Ω air line) in most cases supplied by the equipment manufacturer.

Prior to VNA testing, target impedance limits of $\pm 10\%$ for the traces are validated by means of a time-domain reflectometer (TDR), or the VNA operating in TDR mode, if capable. This should be preferentially done at the PCB supplier prior to shipment. There are three single-ended test traces designed at 48, 50, and 52 Ω nominal to allow for tolerances in PCB manufacturing and selecting of the trace with impedance closest to the 50Ω target.

After calibration, S-parameters are extracted by sweeping frequency from DC up to the highest frequency of interest (e.g., 15-20 GHz), typically in 50 MHz increments. To minimize the repeatability error and the noise error, the VNA is set up to perform multiple (16 total) sweeps in succession and display the average values. Furthermore, at least three physical sample boards are tested, the maximum deviation between the three sets of measurements is verified to be acceptable, and the average values for all three boards are reported. The quality of the launch is verified by examining the frequency dependence of the return loss magnitude $|S_{11}|$. It is desirable to obtain a return loss magnitude not worse than -25 dB at any point within the target frequency range.

The .s2p output file, containing several thousand discrete points, is then passed to a Matlab algorithm, which extracts Dk and Df values from phase and $|S_{21}|$ loss data, as described in the authors' previous paper [9, 10]. The final output product is thus curves for Dk and Df over the frequency range of interest.

Assembly Thermal Simulation and Dk/Df Effects

The S3 test method differs in many ways from the various pre-existing industry-standard test methods for Dk and Df measurements [14], mainly based on narrowband resonator techniques (e.g., Parallel Plate, Two Fluid Cell, Split Post Cavity Resonator, IPC X-Band Stripline, Bereskin Stripline, and Full Sheet Resonance methods) [2, 15-17]. In particular, the S3 method makes use of traveling waves in a PCB-like structure across a wide frequency range, while resonator techniques employ standing waves in a copper-clad or unclad dielectric structure, and are narrow-band, confined to the specific resonant frequencies of the test fixtures used. However, neither class of method has been widely applied to extraction of Dk and Df of dielectric substrates using test vehicle PCBs exposed to the higher temperatures of the assembly process. So far, only limited attention has been paid in literature to this problem, though this question is of great importance for the present-day PCB industry.

The authors are not the first to examine the effects of operating temperature upon PCB material Dk and Df. However, the published works have either been derived from resonator-based test methods [2, 18], or have dealt with frequency spans well below the GHz range, when measurements were carried out using low-frequency impedance analyzer techniques [19, 20]. Though some laminate manufacturers provide data on Dk and Df vs. temperature, such data for frequencies above 10 GHz may be available only for specialty microwave materials, and only at a few frequency points as obtained using resonator test methods [2, 14-18].

Test vehicles as shown in Figure 3, constructed for this work and described in the aforementioned papers [9-11], were first measured at ambient temperature ($23\pm 1^\circ\text{C}$) to obtain baseline values for Dk and Df. Then the boards were exposed to SMT assembly conditions by passing through a reflow oven (Heller, Model 1800EXL), using a representative thermal profile shown in Figure 4. The samples were then re-measured, and changes in Dk and Df were recorded.

The maximum temperature was set at $260 \pm 5/-0^\circ\text{C}$ for those materials rated as Pb-free-compatible (per the laminate manufacturer's data sheet), and at $225 \pm 5/-0^\circ\text{C}$ for materials rated only for eutectic soldering. The time-above-liquidus (TAL) was set at 85 ± 5 seconds to simulate actual conditions on high-complexity products.

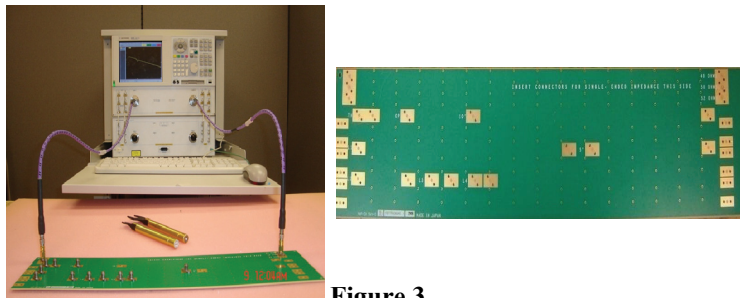


Figure 3
PCB test vehicle for extraction of Dk and Df attached to Agilent E8364B PNA

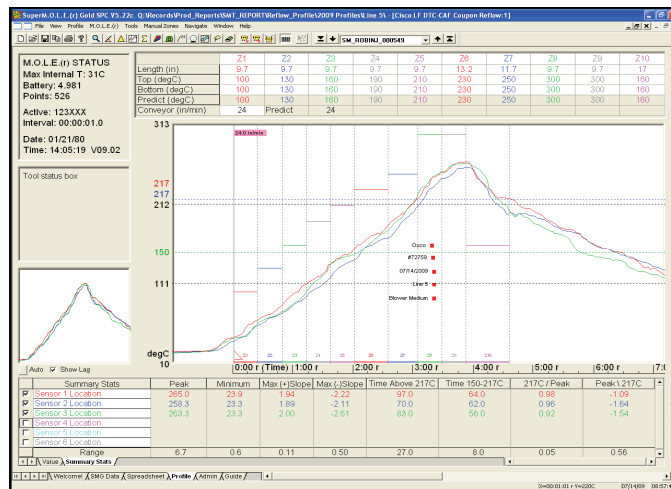


Figure 4
Thermal profile for eutectic assembly simulation

The total thermal exposure consisted of six passes through the SMT oven using the selected profile. A typical product undergoes two SMT passes and one wave-soldering step. However, in any large population of assembled PCBs, some proportion will require rework and repair. Moreover, in cases where a grid-array device or a high-mass device is involved, significant areas of the PCBs will be exposed to an additional thermal cycle to remove the suspect device. Following troubleshooting, another cycle will then be needed to re-attach the original device, or a replacement. Therefore, six cycles were considered to be a reasonable surrogate for the worst-case total thermal exposure likely to be experienced by production boards.

The selection of sample materials was made based on the most widely-used classes of resin system available within our existing materials library. One representative material from each class was chosen as detailed in Table 1, with either Pb-free, or eutectic thermal profiles applied.

Table 1
PCB material classes selected for test

Code	Material Type Description	Pb-free?
A	FR4, High-Tg, Dicy-cure, unfilled	No
B	FR4, High-Tg, Phenolic-cure, filled	Yes
C	Cyanate-ester + FR4 blend, unfilled	No
D	Modified FR4, mid-range Dk/Df, unfilled	No
E	FR4, halogen-free, filled	Yes
F	Non-FR4, mid-range Dk/Df	Yes
G	Non-FR4, low Dk/Df	Yes

The Dk and Df of the tested materials before and after the thermal cycling are shown in Table 2. While the S3 method yields Dk and Df data in the frequency range 50 MHz-20 GHz, the specific values in the table below shown were obtained at 10 GHz.

Table 2
Dk and Df values (10 GHz) before and after 6x thermal exposure, and percent change.

Code	Dk Before	Dk - After	% Chg	Df - Before	Df - After	% Chg
A	4.145	4.149	0.02%	0.0177	0.0179	1.13%
B	4.436	4.439	0.06%	0.0237	0.0239	0.84%
C	3.851	3.857	0.16%	0.0120	0.0124	3.33%
D	3.885	3.886	0.02%	0.0179	0.0182	1.68%
E	4.209	4.219	0.24%	0.0145	0.0158	8.97%
F	4.075	4.047	-0.69%	0.0104	0.0103	-0.96%
G	3.840	3.842	0.05%	0.0075	0.0077	2.67%

All the materials, except F, showed some level of increase in Dk following the thermal exposure. All the materials demonstrated a reasonable level of stability, as the repeatability error margin for the specific network analyzer used (Agilent PNA E8364B) is in the range of 0.5% [13]. The sample of Material F showed a decrease in Dk. This indicates that the prepreg resin might not have been fully cured during the PCB manufacturing process, as the additional thermal cycles of the assembly simulation may have advanced the resin cure, thus lowering the Dk.

Df results showed that most of the samples maintained a reasonable level of stability, except for Material E, whose nearly 9% magnitude of change in Df would be large enough to cause reconsideration of SI margining in sensitive circuit designs. Material C with an increase in Df of over 3% would also be of concern. Material G also demonstrated a larger-than-average change, but given that its Df is the lowest in the group, repeatability noise would potentially play a larger role than with materials having higher Df values. Material F's Df behavior was similar to that observed with its Dk. The fact that both Dk and Df values decreased after thermal exposure supports the hypothesis that the resin was not completely cured during manufacturing.

Elevated Operating Temperature and Dk/Df Effects

Larger form-factor high-performance network equipment typically incorporates a user-configurable selection of circuit cards, which are mated to a backplane PCB within an enclosed chassis. By contrast, smaller form-factor products feature one or two cards in a flat metal case, a so-called "pizza-box" configuration. In either case, thermal management of the chassis is typically achieved through active ventilation. One or more fans direct ambient air across the operating circuit assemblies, which are equipped with a number of heatsinks as required. The heated air is thus exhausted out of the enclosure.

Several classes of components mounted on these PCBs, particularly high-speed ICs and board-mounted power supplies, can generate considerable levels of heat during normal operation. As no chassis is perfectly efficient in ventilation, the areas of the PCB underneath or near such components inevitably reach operating temperatures greater than those of the typical ambient

central-office or data center environments (20-25°C). The effect of these higher temperatures upon Dk and Df of the PCB material should be taken into consideration.

For this phase of the investigation, the above-mentioned thermally-stressed test vehicles were placed in a temperature-controlled environmental chamber and allowed to equilibrate at 50±1°C. After the VNA cables were attached, the temperature was restabilized. Then the calibration was executed, and the S3 test method was applied to extract Dk and Df values. The process was then repeated with the chamber temperature increased to 75±1°C.

It should be noted that for differential temperature measurements the TRL is preferred over the SOLT calibration. The reason is that the TRL calibration structures are built into the PCB under test, so the calibration is properly carried out at the required temperature. This allows for de-embedding effects associated with heating of SMA connectors and cables. The SOLT calibration requires the use of an external standard, which is typically manufacturer-rated for operation only at room temperature. If the SOLT calibration is necessary, differential temperature effects can be minimized by selecting high-quality cables and connectors known to have high thermal Dk/Df stability. Also, temperature effects can be quantified by connecting the two SMA connectors across a dummy load (omitting the test PCB) and examining S-parameter changes at temperatures of interest.

It is useful to further clarify the advantages of using TRL calibration over conventional SOLT calibration. When the test vehicle is exposed to elevated temperatures, the material parameter extraction algorithm proposed in [9, 10] allows for introducing corrections. One correction will take into account the decreased copper conductivity as a result of heating of the structure. It is known that the conductivity of copper in the temperature range of interest decreases almost linearly with the temperature coefficient of about 0.3936% per °C [21]. The other source of potential error in determining dielectric parameters is associated with an additional phase shift at zero frequency because of the thermal expansion of the line's physical dimensions. The algorithm [10, 11] can correct for this, as well. Also, "in situ", i.e., when the test vehicle is heated, the TRL calibration is able to de-embed thermal effects upon port conductors. However, SOLT calibration may be carried out only at non-elevated temperatures, so heating of ports cannot be compensated out by the SOLT procedure.

The effect of elevated operating temperatures on Dk and Df values is demonstrated in Table 3. The data for 23°C (room temperature) is the same as in Table 2.

Table 3
Dk and Df values at 23°C, 50°C, and 75°C; and percent change between 23°C and 75°C

Code	Dk, 23°C	Dk, 50°C	Dk, 75°C	Δ, 23-75°C	Df, 23°C	Df, 50°C	Df, 75°C	Δ, 23-75°C
A	4.149	4.189	4.222	1.76%	0.0179	0.0198	0.0223	24.6%
B	4.439	4.505	4.534	2.14%	0.0239	0.0279	0.0323	35.1%
C	3.857	3.860	3.874	0.44%	0.0124	0.0137	0.0152	22.6%
D	3.886	3.926	3.928	1.08%	0.0182	0.0204	0.0227	24.7%
E	4.219	4.585	4.598	8.98%	0.0158	0.0169	0.0187	18.4%
F	4.047	4.254	4.265	5.39%	0.0103	0.0120	0.0128	24.3%
G	3.820	3.825	3.830	0.26%	0.0077	0.0081	0.0082	6.49%

The Dk values for materials C and G were quite stable over the temperature range, increasing by less than 1%, while material E showed a nearly 9% increase.

However, the Df results presented an entirely different picture. Even the best performer, material G, showed a 6.5% rise in Df, while the other six all increased by double-digit percentages, with material B showing an increase of over one-third.

These results show that at the stage of SI modeling, circuit designers contemplating use of such materials should account for significantly higher Dk and Df values than those at room temperature. Localized "hot spots" on a PCB could have various detrimental effects on SI performance. If certain channels of a parallel bus were to pass through hotter areas of the PCB, significant skew of differential pairs and bus timing errors could appear. Increased Dk values due to the higher temperature would cause a delayed transit time on lines passing through hotter areas of the PCB [15].

Also, since elevated operating temperatures for the PCB materials tested result in higher Df compared to the room-temperature values, greater channel loss and additional frequency dispersion are expected. This too should be taken into account at the SI modeling stage.

It should be noted that variations in Dk and Df with temperature are reversible at the relatively low temperatures of 50°C and 75°C. However, at the higher temperatures resulting from the assembly thermal exposure, the changes in Dk and Df are not reversible, due to the permanent alteration of the polymeric structures of the resin at the molecular level.

Further Work

Beyond the seven classes of PCB materials represented in Table 1, an additional six laminate resin types of potential interest have been identified, and these will be characterized in the near future.

An adjacent area of research will be to investigate the effects of atmospheric moisture absorption by the PCB laminate material. It is well-known that presence of moisture within the resin matrix may increase Dk and Df, as is demonstrated in [22-24]. However, the measurements in this work were carried out using resonator-based narrowband methods, which give results only at specific frequency points.

Moisture absorption is rarely an issue in standard office network equipment, as the environment is typically under fairly stringent temperature and humidity control. However, concerns would arise with equipment intended for outdoor operation, including mobile/portable devices for field use. The current test vehicle design is largely immune to moisture effects due to the external layer surface area being more than 99.9% clad in copper, and the test traces being recessed far from the edges of the board. An alternative version has been designed, in which the external copper shielding has been removed, exposing the base material to the atmosphere. The traces on the resultant board thus become embedded microstrips rather than striplines. The samples are first baked dry to obtain a baseline measurement. Then they are exposed to relatively high humidity until saturation is reached, and measured again. The differential effect of solder mask as a partial moisture barrier can be evaluated by plotting Dk or Df vs. exposure time for boards with and without solder mask applied.

Summary

A non-resonator VNA-based test method (S3) was applied to study of thermal exposure effects on electrical performance of stripline PCBs. The PCB test vehicles that were previously used for extracting Dk and Df values of substrate dielectrics at standard environmental conditions (23°C; <50% RH) were exposed to simulated Pb-free and eutectic PCB assembly conditions, and then re-measured to determine if the thermal exposures induced changes in Dk and Df. Seven test sets were used, each representing a different class of PCB laminate material. The majority of materials demonstrated acceptable stability (minimal change) in both Dk and Df following the thermal exposure.

The same test vehicles were then placed in a temperature chamber, the Dk and Df values extracted at operating temperatures of 50°C and 75°C, and compared to the prior room-temperature measurements. Over an approximately 50°C span, the majority of materials displayed reasonable levels of stability in Dk, but all samples exhibited notable increases in Df values, some of which were unexpectedly large.

Conclusion

Typically, Dk and Df values given on vendor data sheets represent products in raw material form (laminate and prepreg prior to PCB manufacturing steps), which are not necessarily representative of finished PCB assemblies that have undergone multiple thermal exposures. Furthermore, the base material of a functioning PCB assembly operating at temperatures higher than ambient may experience a further effective increase in Dk and Df, additive to any permanent changes resulting from the assembly thermal exposure.

These findings suggest that for high speed circuit designs/layouts which are SI-margin-challenged, Dk and Df should be examined beyond the published “raw material” reference figures. Values more representative of finished PCB assemblies, operating at intended-maximum temperatures, should be utilized in design simulations and SI margin estimations.

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Biographies

Scott Hinaga holds the position of Technical Leader in Cisco's PCB Technology Group, and is responsible for investigation and characterization of new laminate materials. He holds a B.S. from Stanford University, joined Cisco in 2004 and has PCB manufacturing and engineering management experience dating back to 1985.

Marina Y. Koledintseva, Ph.D., has been a Research Professor at the Missouri University of Science and Technology, Electrical and Computer Engineering Department, since 2000. Before that she was a Senior Scientist and Associate Professor of Radio Engineering Department of Moscow Power Engineering Institute (Technical University), Moscow, Russia.

James L. Drewniak, Ph.D., since 1991 has been a Professor with the Missouri University of Science and Technology (MS&T), formerly known as UMR, Electrical and Computer Engineering Department. In 1995-2008 he was the co-director of the EMC Laboratory and the EMC Consortium. In 2002-2007 he was the Director of the Materials Research Center of the same University.

Amendra Koul has been a graduate student (M.S.) with the EMC Laboratory of Missouri University of Science and Technology since 2007. He holds a B.Tech in Electronics and Communication Engineering from Vellore Institute of Technology, Tamil Nadu, India. Currently he is on a co-op/intern with Cisco Systems, San Jose, California.

Fan Zhou has been a graduate student (M.S.) with the EMC Laboratory of Missouri University of Science and Technology since 2008. He has a M.S degree in Electrical Engineering from Beihang University, Beijing, China.

Thermal Effects on PCB Laminate Material Dielectric Constant and Dissipation Factor

Scott Hinaga

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When PCB materials are...

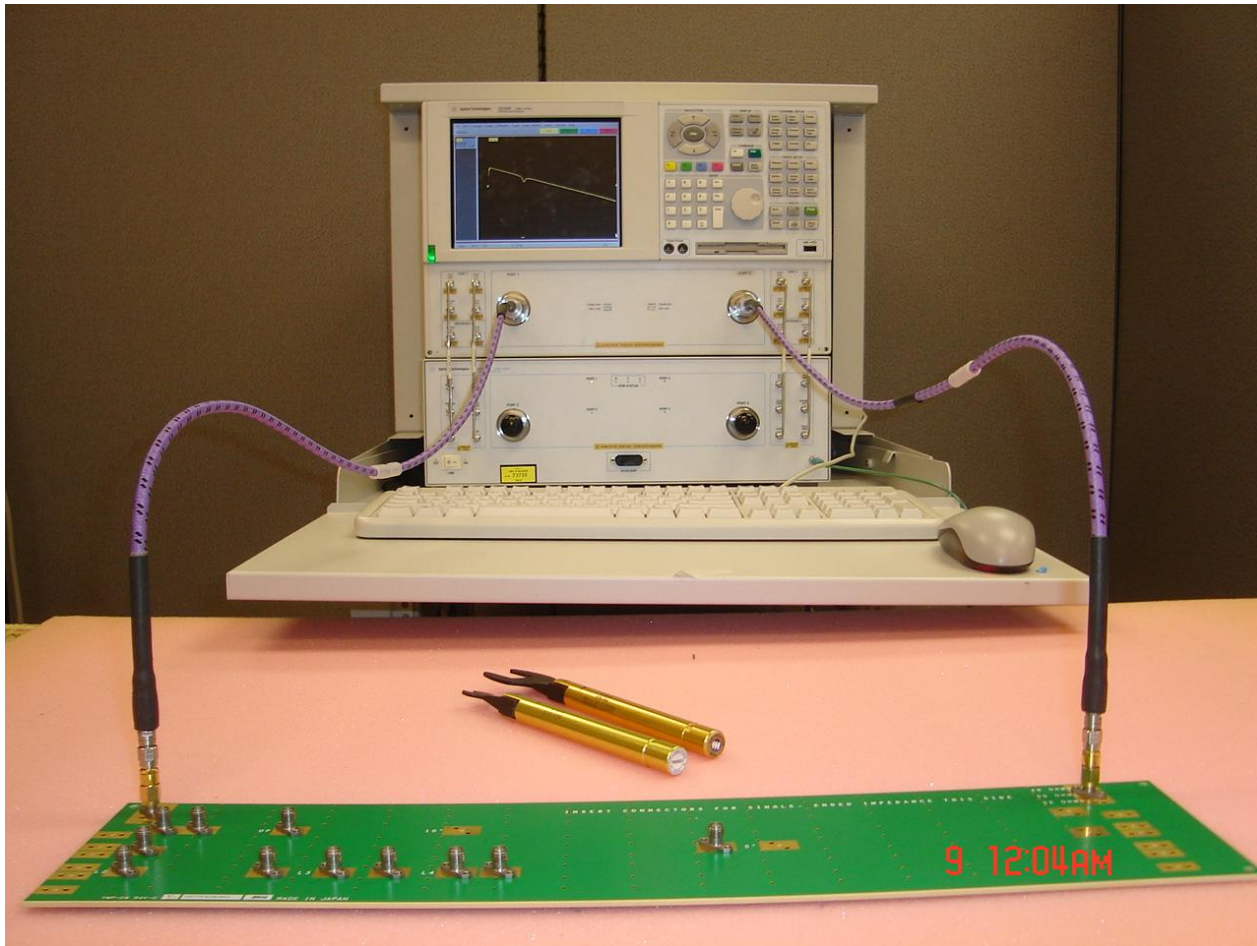
- ❖ Exposed to high temperatures during assembly soldering...
- ❖ Heated to 50-75 deg. C under actual PCBA operating conditions...

What happens to the Dk & Df of the laminate?

This project...

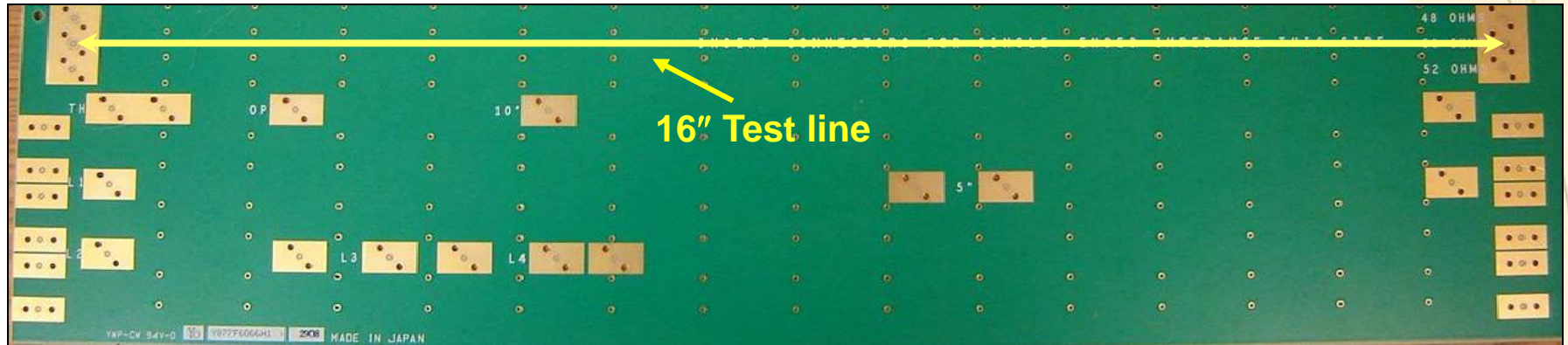
- ❖ Expands on Dk/Df work presented at 2009 APEX
- ❖ Uses the same test method
- ❖ Uses the same test vehicles

Recap of earlier work



2-port VNA-based test method for D_k and D_f over 2-15 GHz range

Recap of earlier work



Test Vehicle

- 16" balanced stripline, 50% RC on both sides
- Launch thru low-loss SMA jacks (unsoldered)
- S-params extracted over 2-15 GHz range
- **Dk** extracted from phase data, and...
- **Df** from $|S_{21}|$ after Cu roughness is backed out

Problem Statement #1

Dk and Df testing by laminators
(by whatever method) performed
on as-is core and prepreg...

***...not representative of a
finished PCBA !***

**Raw Material
(core/prepreg)**

Fab shop ↓ *lamination*

Bare PCB

Assembly ↓ *soldering*

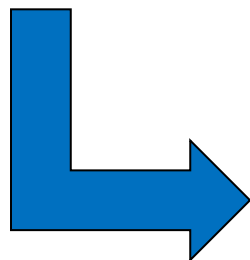
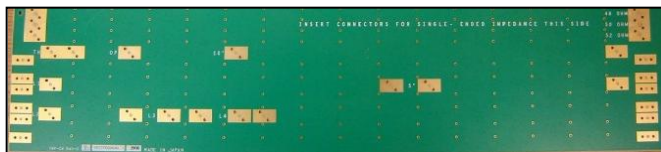
Loaded PCBA

Laminators' Dk/Df values taken **here**,

*but
unfortunately*

OEMs care about Dk/Df values **here !!**

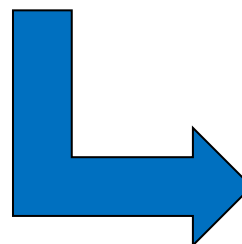
Plan: Toast 'em & test 'em!



Heller 1800EXL



**6 x 260C (Pb-free) or
6 x 225C (Eutectic)**

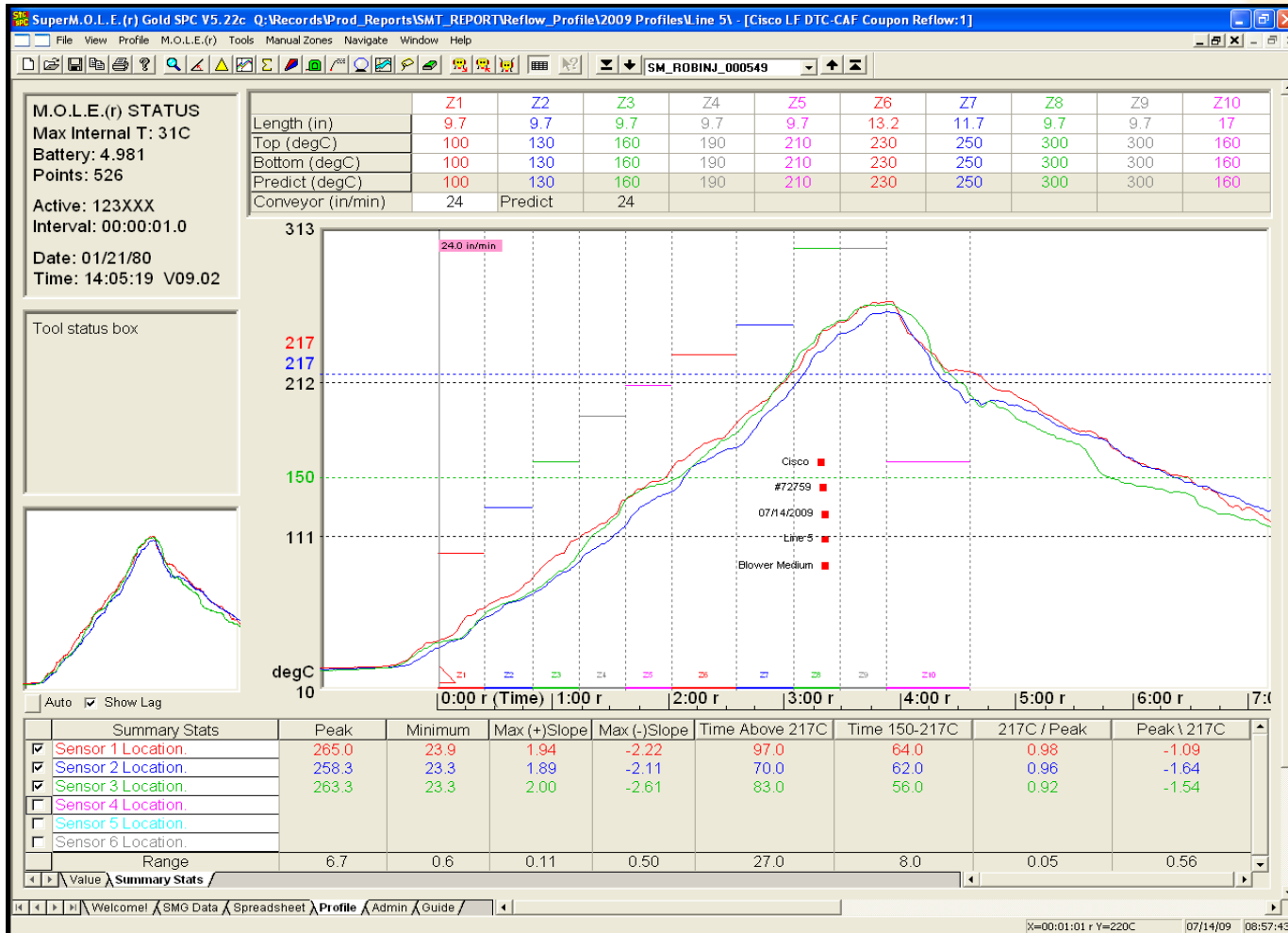


Agilent E8364



7 laminate resin systems evaluated

Reflow profiles



Eutectic profile

Time-above-liquidus (TAL) = 85 sec.
9 Zones

Laminate types

<u>Code</u>	<u>Material Type Description</u>	<u>Pb-free?</u>
A	FR4, High-Tg, Dicy-cure, unfilled	No
B	FR4, High-Tg, Phenolic-cure, filled	Yes
C	Cyanate-ester + FR4 blend, unfilled	No
D	Modified FR4, mid-range Dk/Df, unfilled	No
E	FR4, halogen-free, filled	Yes
F	Non-FR4, mid-range Dk/Df	Yes
G	Non-FR4, low Dk/Df	Yes

***7 resin systems of highest interest
chosen from our materials library***

Dk/Df Results, 10 GHz

Code	Dk (Before)	Dk (After)	Change	Df (Before)	Df (After)	Change
A	4.145	4.149	0.02%	0.0177	0.0179	1.13%
B	4.436	4.439	0.06%	0.0237	0.0239	0.84%
C	3.851	3.857	0.16%	0.0120	0.0124	3.33%
D	3.885	3.886	0.02%	0.0179	0.0182	1.68%
E	4.209	4.219	0.24%	0.0145	0.0158	8.97%
F	4.075	4.047	-0.69%	0.0104	0.0103	-0.96%
G	3.840	3.842	0.05%	0.0075	0.0077	2.67%

- All had good Dk stability
- Df of **C** and **E** increased noticeably
- Dk, Df of **F** decreased! (Under-cured?)

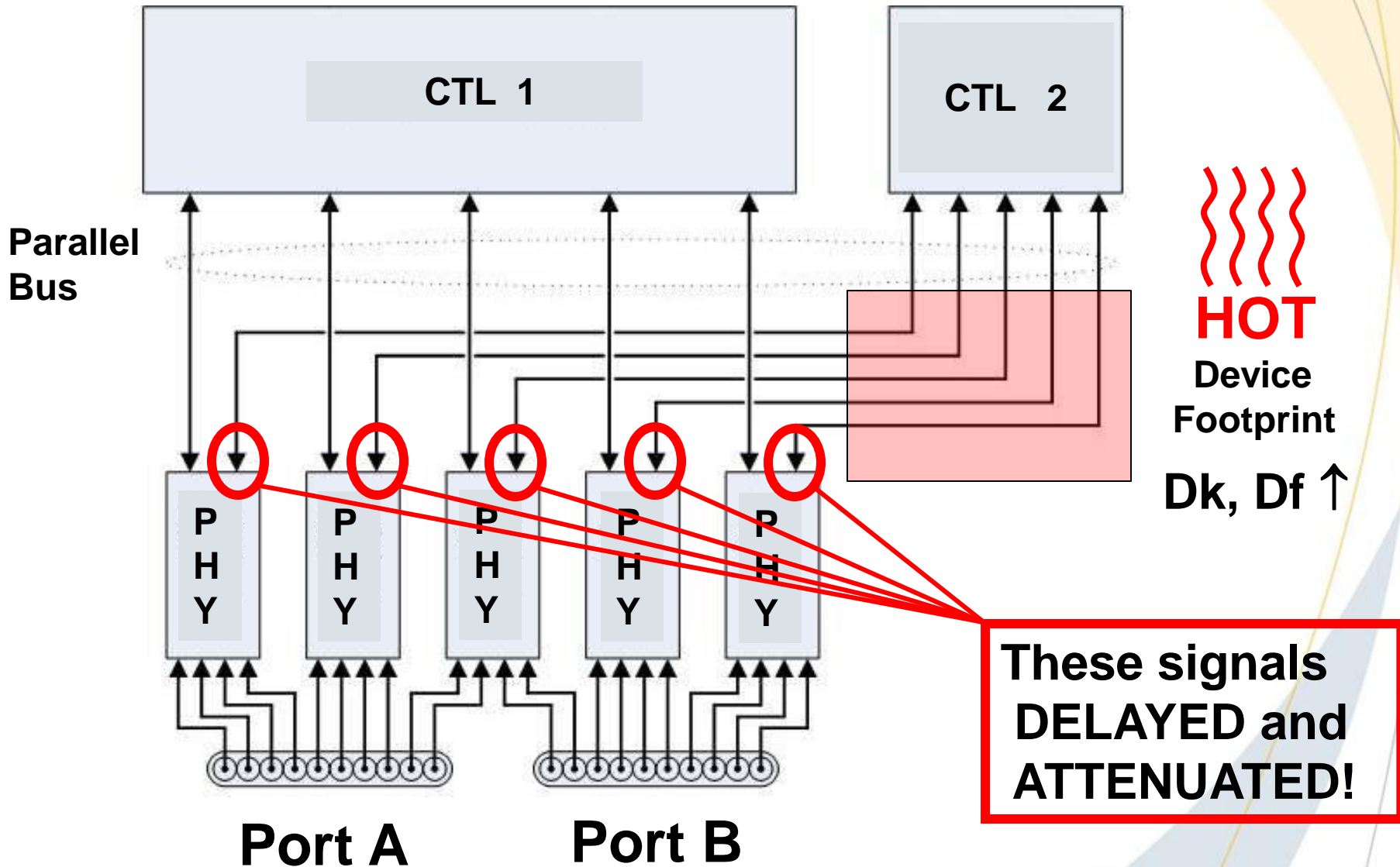
Problem Statement #2

Dk and Df testing by laminators
(by whatever method) performed
at room temperature ...

***...not representative of an
operating PCBA !***

(at least, near hot ICs & pwr units)

Why it matters



Plan: Test 'em at temp!



**50C and 75C in
environmental
chamber**



**Calibrate / test
while heated**

Same boards as run on previous test

Dk/Df Results, 10 GHz

Code	Dk (23C)	Dk (50C)	Dk (75C)	Change, 23-75C	Df (23C)	Df (50C)	Df (75C)	Change, 23-75C
A	4.149	4.189	4.222	1.76%	0.0179	0.0198	0.0223	24.6%
B	4.439	4.505	4.534	2.14%	0.0239	0.0279	0.0323	35.1%
C	3.857	3.860	3.874	0.44%	0.0124	0.0137	0.0152	22.6%
D	3.886	3.926	3.928	1.08%	0.0182	0.0204	0.0227	24.7%
E	4.219	4.585	4.598	8.98%	0.0158	0.0169	0.0187	18.4%
F	4.047	4.254	4.265	5.39%	0.0103	0.0120	0.0128	24.3%
G	3.820	3.825	3.830	0.26%	0.0077	0.0081	0.0082	6.49%

- Dk of **E** and **F** increased noticeably
- Df of **G** increased noticeably
- Df of **A** thru **F** increased **ALARMINGLY !**

Effects are additive

- ❖ Dk, Df increases @ 50-75C are reversible
- ❖ ...but those from assembly are not!
(Permanent degradation of resin matrix)

→ **Yes, the two effects are additive!** ←

Upcoming / future work

- Test six more resin system classes
 - Low-loss, non-FR4
- Effects of humidity / moisture absorption
 - Absorbed water raises Dk and Df
 - Important for outerlayer microstrips
 - ...and embedded microstrips (L2 /Ln-1)
 - Outdoor / mobile service equipment
 - New test vehicle: Outerlayer Cu removed



Summary

- **VNA-based, non-resonator test method**
 - Dk, Df sweep from 2-15 GHz, Stripline structure
- **7 classes of laminate resin systems**
 - Assortment of FR4 and lower-loss non-FR4
- **Dk mostly stable after ass'y simulation**
- **...but some Df values increased**
- **Dk mostly stable at high operating temps**
- **... but *ALL* Df values increased**

SIGNIFICANTLY!

Conclusions

- **Published Dk, Df values for laminates...**
 - Do not always represent materials post-assembly
 - May be invalid at elevated operating temperatures
- **At design stage, SI modeling should...**
 - Use caution with raw-material, room-temp Dk/Df values
 - Consider worst-case operating temp. of the PCBA
- **Designers should consider...**
 - Routing critical nets away from hot components
 - Choosing a lower-Df material if heat is unavoidable
- **If operational SI margins are < expected...**
 - Both types of thermal effects may be in play...