Telecommunications Case Studies Address Head-In-Pillow (Hnp) Defects and Mitigation through Assembly Process Modifications and Control

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ABSTRACT
One of the most perplexing phenomena in the electronic manufacturing industry today is the defect called "head-in-pillow." Head-in-Pillow (HnP) defects occur on the blind solder joints of area array packages such as FBGAs, µBGAs and CSPs. Often these insufficient or intermittent solder joint defects go undetected during manufacturing despite inspection with conventional X-ray systems. They also are insidious reliability defects that often escape the normal testing procedures and fail at the end user site. The head-in-pillow defects typically occur at the corner pins and outer rows of packages and are associated with package warpage. There are new 3D imaging systems that can help detect this, but they rely on the operator to interpret the images. There are BGA video inspection systems that can view under most devices, depending on the standoff, but they are dependent on the access, viewing angle, and operator interpretation. These x-ray and video processes also are very slow and costly.

There are several factors that can contribute to the head-in-pillow phenomena including package co-planarity, package warpage, and assembly issues associated with solder paste characteristics and stencil printing. From a process standpoint, the cause of the head-in-pillow often is the result of the sum of all of the component and assembly process tolerances. This paper will discuss several contributing factors to the head-in-pillow defects and techniques to control them. It will include reviewing DOE for solder paste deposition of five different pastes, Shadow Moiré scans on several problematic devices, cross-section analysis of failed solder joints, and solder paste analysis of "head-in-pillow" pastes. The case studies presented show that process control can mitigate HnP defects but may not be successful for some severe examples of HnP defects.

This paper uses components from telecommunication product case studies to demonstrate the effects of different contributing factors and mitigation techniques for HnP defects. The case studies include reviewing solder paste printing modifications, solder paste DOE, Shadow Moiré scans on several problematic BGA packages, effectiveness of x-ray inspection, and cross-section analysis of failed HnP solder joints. Together, these case studies show that BGA package warpage is a major contributor, but HnP defects can occur when almost any of the assembly process parameters deviate from acceptable practices.

INTRODUCTION

There are several trends in the electronics industry that have increased the challenges of surface mount (SMT) board assembly. These include conversion to Pb-free manufacturing, increased density at both the printed circuit board (PCB) and package level, new package constructions, new laminate material sets, and thicker PCB constructions. One of the consequences of the evolving and challenging technologies has been the increased occurrence of an open joint ball grid array (BGA) defect called head-in-pillow [1-6]. This defect is known by many other names such as head-on-pillow, head-and pillow, ball in cup, ball in socket, and hidden pillow. For the purpose of this paper, the defect will be referred to by the acronym HnP.

The HnP phenomena are characterized by complete melting of both the solder paste and the BGA solder ball but with insufficient coalescence to produce well-formed solder joints. Figure 1 shows examples of HnP defects using: a) an optical photomicrograph of a typical HnP metallographic cross section and b) an optical photomacrograph of the outer row of a BGA with an HnP defect. Figure 1a shows that the BGA ball sits on the solidified paste without forming a contiguous, well-formed solder joint. These are latent defects that are not detected using standard manufacturing test methods such as visual inspection, x-ray, and particularly electrical screening. The latter is important because these defects can pass in-circuit and functional test, only to fail completely or give an intermittent connection after some period of deployment in service.

The increased frequency of HnP defects has coincided with a decrease in component interconnection pitch below 1mm, a decrease in solder paste deposits below 6-mil thickness and an increase in processing temperature to accommodate Pb-Free assembly. HnP is now recognized to the point that inspection systems and solder pastes are being developed to target this problem. Additionally, standards development organizations are attempting to address this from a device standpoint [ref]. Despite these efforts, HnP defects have not been eliminated and in fact, probably are increasing because assembly process windows are decreasing.

Typically, HnP defects are associated with the higher reflow temperatures used in Pb-free manufacturing. Although surface contamination can cause HnP, it is more common for the defect to be attributed to the excessive component and PCB warpage that results from higher temperature processing. This paper will use a number of case studies to illustrate that sufficient warpage can occur in the SnPb reflow range as well as the Pb-free range resulting in HnP defects. The paper also will discuss several contributing factors to the HnP defects and techniques used to mitigate or control them. This will include reviewing DOE data for solder paste deposition of five different pastes, Shadow Moiré data on several problem devices, cross-section analysis of failed solder joints, and a comparison of solder pastes used to mitigate HnP. The case studies presented show that process control can mitigate HnP defects but may not be completely effective in some severe examples of HnP defects.

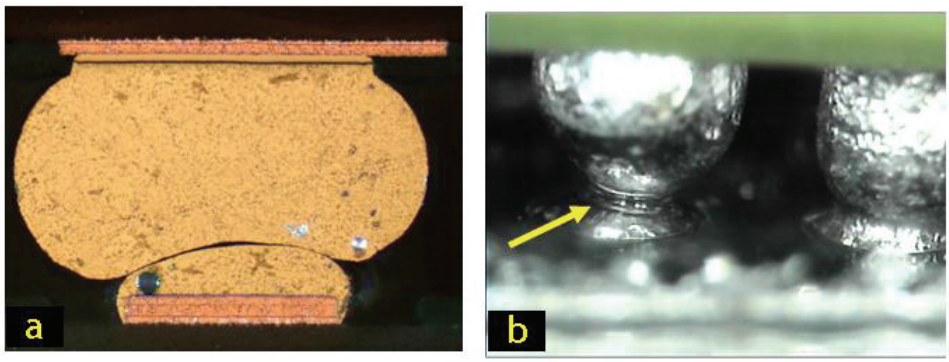


Figure 1. Examples of HnP defects a) optical micrograph of solder joint cross section, and b) Side view of a row of BGA balls with HnP at arrow.

HEAD-in-PILLOW DESCRIPTION

The HnP defects are created during the reflow process and have been described in the work by Amir et al (Intel [1]). Figure 2 shows pictorially how a gap develops between the ball and the solder paste due to dynamic warpage of the package or PCB. If there is insufficient flux activity to remove the oxide coating on the surface of the ball, or there is some contamination on the solder ball or molten solder paste mass, these two will not coalesce as shown in Figure 2d. The end result is an HnP solder joint defect when the package cools below solidification (Figure 2e).

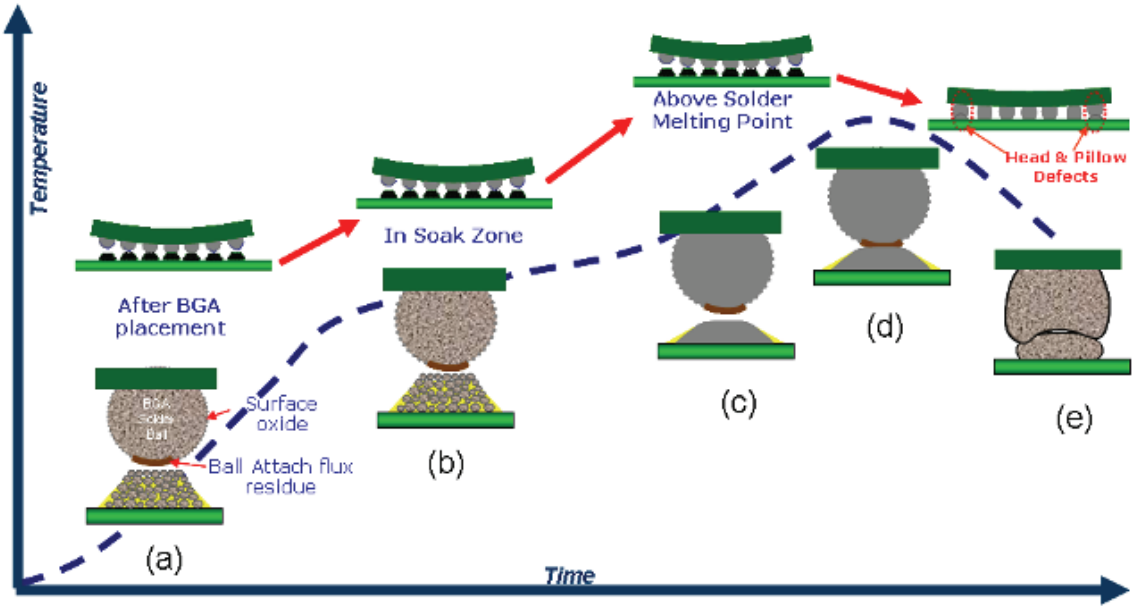


Figure 2. A pictorial representation of HnP defect formation (from Amir et al, reference 1).

CASE STUDY 1 – 144 I/O FINE PITCH BGA

Problem Description

In this application, the FBGA component exhibited extremely low yields (as low as 10%) when used in a complex telecommunication printed circuit board assembly (PCBA). There were multiple SnPb 144 I/O FBGA components soldered onto this PCBA and each had a unique pattern of HnP defects. Data provided by the device supplier indicated that this component was not sensitive to HnP defects when used in high temperature, Pb-free solder assembly process. The basic package pin diagram for the component is shown in Figure 3. Figures 4 and 5 show the defect maps and metallographic cross sections for two devices that exhibited severe HnP open joint failures.

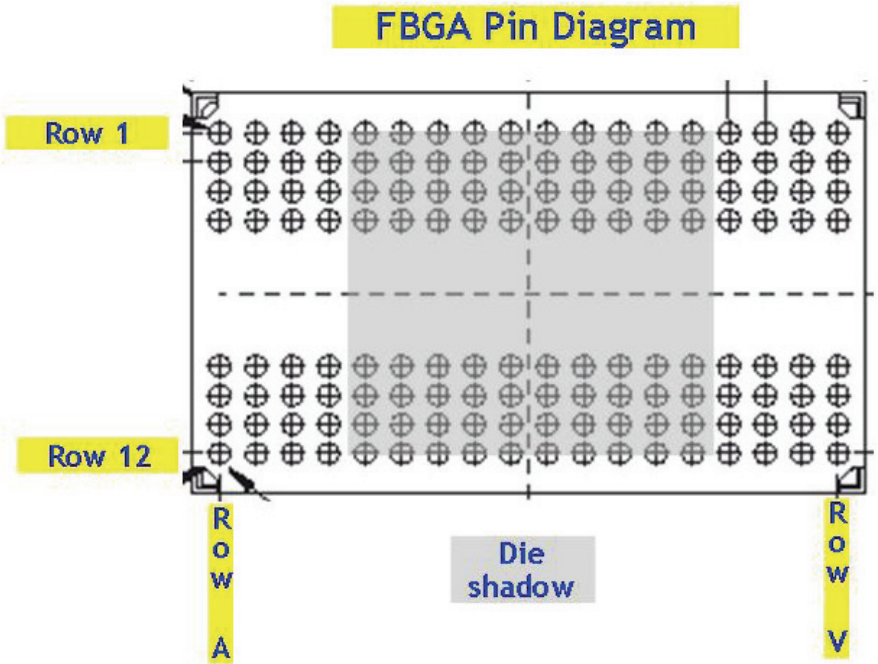
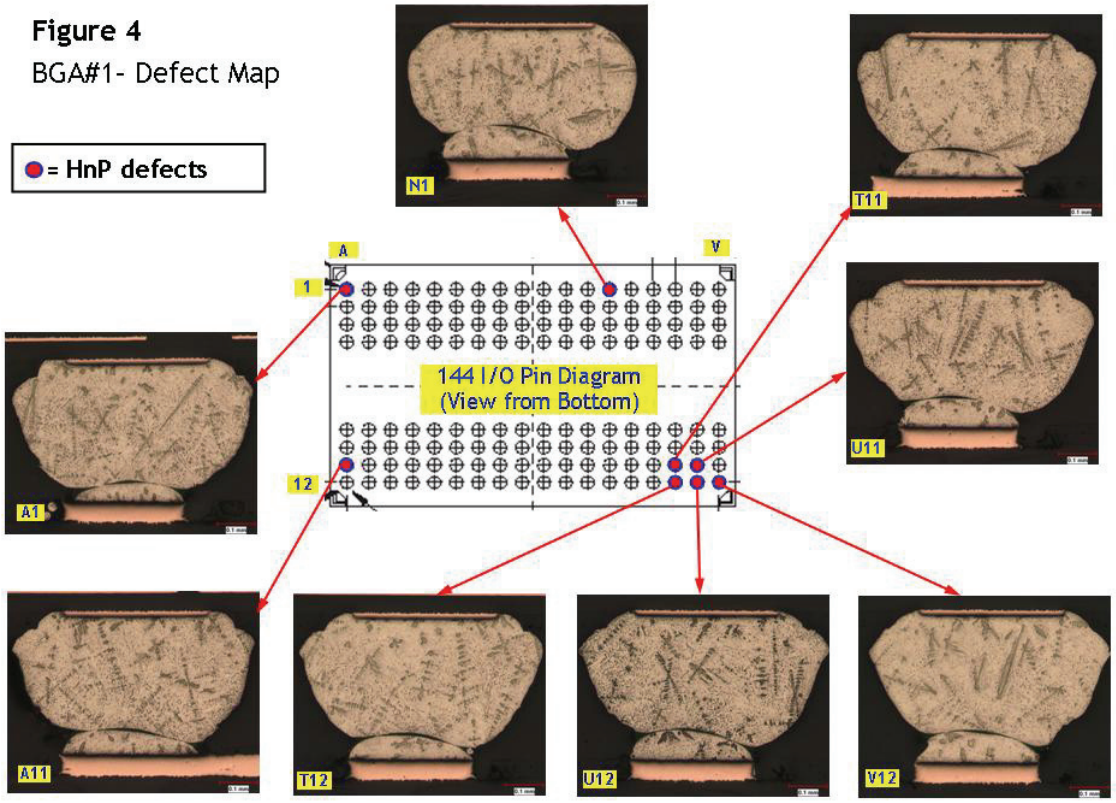
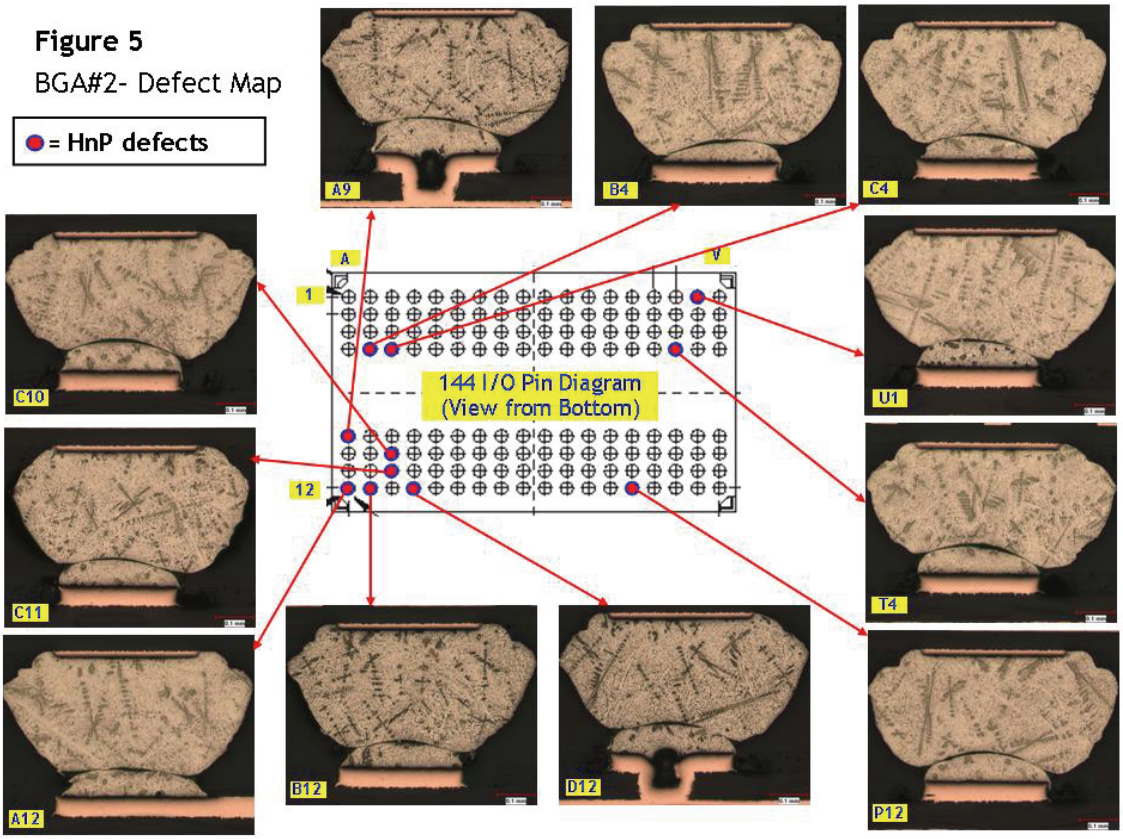


Figure 3. The package pin diagram for the 144 I/O FBGA.

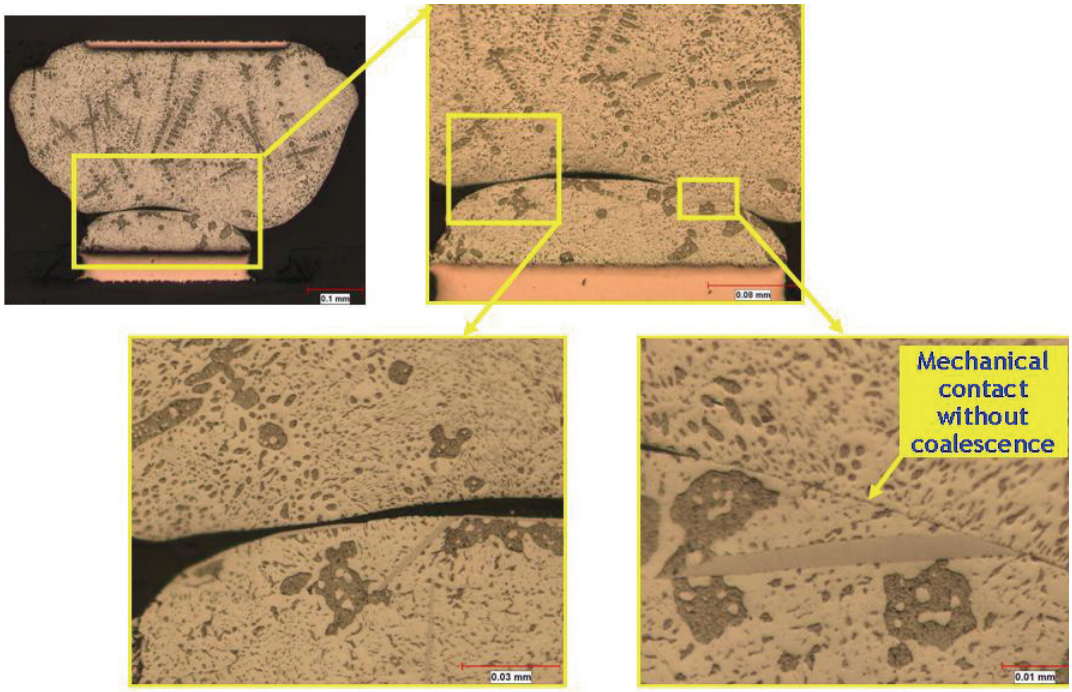




Figures 4 and 5. Defect maps and metallographic cross sections for two SnPb FBGA (labeled BGA #1 and #2) devices that exhibited severe HnP open joint failures.

A comparison of the defect maps for BGA #1 and #2 shows that an identical device can have very differently HnP signatures when assembled onto two different locations of the PCBA. When warpage is the root cause of HnP, the defects characteristically manifest themselves at the corner or outer row sites in BGA packages. While that is generally the case for these two BGAs, their defects are not limited to the corners or edges of the packages. It also is very obvious that the number of defects varies and the defect patterns are not symmetric for the two packages.

Figure 6 shows one of the HnP defects from BGA #1 at higher magnification. These photomicrographs illustrate the potential latent character of the HnP defects. There is good mechanical contact at the interface between the solidified ball and the paste even though there is no coalescence across the interface. This site is located on an inner row and is not likely to be detected with a visual or a detailed microscopic inspection. It definitely will pass electrical testing and may pass thermal screening if adjacent sites are properly soldered and support the integrity of the mechanical connection.



Figures 6. These photomicrographs illustrate the latent nature of the SnPb HnP defects. There is good mechanical contact at the interface between the solidified ball and the paste even though there is no coalescence across the interface.

Root Cause Analysis

The defects are located not only at or near the outside of the package, but also outside the die shadow (see Figures 4 and 5). Contamination would be expected to produce a less localized pattern of detects, which focuses attention on package warpage as the most probable root cause of the HnP defects. Table 1 shows a summary of Shadow Moiré warpage [7] measurements on the 144 I/O FBGA package. There are a number of notable observations in these data. First, the peak warpage occurs at the SnPb (not Pb-free) peak soldering temperature. Second, the warpage is not symmetric around the peak temperature. Third, the warpage is not completely reversible or recoverable following the simulated reflow temperature cycling. Finally, although the room temperature warpage or coplanarity is 70-80 μm (3-4 mils) is quite acceptable, the warpage is substantially greater at the high temperatures in the reflow profile warpage, where HnP is known to occur.

These data do not describe or account for any asymmetry in warpage across the package. Measurements on other similar FBGA packages show similar but not absolutely identical results, thus some of the variation in the defect patterns between BGA #1 and BGA #2 could be the result of package-to-package variations. However, the type of statistical studies need to verify those variations is beyond the scope of this work. It should also be noted that these package warpage measurements obviously can not account for additional effects due to PCB warpage.

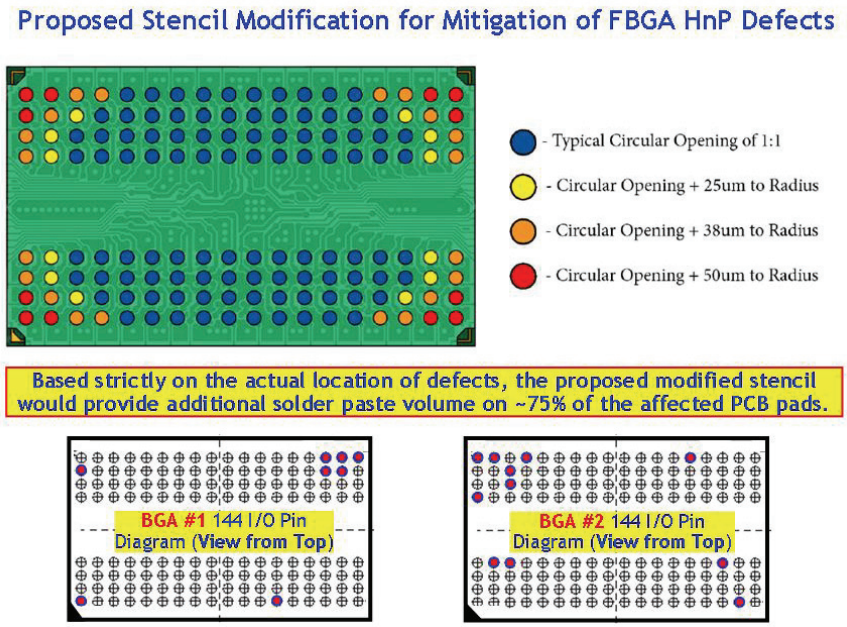
Table 1. A summary of Shadow Moiré warpage measurements on the 144 I/O FBGA package. Note that the peak warpage occurs at SnPb, not Pb-free soldering temperatures.

Temperature °C	Warpage µm
30	70
75	31
150	98
220	137
240	131
260	115
240	98
220	81
150	52
75	42
30	80

Corrective Action

Often there is no alternate device and package available when warpage is identified as a root cause of HnP. In those cases, a common corrective action is to modify the stencil printing to provide additional paste volume to bridge the gap (illustrated in Figure 6) at the potential HnP sites [6]. Such a recommendation for the 144 I/O FBGA is shown in Figure 7. This stencil recommendation was provided by the device supplier and was based on extensive Moiré studies of warpage in the 144 I/O FBGA package. Implementation of this stencil modification improved the manufacturing yields from approximately 10% to 80% but did not eliminate the HnP defects entirely. The stencil modification also introduced some solder bridge (short circuit condition) defects, which is an expected consequence of increasing paste volume with a fine pitch device.

A comparison of the stencil modification and the defect maps shown in the lower part of Figure 7 indicate that the increased paste volume will mitigate the HnP problem in only about 75% of the FBGA sites used in this telecommunications application (Note that these diagrams show the same package layout as those in Figure 4 and 5 but here they are viewed from above to coincide with the stencil pattern.). This result is consistent with both the yield improvement and with the observation that HnP defects were not eliminated completely. Despite the vast improvement, an 80% yield is unacceptably low. However, given the demonstrated ambiguity in all aspects of the HnP defect characterization, it is more critical to recognize that the 80% distribution may contain latent defects that can "escape" into service. In the absence of a definitive non-destructive detection technique, this produces an unknown risk in subsequent field failures.



Figures 7. Proposed stencil modifications and effectiveness in mitigating HnP defects in the telecommunication Case Study 2 application of the 144 I/O FBGA package.

Summary – Limitations in Mitigating HnP though Paste Printing Modifications

Case Study 1 for a 144 I/O, 0.8 mm pitch FBGA shows that HnP defects are not limited to Pb-free assembly and can occur with a typical SnPb soldering profile. Detailed root cause analysis shows that stencil printing modifications that provide additional paste volume at the potential HnP sites can be used to bridge the gap during reflow and minimize HnP defects. However, the effectiveness of printing modifications will depend on the magnitude and extent of the relative warpage between the BGA component and the PCB. The specific application of a 144 I/O FBGA presented here possibly represents a worse case scenario, in which yields will be defined by a tradeoff between bridging and effective soldering resulting from additional solder volume. These results indicate that the characterization of the 144 I/O FBGA HnP and corrective action described here can not be translated directly to other applications of the 144 I/O FBGA without incurring risk.

CASE STUDY 2 – 484 I/O PBGA

Problem Description

In this application, a 19mm x 19mm. 0.8 mm pitch, 484 I/O PBGA component exhibited variable or erratic production yields when used in a complex telecommunication printed circuit board assembly (PCBA). The PCBA contained an array of multiple SnPb 484 I/O PBGA (Figure 8) components. Only some of the sites had HnP defects, the frequency of defects varied dramatically from one PCBA to another, and the overall yield was approximately 80%. Defects were mostly localized at the corners and in the outer rows of the BGA but each component location and PCBA had a unique pattern or number of HnP defects. Optical inspection images of HnP defects are shown in Figure 9. Data provided by the device supplier indicated that this component was susceptible to warpage but was less sensitive to HnP defects when used in high temperature, Pb-free solder assembly process.

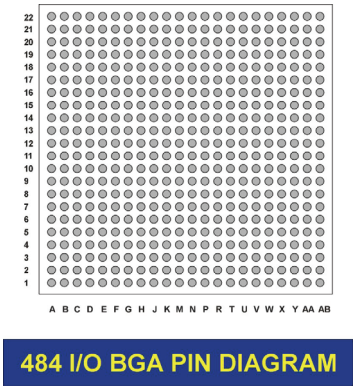


Figure 8. The 484 I/O PBGA pin diagram.

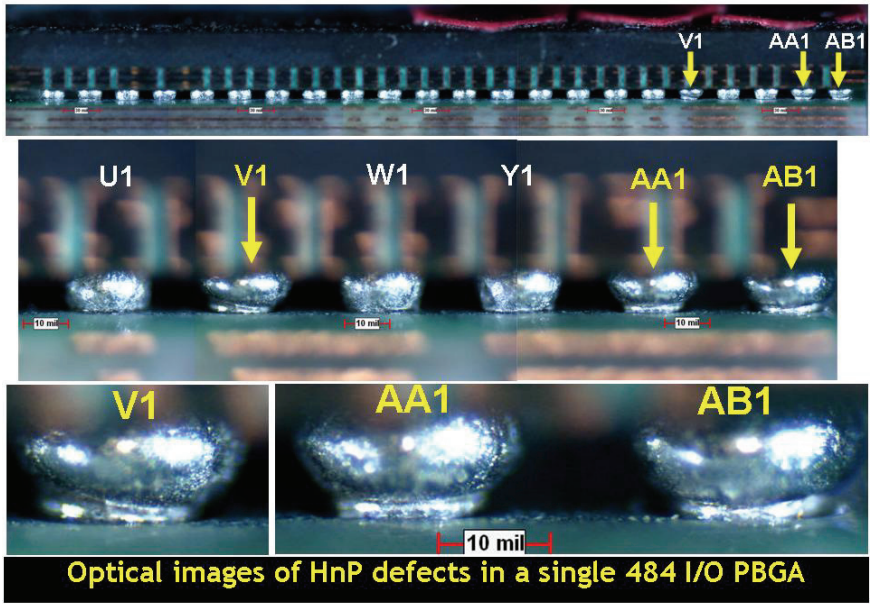


Figure 9. Optical images of multiple HnP defects in a single 484 I/O PBGA**.**

Multiple sets of detailed photomicrographs of HnP defects in the 484 I/O PBGA are shown in Figures 10-12. Collectively, these photomicrographs illustrate the scope of the HnP problem with the 484 I/O PBGA used in this telecommunication

application, as well as the subtle and insidious latent character of HnP defects. The photomicrographs in Figure 10 show an HnP defect that will likely fail electrical testing due to the gap that exists at the interface between the solder ball and paste after resolidification. The photomicrographs in Figure 11 show an HnP defect that is very likely to pass electrical testing and may pass thermal screening and escape detection, only to fail after some undetermined time in service. The ball and paste in this solder joint are making good mechanical contact, but the highest magnification images show that there is no continuity in the solder microstructure across the interface. An argument could be made that a sub-microstructural, diffusion bond exists between the two masses of solder but there clearly has been no actual solder coalescence and solidification across the interface. The photomicrographs in Figure 12 show an HnP defect that will pass all routine factory testing. The ball and paste in this solder joint are connected across only about 30-40% of the area of a normal, well-formed solder. There are no existing data that could be used to predict the risk of failure for this solder joint in service.

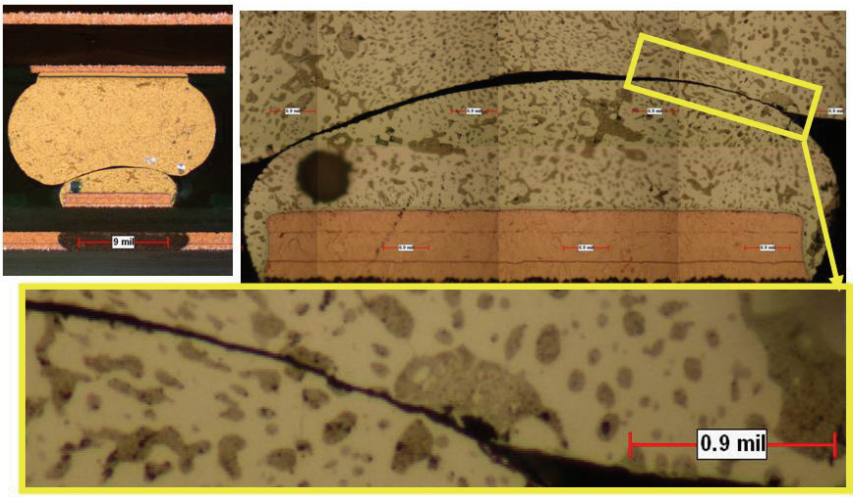


Figure 10. A series of optical photomicrographs of an HnP defect in the 484 I/O PBGA. This HnP defect is likely to be detected in electrical testing in the factory due to the gap between the solder ball and paste following reflow and resolidification.

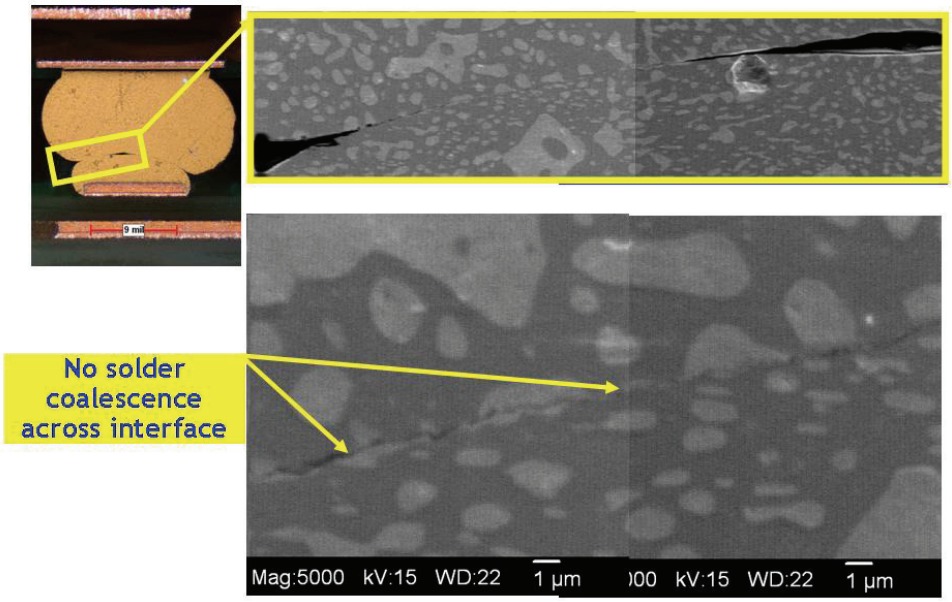


Figure 11. A series of optical and scanning electron micrographs of an HnP defect in the 484 I/O PBGA. This HnP defect may not be detected in the factory due to the good mechanical contact at the HnP interface between the solder ball and paste.

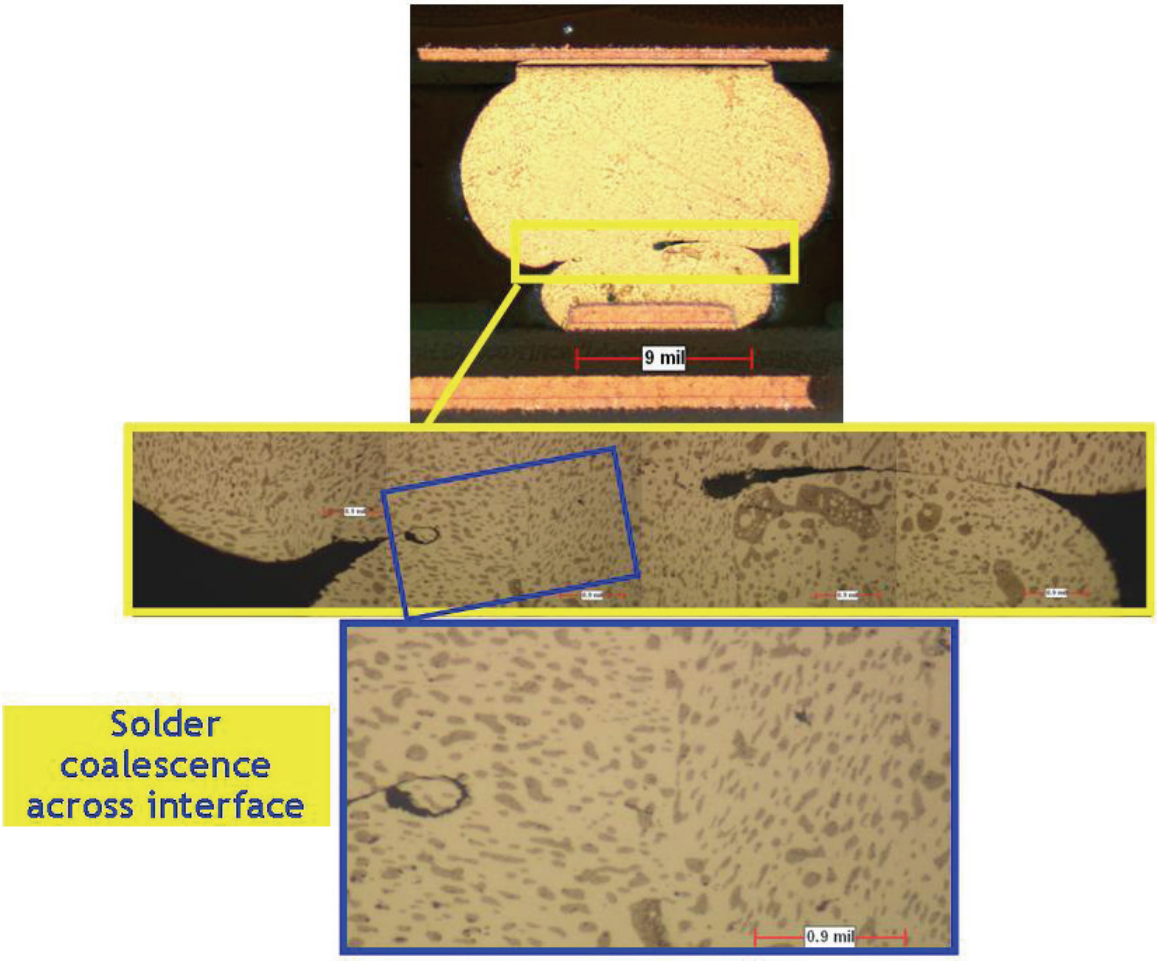


Figure 12. A series of photomicrographs of a HnP defect in the 484 I/O PBGA that will pass all routine factory testing. The ball and paste in this solder joint are connected across about 30-40% of the area of a normal, well-formed solder. The risk of failure of this latent defect cannot be quantified.

Root Cause Analysis

Based on the characteristics of the yield data, the initial focus of the root cause analysis was on package coplanarity or warpage. The most common technique for characterizing the extent of the warpage is by performing a Shadow Moiré scan [7]. Shadow Moiré scans can detect surface deviations dynamically using a simulated surface mount reflow profile at specific temperature read points of interest. The Shadow Moiré scans from one of the devices from the initial set are show in Figure 13. The scans simulate a reflow profile by starting at room temperature, peaking at 230º C and then returning to room temperature.

The results of the Moiré testing indicate significant package warpage occurs throughout the reflow process temperature range. Table 2 summarizes the Moiré results for four devices, showing the initial coplanarity measurements, peak coplanarity measurements, and the total variation through the reflow temperature range. The data in this table show there is a maximum coplanarity or warpage of 200.7 microns (7.9 mils) during the reflow process. Four additional devices were sent to the packaging house for independent confirmation of the Moiré measurements. Those results are summarized in Figure 14 and show a maximum warpage as great as 219.0 microns (8.6 mils) with a deviation from flatness of approximately 75 microns (3 mils) at SnPb liquidus. The second set of data provides confirmation of the findings from the initial set of measurements shown in Table 2. These Moiré data show similar trends as the 144 I/O FBGA discussed in Case Study 1.The warpage is not symmetric around the peak temperature and is not completely reversible or recoverable following the simulated reflow temperature cycling.

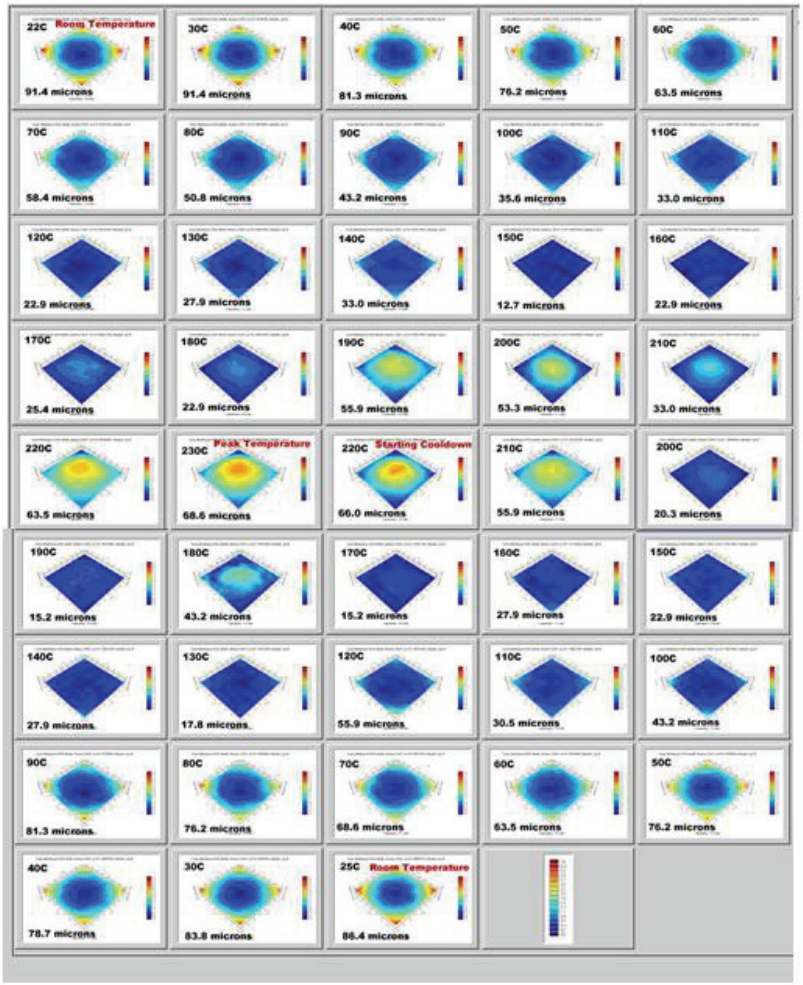


Figure 13. Example of a Shadow Moiré output scans for a 484 I/O PBGA.

Table 2. Summary of Shadow Moiré results for 4 different 484 I/O PBGA components.

Device Number	Initial Co-planarity µm (microns)	Peak Co-planarity µm (microns)	Total Variation µm (microns)
1	91.4 @ (22ºC)	68.6 @ (230ºC)	160.0
2	104.1 @ (22ºC)	83.8 @ (180ºC)	188.0
3	99.1 @ (22ºC)	58.4 @ (210ºC)	157.5
4	96.5 @ (200ºC)	104.1@ (90ºC)	200.7

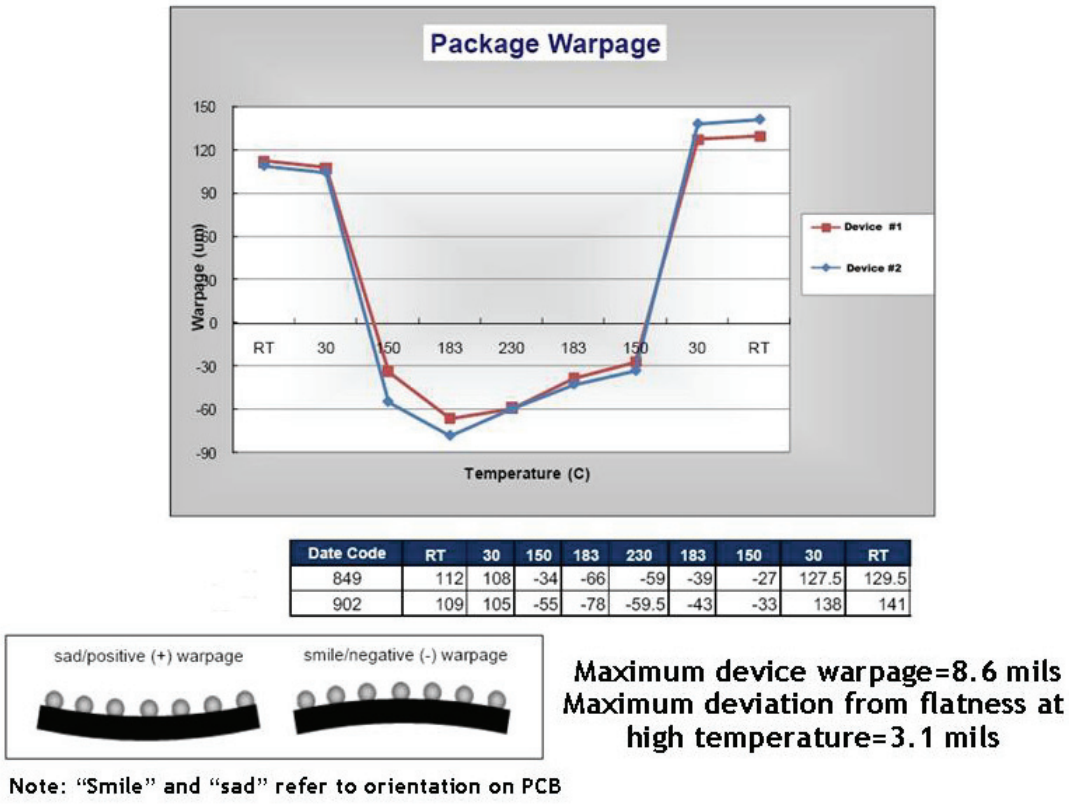


Figure 14. Summary of the Shadow Moiré testing of four additional 484 I/O, 0.8 mm pitch PBGA components performed independently at the packaging house.

The Shadow Moiré warpage results for the 484 I/O PBGA show that the maximum deviation in package flatness occurs in the SnPb reflow range above 183º C. Discussions with the device supplier revealed that a major change in the package mold compound had been made to accommodate the brittle properties of the device 90 nm low-K dielectric. Working in conjunction with the device supplier, Shadow Moiré was performed on two older generations of the device that used a different mold compound. The Moiré results showed that the component with the newer mold compound warped approximately 40% more than the older generation component.

In summary, the Moiré measurements and device supplier data show there is a certain amount of warpage inherent in the 484 I/O PBGA components. The warpage can not be eliminated and it can vary significantly from component to component. In the worse case interactions with localized PCB warpage, this can result in HnP defects. In view of the package constraints, mitigation of those defects must be focused on surface mount assembly process modifications or controls.

Stencil Design, Solder Paste Selection and Paste Printing

The art of stencil printing has become a very complex operation due to the extreme mix of component technologies used in complex telecommunication designs. These components include micro-discrete resistors and capacitors, super-large discretes, large plastic and ceramic area arrays, 0.4 mm pitch QFP and TSOP, 0.5 mm pitch QFN, and large power supplies and transformers. To handle these components, varying volumes and heights of solder paste are needed, which makes stencil design an important factor in the Design For Manufacturability (DFM) reviews. The use of 5 mil stencils has become common with most contract manufacturers, which may satisfy IPC-610D inspection criteria but may not be sufficient to avoid HnP defects. One other important factor to consider is variation in solder paste properties and performance from manufacturer to manufacturer. Some solder pastes in fact, are advertised as being capable of mitigating HnP defects. Good, consistent print quality, which is required to mitigate HnP risks, is a challenge considering the need to balance all the potential design and manufacturing constraints.

A two-phase solder process analysis was conducted as a result of the outcome of the preliminary root cause warpage analysis. The first phase was a Design of Experiment (DOE) to evaluate solder paste printing and the second phase was an evaluation of the impact of solder printing on assembly and propensity for HnP. The DOE developed specifically to examine the solder paste printing performance used the normal line output as the baseline metric. Automated 100% Solder Paste Inspection (SPI) was done for six different commercial solder pastes with the DOE being focused specifically on the 484 I/O PBGA devices.

The paste printing DOE consisted of 30 printed boards of each paste and generated scatter plots for area, height, and volume. Following the printing DOE an assembly DOE was run to assess the ultimate performance of the paste printing. Figure 15 shows the scatter plots for the paste printing DOE.

The scatter plots show that paste D clearly had the tightest, most consistent variations in area, height, and volume. Pastes A, C, and F had some aperture clogging and required additional cleaning. These data were used to select the pastes for the assembly phase of the study. Paste C was eliminated based on poor performance and paste E was eliminated due to availability. Despite poor print performance, pastes A and F remained in the assembly phase matrix because both pastes have advertised effectiveness for eliminating HnP defects. The effectiveness of these pastes is based on their prolonged flux activity, which promotes wetting and soldering better during the ramp down [4]. Thus, solder pastes A, B, D, and F were chosen for the final assembly evaluation phase.

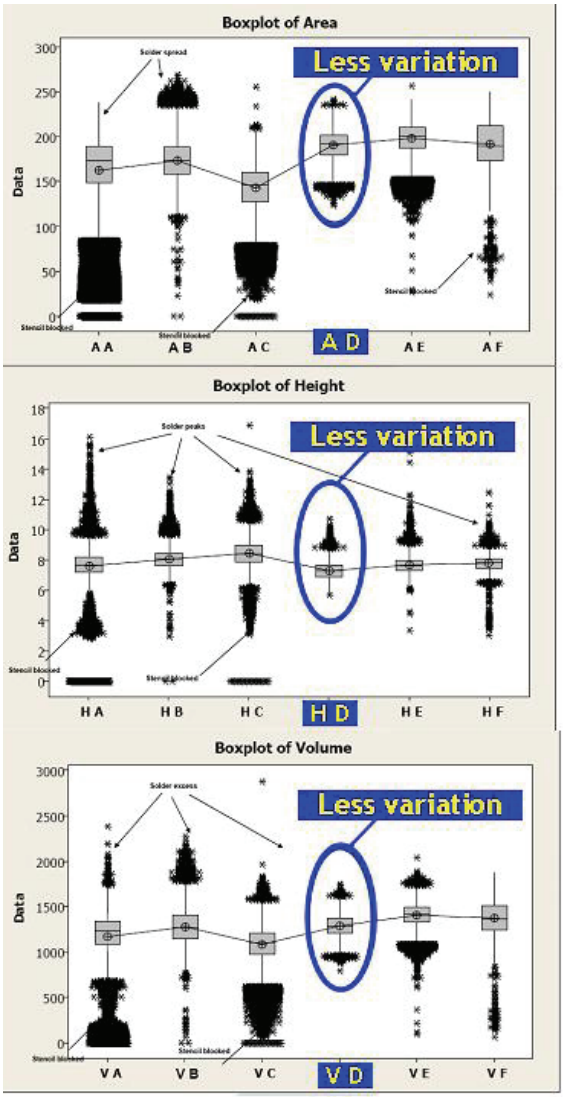


Figure 15. DOE scatter plots for solder paste area (top), b) height (middle), and c) volume (bottom). Solder paste "D" in blue was the best performer with the lowest variations in area, height, and volume.

The sample size for the assembly matrix was 50 each for pastes A, B, and F and 70 each for D. The yield results are showed in Table 3. In the SMT operations, paste A performed well despite its poor performance in the paste DOE. Paste D showed poor results in the SMT operations due to shorts. It appears that the added volume of solder paste resulted in increased shorts, which is a common over-correction when dealing with HnP. Although the assembly yield for paste D was lower than the other pastes because of solder shorts, from a product *reliability* standpoint paste D had the best results in the thermal test indicating that there would be fewer escapes related to HnP defects with paste D than the other pastes. This is an important finding because it indicates that a product risk analysis should be conducted to determine if a lower assembly overall yield actually provides better product reliability and a lower life cycle cost. In simplest terms, this is reduced to a tradeoff between

solder shorts that can be detected and corrected in the factory and HnP defects that may escape manufacturing, reduce reliability, and increase life cycle cost.

Table 4 shows the defects associated with the 484 I/O devices as a function of assembly operation. There were no visible defects identified during SMT. The 5DX (X-ray) operation was unable to detect HnP but it did detect one short each with pastes B and D. These two defects were associated with the increase in solder volume due to the increase in solder height and area. For the In Circuit Testing (ICT), Functional Testing and Thermal Screening Testing operations, the 484 I/O device failures were inspected using a BGA video microscope to confirm the HnP defects. All the failures detected during ICT, Functional Test, and Thermal testing for devices assembled with pastes A, B, and F were confirmed as HnP defects. The Thermal Test failure for paste D was not confirmed as an HnP on the outer perimeter and X-ray inspection did not detect HnP in the inner rows. The device was immediately re-reflowed but it continued to fail. and it was presumed to be a device failure. Since paste D had the most consistent results in the print DOE and showed the best performance for mitigating HnP defects in the assembly testing, it was considered the best candidate for corrective action.

The data from the two-phase DOE showed that a carefully chosen combination of paste selection and print control could provide significant mitigation of HnP defects. When solder paste D was implemented into the production process, it was done in conjunction with incorporation of 100% solder paste inspection (SPI) to enable improved manufacturing process control. The SPI was viewed as a critical step because it was needed to maintain control of a soldering process with a relatively narrow window for success. By all accounts, it seems that deviation from the optimum process window results in unacceptable levels of HnP defects in the 484 I/O devices. The corrective action plan required process changes and quality monitoring that deviated from conventional manufacturing practices. Those process changes required substantial resource commitments in manufacturer but this eliminated nearly all HnP defect, and resulted in acceptable production yields.

A few brief reflow trials showed that the reflow profile did not have as much of an impact as might be expected. This may not be true for all cases of HnP, but the 484 I/O devices tended to have serious warpage in the 150-200º C range and had minimal additional warpage up to 260º C. Therefore, minor profile adjustments had no measureable effect on the incidence of HnP. The profiles used for the assembly DOE were adjusted to align with the profile parameters recommended by paste manufacturers.

Table 3. Overall assembly results for pastes A, B, D, & F.

Operation	B	D	F	A
SMT Bottom	80.00%	85.51%	84.00%	98.00%
SMT Top	84.00%	42.03%	84.00%	92.00%
5DX	86.00%	75.38%	88.00%	88.00%
ICT	86.00%	82.81%	85.71%	86.00%
Functional Test	100.00%	100.00%	100.00%	100.00%
Thermal Test	89.19%	93.44%	87.88%	81.25%

Table 4. 484 I/O PBGA device defects. Paste D was selected for process corrective action

Operation	B	D	F	A
SMT Bottom	0	0	0	0
SMT Top	0	0	0	0
5DX	1	1	0	0
ICT	4	0	1	10
Functional Test	1	0	2	3
Thermal Test	5	1	1	0

Summary – Mitigating HnP by Controlling the Manufacturing Processes

The analysis for Case Study 2 for a 484 I/O, 0.8 mm pitch PBGA shows that it may be possible to control the onset of HnP defects caused by component warpage through extraordinary manufacturing process controls. In this case, a combination of

solder paste selection, stencil print modifications, enhanced inspection techniques, and diligent monitoring of all the processes provided the only practical path for corrective action. It can not be emphasized enough that it was critical to develop good process methods and continue to monitor their effectiveness in practice.

CASE STUDY 3 – BGA HnP in New Product Introduction (NPI)

Problem Description

In this application various complex telecommunications Pb-free development products exhibit intermittent or open FBGA and PBGA component solder joints. The rapid expansion of 3G and 4G telecommunications has dramatically changed New Product Introduction (NPI). Design cycles have been reduced from years to months, and multiple designs are being developed simultaneously to meet customer demands for features and performance. The combination of high-mix, low-volume, product diversity, and aggressive schedules is causing an increased occurrence of HnP and intermittent BGA solder joint defects in NPI. Figure 16 shows two examples of new telecommunication products. The PCBA geometries are considerably different and there is a wide range of BGA component sizes and pin counts being used as evidenced by the x-ray images included in Figure 16.

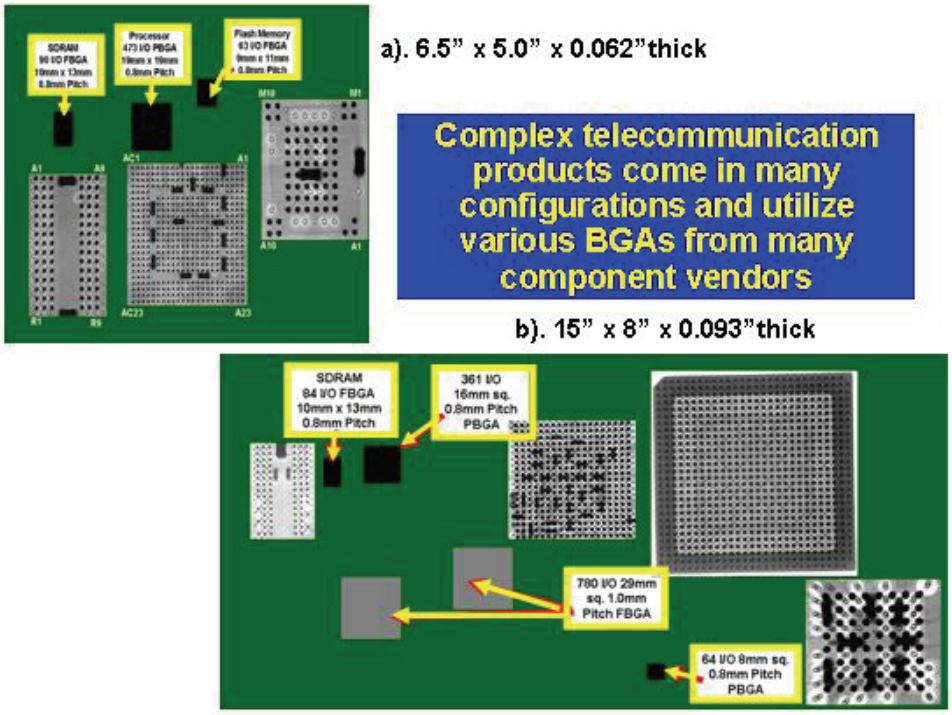


Figure 16. Examples of variation and range of components seen in telecommunication NPI.

It is common for test coverage development to be incomplete in NPI. In many cases visual inspection and conventional x-ray are the only inspection tools in use. However, interpretation of optical and x-ray images can be very operator dependent. Figure 17 shows optical and x-ray images of corner sites on the 473 I/O PBGA from Figure 16. It is easy to see from these images that the solder joint is "lumpy". Without extensive root cause analysis, it was difficult to determine if the lumpiness was due to inadequate reflow temperature, insufficient solder paste, or insufficient flux activity due to a poor or dried out solder paste.

Similar to Case Studies 1 and 2, many of the solder joint defects appear to be located at corner or edges of packages. Note that there may be defects at interior sites that can not be detected with simple visual, optical, or x-ray inspection. The high-mix, low-volume start and start/stop mode of operation in an NPI environment is not conducive to acquiring statistical failure information needed to identify the defect root cause. Figure 18 shows solder joint defects in a 473 I/O PBGA on another NPI build. The defects on this board show not only HnP and insufficient solder joints but also no-solder defects. There is also a misalignment of the BGA balls to the PCB pads. The no-solder defects may have been due to plugged stencil apertures and the insufficient and HnP defects may have been due to poor release of solder paste from stencil apertures.

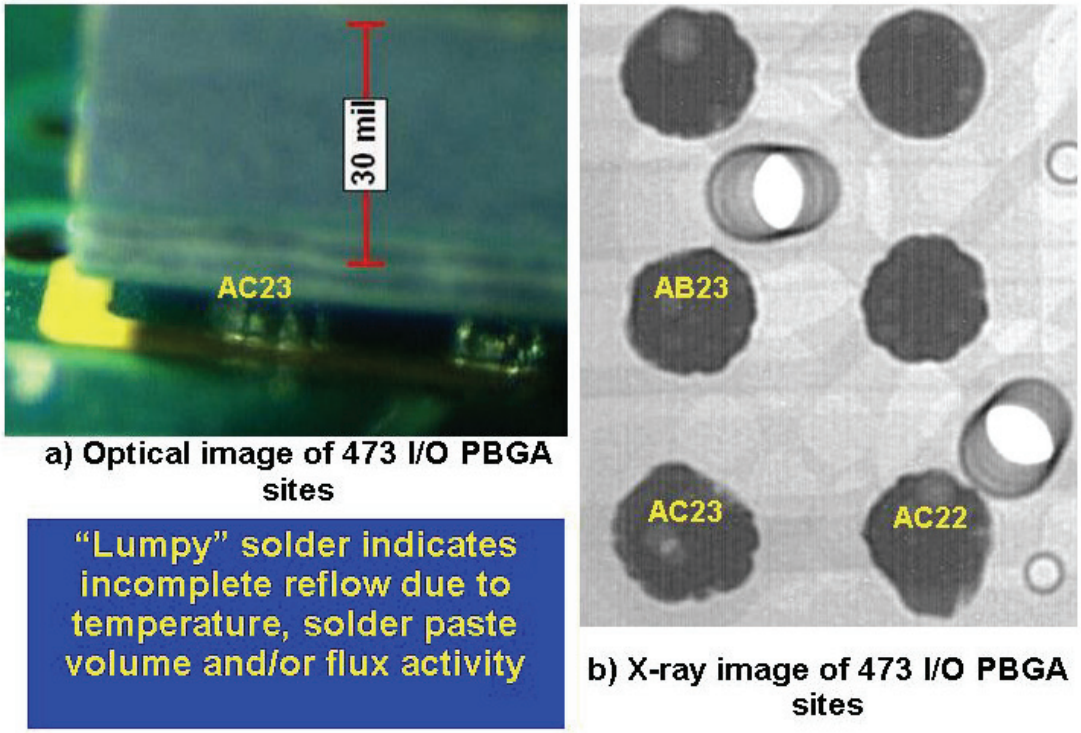


Figure 17. Lumpy solder joints on a 473 I/O 0.8mm pitch PBGA

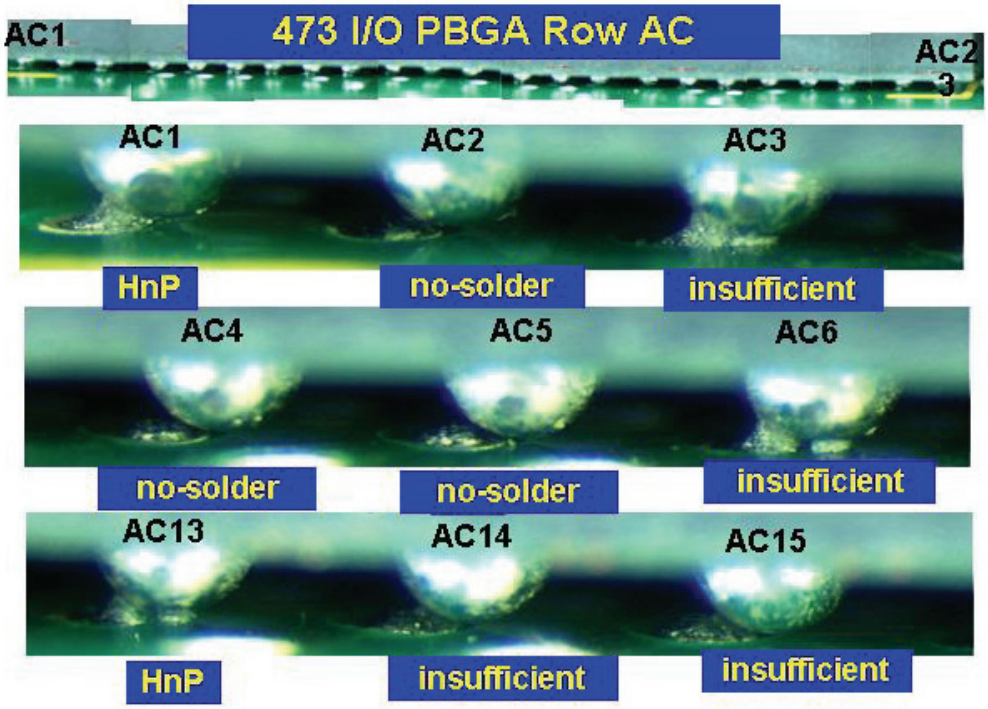


Figure 18. 473 I/O PBGAs in another NPI build exhibit various defect signatures than those in Figure 17.

Figures 19 through 22 show HnP defects in 84 I/O FBGA and 64 I/O PBGAs on other NPI products. The HnP defect in Figure 20 could be detected using a small 45 degree inspection mirror on the end of probe or by using a BGA video inspection tool. An examination of the 84 I/O FBGA conventional 2D x-ray image in Figure 21, shows an apparent difference between the A3 HnP defect and surrounding ball sites. However, without the optical image the x-ray image is not sufficient to identify this solder joint anomaly as HnP. In fact, one would be hard pressed to determine from the x-ray image that this was a defective solder joint site.

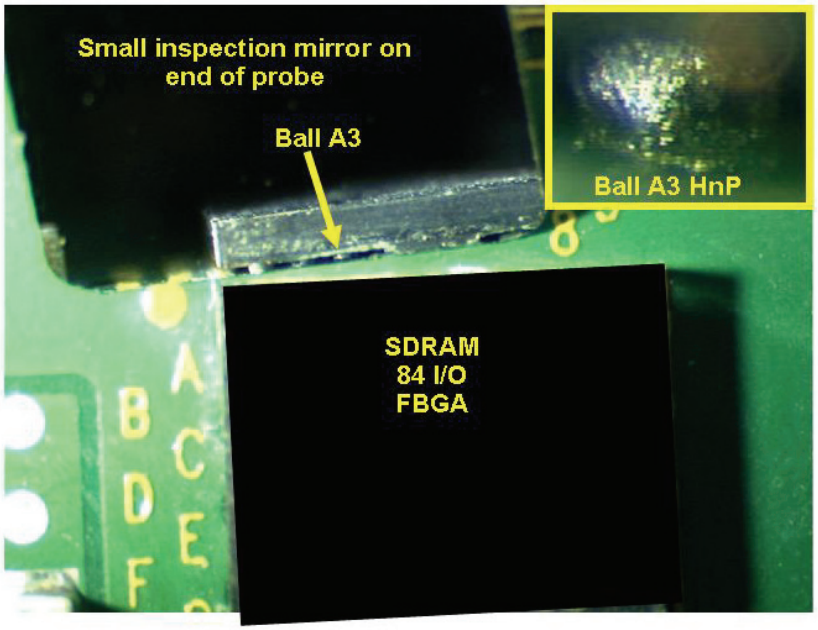


Figure 19. HnP defect on 84 I/O SDRAM FBGA. The optical inspection system or microscope and mirror may be useful for a BGA not near the PCBA edge but these are difficult to use, have marginal image quality, and require operator skill and experience.

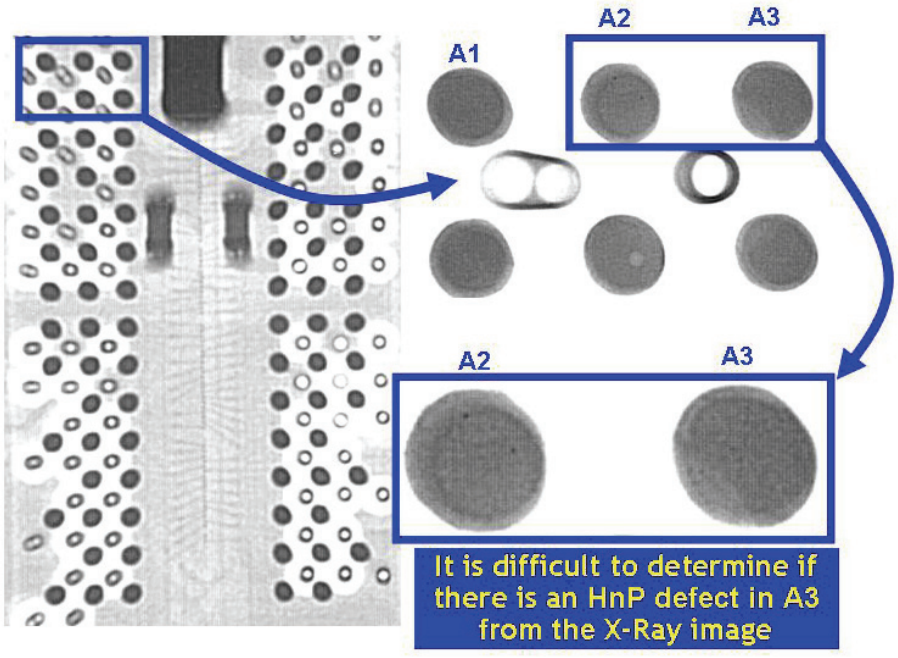


Figure 20. The HnP defect on the 84 I/O SDRAM FBGA is difficult to detect with x-ray inspection.

The conventional 2D x-ray image of defects on a 64 I/O PBGA presented in Figure 21 can not identify HnP or insufficient solder joints. In the absence of the optical inspection images shown in Figure 22, it would be impossible to determine that these sites had HnP and insufficient solder joint.

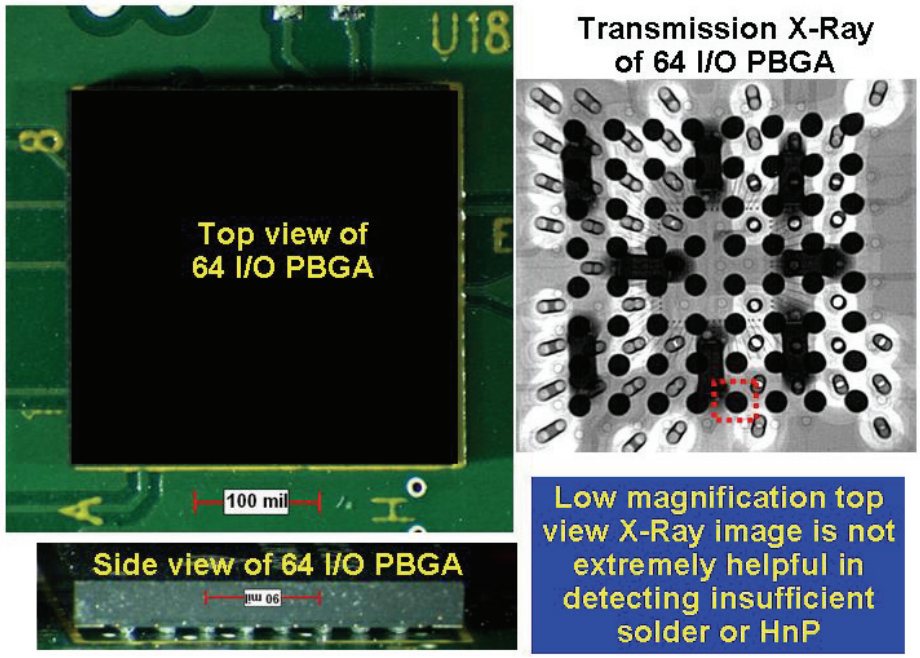


Figure 21. Conventional 2D x-ray imaging is not adequate for detecting HnP or insufficient solder defects.

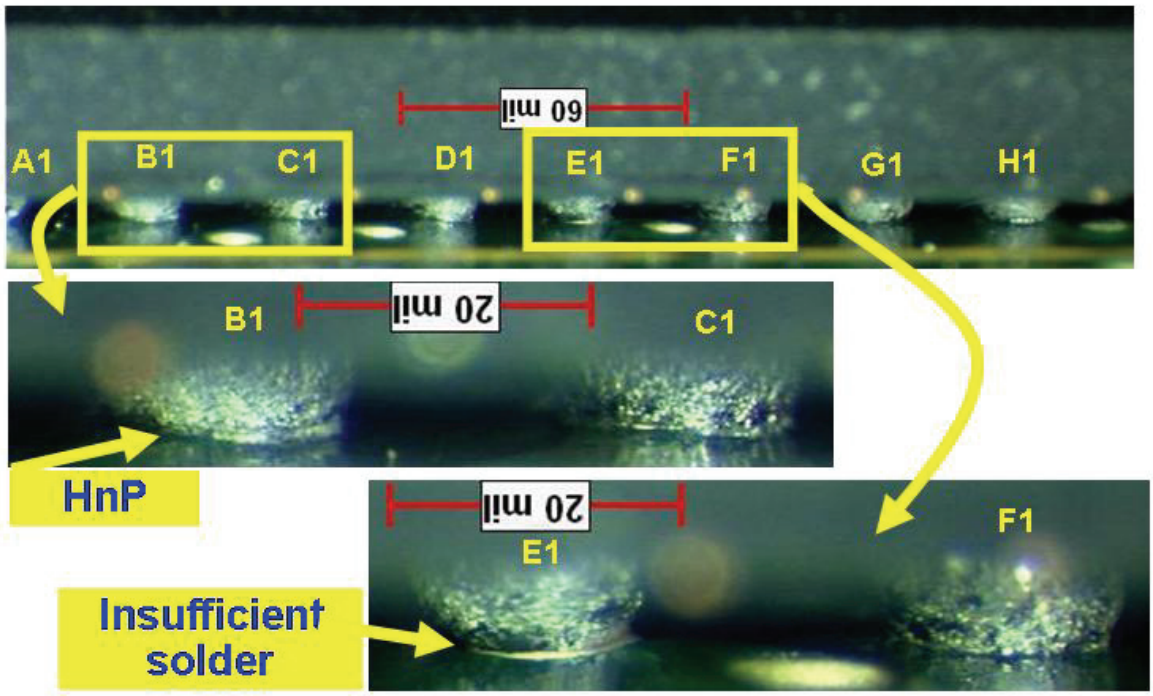


Figure 22. Optical inspection images of outer edges of BGAs is a time-consuming process but it may be necessary to detect HnP or insufficient solder defects.

Root Cause Analysis

Although the defects seen in Case Study 3 are at or near the outside edge of packages, the different types of defects including lumpy joints, HnP, insufficient and no-solder defects suggest that there are quality and process problems in addition to package warpage. Although some of the HnP intermittent solder joint defects were detected during visual inspect after an NPI build, functional testing of other boards during Design Verification Testing (DVT) revealed intermittent solder joints on boards that passed optical inspection. The incurred cost of these product assemblies and the customer demands prohibited the type of destructive physical analysis that was done in Case Studies 1 and 2. A few of the defective NPI boards were re-flowed using a BGA repair station and a few were re-reflowed using the original SMT assembly process in an attempt to fix

the intermittent solder joints. The additional heating cycles seemed to help on some boards but they did not correct all the intermittent defects. It is important to note that even some that appeared to be corrected again failed during subsequent DVT.

In an effort to determine the root cause for the intermittent and HnP defects, a detailed review of the assembly process and operations was conducted. This review determined that while package and board warpage was certainly a major contributing factor to HnP defects, the situation was exacerbated by insufficient attention to the up-front assembly process, specifically solder paste and stencil printing. Many of the automatic inspection features of stencil printing machines were not being used and inspection of solder paste prints for area array packages was only being conducted on the initial board processed. More importantly, it was found that solder paste time on a stencil was not being monitored and the practice of not recording the re-use of solder paste was not only causing poor release of solder paste from stencil apertures but also the partially dried out paste was reducing the fluxing action during reflow.

Corrective Action

The initial corrective action was to increase the solder paste volume by using a thicker stencil. What at first appeared to be an easy and obvious corrective action for insufficient and HnP defects, actually resulted in increased frequency of defects. The real mitigation for insufficient and HnP solder joint defects in this NPI assembly was to insure that the correct amount of a "good" solder paste was applied to each area array package footprint. This entailed monitoring solder paste out-of-jar exposure time, using more of the stencil printer automatic inspection features, and manually inspecting solder paste prints on all area array footprints. Utilization of a solder paste specifically formulated to address HnP defects and laser cut and electroformed stencils instead of chemically etched stencils also proved helpful in mitigating insufficient and HnP defects. Increasing stencil apertures helped release of solder paste and increased solder paste volume but also increased the occurrence of solder bridges. From a solder assembly process perspective, the root cause of the HnP defect was the result of the sum of all the component and assembly process tolerances.

Summary – Mitigating HnP in NPI Environment

The lessons from Case Studies 1 and 2 have shown that component tolerance issues are an important factor in HnP defects and the results from Case Study 3 have shown that stricter assembly process controls may be required. It is important to recognize that conventional or historical specifications and guidelines may not be sufficient to prevent solder defects such as HnP within the constraints of the current design and manufacturing environments.

DISCUSSION

Root Cause of HnP

There are several factors that can contribute to the HnP phenomena including package co-planarity, package warpage, PCB warpage, and assembly issues associated with solder paste characteristics and stencil printing. There would be far less incidents of HnP if package warpage was eliminated completely but of course, that is not practical. Furthermore, BGA package warpage and coplanarity issues have existed since the advent of non-ceramic substrates [5]. While the case studies presented in this paper certainly suggest that warpage is a major contributor to HnP, they also show that the HnP root cause often results from a build-up of all of the component, printed circuit board, and assembly process tolerances. Tolerance build-up can in fact, lead to HnP with packages that meet nominal package warpage specifications.

In an indirect way, the ongoing conversion to Pb-free manufacturing may be partly responsible for the increase in HnP defects. Over the past 5 years, device suppliers and packaging houses have been modifying their offerings in preparation for compatibility with high temperature, Pb-free assembly processes. As a result, most of the current BGA package offerings exist in SnPb and Pb-free versions, with the only physical difference being the solder ball composition. However, these packages must now perform adequately for both SnPb and Pb-free soldering applications, which includes a significantly larger temperature range than the SnPb process alone. These case studies show that HnP defects are not limited to Pb-free assembly and can occur with typical SnPb solder assembly. Furthermore, some of the warpage data indicate that performance may be adequate for one reflow range but not the other (SnPb vs. Pb-free).

Industry Standards

There are two major industry standards for package warpage, the JEDEC, U.S. Standards [8-10] and JEITA, Japanese Standard [11]. The JEITA standard has the tighter tolerances and many devices, including several discussed here, fail to meet this standard. At the same time many of these devices that met the JEDEC standards exhibited HnP assembly defects in production. This would imply that the JEDEC standards do not sufficiently account for the end-point manufacturing requirements and constraints. This can create awkward situations in terms of corrective action when the warpage is indicted as the root cause of HnP but the industry standard does not support that conclusion.

Inspection and Detection of HnP

Detection of HnP defects is challenging, even when they are located in the outer, more accessible rows. There is no doubt that BGA video cameras and other optical or visual methods can detect HnP and sophisticated 5DX X-ray systems can detect some but not all HnP defects. The problem is that the manner in which that these methods are used in routine factory inspections is likely to find the HnP defects. These methods are best at finding defects when they are used as custom inspection tools, which requires skilled operators and is not compatible with high speed production.

Rework or Repair of HnP

When an open circuit BGA failure is detected, there may be an attempt to correct the problem by re-reflowing the BGA solder joints using either the SMT line or a BGA repair station. Reflow or repair methods were applied to the HnP defects in Case Study 3 and the results were mostly unacceptable. This should not come as a surprise, since same warpage that caused the original defect again will come into play during subsequent reflows. Another major reason that HnP rework is undependable is because "HnP" is not a single defect mode but rather a spectrum of solder defects as illustrated in Figures 10-12. In Case Study 3, some of those defect structures responded positively to re-melting, while others continued to fail. Even more importantly, some that appeared to be corrected initially again failed during subsequent testing. The real concern is that re-reflowing may only "stick" these interfaces together without forming a true solder joint as shown in Figure 10. These latent defects can escape manufacturing and fail in service. For this reason, these repair operations are considered high reliability risks and are not recommended even if the defect population is fairly well-characterized.

CONCLUSIONS AND RECOMMENDATIONS

The conclusions and recommendations from the HnP defect analyses for the three telecommunications Case Studies are as follows:

- BGA package warpage is a major contributor to HnP defects, but HnP can occur when almost any of the assembly process parameters deviate from acceptable practices. Often tolerance build-up of all the process parameters leads to HnP defects. This can happen even in cases where package performance is consistent with existing industry warpage specifications.
- HnP defects are not limited to Pb-free assembly and can occur with typical SnPb solder assembly.
- If a device or package exhibits HnP due to peak warpage at SnPb soldering temperatures, it may not necessarily exhibit susceptibility to HnP defects when used at higher, Pb-free soldering temperatures.
- Stencil printing modifications that provide additional paste volume at the potential HnP sites can be used to bridge the gap during reflow and minimize HnP. This is not a foolproof technique; its effectiveness will depend on the magnitude and extent of the relative warpage between the BGA component and the PCB. The specific application shown here of the 144 I/O FBGA may represent a worse case scenario, in which yields will be defined by a tradeoff between bridging and effective soldering resulting from additional solder volume.
- Together, these results show that the root cause analysis and characterization of a specific case of HnP and recommended corrective action may not be appropriate for other applications of the same BGA package. It is recommended that specific empirically-based guidance be developed for each case of HnP, and each combination of BGA and PCBA design.
- Routine factory BGA inspection systems and electrical test methods can not be expected to detect, screen or eliminate all HnP defects.
- Adherence to conventional specifications and guidelines may not be sufficient to prevent HnP solder defects within the constraints of the current design and manufacturing environments. When package warpage is the primary cause of HnP, the only practical corrective action available to manufacturing is to develop custom assembly processes and methods and diligently monitor their effectiveness in practice.
- Case Study 2 showed that the SPI (solder process inspection) and additional quality monitoring that exceeded conventional manufacturing practices were critical in order to maintain control and enable success over a relatively narrow window. Deviation from this narrow, custom process window caused the HnP defects.
- Correcting HnP defects by re-reflowing (re-melting) is considered a high reliability risk and is not recommended.
- Industry standards organizations could ameliorate the HnP situation by scrutinizing the cause and effect relationship between package warpage and HnP and by developing guidelines that would drive improvements in package warpage performance. Process modifications can mitigate HnP defects but may not eliminate defects or "escapes." Additionally, these mitigation practices tend to shrink process windows, and make overall process control more difficult and costly. Even moderate increases in defect and field return rates can be devastating in today's cost-conscious environment. The preferred corrective action is to minimize warpage to the extent that extraordinary process modifications and controls can be avoided.

ACKNOWLEDGMENTS

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Telecommunications Case Studies Address Head-in-Pillow (HnP) Defects and Mitigation through Assembly Process Modifications and Control

Russell Nowland[1], Richard Coyle[1],
George Wenger[2], and Peter Read[1]

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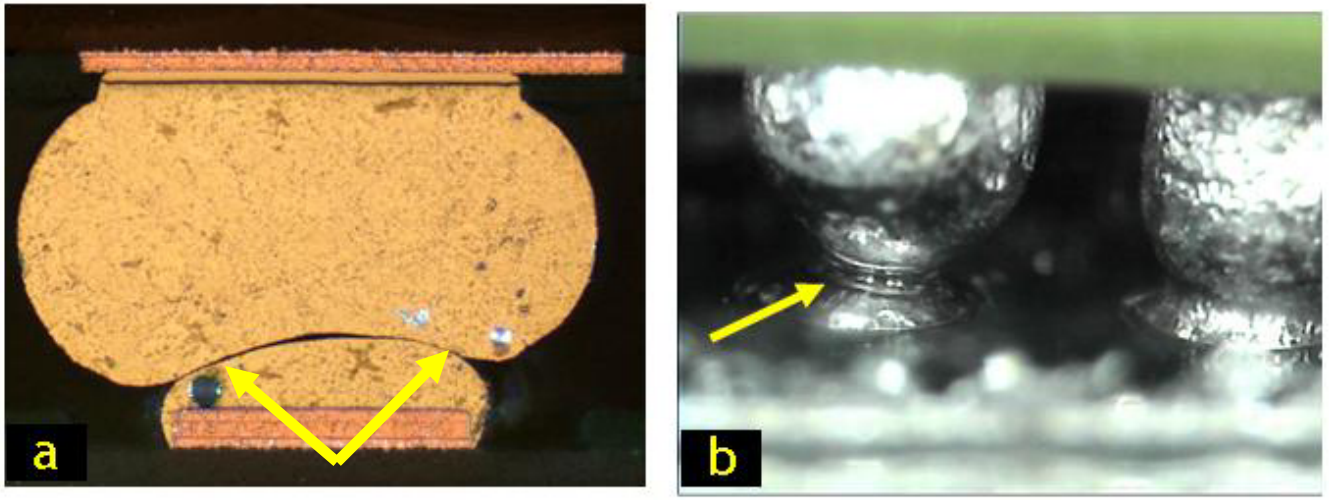
OUTLINE

- Background Information
- Head-in-Pillow (HnP) Defect Formation
- 3 Case Studies of HnP (144 I/O FBGA, 484 I/O PBGA, multiple BGAs in NPI)
  - Problem statement
  - Root cause Analysis
  - Corrective action or mitigation
- Discussion
- Conclusions and Recommendations

HEAD-in-PILLOW (HnP) DESCRIPTION

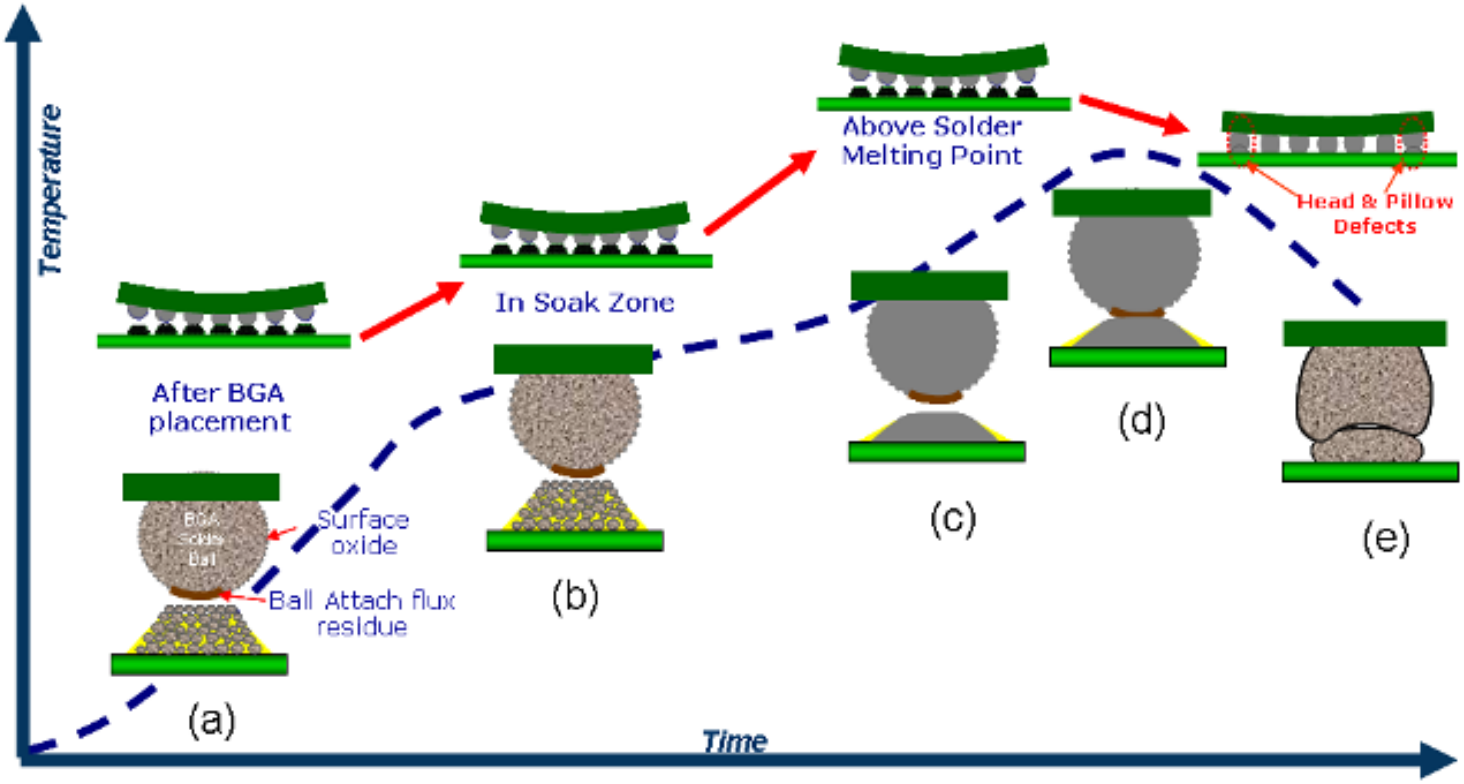
- Evolving package and PCB technologies have resulted in an increase in an open or intermittent ball grid array (BGA) defect called *head-in-pillow* (also called head-on-pillow, head and pillow, ball-in-cup, ball and socket).
- Head-in-Pillow (HnP) is characterized by complete melting of both the solder paste and the BGA solder ball but with insufficient coalescence to produce well-formed solder joints.



The solder ball and paste melted but did not coalesce.

HEAD-in-PILLOW DEFECT MECHANISM

- HnP defects are created when a gap develops between the ball and the solder paste during the reflow process due to dynamic warpage of the package or PCB. Insufficient flux activity on the surface of the ball or contamination on the solder ball or molten solder paste prevents coalescence.



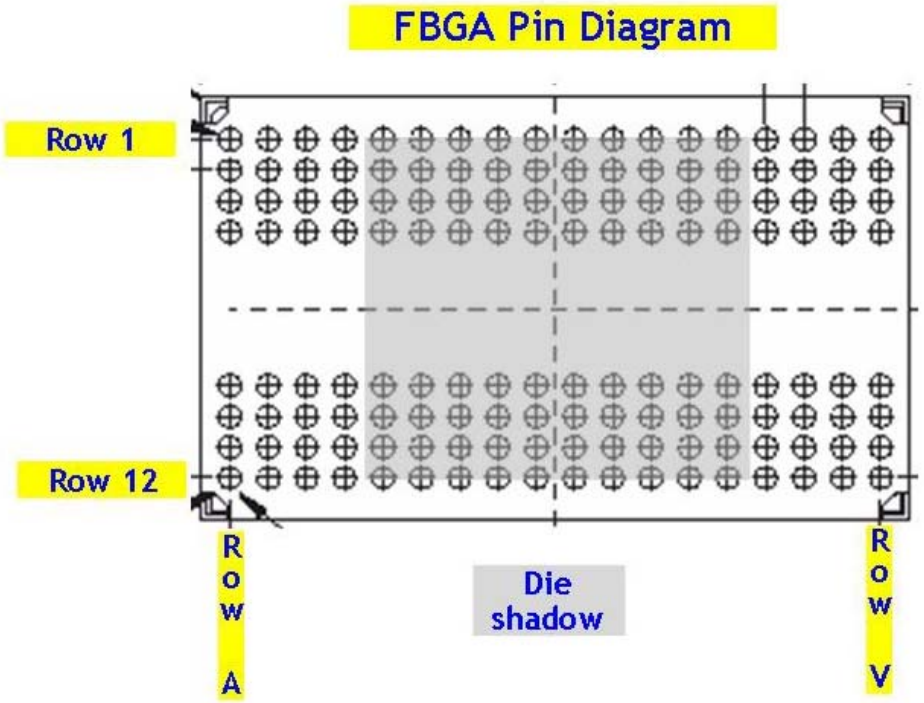
from Amir et al (Intel), SMTAI 2009

CASE STUDY 1

144 I/O FINE PITCH BGA (FBGA)

Problem Description

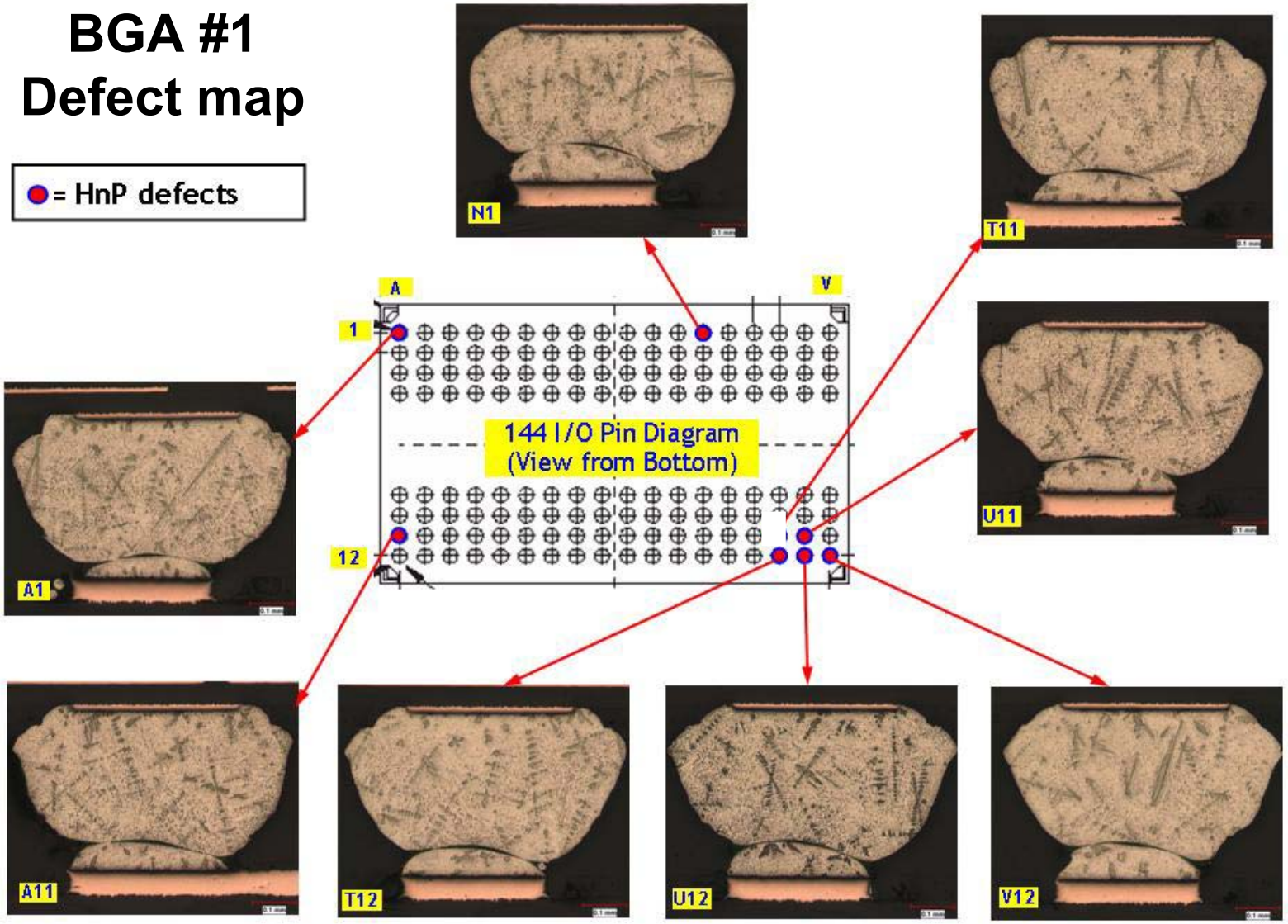
- Multiple ***SnPb*** 144 I/O 0.8 mm pitch FBGA components are soldered onto a large telecom PCBA
- Each BGA location on the PCBA has a unique occurrence frequency and pattern of HnP defects.
- Device supplier data indicated that component was not sensitive to HnP defects when used in a ***Pb-free solder*** assembly process.



CASE STUDY 1
144 I/O FINE PITCH BGA (FBGA)

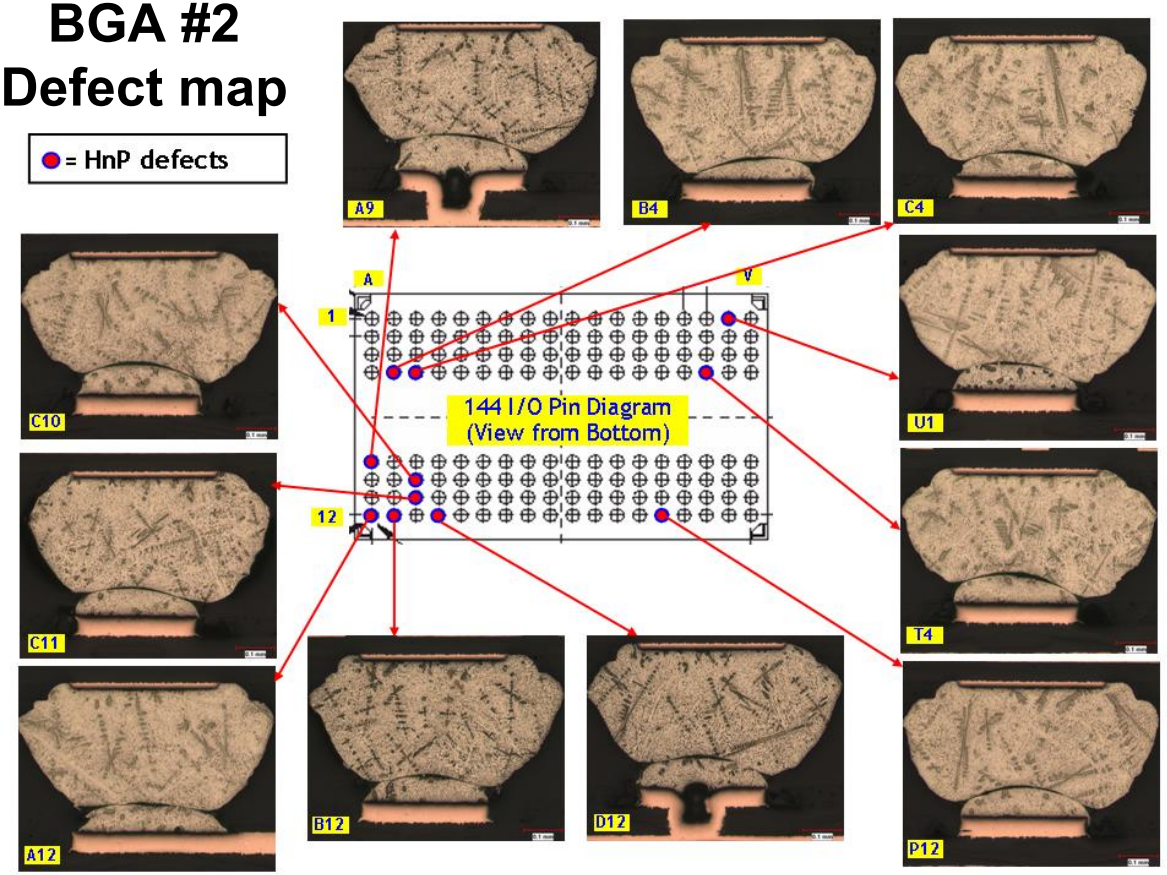
BGA #1
Defect map

● = HnP defects



CASE STUDY 1
144 I/O FINE PITCH BGA (FBGA)

BGA #2
Defect map

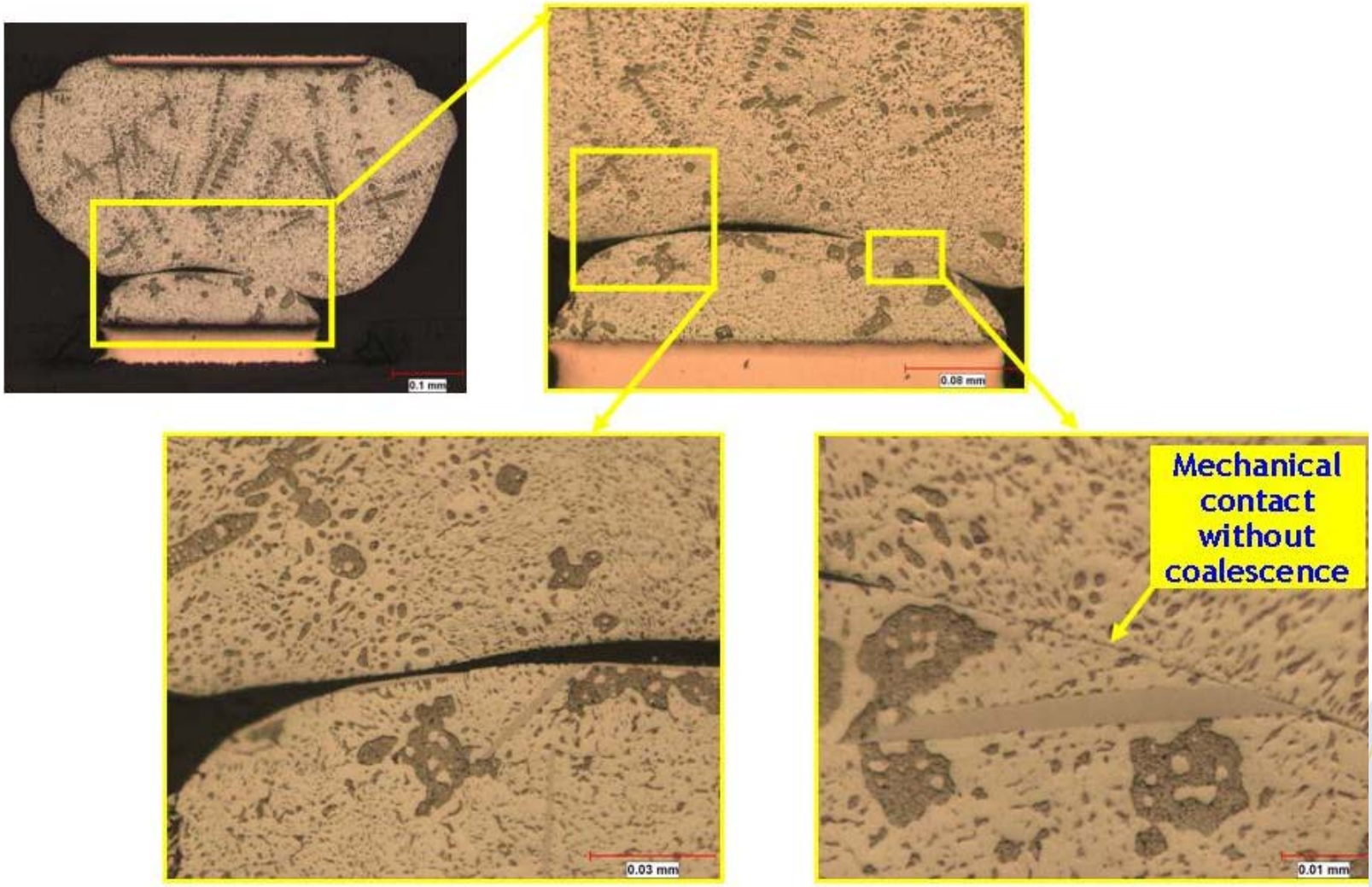


- **Variations in HnP appearance.**
- **Defects not limited to the corners or edges of the package.**

CASE STUDY 1
144 I/O FINE PITCH BGA (FBGA)

This is an insidious type of HnP defect because it can escape manufacturing and result in an early failure.

BGA #1 U11



CASE STUDY 1

144 I/O FINE PITCH BGA (FBGA)

Observations

- Identical devices have very differently HnP signatures when assembled onto two different locations of the PCBA.
- Defects are not *limited* to the corners or edges of the packages, the number of defects varies by PCBA location, and the defect patterns are not symmetric for the two packages.
- The HnP problem is not limited to Pb free assembly. Peak warpage occurs at SnPb peak temperature

Moiré Data

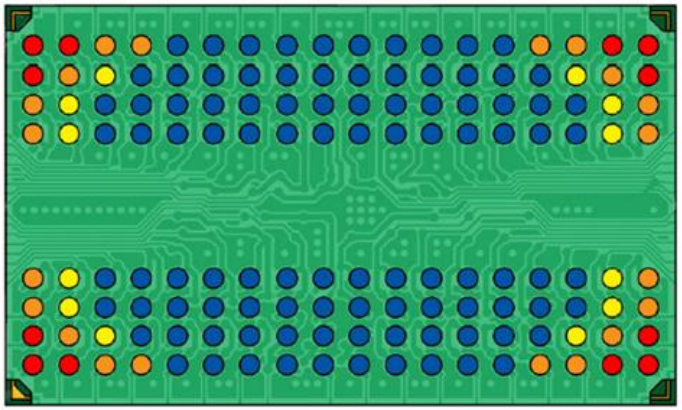
Temperature °C	Warpage μm
30	70
75	31
150	98
220	**137**
240	131
260	115
240	98
220	81
150	52
75	42
30	80

CASE STUDY 1

144 I/O FINE PITCH BGA (FBGA)

Corrective Action

Proposed Stencil Modification for Mitigation of FBGA HnP Defects



- Typical Circular Opening of 1:1
- Circular Opening + 25um to Radius
- Circular Opening + 38um to Radius
- Circular Opening + 50um to Radius

Based strictly on the actual location of defects, the proposed modified stencil would provide additional solder paste volume on ~75% of the affected PCB pads.

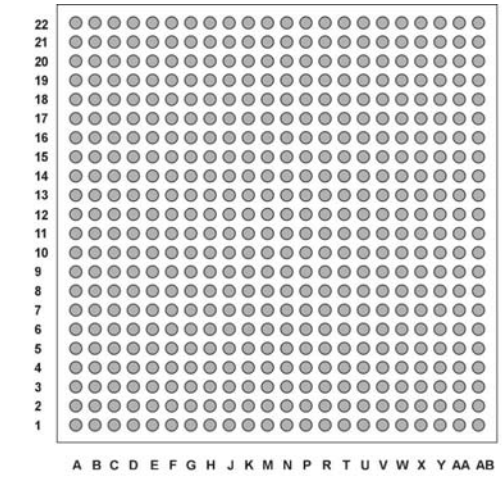
- **There are limitations to mitigating HnP though paste printing.**
- **Note: This modification proved successful in some applications of the 144 I/O FBGA.**

CASE STUDY 2

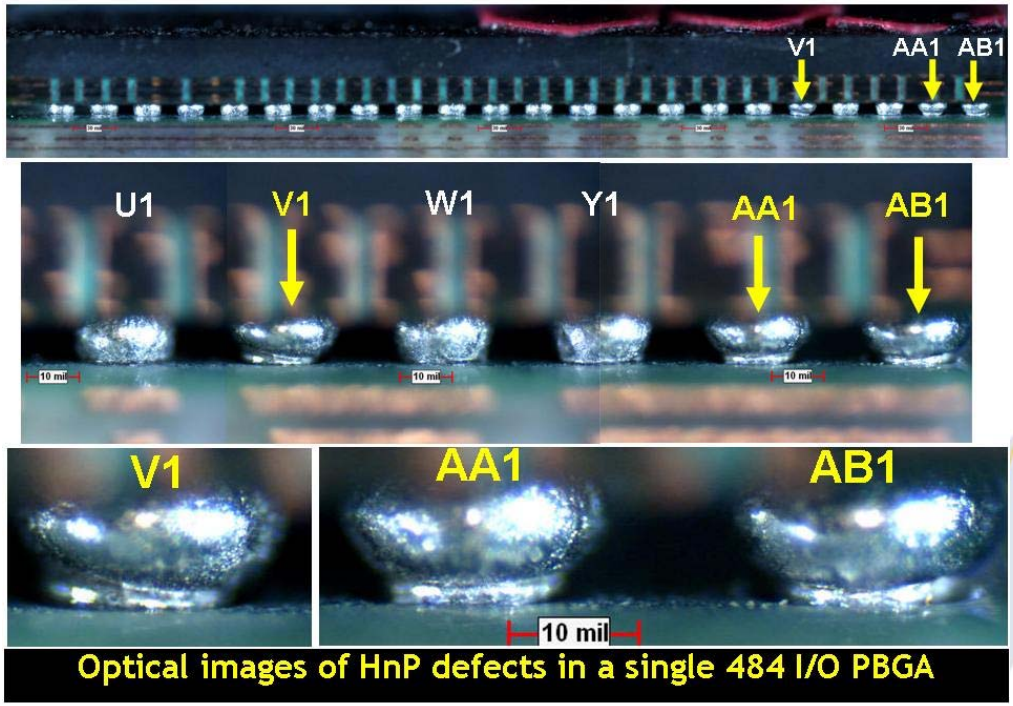
484 I/O 0.8 mm Pitch Plastic Ball Grid Array (PBGA)

Problem Description

- The SnPb PBGA exhibited erratic production yields when used in a complex telecommunication PCBA. The PCBA contained an array of multiple components. Only some of the sites had HnP defects, the frequency of defects varied dramatically from one PCBA to another, and the overall yield was approximately 80%. Defects were mostly localized at the corners and in the outer rows of the BGA but each component location and PCBA had a unique pattern or number of HnP defects.



484 I/O BGA PIN DIAGRAM

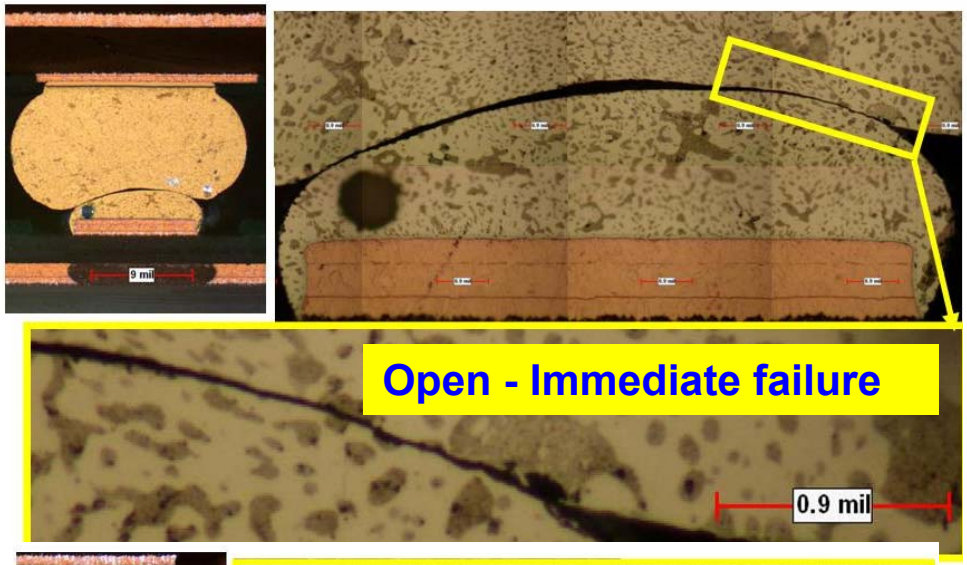


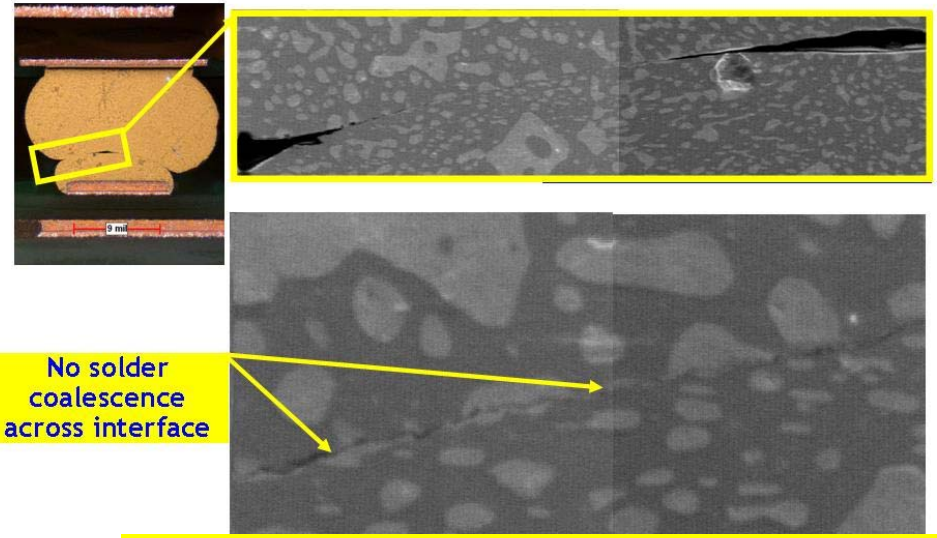
Optical images of HnP defects in a single 484 I/O PBGA

CASE STUDY 2

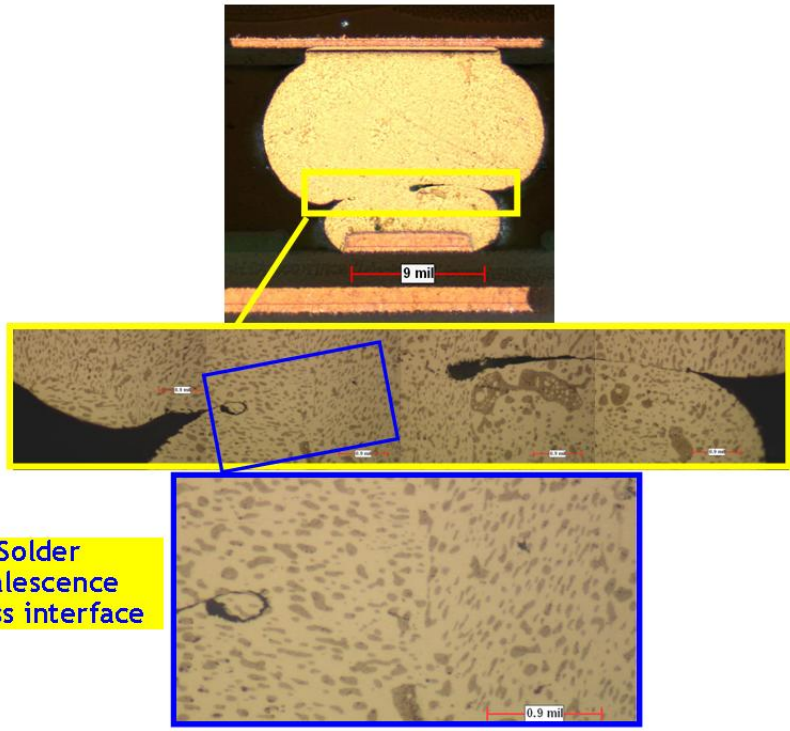
484 I/O 0.8 mm Pitch Plastic Ball Grid Array (PBGA)

Three Different Types of HnP





Contacting – Early failure risk (cold solder joint)



Soldered – Possible long term reliability risk

CASE STUDY 2

484 I/O 0.8 mm Pitch Plastic Ball Grid Array (PBGA)

Three Different Types of HnP

Root Cause Analysis

- Peak warpage occurs in the critical range of SnPb reflow

Summary of Shadow Moiré results for 4 different 484 I/O PBGA components.

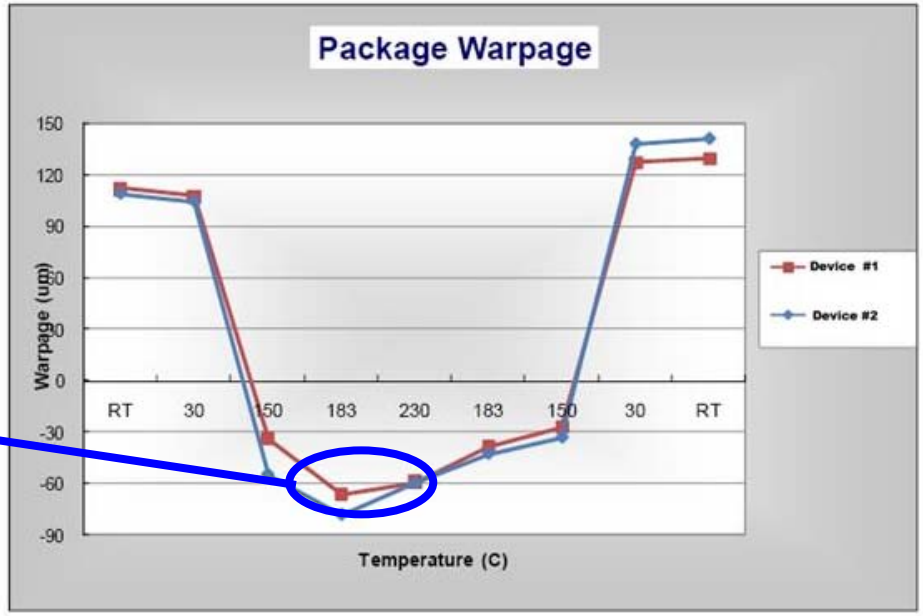
Device Number	Initial Warpage μm (microns)	Peak Warpage μm (microns)	Total Variation μm (microns)
1	91.4 @ (22ºC)	68.6 @ (230ºC)	160.0
2	104.1 @ (22ºC)	83.8 @ (180ºC)	188.0
3	99.1 @ (22ºC)	58.4 @ (210ºC)	157.5
4	96.5 @ (200ºC)	104.1@ (90ºC)	200.7

CASE STUDY 2

484 I/O 0.8 mm Pitch Plastic Ball Grid Array (PBGA)

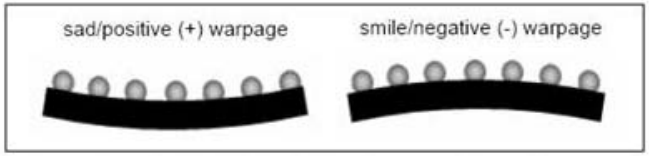
Three Different Types of HnP

Root Cause Analysis – Warpage-Induced HnP Defects



HnP defects form in this temperature range

Date Code	RT	30	150	183	230	183	150	30	RT
849	112	108	-34	-66	-59	-39	-27	127.5	129.5
902	109	105	-55	-78	-59.5	-43	-33	138	141



Maximum device warpage=8.6 mils
Maximum deviation from flatness at high temperature=3.1 mils

Note: "Smile" and "sad" refer to orientation on PCB

CASE STUDY 2

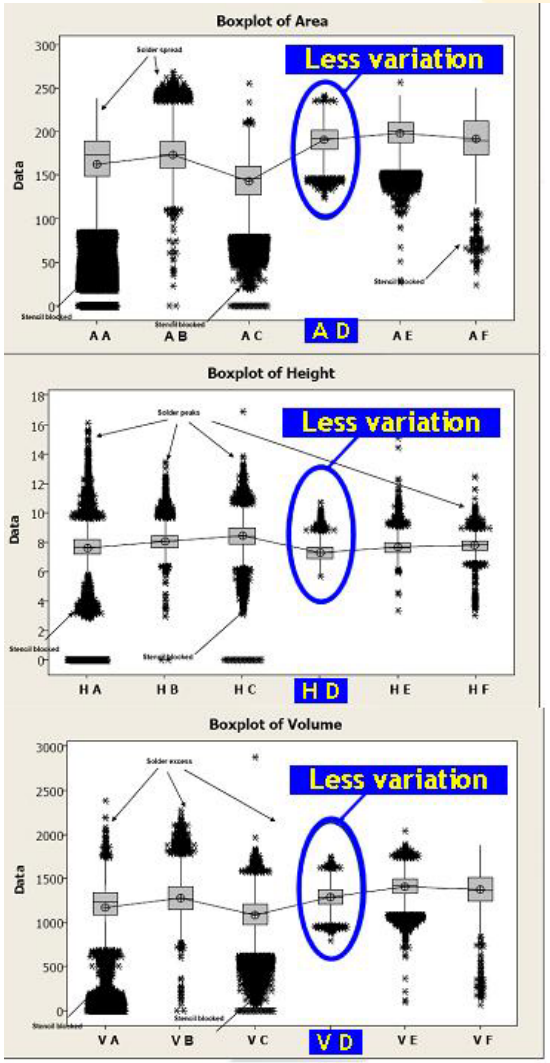
484 I/O 0.8 mm Pitch Plastic Ball Grid Array (PBGA)

A two-phase solder process analysis was conducted based on the results of the warpage analysis.

- Phase 1 – Conduct a DOE to evaluate solder paste printing of 6 commercial solder pastes.

- Phase 2 – Evaluate the relationship between solder printing, assembly, and propensity for HnP.

- Solder paste "**D**" was the best performer with the lowest variations in area, height, and volume in Phase 1.



CASE STUDY 2

484 I/O 0.8 mm Pitch Plastic Ball Grid Array (PBGA)

- Solder paste "**D**" was the best performer with the highest overall assembly yield and was selected for process corrective action
- The comprehensive corrective action plan included solder paste selection, stencil print modifications, enhanced inspection techniques, and diligent monitoring of all the processes

Operation	B	D	F	A
SMT Bottom	80.00%	85.51%	84.00%	98.00%
SMT Top	84.00%	42.03%	84.00%	92.00%
5DX	86.00%	75.38%	88.00%	88.00%
ICT	86.00%	82.81%	85.71%	86.00%
Functional Test	100.00 %	100.00 %	100.00 %	100.00 %
Thermal Test	89.19%	93.44%	87.88%	81.25%

Overall assembly results for pastes A, B, D, & F.

Operation	B	D	F	A
SMT Bottom	0	0	0	0
SMT Top	0	0	0	0
5DX	1	1	0	0
ICT	4	0	1	10
Functional Test	1	0	2	3
Thermal Test	5	1	1	0

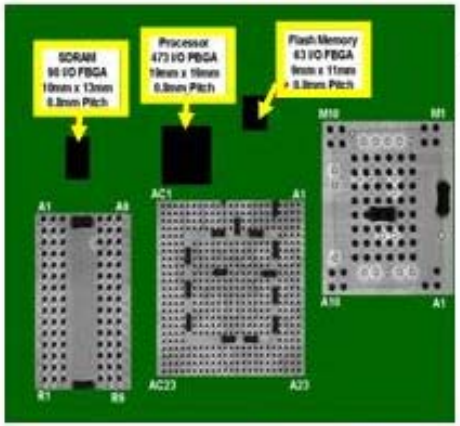
484 I/O PBGA device defects

CASE STUDY 3

BGA HnP in New Product Introduction (NPI)

Problem Description

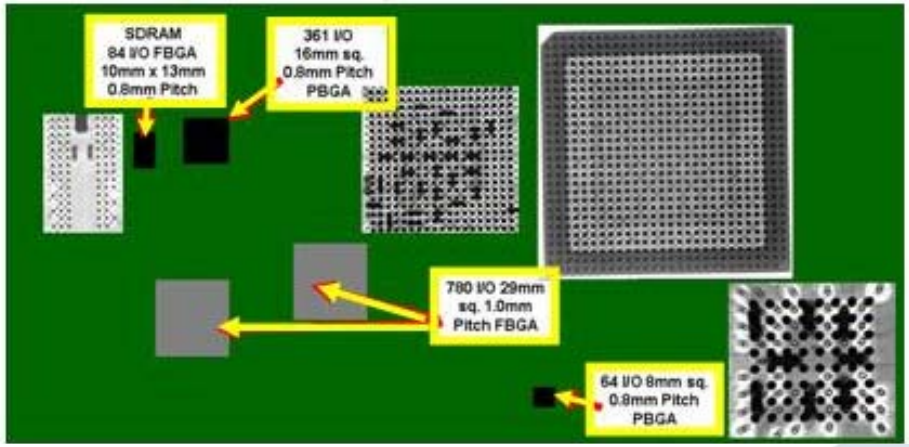
- Design cycles have been reduced from years to months, and multiple designs are being developed simultaneously to meet customer demands. The combination of high-mix, low-volume, product diversity, and aggressive schedules is causing an increased occurrence of HnP.



a). 6.5" x 5.0" x 0.062"thick

Complex telecommunication products come in many configurations and utilize various BGAs from many component vendors

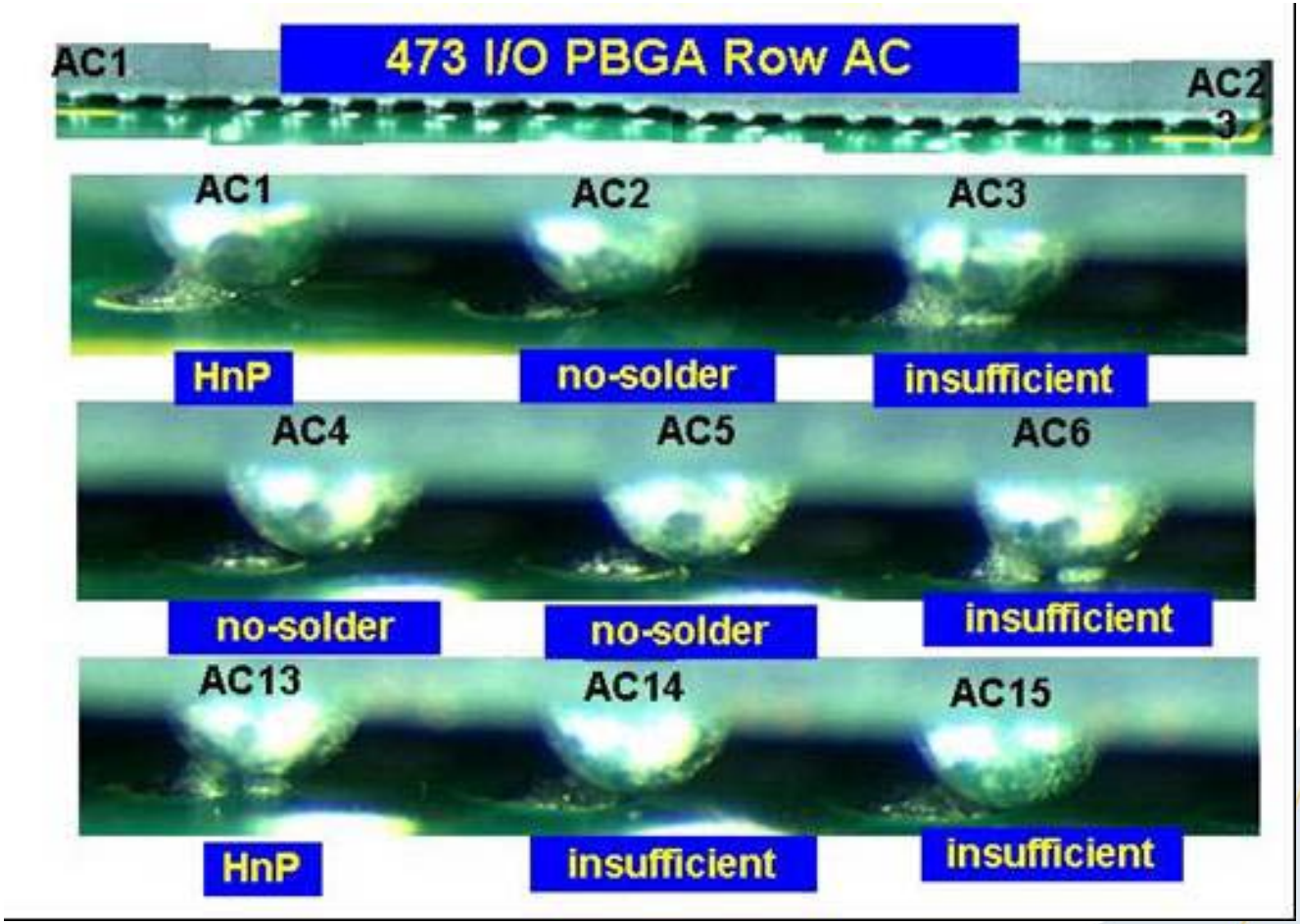
b). 15" x 8" x 0.093"thick



CASE STUDY 3

BGA HnP in New Product Introduction (NPI)

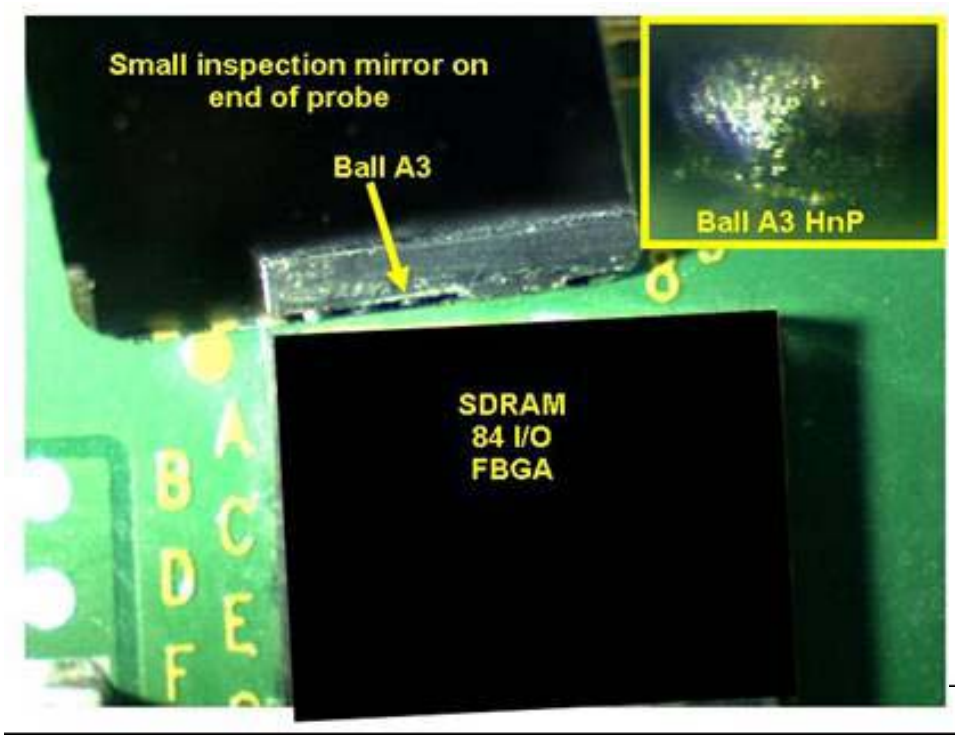
- **Various solder defects including insufficient and no-solder defects, *in addition* to HnP suggest that there are quality and process problems besides package warpage.**

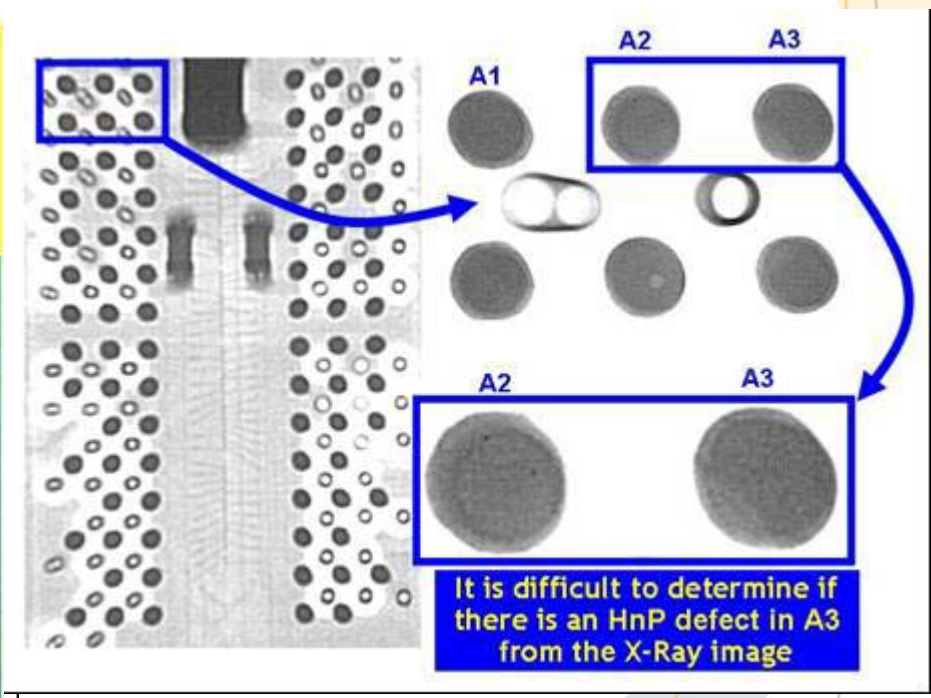


CASE STUDY 3

BGA HnP in New Product Introduction (NPI)

- HnP defects in 84 I/O SDRAM
- Note: HnP can not be identified with X-ray

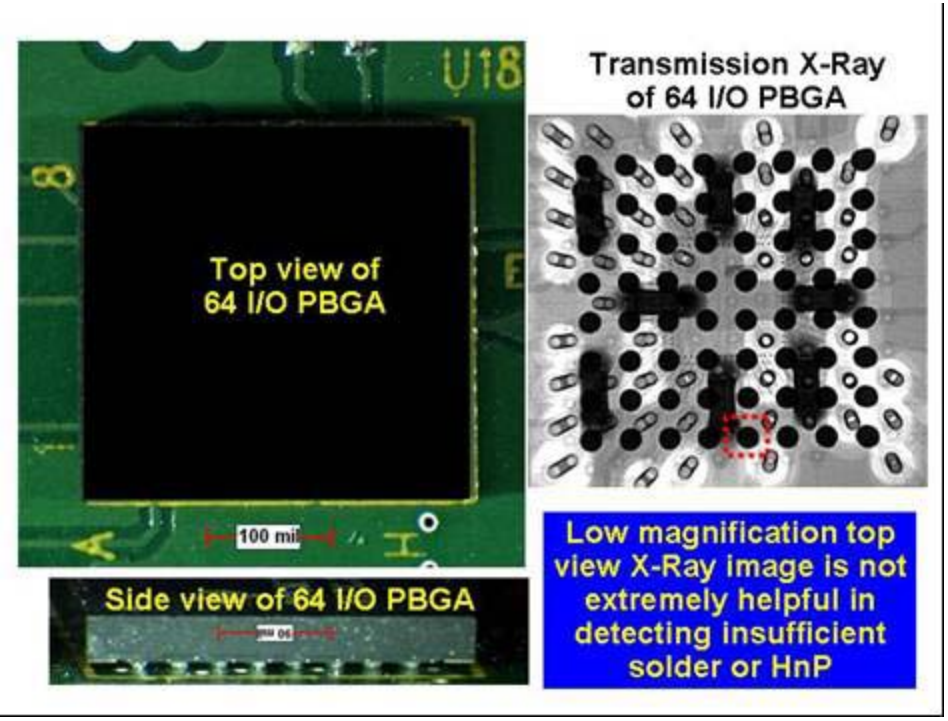


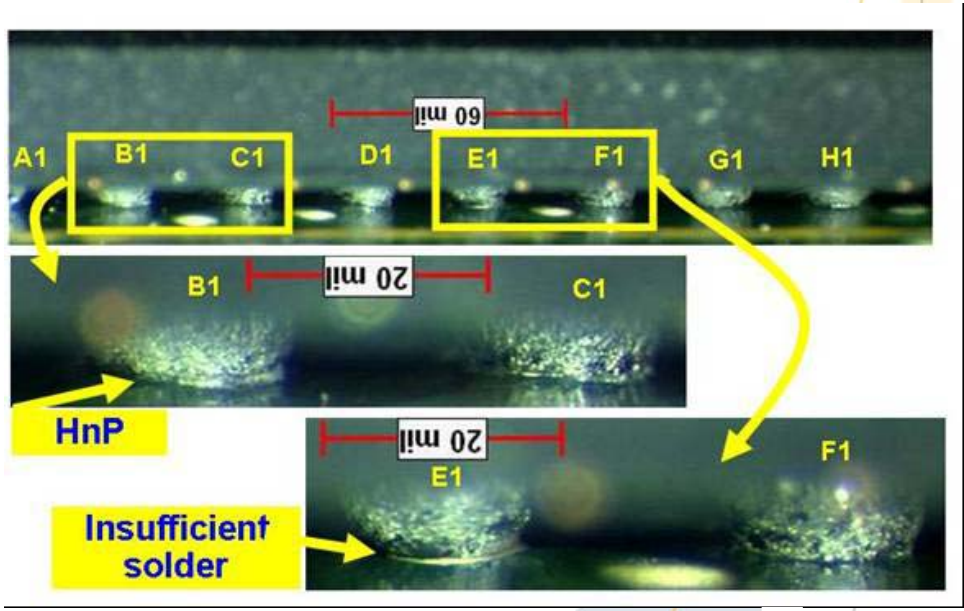


CASE STUDY 3

BGA HnP in New Product Introduction (NPI)

- HnP defects in 64 I/O PBGA can not be identified with 2D X-ray
- Time-consuming manual optical inspection may be required





CASE STUDY 3

BGA HnP in NPI

Root Cause and Corrective Actions

- Package and board warpage was a major contributing factor. HnP was exacerbated by insufficient attention to the up-front assembly process, specifically solder paste and stencil printing.
- HnP was reduced by insuring that the correct amount of a “good” solder paste was applied to each area array package footprint. This entailed monitoring solder paste out-of-jar exposure time, using the stencil printer automatic inspection features, and manually inspecting solder paste prints on all area array footprints.
- Increased stencil apertures helped release of solder paste and increased solder paste volume but also increased the occurrence of solder bridges.
- HnP was reduced by utilizing solder paste specifically formulated to address HnP defects and laser cut and electroformed stencils instead of chemically etched stencils.
- From an assembly process perspective, the root cause of HnP was the result of the sum of all the component and assembly process tolerances.

CONCLUSIONS and RECOMMENDATIONS

- BGA package warpage is a major contributor to HnP defects. Tolerance build-up of all the process parameters also leads to HnP defects, even in cases where package performance is consistent with industry warpage specifications.
- When package warpage is the primary cause of HnP, the only practical corrective action available to manufacturing is to develop custom assembly processes and methods and diligently monitor their effectiveness in practice.
- Stencil printing modifications can be used to bridge the gap during reflow and minimize HnP. Process modifications can mitigate HnP defects but may not eliminate defects or “escapes.” Additionally, these mitigation practices tend to shrink process windows, and make overall process control more difficult and costly.
- The root cause analysis and characterization of a specific case of HnP and recommended corrective action may not be appropriate for other applications of the same BGA package. It is recommended that specific empirically-based guidance be developed for each case of HnP, and each combination of BGA and PCBA design.

CONCLUSIONS and RECOMMENDATIONS

- HnP defects are not limited to Pb-free assembly and can occur with typical SnPb solder assembly.
- Routine factory BGA inspection systems and electrical test methods can not be expected to detect, screen or eliminate all HnP defects.
- Correcting HnP defects by re-reflowing (re-melting) is considered a high reliability risk and is not recommended.
- Industry standards organizations should work to reduce the incidence of HnP by developing guidelines that would drive improvements in package warpage performance.
- The preferred corrective action is to minimize warpage to the extent that *extraordinary* process modifications and controls can be avoided. In these case studies, warpage was a major contributor to HnP defects but the situation was exacerbated by insufficient attention to the up-front assembly process, specifically solder paste and stencil printing.