

Benefits and Limitations of Universal, low-pin count Automated Test Equipment for Printed Circuit Assemblies

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Abstract

This paper discusses the benefits and limitations of universal, low-pin count Automated Test Equipment for Printed Circuit Assembly (PCA) testing utilizing the test access port (TAP) defined in IEEE Std. 1149.1. The test equipment under consideration allows the application of a wide variety of JTAG/Boundary Scan connectivity and pseudo functional tests, ideal for use as a desktop test system for prototype verification and production test. In particular, we will present ways of creating test applications that utilize embedded test resources in the Unit Under Test (UUT) and tester channels provided by the ATE in a compact and all-inclusive fashion. The paper will also discuss overall cost of test reductions achievable with such test equipment.

Introduction

Before discussing the benefits and limitations of universal, low-pin count Automated Test Equipment utilizing the test access port (TAP) defined in IEEE Std. 1149.1, we are going to compare some of the most commonly used test methodologies in today's electronics manufacturing environment. Table 1 compares six such test methodologies at a qualitative level, summarizing the capabilities to detect certain types of defects and pointing out major benefits and disadvantages of each method. The six test methodologies compared here are Automated Optical Inspection (AOI), Automated X-Ray Inspection (AXI), In-Circuit Test (ICT), Flying Probe Test (FPT), Functional Test (FT), and Boundary Scan (BScan). [1] [2] [3]
We have listed a number of different types of faults, classified in Soldering Defects, Placement Errors, and Electrical Defects. The first category includes **Soldering Defects**:

- **Visible Shorts**, for example, can be detected by all six test methodologies. One may not want to use X-Ray inspection to look for this type of defect, though, since X-Ray equipment is expensive and X-Ray tests are typically slow.
- For **Hidden Shorts**, on the other hand, X-Ray is a good inspection methodology, whereas AOI obviously cannot detect such hidden shorts. In-Circuit Test, Flying Probe Test, Functional Test, and Boundary Scan, all can detect hidden shorts because they actually test the electrical properties of the Unit Under Test, rather than just visually inspecting the UUT.
- **Visible Opens**, again, can generally be detected by all six test methods, while
- **Hidden Opens** cannot be detected by AOI equipment and may be difficult to detect with X-Ray equipment.
- Inspection equipment is good, though, for analyzing the **Quality of solder joints**, whereas the other four test methods compared here cannot say much if anything about solder joint quality.

Moving on to the second category, **Placement Errors**:

- **Missing components** can generally be detected by all six test methodologies, with some exceptions.
- A **wrong component** can typically be detected by the electrical test methodologies, but not by X-Ray inspection. AOI can detect a wrong component only if there is a visually recognizable feature that differentiates it from the correct component and the AOI test is capable of picking up this difference.
- Problems related to **Component orientation**, on the other hand, are typically detectable by AOI, as well as by the electrical test methods. X-Ray inspection, however, usually cannot detect orientation problems.
- **Misplaced or misaligned components** whose device pins still make contact with the pad on the PCB can cause problems later during shipping and handling or once the product is deployed by the end user. Such alignment issues typically can be picked up only by inspection equipment, but not by electrical test methods.

Table 1 - Comparing Test Methodologies

Defect Type	AOI	AXI	ICT	FPT	FT	BScan
Visible Shorts	✓	✓*	✓	✓	✓	✓
Hidden Shorts	–	✓	✓	✓	✓	✓
Visible Opens	✓	✓*	✓	✓	✓	✓
Hidden Opens	–	Difficult	✓	✓	✓	✓
Solder Quality	✓	✓	–	–	–	–
Missing Component	✓	✓	✓	✓	✓	Partially
Wrong Component	Partially	–	✓	✓	✓	Partially
Orientation	✓	–	✓	✓	✓	✓
Misplaced / Alignment	✓	✓	–	–	–	–
Defective Component	–	–	✓	✓	✓	✓
Defective PCB	–	–	✓	✓	✓	✓
ESD / EMI	–	–	Partially	Partially	✓	Partially
Design Problems	–	–	–	–	✓	Partially
Software Defects	–	–	–	–	✓	Partially
Benefit	Early in Process	X-Rays	Fast	No Fixture	Functional	Versatility
Disadvantage	No Electrical Test	High Cost	Requires Fixture	Slow	High Cost	Digital Only**

* not reasonable

** new standards and tester specific capabilities add mixed signal and analog capabilities

The third category of defects discussed here, **Electrical Defects**, per definition cannot be detected by inspection equipment. The four electrical test methods vary in their capabilities to detect these types of defects.

- **Defective components** and **defective PCBs** can typically be identified by all four electrical test methods, while
- **ESD** related problems, **circuit design** related problems, and **software** related faults are typically detectable only by Functional Test equipment and partially by Boundary Scan equipment.

Each of the six test methods discussed here has its merits. AOI, for example, can be used very early in the manufacturing process, keeping the rework cost low. The downside of AOI, however, is the lack of verification of the UUT's electrical properties.

Automated X-Ray Inspection has the benefit of being able to inspect hidden solder joints that otherwise may be difficult to verify. AXI equipment can be very expensive, though, and test execution time can be lengthy. Also, X-Ray equipment does not verify any electrical properties of the UUT.

The main benefits of In-Circuit Test are the speedy test execution and the thorough test of board-level electrical properties, as long as sufficient test access is provided. And that test access can be quite a handicap these days - the bed-of-nail test fixtures ICT requires can become very expensive and the number of circuit nodes that are accessible with nail probes may be rather limited on complex PCBs, reducing the test coverage achievable with ICT.

Flying Probe Testers don't use a bed-of nail fixture like ICT; rather they have a number of independently moving probe heads that can be used to contact accessible circuit nodes. The types of tests a Flying Probe Tester can execute is very similar or even identical to an In-Circuit Tester, however, it does so at a much slower speed, since the circuit nodes are contacted sequentially rather than in parallel.

One might think Functional Test is perfect when looking at Table 1, since it can detect most of the listed defects. However, Functional Test development is usually manual and time consuming, diagnostic capabilities can be rather limited, test execution time can be length, depending on UUT complexity, and Functional Test equipment can be expensive.

Boundary Scan has the benefit of being able to be used throughout the product life cycle and potentially without any fixturing requirements. Boundary Scan tests can even be embedded on a board or in a system, for remote tests and/or to be part of power-on self tests. On the downside, Boundary Scan focuses on digital circuitry. However, Boundary Scan cluster tests, integrations with Functional Test, and new and upcoming IEEE standards can overcome this limitation to a large extend.

Typical JTAG/Boundary Scan test system setups in production environment

Now let's discuss common ways JTAG / Boundary Scan is used in a manufacturing environment.

Figure 1 illustrates a typical electronics manufacturing flow, implementing various test methodologies. Automated Optical Inspection (AOI) is widely used after component placement and before reflow soldering. Any defects detected at this time can usually be reworked quickly and without too much effort. Often there is another AOI or even X-Ray Inspection step after reflow soldering, with the purpose of identifying bad units before passing them on to the next stage and to rework them immediately, if possible. Since inspection methods don't verify the electrical features of the unit under test, most test strategies include at least one electrical test methodology focused on manufacturing defects such as opens and shorts prior to running a functional test. Examples are Flying Probe Testers, In-Circuit Testers, Manufacturing Defect Analyzers, or a combination of those. Those types of testers often times can provide much better diagnostics of manufacturing defects compared to Functional Test. Again, we would want to rework any faulty UUTs prior to spending test time on Functional Test equipment.

For some UUTs it may actually make sense to use a low-cost, benchtop tester that focuses on Boundary Scan testing, perhaps providing a set of analog and digital test channels for additional access through a simple bed-of-nail fixture, to supplement or even to replace ICT or FPT.

Practically all manufacturing test strategies include at least one Functional Test stage to verify whether the product functions per specification prior to shipment to the customer.

None of these mentioned test methodologies is perfect, which is the reason why there is typically a combination of these test methods deployed in electronics manufacturing.

Under certain circumstances it makes sense for Boundary Scan tools to be integrated with other automated test equipment, such as Flying Probe, ICT, or Functional Test. For example, a Flying Probe Tester could provide additional test access for Boundary Scan by strategically placing the flying probes on circuit nodes that otherwise would not be completely testable with Boundary Scan alone. Or, an In-Circuit Test bed-of-nail fixture could be much less complex and less expensive if nails don't need to be provided for circuit nodes that are tested with Boundary Scan. Functional Tests can benefit from the simple pin level access provided by Boundary Scan, which could reduce test development time significantly.

Of course, Boundary Scan can also be applied at rework or repair stations.

Even Automated Optical Inspection systems could make use of integrated Boundary Scan tools, as long as power can be provided to the UUT. That way, Boundary Scan can provide the electrical tests that an AOI machine normally is lacking.

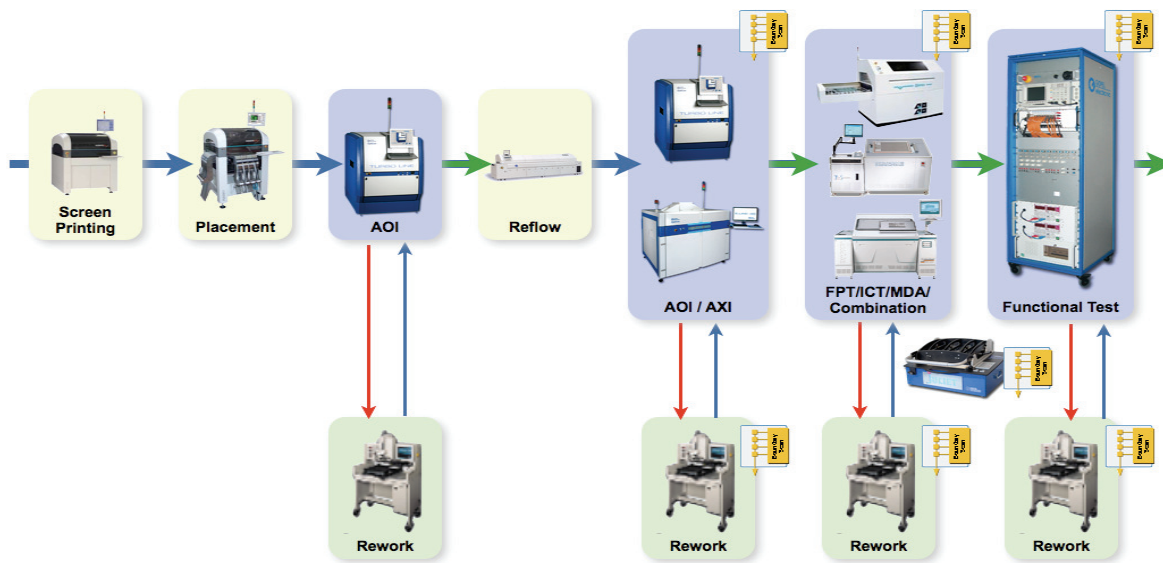


Figure 1 - A typical Production Flow for printed circuit assemblies

A classification of JTAG / Boundary Scan applications

Figure 2 illustrates a classification of JTAG / Boundary Scan applications. One of the most common types of Boundary Scan applications is board level connectivity test. This class of applications includes different types of tests that focus on manufacturing defects such as open pins and shorted nets. This covers mostly the digital parts of the circuitry. Even though Boundary Scan access can be used for the detection of static faults, such as the aforementioned opens and shorts, the test access is limited to Boundary Scan compliant devices and the coverage for dynamic faults is limited. It is desirable to test as much of non-Boundary Scan circuitry as possible with so-called Cluster Tests.

The next class of Boundary Scan applications focuses on in-circuit- or in-system programming of CPLD, FPGA, serial EEPROM and FLASH devices, as well as on-chip memory in micro controllers or digital signal processors, for example.

The third class of applications utilizing the Test Access Port defined in IEEE 1149.1 focuses on device emulation functions applied to board level tests. This includes the functional verification of bus interfaces integrated in a Boundary Scan device as well as structural and functional verification of board level connections to memory devices and bus interface controllers, for example. Many different On-Chip Emulation implementations exist today, with various interfaces and protocols. Nearly all JTAG Emulation structures implemented in ICs are vendor specific designs.

Our last class of Boundary Scan applications involves additional tester hardware in order to improve the test coverage by including peripheral interfaces or by providing extra test access beyond the Boundary Scan cells built-in to devices on the Unit Under Test.

Automated Test Equipment utilizing the test access port (TAP) defined in IEEE Std. 1149.1 and designed to provide auxiliary test resources, such as analog and digital tester I/O channels, can potentially support all four of these classes of JTAG / Boundary Scan applications.

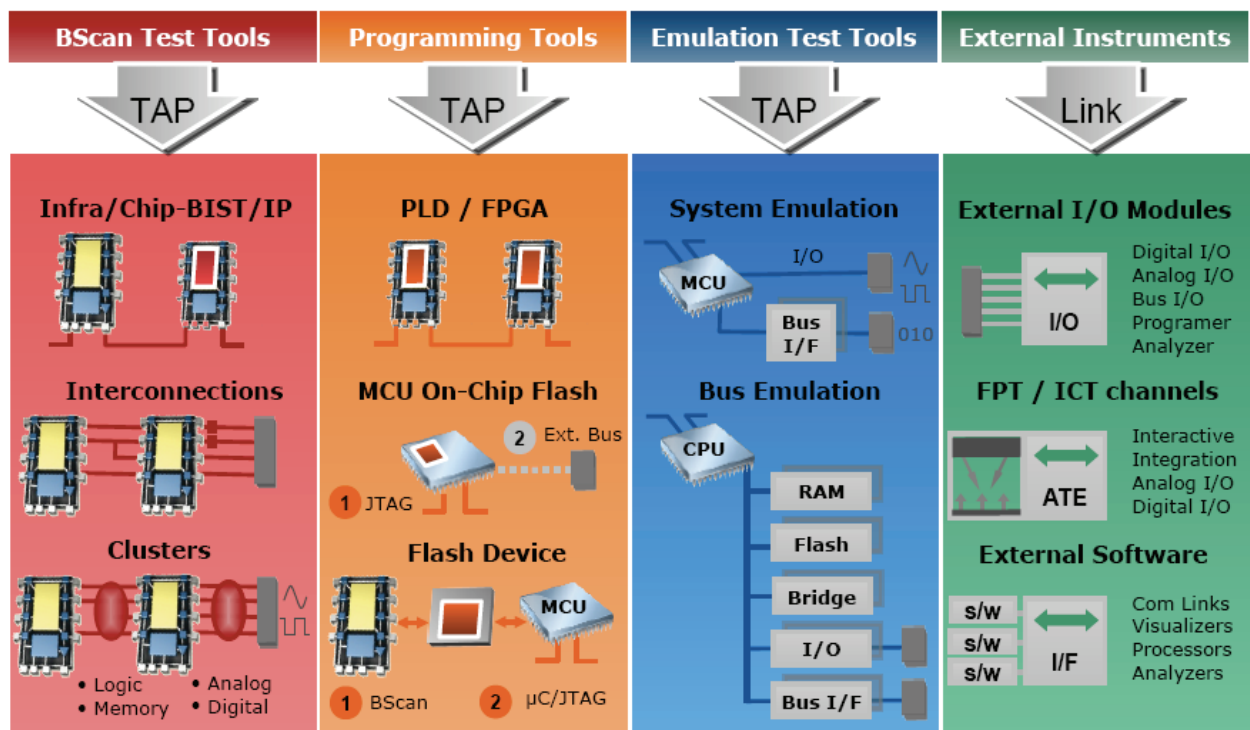


Figure 2 - JTAG / Boundary Scan applications classified

Universal, low-pin count Automated Test Equipment for Printed Circuit Assembly

Frequent board-level Design-For-Test (DFT) problems related to JTAG/Boundary Scan include the inaccessibility of Test Access Port (TAP) signals via connector pins, Compliance Enable pins that are only accessible via test points, inefficient handling (operators have too many cables to manage), and cumbersome power supply management.

Often times, the Boundary Scan test coverage could be dramatically improved if test points or connector pins on the Unit Under Test (UUT) could be accessed with Tester I/O and the overall fault coverage for a UUT could be improved by accessing its analog and mixed-signal circuitry with tester resources.

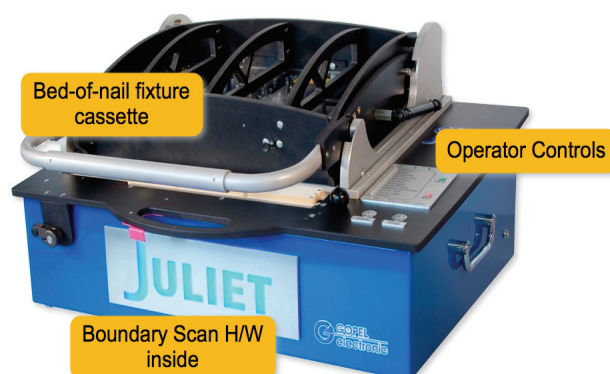


Figure 3 - Example of a universal, low-pin count Automated Test Equipment for Printed Circuit Assembly Test

GOEPEL's JULIET™ (

Figure 3) is an example for an off-the-shelf, completely integrated stand-alone desktop JTAG/Boundary Scan Tester for prototyping and manufacturing test. The compact, modular system integrates all test electronics and is controlled by an external PC or laptop via USB 2.0 or LAN. The tester features a mass interconnect interface and an exchangeable UUT adaptor, allowing quick system reconfigurations for different UUTs and providing easy access to the UUT's test points via nail probes or to the UUT's peripheral interfaces via connector pins. For efficient use in the manufacturing environment, such stand-alone Boundary Scan testers benefit from features such as:

- Automated detection of the UUT fixture type,
- Automated loading of test programs (e.g. from a central server),
- Automated detection of procedures to be executed (such as interconnection test, memory access test, Flash programming, etc.), and
- Automated execution of tests after engaging the test fixture.

A universal, low-pin count Automated Test Equipment based on JTAG/Boundary Scan should integrate a Boundary Scan controller (to interface with the Boundary Scan chain(s) on the UUT), fixture electronics for testing the UUT's peripheral analog and digital I/O, Power Supply for the UUT, and maybe even a barcode reader. An operator interface with display and control elements and support for parallel and at-speed testing further improve the tester's readiness for the production environment.

Example applications

With the resources listed above, such universal, low-pin count Automated Test Equipment allows the execution of Boundary Scan tests, in-system-programming of Flash and PLD, Micro-Controller (MCU) on-chip programming, functional emulation tests, and interface tests. Such a tester could furthermore be set up to test or program multiple UUTs in parallel, e.g. to improve test or programming throughput.

Let us consider a UUT that features the following major components:

- A Boundary Scan enabled micro-controller (μC) that also offers On-Chip Emulation resources accessible through its JTAG port,

- A Boundary Scan enabled FPGA device,
- Two SRAM devices that are not Boundary Scan enabled but which are connected to the FPGA device,
- Two FLASH devices that are not Boundary Scan enabled but which are connected to both the μ C and to the FPGA,
- Four DDR2 SDRAM devices that are not Boundary Scan enabled but which are connected to both the μ C and to the FPGA,
- A proprietary bus connector with 82 (mostly digital) signals and a number of Power and Ground connections, and
- Various peripheral interface circuits, neither of which are Boundary Scan enabled, but all of those can be controlled from the μ C device.

For such an UUT, a variety of test applications can be executed under control of Boundary Scan test equipment with the appropriate resources:

- An Infrastructure Test verifies the integrity of the Boundary Scan chain and confirms that the correct Boundary Scan devices (component types for μ C and FPGA) are mounted on the UUT;
- The Interconnect Test utilizes Boundary Scan I/O pins on the μ C and the FPGA in order to verify connectivity between such pins, with the purpose to detect and diagnose manufacturing defects such as open pins or shorted nets.
- Since some of the Boundary Scan I/O signals on the μ C and FPGA are connected to the bus interface connector on this UUT, wiring tester resources to the respective interface connector pins (via probes contacting the connector pins or via a mating interface connector) allows the system to detect opens on these connector pins. In this manner we can also extend the test coverage for signals that feature only a single Boundary Scan pin on the UUT and therefore would have very limited testability without additional tester resources connected to these signals for stimulation and observation.
- The connections between the two SRAM devices and the FPGA device can be tested as part of a so-called Memory Cluster Test. This tests detects opens and shorts on the address, data, and control signals connected to these SRAMs.
- Similarly, connectivity to the two FLASH devices can be tested – and the FLASH device types can be identified – by reading their Manufacturer IDs and Device IDs by means of Boundary Scan access from the μ C or the FPGA. Just reading these IDs does not test the address and data pins on the FLASH devices extensively (not all pins are tested for high and low logic level), but it proves the basic accessibility of the FLASH. A more extensive test, similar to the Memory Cluster Tests for the SRAM devices, would entail erasing the FLASH devices, and programming specific test pattern to the FLASH memory. This would make for a rather long test execution time and therefore is rarely practiced. An alternative technique is currently being defined by the IEEE P1581 working group, which would allow to test the connections to memory devices, including FLASH devices, without actually writing or reading memory contents, but rather by utilizing a simple combinatorial logic inserted between memory input and output pins while the device is in P1581 test mode. As promising as this technique is, this capability is not yet implemented in devices currently available on the market.
- Connectivity to the four DDR2 SDRAM devices can be verified with Boundary Scan controlled Memory Cluster Tests similar to the test for the SRAM devices, writing to and reading from the memory devices by means of Boundary Scan access from the μ C or the FPGA. This method works as long as the Boundary Scan device(s) have access to all memory pins needed for successful write and read operation, which in the case of SDRAM also includes the clock signal(s). In practice such clock signals may be wired directly to functional clocks, though, with no means to control the clock signal via Boundary Scan – in such cases a Boundary Scan controlled Memory Cluster Test is not possible. A relatively long test execution time can also be problematic. And last, but not least, Boundary Scan access is relatively slow, which means the connections to the memory devices are not tested at functional speed, but rather at a much slower access rate. These problems can be overcome by utilizing the On-Chip Emulation (OCE) resources available in the μ C, which are accessible through its JTAG port. We can use access to the μ C address, data, and control bus from these OCE resources to execute write and read access cycles to the memory devices at functional speed, using the JTAG port only to initialize the test and to read back the test result. In this manner we can execute

Memory Cluster Tests at the normal, functional speed, while obtaining the same diagnostic detail as in Boundary Scan controlled Memory Cluster Tests in case of a defect.

- The various peripheral interface circuits on the UUT can all be controlled from the μC device. Some of those circuits can be tested with standard Boundary Scan access from the μC and by providing tester I/O channels to the respective peripheral interface connector pins. However, other interface circuits would benefit from faster test execution or may not even be controllable via Boundary Scan from the μC . Since the μC provides On-Chip Emulation (OCE) resources with access to the μC pins controlling these on-board interface circuits, we can utilize the OCE capabilities to execute pseudo-functional tests for such peripheral interface (examples are USB interfaces, Ethernet ports, CAN buses, etc.) [4], again supported by tester resources wired up to the respective connector pins on the UUT (through nail probes in the bed-of-nail adapter or through mating interface connectors), see

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- Figure 4 below.

As a result of the combined execution of these tests a very high test coverage can be achieved.

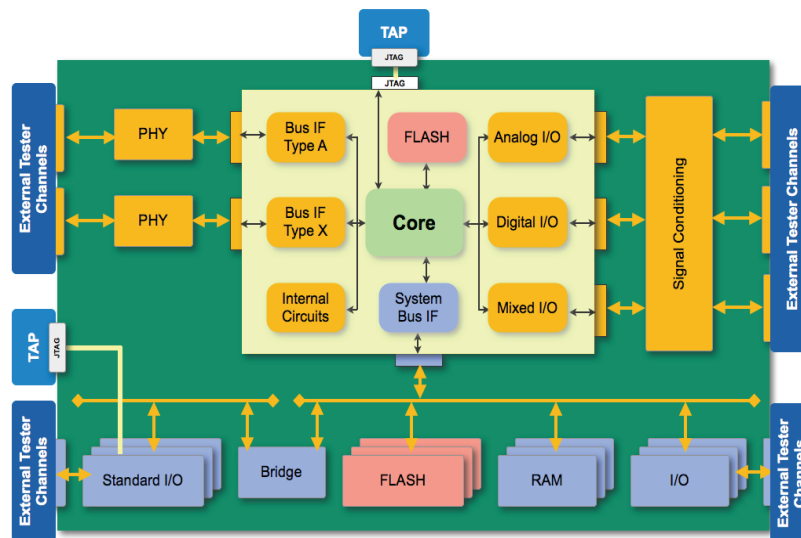


Figure 4 - PCA with micro-controller, peripheral interface circuitry (accessed by Tester I/O), and various memory devices

Benefits and limitations

When compared to ad-hoc test setup for stand-alone Boundary Scan, the universal, low-pin count Automated Test Equipment discussed above has the potential to improve the handling of the UUT as well as the test coverage achievable with Boundary

Scan. This is especially true for the types of tests that require additional tester resources to provide stimulus to the UUT or to observe UUT signals, as discussed previously.

Using off-the-shelf test equipment for such tests rather than ad-hoc setups reduces the test development time and the test setup time. Furthermore, utilizing Boundary Scan and especially On-Chip Emulation access for pseudo-functional tests can reduce the test development time and test execution time required for the “real” functional test of the UUT.

Universal, low-pin count Automated Test Equipment has the potential to reduce the cost of test and - when compared to less flexible and more expensive ad-hoc test solutions - improves UUT handling and the overall test depth and fault coverage.

Test equipment of the type discussed in this paper cannot replace more advanced functional test equipment, or full-featured in-circuit testers. Rather, the purpose of universal, low-pin count Automated Test Equipment, as discussed here, is to reduce the efforts to be put into functional test development and potentially to simplify the functional tests, reducing test execution time.

References

- [1] Ken Parker, “The Boundary Scan Handbook”, 3rd Edition, 2003, Kluwer Academic Publishers
- [2] Stig Oresjo, “How defect coverage as a variable can be used to determine test and inspection strategies”, Board Test Workshop 2005
- [3] Jukka Antila, Markku Moilanen, “Test process Efficiency Analysis with Basic Quality Data”, European Test Symposium 2005
- [4] Thomas Wenzel, Heiko Ehrenberg, “Combining Boundary Scan and JTAG Emulation for advanced structural Test and Diagnostics”, White Paper, www.goepel.com

Benefits and Limitations of Universal, low-pin count Automated Test Equipment for Printed Circuit Assemblies

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Outline

- Overview of Test Methodologies
- Classification of JTAG / Boundary Scan Applications
- Concept of universal, low-pin count ATE
- Example UUT and test applications

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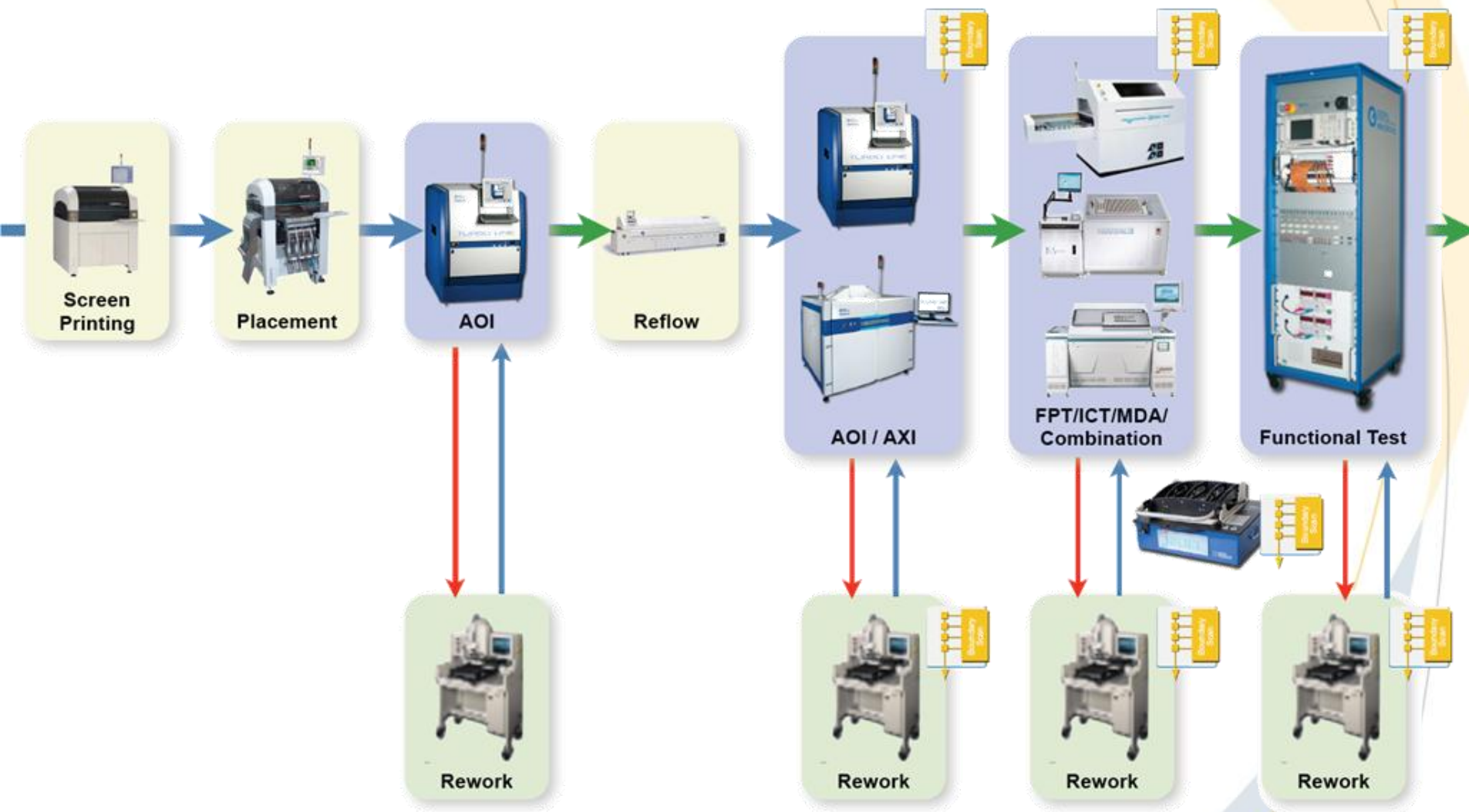
*JTAG/Boundary Scan,
AOI, AXI, Digital Image Processing,
Functional Test, Automotive Test*

Overview of Test Methodologies

Defect Type	AOI	AXI	ICT	FPT	FT	BScan
Visible Shorts	✓	✓ but not reasonable	✓	✓	✓	✓
Hidden Shorts	—	✓	✓	✓	✓	✓
Visible Opens	✓	✓ but not reasonable	✓	✓	✓	✓
Hidden Opens	—	difficult	✓	✓	✓	✓
Solder Quality	✓	✓	—	—	—	—
Missing Component	✓	✓	✓	✓	✓	partially
Wrong Component	partially	—	✓	✓	✓	partially
Orientation	✓	—	✓	✓	✓	✓
Misplaced / Alignment	✓	✓	—	—	—	—
Defective Component	—	—	✓	✓	✓	✓
Defective PCB	—	—	✓	✓	✓	✓
ESD / EMI	—	—	partially	partially	✓	partially
Design Problems	—	—	—	—	✓	partially
Software Defects	—	—	—	—	✓	partially
Benefit	Early in Process	X-Rays	Fast	No Fixture	Functional	Versatility
Disadvantage	No Electrical Test	Expensive	Requires Fixture	Slow	Expensive	Digital only*

Electrical Defects Placement Errors Soldering Defects

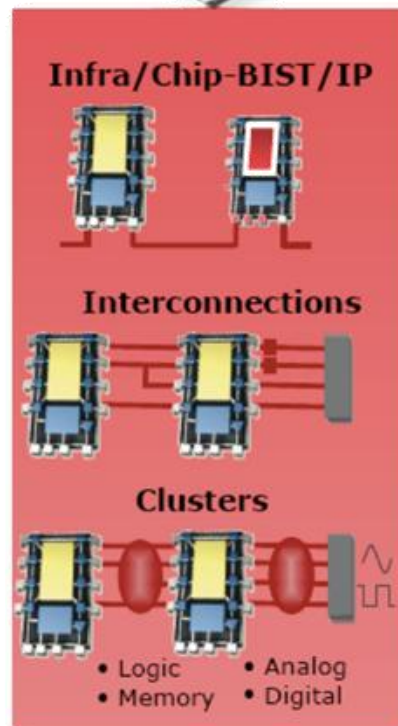
Typical Production Flow



JTAG / Boundary Scan Applications

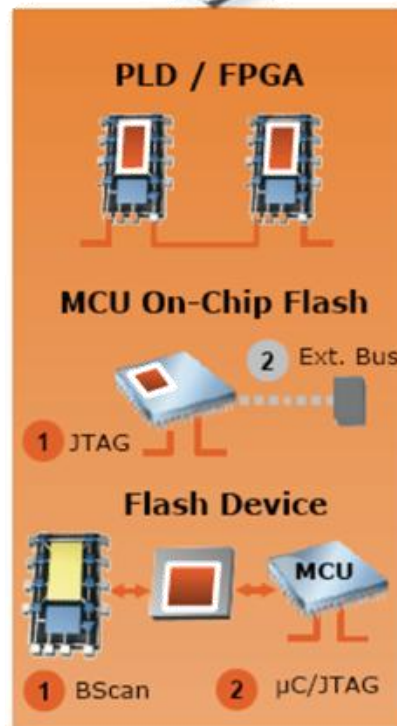
BScan Test Tools

TAP



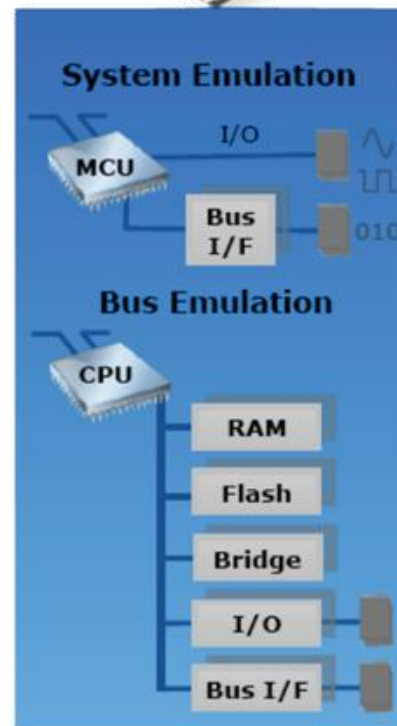
Programming Tools

TAP



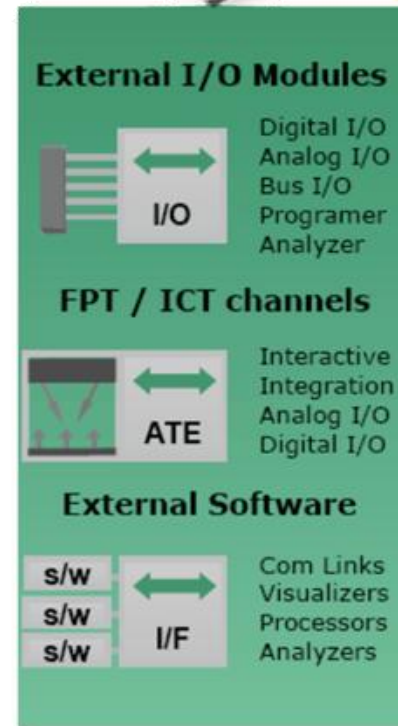
Emulation Test Tools

TAP



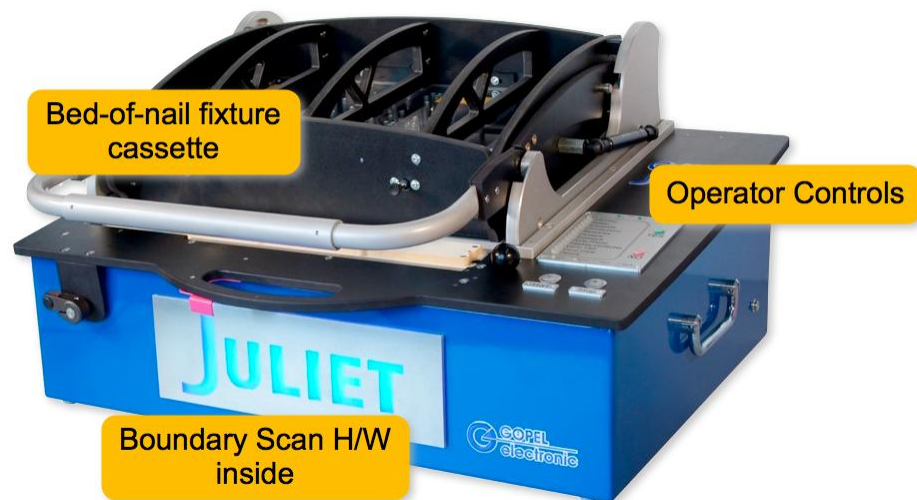
External Instruments

Link



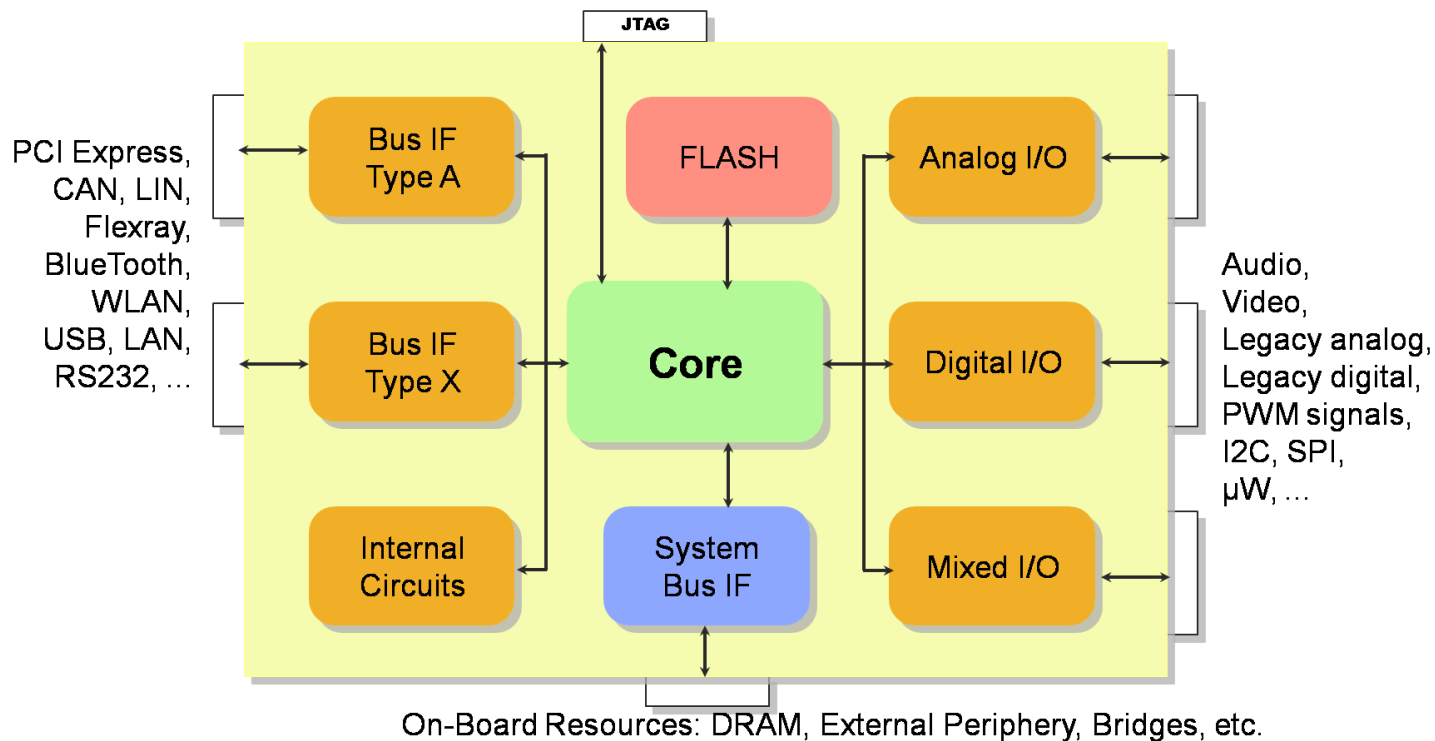
Universal, low-pin count ATE for PCA

- Integrated test/fixture electronics, power supply
- Bed-of-nail fixture / mass interconnect
- Compact, modular, JTAG/Boundary Scan based
- Interchangeable UUT adaptor
- Single UUT or Panel test



Emulation Test

Generic μ P / MCU / CPU model (On-Chip Resources)

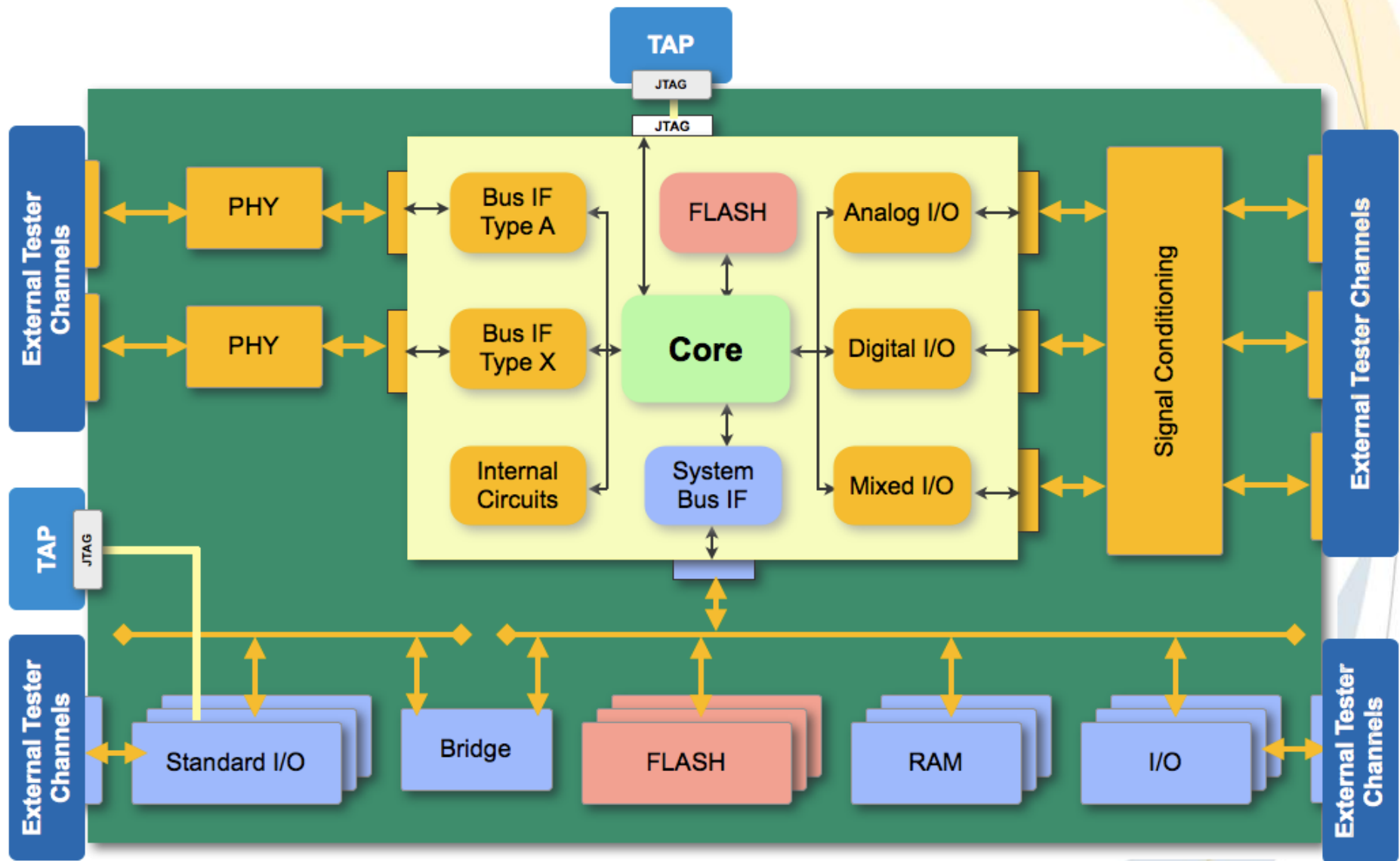


Application Type A:
Programming Functions for
On-Chip or external FLASH

Application Type B:
Bus Control Functions for
Bus Emulation Test

Application Type C:
Test Functions for
On-Chip Resources

Example UUT, test applications



Summary

Universal, low-pin count ATE for PCA benefits:

- Low-cost, modular, portable, off-the shelf
- Utilize Tester I/O to extend UUT test coverage
- Integrated functional test capabilities (OCE)
- Reduce overall cost of test



Thank you ...

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