PCB Design Principles for QFN and Other Bottom Termination Components

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Abstract
Although many of the QFN and bottom termination products are small in outline and utilize a plastic encapsulated copper lead-frame structure they do not resemble the more traditional small outline (SOIC) lead-frame packaged semiconductors because the termination features do not extend beyond the package edge. Many of the QFN packages have an exposed die attach pad (DAP) feature on the package bottom surface to provide a more direct thermal interface with the mating circuit board surface. Since there is no protruding lead on the package and DAP features are relatively large, solder defects are often beyond acceptable levels.

Key issue: Because the DAP feature can be rather large, printing solder paste with a matching outline can result in uneven solder distribution during the assembly process. This uneven solder distribution causes the parts to tilt, often causing solder bridging and/or disconnect of the perimeter located terminal contacts.

Solution: To compensate for this condition and potentially reduce solder defects, unique DAP print pattern variations can be adopted. Optimizing the solder stencil pattern will ensure that the package bottom surface remains parallel with the circuit board surface during the reflow solder attachment process.

In this paper we will review a wide range of plastic encased no-lead package configurations, industry package standards, and terminal design variations as well as defining the criteria for land pattern design and solder paste stencil development and assembly process methodologies detailed in the new IPC-7093 standard, *"Design and Assembly Process Implementation for Bottom Termination Components".*

Introduction
With a goal of reducing packaging costs and addressing the need for miniaturization, several semiconductor suppliers have adopted bottom surface termination configurations. These semiconductor package variations go by such diverse names as Quad Flat Pack No-Lead (QFN), Land Grid Array (LGA), Small Outline No-Lead (SON), Plastic Quad Flat No-Lead (PQFN), Micro Lead Frame Plastic (MLFP™), Micro Lead-Frame Package (MLP™) and many more. Many of the QFN and SON devices utilize a copper lead-frame for die attach and wire-bond but, because the lead contacts do not protrude outside the body outline, they are classified as leadless or 'no-lead'. The terminations can be positioned on two sides or four sides of the package body typical of those shown in **Figure 1**. For, more complex high pin-count applications, the contact features may be spaced closer together or, when necsasary, the package can be configured to accommodate multiple rows of contacts.

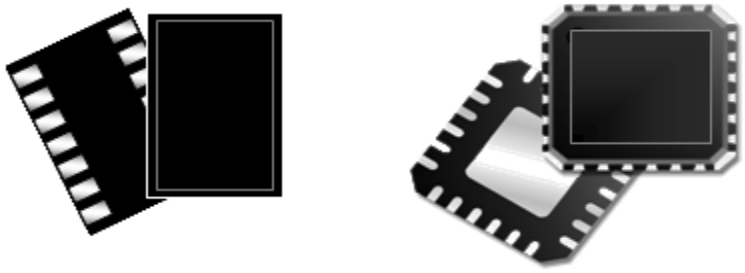


Figure 1. Comparing SON and QFN bottom termination semiconductor packaging.

The QFN and SON often qualify as a Chip Scale Package (CSP) because the outline of the package is commonly only slightly larger than the die element. Although many of the QFN and SON devices utilize a copper lead-frame for die attach and wire-bond, other package variations adopt multilayer ceramic or organic substrate technology for packaging.

The definition developed by the Joint Electronic Device Engineering Council (JEDEC) for the SON package family is a 'no-lead rectangular semiconductor package with metalized terminals on two sides of the bottom surface of the package'. JEDEC defines the QFN as a 'no-lead semiconductor package with metalized terminals on four sides of the bottom surface of the package'. Although a single row of contacts located along the edges of the bottom surface of the QFN package body is most common, the contacts may also be arranged in 2 or 3 rows. Typical of the single row QFN, the multiple row QFN package is often a lead-frame based product as well.

Standards developed for these leadless package families extend a great deal of latitude for the suppliers. A Joint Committee 11 (JC-11) within the JEDEC organization has developed guidelines for manufactures that define several no-lead package outlines that include several variations that define contact geometry, contact pitch and contact location in relation to the outer edge of the package unit (pullback or no-pullback). The no-pullback variation for example, is when the bottom located contact geometry is positioned even or flush to the outer edge of the package outline. The pullback and no-pullback contact variations are compared in **Figure 2**. The lead-frame type QFN package families are generally furnished with a contact pitch of 1.0mm or less with a package outline ranging from (but not limited to) 3.0mm square to 9.0mm square.

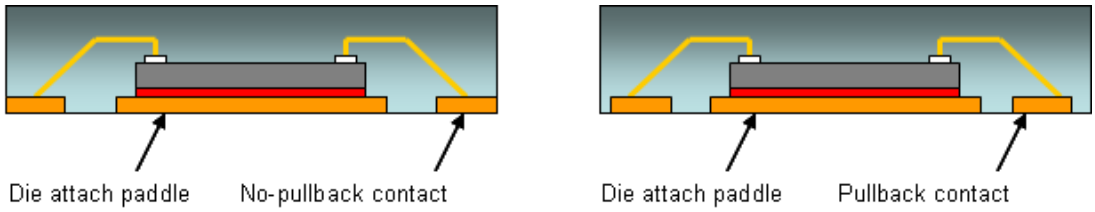


Figure 2. Terminal-to-edge variations for BTC semiconductor packaging.

QFN/SON Lead-Frame Package Assembly

The lead-frame developed for QFN and SON packing is typically configured in an array format to enable a more efficient assembly process. The package assembly sequence and methodology is typical of other lead-frame based semiconductors. The die element is first bonded to the top surface of the die attach paddle (DAP) followed by wire-bond termination from the perimeter bond pads on the die element to the terminal contact features of the lead-frame. The package is completed when the plastic casing is molded around the die and wire-bond area leaving only the bottom area of terminals and the die attach paddle (DAP) feature exposed for solder attachment. When DAP remains exposed outside the mold compound, it serves as thermal transfer feature to conduct heat away from the die element and package body. Following the molding process the individual package units will be singulated for testing. The mold tooling can be designed for either punch singulation or saw singulation processes. The mold designs that are commonly furnished for the QFN and SON package are either segmented or monolithic as compared in **Figure 3**.

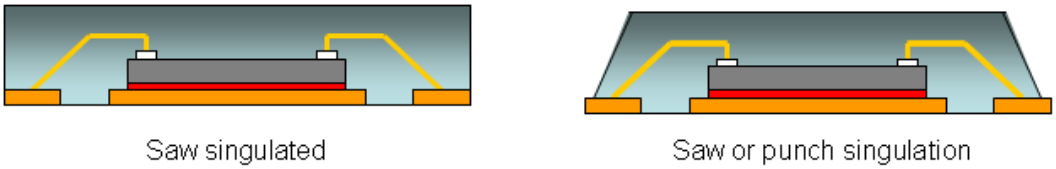


Figure 3. QFN/SON monolithic and tapered edge overmold profile variations.

The segmented mold tool is designed to furnish a tapered side wall on all four sides of the package unit. This variation is often referred to as the Hershey Bar design allowing access to the slightly protruding (no-pullback) copper lead area enabling singulation by punching or saw cutting. The alternative mold variation furnishes a common monolithic encapsulation over all device units requiring saw singulation.

In reviewing the component suppliers' specifications you will observe that the terminals may be flush to the outer edge of the package or slightly recessed from the package edge. In the case of saw singulated devices compared in **Figure 4**, all or part of the ends of the copper lead-frame structure will remain exposed**.**

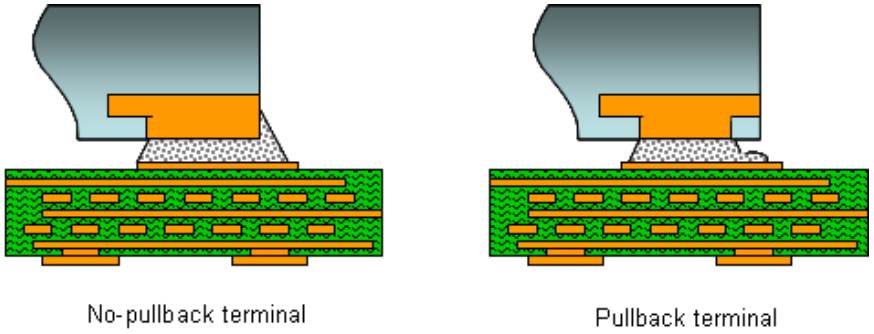
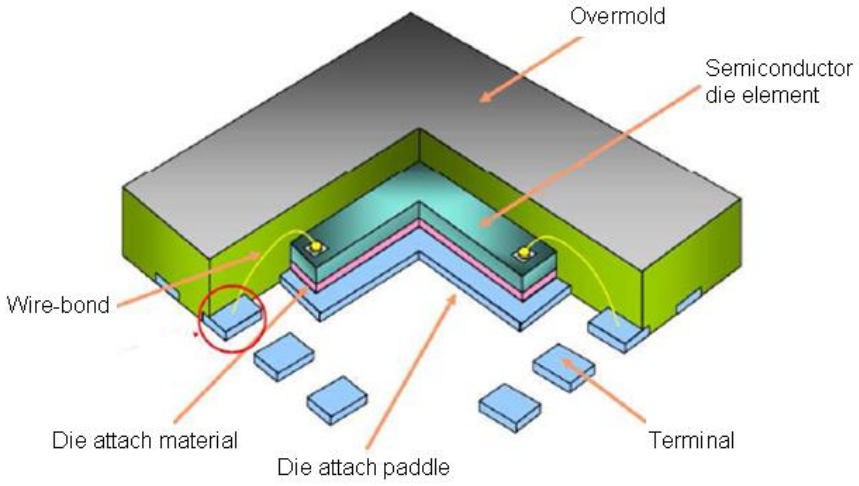


Figure 4. Land pattern to terminal alignment.

Land Pattern Development and Circuit Routing

In order for the QFN and SON packaged semiconductor to meet peak performance criteria, the designer is advised to carefully plan the land pattern geometry for mounting the device. Additionally, a strategy will need to be developed for circuit conductor interface. In developing the land patterns one must consider dimensional tolerances for the package, the circuit board fabrication tolerance and the placement tolerances associated with the board level assembly process. As noted, the QFN and SON package outline may be square or rectangular and can be furnished with symmetric or asymmetric terminal patterns. Contact spacing is significant as well. Although the JEDEC package design guideline standards allow the manufacturer a choice of several contact pitch variations, a majority of the no-lead products actually reaching the market have been supplied with either 0.65 mm or 0.50 mm pitch, however, QFN devices with 0.40mm pitch are also being offered for limited applications. The exposed DAP serves to assist in transferring any thermal rise generated by the die element directly onto the host circuit structure. A typical QFN with the exposed DAP is shown in **Figure 5**.



Example source: Texas Instruments

Figure 5. QFN showing terminal contacts and DAP feature

The DAP may be solid as shown or segmented into a matrix format. The joining of the exposed DAP to a mating land area on the circuit board is achieved by printing or depositing solder or by applying a thermally conductive compound prior to device placement. In regard to the land pattern layout, the PCB designer will find that suppliers will generally furnish components with a balanced contact pattern to minimize unequal surface tension forces that may occur during the reflow solder assembly process. Non-symmetric package configurations do exist, however, and corner population of terminal features is also an option on the QFN package.

Since the terminal features are flush with the bottom surface of the package, the electrical and mechanical connection between the package and the circuit board relies on the solder provided on the land surface. Although JEDEC has established guidelines to define the mechanical features and tolerance limits on the QFN and SON device families, manufacturers often deviate from those guidelines. Before beginning the land pattern development, the 'Association Connecting Electronics Industries' (IPC) strongly recommends a thorough review of the supplier's data sheet. Additionally, when developing the SON and QFN land pattern in the CAD library the PCB designer is expected to consider a number of component package tolerance factors.

In regard to guidance for land pattern development, the IPC-7093 standard can be a valuable source. The standard recommends that the designer first consider the profile tolerances (+/-X.XX) in the package outline drawing developed by the supplier. It recommends that, rather than a 'plus' and 'minus' factor, that the tolerance limits be converted into Maximum Material Condition (MMC) and Least Material Condition (LMC). In order to determine the pad pattern dimensions, three sets of tolerances are involved; one set for the overall package outline (min./max.) dimensions and the other two sets for defining the min./max. dimension for the terminal geometry. Since it is unrealistic to assume that all three tolerances will be at their worse case, a more realistic RMS (root-mean-square) system is recommended. In addition to component tolerances, the circuit board fabrication and assembly systems tolerance must considered. The tolerance variation is typically within 50 microns for both the circuit board and component placement systems. The designer can assume that the tolerance range for placement is based on the understanding that machines suitable for fine-pitch device assembly have a positional accuracy ranging between 20 and 70 microns.

After averaging all of the tolerance variables the designer will need to calculate the land pattern protrusion dimension in order to establish a solder joint profile. The designer must also consider some devices may have developed an oxidation on the termination ends that will not 'wet' during assembly processing.

The minimum values for land protrusion recommended in the IPC-7093 standard for calculating the QFN and SON land pattern dimensions are:

Minimum Toe Protrusion = JT min = 0.1mm
Minimum Heel Protrusion = JH min = 0.05mm
Minimum Side Protrusion = JS min = 0.0mm

The values shown recognize that both sides and at least one end of the terminal contacts are embedded in the mold compound. Although it will not be practical to expect solder fillets to be formed on the terminal sides (JS), a minimal protrusion (JH) of the land pattern at the heel will compensate for any component tolerance variation. In addition, since the land pattern dimension is generally slightly longer than the nominal terminal dimension on the component, solder joints may assume a slight angular solder joint profile typical of those illustrated in **Figure 6**.

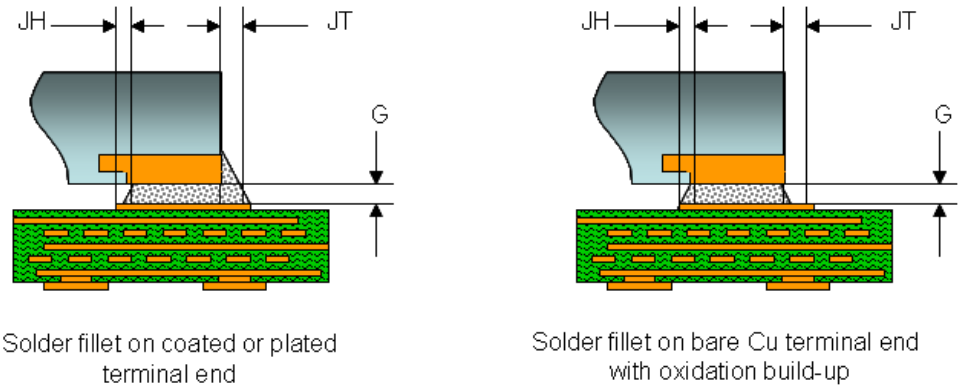


Figure 6. Comparing the solder fillet profile on QFN and SON terminal ends.

To assist in providing process compatible land pattern geometry, designers can now gain access to a land pattern calculator tool 'IPC-7351 LP'. The software finishes land pattern data for a number of already available SMT components but it also allows the designer to tailor and customize the land patterns to achieve specific solder fillet goals for most no-lead components currently in the market. In using this software tool the PCB Designer can significantly reduce the time required to build CAD libraries.

PCB Surface Finish Options

In specifying surface coatings on the circuit board, both soldermask and surface plating or oxidation inhibitors must be defined. The land patterns and thermal pad(s) on the printed circuit board will be either soldermask defined (SMD) or non soldermask defined (NSMD). Most often, each land pattern on the PCB will be NMSD, having its own soldermask opening with a narrow web of mask between two adjacent pads. In general, the solder mask opening will be 120 to 150 microns larger than the PCB land pattern resulting in 60 to 75 micron clearance between the land pattern and soldermask. This will compensate for soldermask registration tolerances, typically between 50 to 65 microns (depending upon the board fabricators' process control capabilities). To ensure robust adhesion, the soldermask 'web' separating lands should be at least 75 microns in width. The 0.4mm pitch package, however, with PCB land pattern width of 250 microns, a solder mask web between lands may not be practical. For this application it is recommended that the designer provide a single 'window' opening around all land patterns on each side of the package with no solder mask web between the lands or to revert to the soldermask defined alternative. The illustration furnished in **Figure 7** compares four QFN/SON soldermask to land variations.

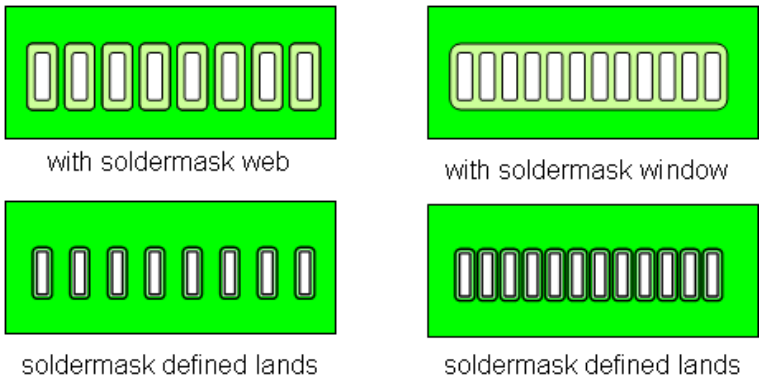


Figure 7. Comparing non-soldermask defined (NSMD)and soldermask defined (SMD) land pattern variations.

When the clearance between the perimeter contact lands and thermal pad are very close it is recommended that the thermal pad area be solder mask defined in order to avoid any solder bridging between the thermal pad and the perimeter pads. In this case, the mask opening should be approximately 100 microns smaller to overlap the thermal pad perimeter on all four sides.

In regard to solder process compatibility, commercial QFN packages are most often furnished with one of two alloy finishes: post plated Matte-Tin, and pre-plated Nickel-Palladium with a flash of Gold. Because of the relatively small contact surface area, ensuring a robust solder interface requires a PCB surface finish free of oxide coating and very precise solder paste print control. The designer and process engineer will need to confer as to what will be the best surface finish for the attachment sites. Typical alternatives include Immersion Tin (IT), Immersion Silver (IS), Electroless Nickel/Immersion Gold (ENIG) or an Organic Solder Preservative (OSP) that coats the bare copper surface and inhibits oxidation. Users suggest that for a PCB using a Hot Air Solder Leveling (HASL) process to coat the land patterns, the surface flatness should be controlled within 28 microns.

Board Level Assembly Process Overview

The market growth for the QFN and SON products is due in part to their relatively small package outline , however, low manufacturing cost is a primary driver that has enabled wide spread use of the no-lead configuration. Low package level assembly cost may not automatically translate into overall low board level manufacturing cost because the no-lead package structure presents a number of assembly process challenges. There are a number of physical factors related to the assembly process that may have significant effect on process efficiency. Some of these factors include controlling the amount of solder paste provided on the peripheral contact sites and developing a print pattern on the DAP mating surface that will prevent package shift during the reflow solder process. Although many factors related to assessment of the solder assembly process is defined in IPC-A-610E, the dimensional requirement for solder joint thickness (G) noted above is not defined. Also, the potential for opens in solder joint and excessive voiding in the thermal pad are key concerns. It is paramount that the package and PCB remain very flat to achieve a satisfactory mechanical and electrical interface. In addition, to control the effects of the large surface area of the die attach pad feature during the reflow soldering process, it will be necessary to tailor the solder stencil pattern or to partition the mating thermal plane on the PC board.

You will observe that a majority of the no-lead packaged semiconductors in the commercial market utilize conventional copper lead-frame technology and package size and shape may not be uniform from one supplier to another. Package size is determined by several factors including die dimensions, number of contact terminals and the contact pitch of the lead-frame. As noted above, the formation of the toe fillet (TF) for QFN and SON devices are not guaranteed because after sawing or

punch singulation, the bare copper ends terminals are prone to oxidation. It is generally observed, however, that the toe fillets may occur if the supplier has added an oxidation inhibitor or alloy plating to the exposed copper terminal ends. The toe fillet, if formed during assembly, may improve the solder joint reliability and, for products exposed to more harsh environments, allocation should be made for its formation. The type of solder paste used for board level assembly and environmental conditions for device storage is a factor as well. During the solder reflow process the printed solder paste will reach a liquidus state to promote joining. While undergoing this process the solvent and flux content in the paste is expelled to allow the remaining solids to join into a single mass on the thermal pad(s).

In defining the solder joint profile for the QFN and SON bottom terminal devices, the IPC-A-610E states that *"The mounting and solder requirements for SMT terminations shall meet the criteria for the type of lead termination being used".* This statement is not really definitive, leaving the solder interface requirement open for agreement between the supplier and user. While the lack of traditional leads allows lower package thickness and better electrical and thermal performance, the low standoff height may also trap flux residue, and if the remaining flux is active, the corrosion potential is increased. Many users believe that to provide clearance for cleaning and to ensure a more robust solder mechanical interface of the device to the PCB, a target standoff dimension should be close to 50 microns (2 mils). Furthermore, the IPC-7093 standard recommends that to optimize the reliability of the solder joints on the perimeter lands, the thickness of solder paste furnished on the lands should about 100 to125 microns (4 to 5 mils). This volume of solder will result in a finished standoff dimension of around 50 to 75 microns (2 to 3 mils) respectively after reflow soldering. The first step in achieving good standoff is the solder paste stencil design for perimeter pads. The stencil aperture opening should be designed so that maximum paste release is achieved. This is typically accomplished by considering the following two ratios:

1. Area Ratio = Area of aperture opening to aperture wall area
2. Aspect Ratio = Aperture width to stencil thickness

For the rectangular aperture openings commonly developed for QFN and SON package, ratios are given as: Area Ratio = LW/2T(L+W), and the Aspect Ratio = W/T Where 'W' reflects the aperture width and 'T' defining the stencil thickness. The stencil is commonly laser cut and electro polished. The polishing helps in smoothing the stencil walls resulting in better solder paste release during printing. It is also recommended that the stencil aperture tolerances be tightly controlled to prevent excessive aperture size reduction, especially for 0.4mm and 0.5mm pitch devices. Although component suppliers may have a specific recommendation for solder paste print area-to-land area, a 1:1 stencil aperture to PCB land area is generally acceptable. It is not uncommon, however, to reduce aperture length in the stencil for the pullback terminal variations because of the smaller terminal area on the package.

In order to effectively remove the heat from the package and to enhance electrical performance the DAP needs to be physically joined to the PCB thermal pad. Printing solder paste in a size equal to the thermal pad on the PCB has not been successful. During the reflow process users have observed that the liquidus solder lifts the device and creates a pivot point near the center of the DAP. As the solder cools the device can tilt toward one side, often creating shorts in one area and opens in another. If solder is to be used for joining the thermal features it is recommended that, rather than one large opening matching the thermal pad outline, a smaller pattern of multiple openings on the thermal pad region be used. This will initially result in approximately 50% to 80% printed solder paste coverage. The illustration in **Figure 8** compares the affect of full area solder printing on the thermal pad to one that has been segmented to reduce solder volume.

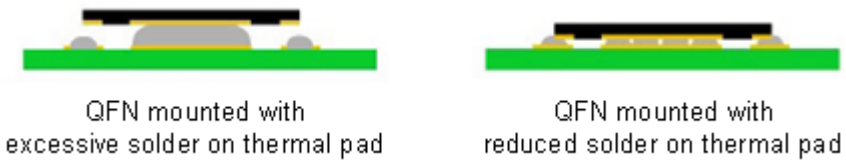


Figure 8. The affect of depositing a single solder paste pattern to a segmented pattern on the thermal pad.

To further optimize heat transfer from the thermal pad layer on the outer surface of the PCB to the inner or bottom layers, it will be necessary to include a number of plated thermal vias within the thermal pad design. The number of thermal vias needed will depend on the application, anticipated power dissipation and electrical requirements. To further enhance thermal transfer the designer can add 0.3 mm (.008") diameter plated vias within the intersections separating the solder paste stencil openings.

The example shown in **Figure 9** is typical of a segmented solder paste pattern designed to minimize the tilting affect and optimize levels of solder coverage.

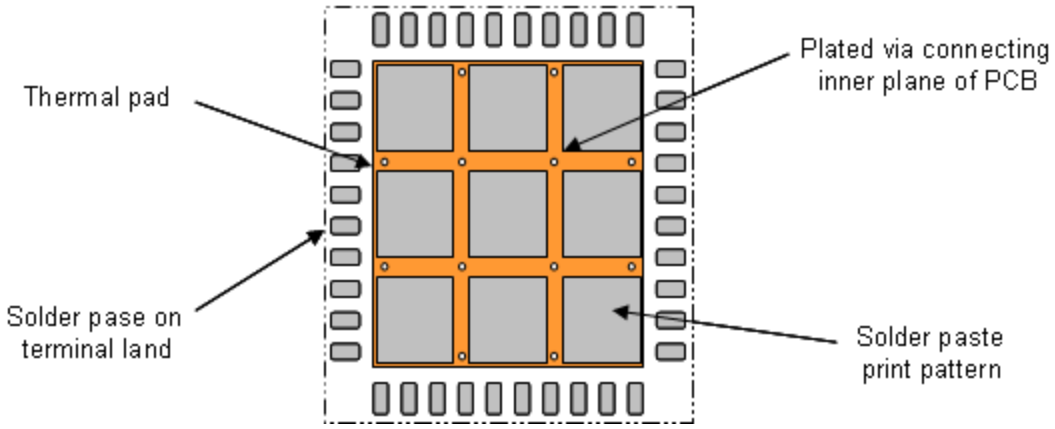


Figure 9. Segmented solder paste pattern with plated vias on thermal pad.

For DAP sizes between 2.10mm and 4.40mm square, four openings are recommended separated by 0.20mm to 0.30mm wide street. This will reduce solder paste coverage by 70% to 85% and promote leveling during reflow soldering. For the DAP areas that are greater than 4.40mm square the process engineer may want to specify a stencil that can furnish additional stencil openings separated by the 0.20mm to 0.30mm wide streets. This segmented pattern should be calculated to reduce solder paste coverage by 65% to 85% to further enable a degree of self-leveling.

Conclusion

Solder joint reliability remains a concern, especially for the larger outline QFN package. The more traditional SMT leaded packages (SOIC, QFP) have relatively long and somewhat flexible leads. The BTC packages on the other hand, do not have a lead extension and physical form that can absorb stresses and strains introduced by the differing coefficient of thermal expansion between the package and the substrate. Because of the electronic industry transition to the rather brittle, tin-rich, RoHS compliant solder alloys and the very low stand-off height of the no-lead package, one can expect a relatively shorter solder joint life, especially for products exposed to very harsh environments.

In order to assist the PCB designer and assembly process specialists' that are considering implementation of these package families, an IPC task group was formed to develop a new document that furnishes both guidance and end product requirements. The result of the effort is a design and assembly process implementation document to focus exclusively on the no-lead package families; IPC-7093, *'Design and Assembly Process Implementation for Bottom Termination Components'*. The term 'Bottom Terminal Components' generically includes all no-lead package types since they require a common approach for design and assembly. Much of the information conveyed in this paper was actually drawn from the document. Although it may not furnish a complete recipe for all no-lead component families, it does identify many of the characteristics that can influence the successful implementation of a robust and reliable assembly processes.

References:

1. JEDEC Publication 95, Design Guide 4.8, *'Plastic Quad and Dual Inline, Square and Rectangular, No-Lead Packages with Optional Thermal Enhancements'*
2. IPC-7093 *'Design and Assembly Process Implementation for Bottom Termination Components'*
3. IPC-7351 LP, '*Land Pattern Calculator*, an IPC authorized software tool supplied (at no cost) by Mentor Graphics
4. ASAT LPCC *'Application Note for Leadless Plastic Chip Carrier'*
5. Amkor MLF, *'Application Note for Surface Mount Assembly of Micro Leadframe Packages'*
6. Carsem MLP, '*Application Note for Micro Leadframe Package'*
7. Solberg, V, '*Designers Guide to Lead-Free SMT, Components, PCB Materials, Plating and Surface Coatings'*, IPC APEX 2009 technical conference proceedings (down load at www.pcbdesign007.com/pdf/pb-freeSMT.pdf)

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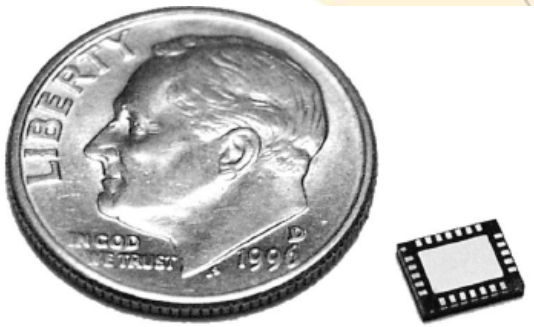
- An IPC task group was formed to develop the IPC-7093, *'Design and Assembly Process Implementation for Bottom Termination Components', a* document focusing exclusively on the no-lead package families;
  - The term 'Bottom Terminal Components' generically includes all no-lead package types since they require a common approach for design and assembly.
- *Although it may not furnish a complete recipe for all no-lead component families, it does identify many of the characteristics that can influence the successful implementation of a robust and reliable assembly processes.*

Topics of discussion



Source: National Semiconductor

- BTC Packaging Overview
- QFN/SON Lead-Frame Package Assembly
- Land Pattern Development and Circuit Routing
- PCB Surface Finish Options
- Board Level Assembly Process Overview
- Summary and Conclusion

Bottom Termination Components

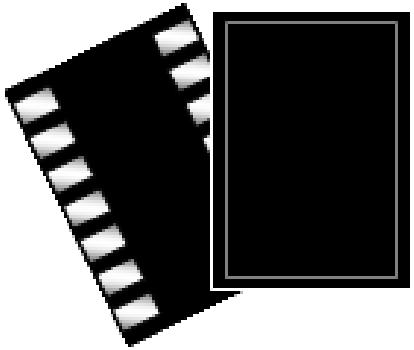
These semiconductor package variations go by such diverse names as Quad Flat Pack No-Lead (QFN), Land Grid Array (LGA), Small Outline No-Lead (SON), Plastic Quad Flat No-Lead (PQFN), Micro Lead Frame Plastic (MLFP™), Micro Lead-Frame Package (MLP™) and many more.

QFN and SON Semiconductor Packaging

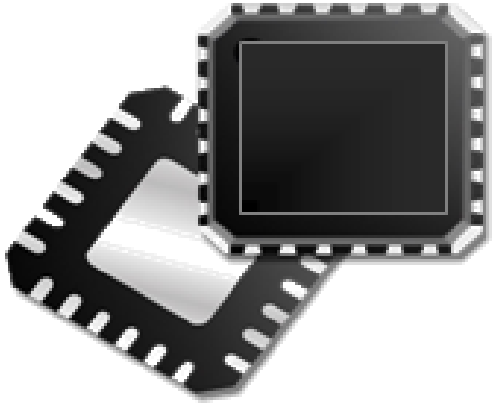
- The JEDEC[1] definition for the SON is:
  - a ‘no-lead rectangular semiconductor package with metalized terminals on two sides of the bottom surface of the package’.
- The JEDEC definition for the QFN is:
  - a ‘no-lead semiconductor package with metalized terminals on four sides of the bottom surface of the package’.

[1] Joint Electronic Device Engineering Council

- Many of the QFN and SON packages will be furnished with an exposed die attach paddle (DAP) feature on the package bottom surface for direct thermal interface with the mating circuit board.

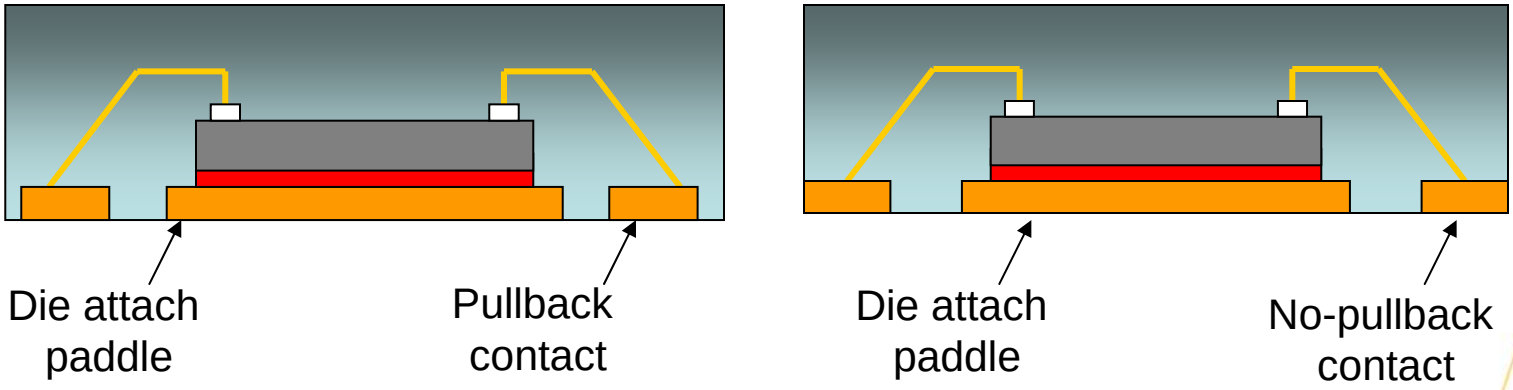


SON

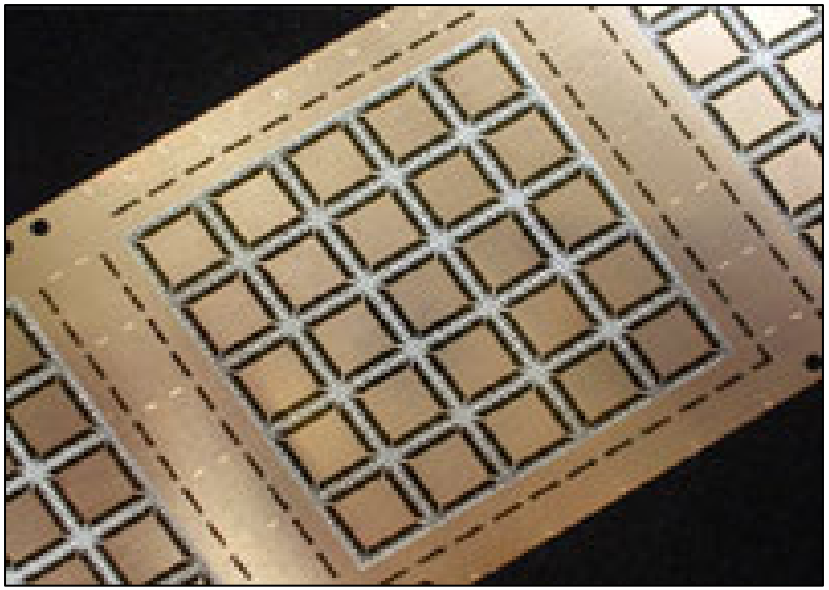


QFN

- JEDEC standard guidelines allow several no-lead package outline variations that define:
  - contact geometry and pitch
  - contact location; pullback or no-pullback



QFN/SON Lead-frame Package Assembly

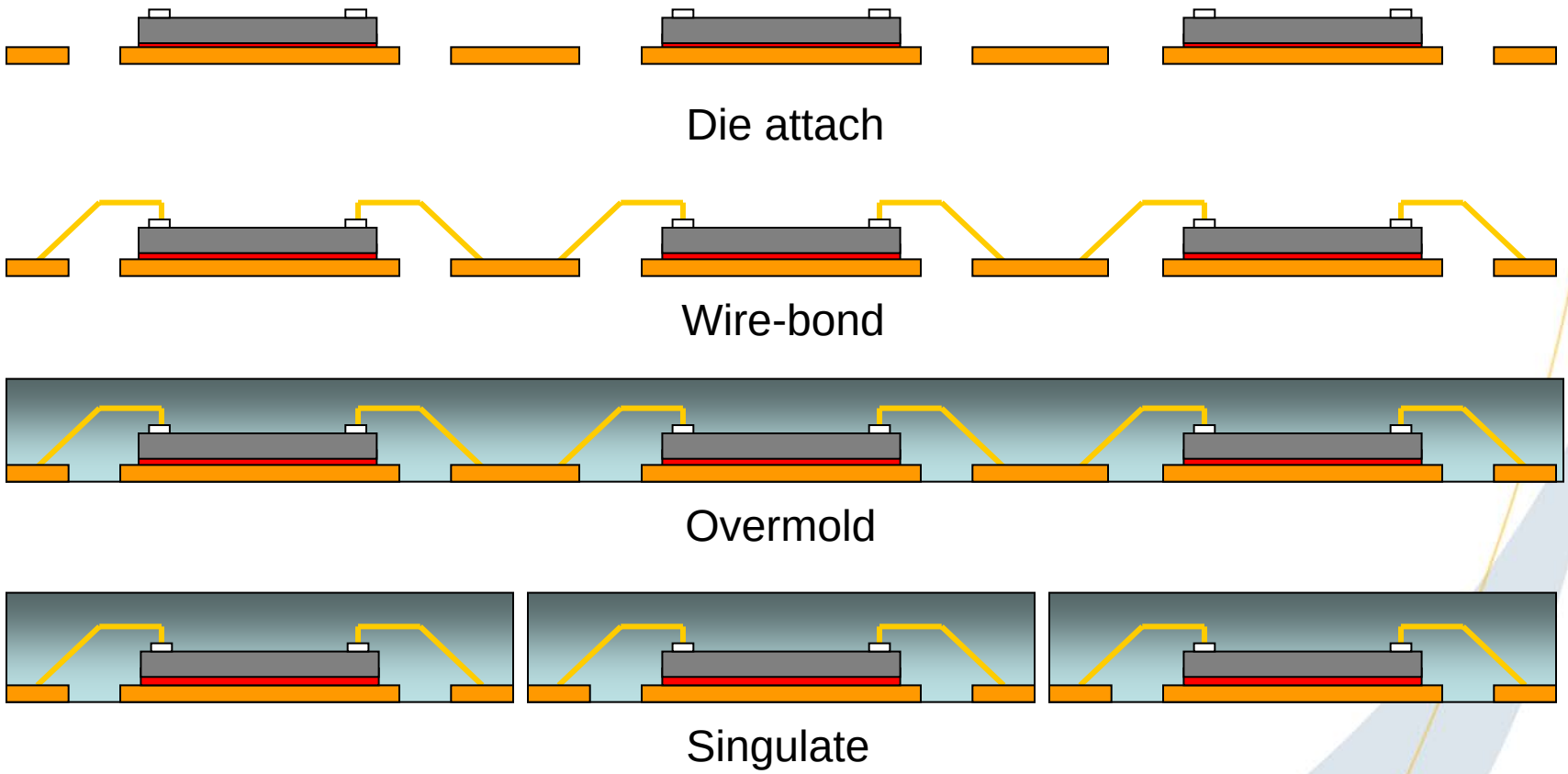


Example source: QPL Group

- The lead-frame developed for QFN and SON packaging typically uses a Cu foil strip that is pattern etched or punched and configured in a matrix format to enable an efficient package assembly process.

Package Assembly Sequence

The package assembly sequence and methodology for QFN and SON is typical of other lead-frame based semiconductors.



- The mold tooling can be designed for either a punch singulation or a saw singulation process.
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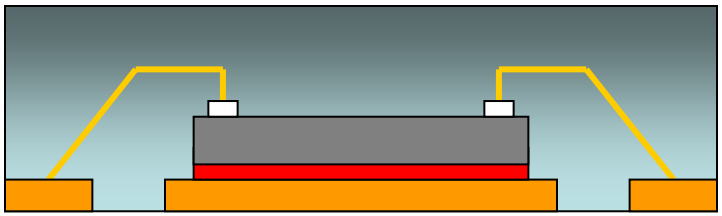
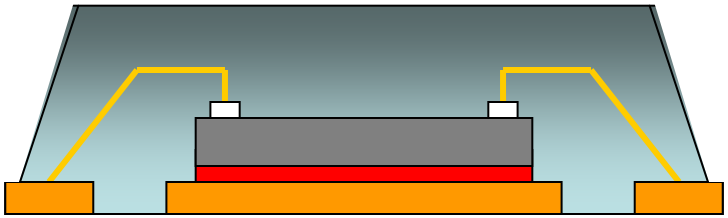


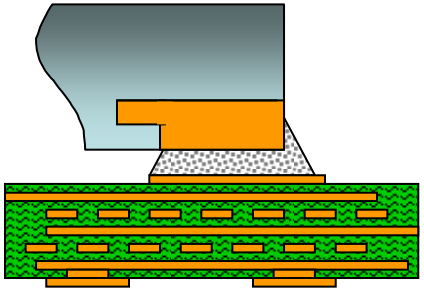
Monolithic mold design
for saw singulation



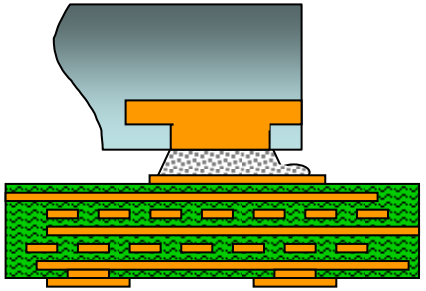
Segmented mold design
for saw or punch singulation

Terminal Design Variations

- In reviewing the component suppliers' specifications you will observe that the terminals may be flush to the outer edge of the package or slightly recessed from the package edge.



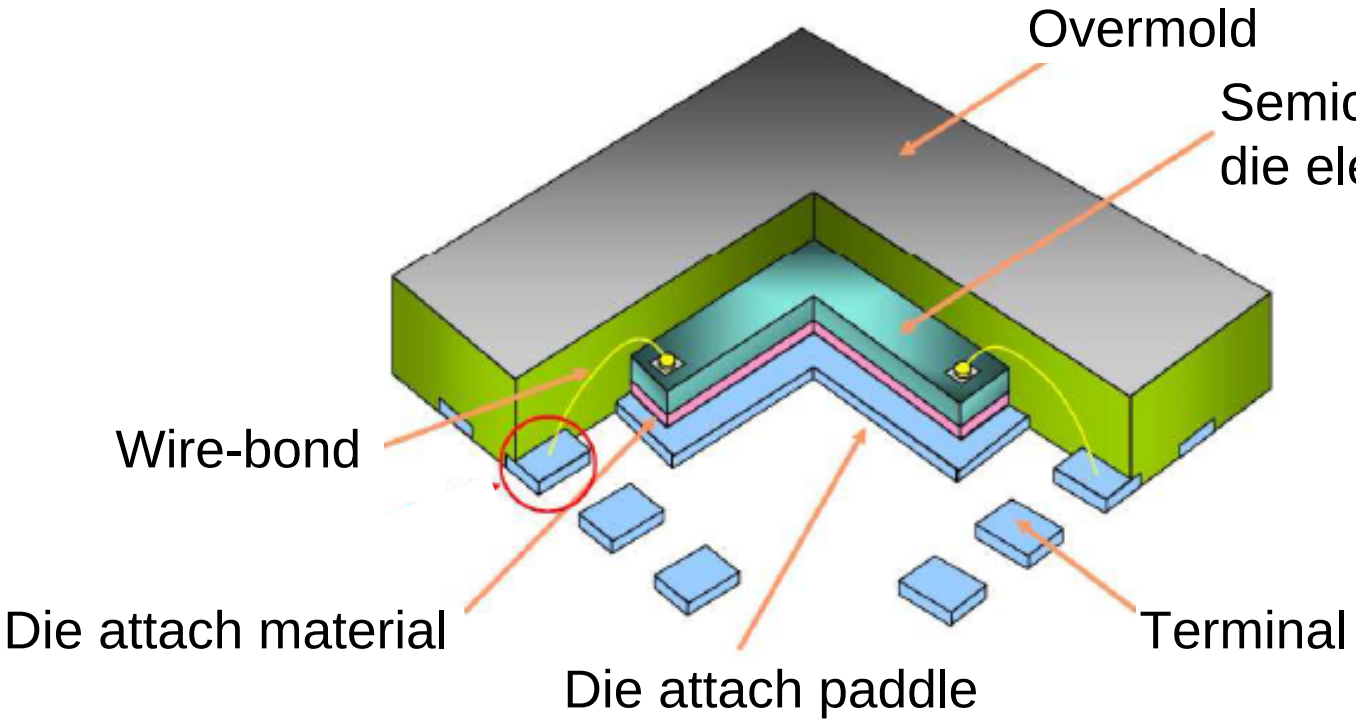
No-pullback terminal



Pullback terminal

In the case of saw singulated devices, all or part of the ends of the copper lead-frame structure will remain exposed.

Thermally Enhanced QFN

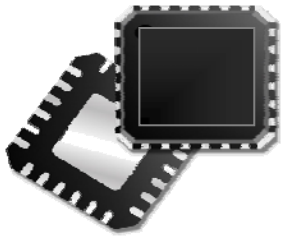


- The exposed DAP serves to assist in transferring any thermal rise generated by the die element directly onto the host circuit structure.

Example source: Texas Instruments

Land Pattern Development and Circuit Routing

- In developing the land patterns one must consider dimensional tolerances for:
  - the package outline and features
  - circuit board fabrication processes
  - the board level assembly process
- The JEDEC package design guideline standards allow the manufacturer a choice of several package outline and contact pitch variations



QFN Outline Variations

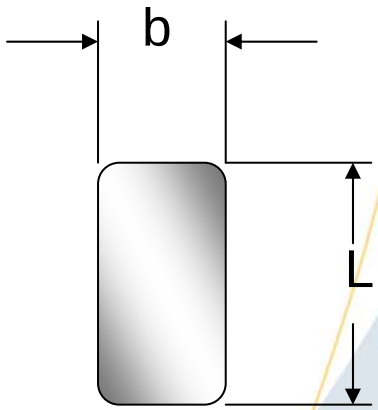
Body Outline	Terminal Count by Pitch 0.65 mm	0.50 mm
5.00 x 5.00	36	52
6.00 x 6.00	44	68
7.00 x 7.00	60	84
8.00 x 8.00	76	100
9.00 x 9.00	84	116
10.00 x 10.00	100	132
11.00 x 11.00	108	148
12.00 x 12.00	124	164

- Maximum terminal counts are calculated using established JEDEC formulas

Contact Pitch and Terminal Dimensions

- A majority of the no-lead products have been supplied with either 0.65mm or 0.50mm pitch but, devices with 0.40mm pitch are also being offered for limited applications.

Contact Pitch (e)	**Dimension** (mm)					
	b			L		
	min.	nom.	max.	min.	nom.	max.
0.65	0.35	0.40	0.45	0.35	0.40	0.45
0.50	0.25	0.30	0.35	0.25	0.30	0.35
0.50 [1]	0.20	0.25	0.30	0.25	0.30	0.35
0.40	0.15	0.20	0.25	0.20	0.25	0.30



[1] Optional variation to expand the clearance between terminal features

Land Pattern Calculation

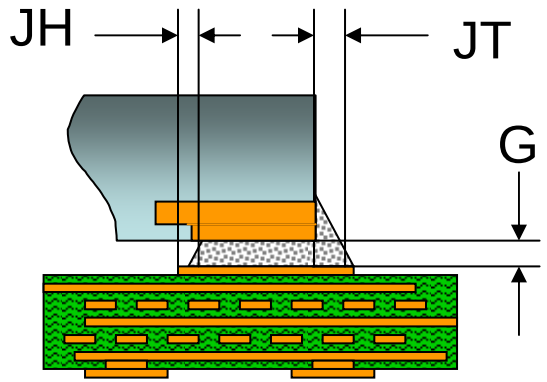
- The IPC-7093 standard recommends that the designer first consider the profile tolerances (+/-X.XX) in the package outline drawing developed by the supplier.
- Then convert the ‘plus’ and ‘minus’ tolerance limits into Maximum Material Condition (MMC) and Least Material Condition (LMC).
- To determine the pad pattern dimensions, three sets of tolerances are involved;
  - one set for the overall package outline (min./max.) dimensions.
  - the other two sets are used to define the min./max. dimension for the terminal geometry (b and L).

Allowances for PCB Fabrication and Assembly

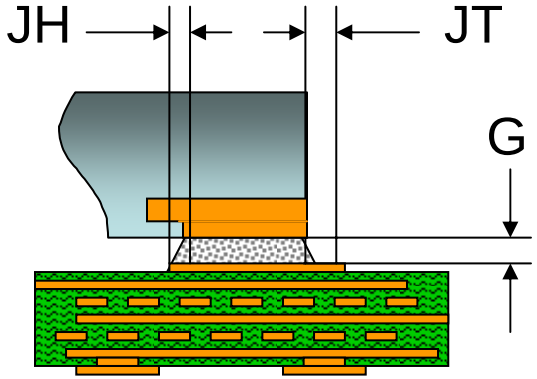
- In addition to component tolerances, the circuit board fabrication and assembly systems tolerance must considered.
- The tolerance variation is typically within 50 microns for both the circuit board and component placement systems.
  - The tolerance range for placement is based on the understanding that machines suitable for fine-pitch device assembly have a positional accuracy ranging between 20 and 70 microns.

Establishing Land Pattern Criteria

The designer must consider that some devices may have developed oxidation on the termination ends that will not ‘wet’ during assembly processing.



Solder fillet on coated or plated terminal end



Solder fillet on bare Cu terminal end with oxidation build-up

Formula for QFN/SON Land Pattern Calculation

- The minimum values for land protrusion recommended for calculating the QFN and SON land pattern dimensions are:
  - Minimum Toe Protrusion = JT min = 0.1mm
  - Minimum Heel Protrusion = JH min = 0.05mm
  - Minimum Side Protrusion = JS min = 0.0mm
- The values shown recognize that both sides and at least one end of the terminal contacts are embedded in the mold compound.

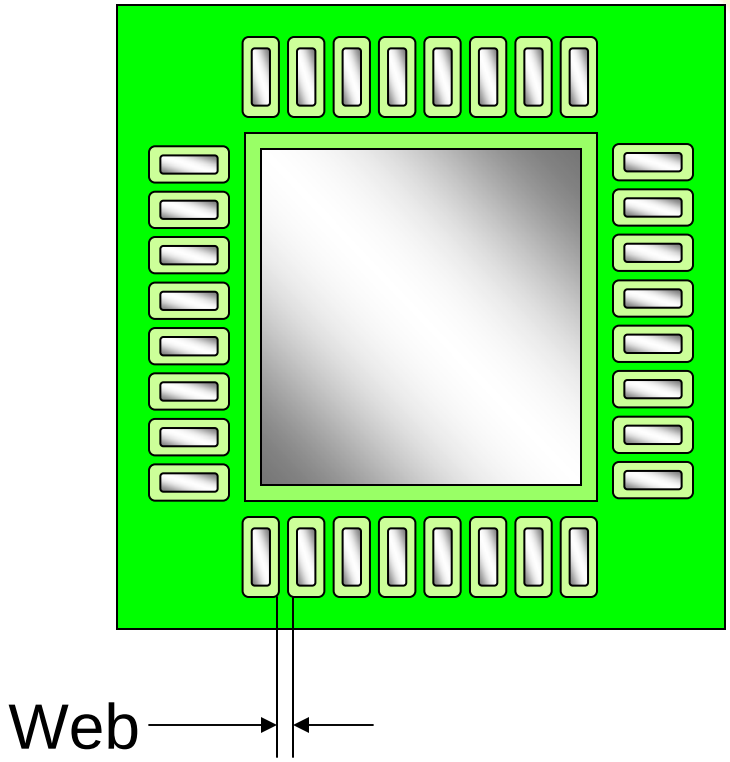
To assist in providing process compatible land pattern geometry, designers can now gain free access to a land pattern calculator tool 'IPC-7351 LP' from Mentor Graphics.

PCB Surface Finish Options

- In specifying surface coatings on the circuit board, both soldermask and surface plating or oxidation inhibitors must be defined.
- Soldermask:
  - The land patterns and thermal pad(s) on the printed circuit board will be either soldermask defined (SMD) or non soldermask defined (NSMD).
- Most often, each land pattern on the PCB will be NMSD, having its own soldermask opening with a narrow web of mask between two adjacent pads.

Non Soldermask Defined (NSMD) Lands

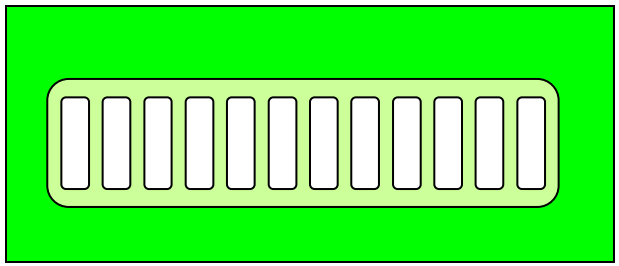
- To ensure robust adhesion, the soldermask ‘web’ separating lands should be at least 75 microns in width.



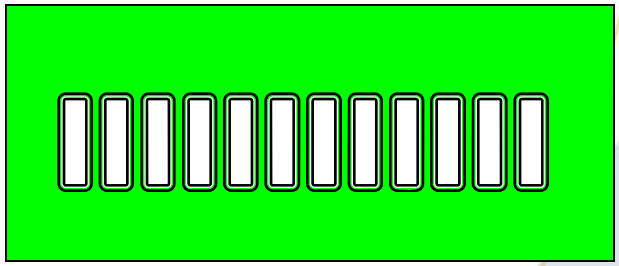
In general, the solder mask opening will be 120 to 150 microns larger than the PCB land pattern resulting in 60 to 75 micron clearance between the land pattern and soldermask.

Soldermask on Fine Pitch SON/QFN

- When using the 0.4mm pitch no-lead package, consider furnishing a single ‘window’ opening around all land patterns or adapting the soldermask defined land pattern option.



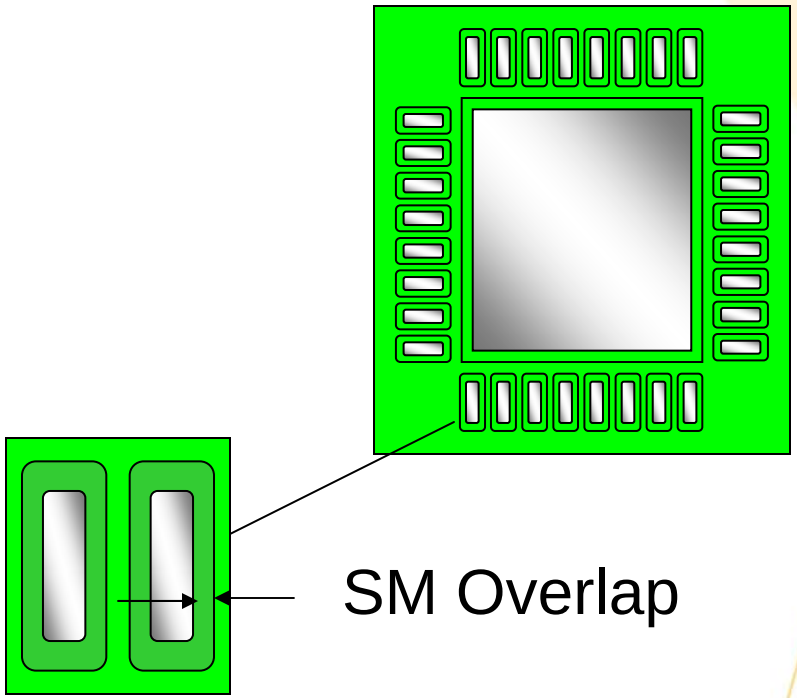
with soldermask window



soldermask defined lands

Soldermask Defined (SMD) Lands

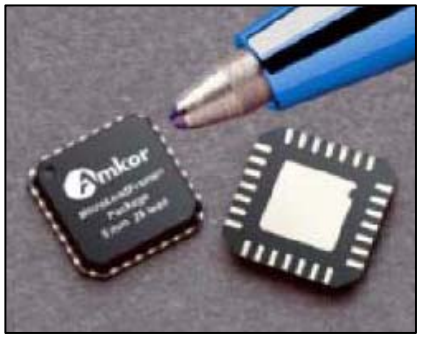
- When the clearance between contact lands and thermal pad are very close it is recommended that the features be solder mask defined to avoid any solder bridging between perimeter lands and thermal pad.



For SMD applications, the mask opening should be approximately 100 microns smaller than the land and thermal pad to overlap the land and thermal pad on all four sides.

Solder Process Compatibility

- Commercial QFN packages are most often furnished with one of two Pb-free alloy finishes:
  - post plated Matte-Tin,
  - pre-plated Nickel-Palladium with a flash of Gold.



Example source: Amkor

- Because of the relatively small contact surface area, ensuring a robust solder interface requires a PCB surface finish free of oxide coating.

PCB Plating and Coating Options

- The designer and process engineer will need to confer as to what will be the best surface finish for the attachment sites.
- Typical alternatives include;
  - Immersion Tin (IT)
  - Immersion Silver (IS)
  - Electroless Nickel/Immersion Gold (ENIG)
  - Organic Solder Preservative (OSP*)

*OSP coats the bare copper surface and inhibits oxidation.

Board Level Assembly Process Overview

- The market growth for the QFN and SON products is due in part to their relatively small package outline , however, low manufacturing cost is a primary driver that has enabled wide spread use of the no-lead configuration.
  - Low package level assembly cost may not automatically translate to a lower board level manufacturing cost because the no-lead package structure presents a number of assembly process challenges.

- Some of the physical factors related to the assembly process efficiency.
  - Controlling the volume of solder paste on the peripheral contact sites.
  - Developing a print pattern on the DAP mating surface that will prevent package shift during the reflow solder process.
- Although many factors related to assessment of the solder assembly process is defined in IPC-A-610E, the dimensional requirement for solder joint thickness (G) is not defined.

QFN Solder Process Assessment

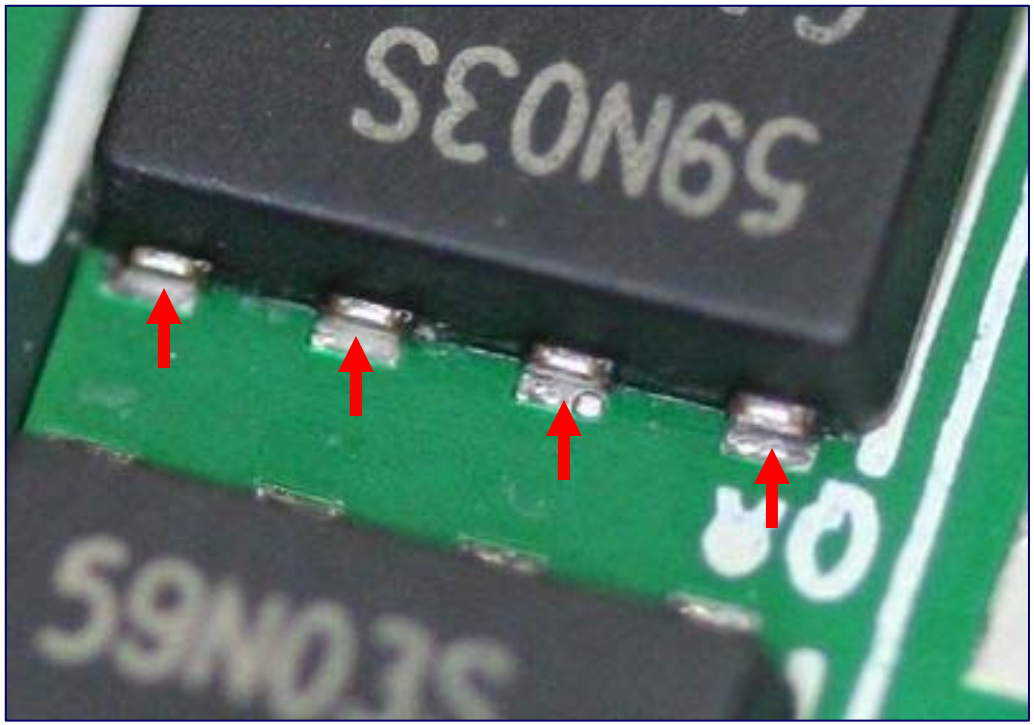
Table 8-13 Dimensional Criteria - PQFN

Feature	Dim.	Class 1	Class 2
Maximum Side Overhang	A	50% W, Note 1	25% W, Note 1
Toe Overhang (outside edge of component termination)	B	Not permitted	
Minimum End Joint Width	C	50% W	75% W
Minimum Side Joint Length	D	Note 4	
Solder Fillet Thickness	G	Note 3	
Minimum Toe (End) Fillet Height	F	Notes 2, 5	
Termination Height	H	Note 5	
Solder Coverage of Thermal Pad		Note 4	
Land Width	P	Note 2	
Termination Width	W	Note 2	

Source: IPC-A-610E

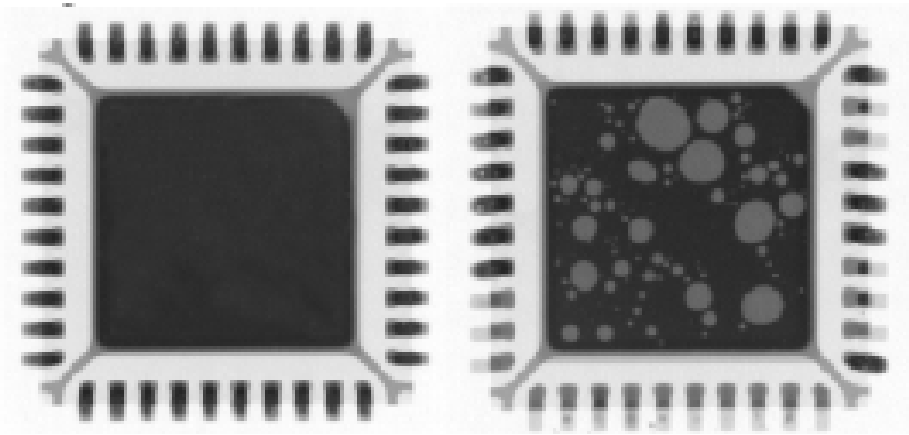
Note 1. Does not violate minimum electrical clearance.
Note 2. Unspecified parameter or variable in size as determined by design.
Note 3. Wetting is evident.
Note 4. Not a visually inspectable attribute.
Note 5. Toe (end) surfaces are not required to be solderable. Toe fillets are not required.

Regarding Toe Fillet on Terminal Ends



Due to the singulation process, the exposed copper terminal end surfaces are not required to be solderable therefore, a toe fillet is not a requirement.

- Other assembly process related concerns;
  - There is a potential for opens in solder joints and excessive voiding in the thermal pad



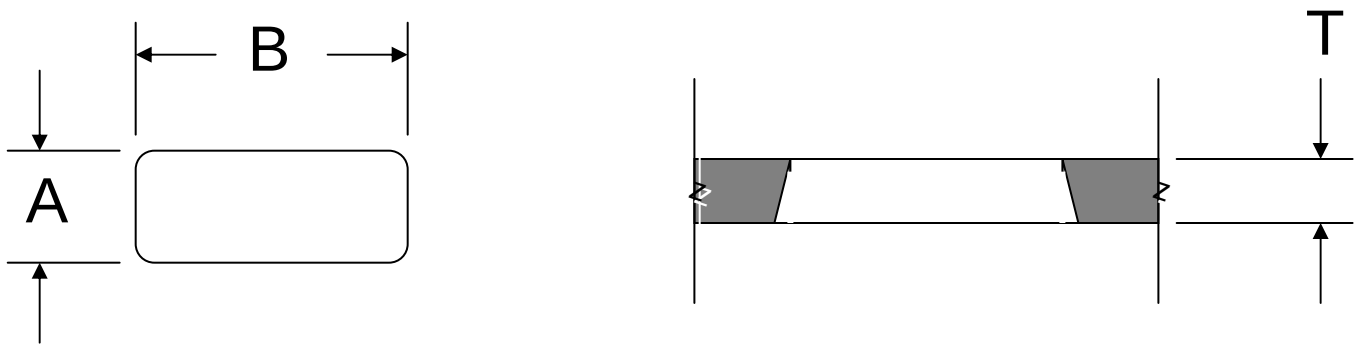
- It is paramount that the package and PCB remain parallel during the assembly process to achieve a satisfactory mechanical and electrical interface.

Solder Printing

- The IPC-7093 standard recommends that to optimize the reliability of the solder joints on the perimeter lands, the standoff dimension after reflow processing should be approximately 50 microns (2 mils).
  - *Many users believe that this thickness will provide clearance for cleaning and furnish a robust electrical and mechanical interface.*
- To achieve this standoff dimension the thickness of solder paste printed onto the lands should be no less than 100 microns (4 mils).

Solder Stencil Fabrication

- When using laser to ablate the stencil openings, the aperture sidewall will be slightly tapered.
- The tapered sidewall of the aperture will enhance solder paste release during printing.



(A x B) x T = solder paste volume *[1]*

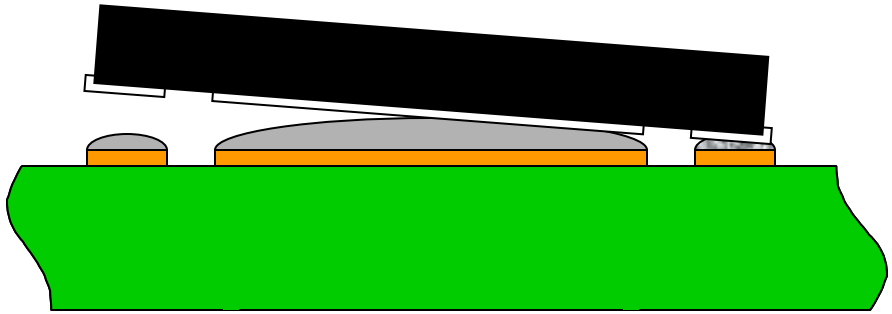
[1] The alloy solids make up about 50% of the total volume of the solder paste used for stencil printing.

Stencil Aperture Criteria

- Although component suppliers may have a specific recommendation for solder paste print area-to-land area, a 1:1 stencil aperture to PCB land area is generally acceptable.
  - It is not uncommon, however, to reduce aperture length in the stencil for the pullback terminal variations because of the smaller terminal area on the package.
- To control the effects of the large surface area of the thermal pad feature during the reflow soldering process, it will be necessary to tailor the solder stencil pattern or to partition the mating thermal plane on the PC board.

Comparing the Affect of Print Pattern on Reflow Solder Process

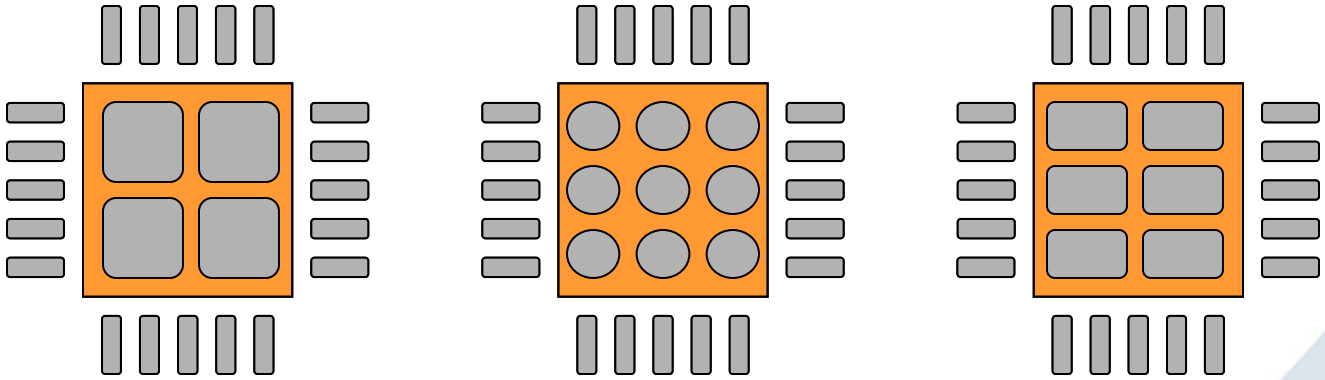
- Users have observed that during the reflow process the liquidus solder can raise the device creating a pivot point near the center of the DAP.



- As the solder cools the device can tilt toward one side, often creating shorts in one area and opens in another.

Stencil Partitioning on Thermal Pad

- When solder is to be used for joining the thermal features it is recommended that, rather than one large opening matching the DAP outline, a pattern of smaller openings be furnished on the thermal pad region to provide approximately 50% to 80% printed solder paste coverage.



Comparing the Affect Using a Partitioned Print Pattern

- By partitioning the print pattern on the thermal pad, solder paste will retain a more planer profile during reflow soldering.

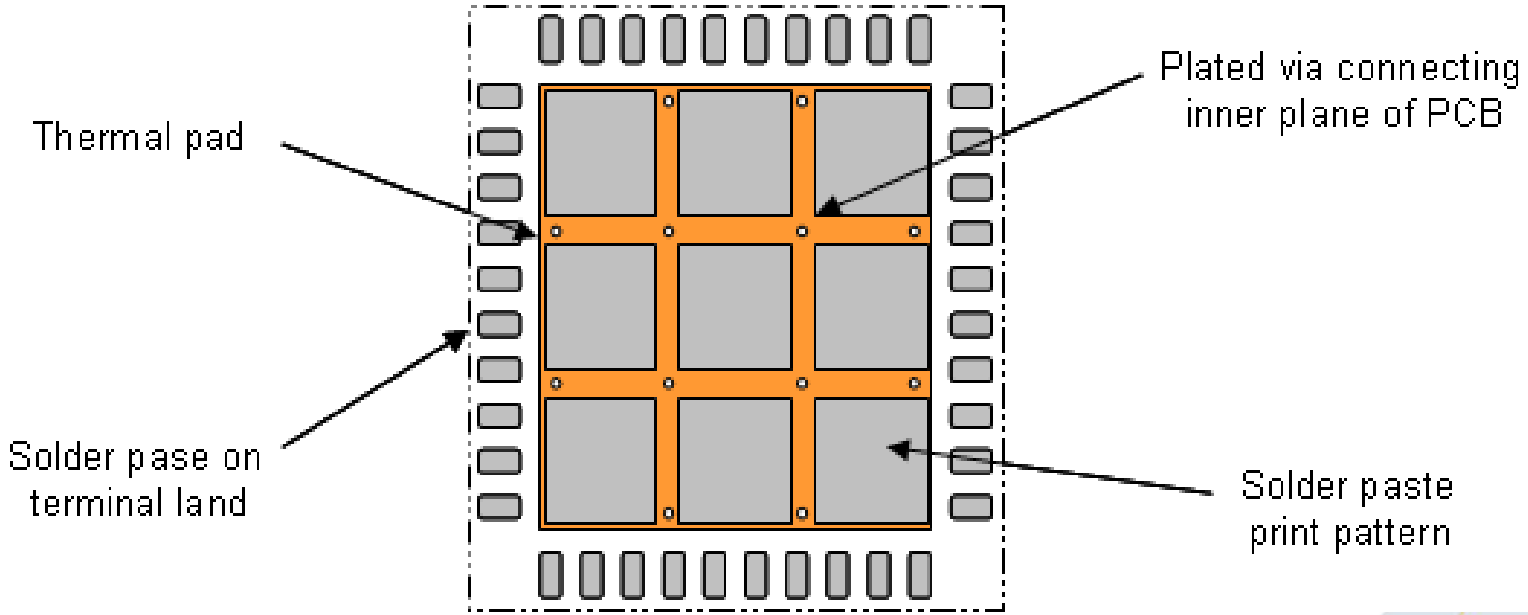
Rather than coagulating in the center of the thermal pad during reflow soldering, the partitioned solder pattern will maintain a uniform interface between surfaces.

Recommendations for Stencil Partitioning

- For DAP sizes between 2.10mm and 4.40mm square, four openings are recommended separated by 0.20mm to 0.30mm wide street.
  - This will reduce solder paste coverage by 70% to 85% and promote leveling during reflow soldering.
- For the DAP areas that are greater than 4.40mm square the process engineer may want to specify a stencil that can furnish additional stencil openings.
  - These segmented patterns should be calculated to reduce solder paste coverage by 65% to 85% to further enable a degree of self-leveling.

Improving Thermal Control

- To further enhance thermal transfer the designer can add a number of 0.3 mm (.008”) diameter plated vias within the intersections separating the solder paste stencil openings.



Summary and Conclusion

- For a majority of commercial applications the no-lead package is finding wide acceptance.
- There remains a number of concerns, however, by users developing products for use in harsh environments.
  - This is due in part to the very low stand-off height of the no-lead package and the electronic industries transition to RoHS compliant solder alloys and PCB materials.

Summary and Conclusion cont.

- The more traditional SMT leaded packages (SOIC, QFP) have relatively long and somewhat flexible leads to compensate for the coefficient of thermal expansion differentials of dissimilar materials.
- The tin-rich Pb-free solder alloys are far more brittle than their eutectic predecessors-
  - When exposed to extreme thermal operating conditions the Pb-free solder used to attach the no-lead packages cannot absorb the stresses and strains introduced by the differing CTE between the package and the PCB substrate.

BTC Task Group Member Recognition:

Richard Arnold	Continental Automotive Systems, Seguin TX	User
Scott Buttars	Intel (Hawthorn Farm Campus)	User
Bev Christian	Research In Motion	User
Don Dupriest	Lockheed Martin MFC	User
Werner Engelmaier	Engelmaier Associates, L.C.	General Interest
Thomas Gardeski	Gemini Sciences	General Interest
Mike Green	Lockheed Martin Space Systems	General Interest
Dave Hillman	Rockwell Collins	User
Constantin Hudon	Varitron Technologies inc.	User
Bill Kunkle	MET Assocs	General Interest
Paul Lotosky	Cookson Electronics	Supplier
Jack Olson	Caterpillar, Inc.	User
Richard F. Otte	PROMEX INDUSTRIES INC	Supplier
Stanton Rak	Continental Automotive Systems – Deer Park, IL	User
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Bob Wettermann	BEST Inc	Supplier
Linda Woody	Lockheed Martin	User

Thank you

Vern Solberg
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