A Comparison of Registration Errors Amongst Suppliers of Printed Circuit Boards

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Abstract
Misregistration of holes is the maximum amount of variation between the centerlines of all terminal pads within one plated through hole in a printed circuit board. The impacts of misregistration can be very serious due to possible electrical opens caused by breakouts or a short or intermittent connection due to a violation of the minimum clearance. This study highlights the differences in registration in Printed Circuit Board (PCB) samples made by the same supplier at two geographical locations. The intent is to determine a statistical correlation between the populations of registration error measurements taken on samples, from layer-to-layer or across layers, and reliability or performance risk. The study includes comparisons between PCB samples made in both the locations. The focus of the comparison includes studying whether both populations reflect the same statistical results, trying to understand where the difference in population occurred and maybe answer the question - which population has the lower amounts of misregistration between layers. Misregistration occurs during board fabrication and is directly attributed to problems involved with the production of the artwork, with artwork materials, with the setup procedures during lamination, and/or with the dimensional instability of the laminate materials used.

Introduction
Printed circuit boards (PCBs) provide the wiring substrate for electronic packaging upon which electronic components are installed to realize functional circuits. PCBs are used in a variety of electronic systems from simple one-transistor amplifiers to large super computers. A PCB serves three main functions: 1) it provides the necessary mechanical support for the components in the circuit 2) it provides the necessary electrical interconnections and isolation, and 3) it bears some form of legend identifies the components it carries.

Printed circuit boards can be classified into three categories based on their construction and physical characteristics: rigid, flexible and rigid-flex boards. Rigid circuit boards are a composite laminate structure in which solid copper sheets are laid down and separated with a dielectric material, which is commonly an epoxy resin system. Rigid boards represent the most widely used category and they can be built from different materials systems. Flexible printed circuits consist of thin copper foil bonded to a thin plastic base. The base material most frequently used is polyester film[1][3]. This type of board is usually limited to a single- or double-sided board and is only used for very small components. The third category is the rigid-flexible boards which is a combination of rigid and flexible boards bonded together[7]. The rigid portion supports the components while the flex portion allows the structure to be folded. For the purposed of this paper, ceramic-based circuit boards used in analog and high-speed multichip modules are not addressed.

Attention will be given to the rigid printed circuit boards since they represent the highest volume used industry-wide and it is within this category that the major challenges in terms of fabrication, materials, and applications are encountered[2]. Rigid printed circuit boards can be further categorized in terms of circuit complexity and base materials. Circuit density can force the design to be single-sided, double-sided, or multi-layer. A single sided board has interconnect metallization on one side only, while the double-sided board has metal interconnects on both sides. On double sided boards, connections between the two layers are made with small conductive holes called “vias”. A multilayer board has metal interconnects on one or more internal layers in addition to the top and bottom.

Changes in substrate technology have been very active since the 1980s when applications and performance advantages were realized from miniaturizing electronics.[4][5] Technology roadmaps lead towards higher densities continually requiring newer materials, new test equipment, and new assembly equipment.

Part design and PCB design go “hand-in-hand.” Some of the challenges associated with increased computing and data processing performance in smaller form factors are thermal management, signal loss and crosstalk, difficulty manipulating small components, reduced tolerance for misplaced component leads and solder, Electrostatic Discharge (ESD) protection, and reduced tolerance for machining variation. In order for modern integrated circuit chips and their packages to be compatible with the PCB, the PCB designer has to design the substrate with an equally state-of-the-art technology in a manner that would enable easier assembly and better performance. Thus, the total number of components attached to a single assembly is increasing, while the available real estate on the substrate is shrinking. With increased complexity comes

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increased I/O count and reduced I/O and pad pitch in packages. Reduced I/O and pad pitch brings challenges for both assemblers and bare board manufacturers in terms of handling, registration, co-planarity, and alignment for the assemblers and issues of land size, solder mask, and electrical tests for the board manufacturers. Design challenges for board manufacturers arise when escape routing of high I/O packages is done by increasing the line density between vias.

Major challenges in manufacturing printed circuit boards to the specifications are equipment based and include manufacturing equipment, assembly equipment and testing equipment. Larger boards with narrower vias and denser lines pose difficulties. Better patterning techniques help in developing lines with lesser width and pitch. Misregistration is the maximum amount of variation between the centerlines of all terminal pads within one PTH. Misregistration occurs during board fabrication. A few causes of misregistration include:

- Dimensional instability of the base material including the prepreg
- Registration of the artwork
- Careless punching of artwork and/or layers
- Out-of-parallel laminating plates
- Inadequate pinning
- Unstable artwork
- Worn or deformed holes in the artwork

Misregistration is usually detected optically by observing a vertical cross-section right through the middle of the PTHs. However, this process is destructive and time consuming. Inspection by means of x-ray is another inspection technique. Not only is the technique non-destructive, but the throughput in x-rays is high. The amount of misregistration is determined by calculating the difference between centerlines of terminal pads that are shifted to extreme positions. The impacts of misregistration can be very serious due to a possible short caused by violation of the minimum clearance.

The lamination process involves the impregnation of the weave fabric with epoxy to form a laminate. During the lamination process the thin-core inner-layers are subjected to heat and pressure and compressed into a laminated panel[6][10][11][12]. Sheets of material consisting of glass fibers impregnated with epoxy resin, known as prepreg or b-stage, are slipped between the layers and bond the layers together. Prepreg is available in different styles with varying ratios of resin to glass fibers. This choice of differing epoxy resin to fiber glass ratios allows the manufacturer to control the thickness between layers and to provide the appropriate amount of resin flow between circuitry. Lamination steps are fairly consistent among manufacturers. In lamination, the pressing parameters must closely match what the laminator recommends. If the heat rise of the pressed book is not maintained as per manufacturer's specifications, the resin will not have enough time to properly wet-out the cores that are being pressed. Laminate voids or other lamination defects may occur as a result. One lamination process is a Standard Hydraulic Lamination. Steam press, hot oil press, or electrical resistance heaters are common elements used by this process to heat the PCB. Using the steam and hot oil method allows for a higher heat rate to be achieved but the maximum temperature reached is relatively low. A caution for the steam press is the lamination temperature may not be met during a typical lamination process.

The second process is Vacuum-Assisted Hydraulic Lamination (VAHL). This is the most widely accepted process practice in the industry today. Before the lamination process occurs a vacuum cycle of 15 to 60 minutes occurs where moisture, air, and other volatiles are pulled out from the PWB stack. Note that this is very different from a pushing out method as utilizing a pushing out method can still cause volatiles to be trapped in the finished PCB. Then follows a typical Hydraulic Lamination process. The vacuum cycle helps lower the pressure need for lamination. Lower pressures can help reduce the effect of misregistration by roughly a thousandth to two thousandth of an inch. In the world of electronic packaging this is very substantial and allow even smaller traces to be created and increase the amount of signals in a layer on a board.

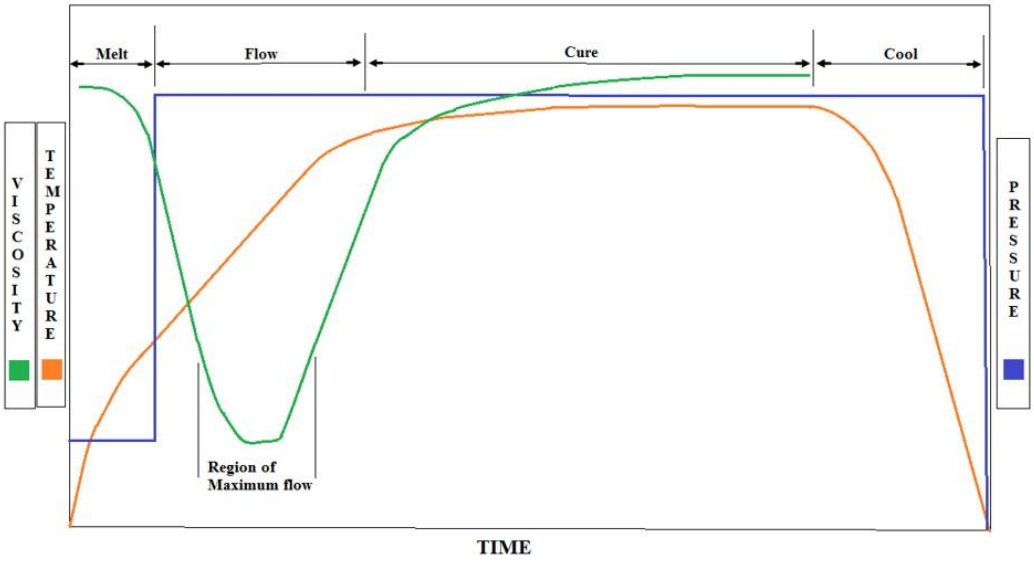

Figure 1 Overview of the time, temperature and pressure relationship used during the printed circuit board lamination process.

The third process is an Autoclave Lamination. The PCB is sealed in a vacuum chamber with high-pressure heated gas. This creates a uniform hydrostatic pressure force. The downfall to this process is the pre-vacuum cycle will take much more time than a VAHL and the heat up rate is slower compared to the other lamination process.

Registration can be different for different laminate materials and between suppliers. Figure 2 shows a schematic illustration of a printed circuit board internal annular ring. Typical materials chosen for the main structure of the boards include FR4, polyimide, HDI-FC film or halogen-free. The selection of the material consequently decides which lamination process is used by the suppliers. Another driver is the decision of what kind of prepreg is chosen. Some designers may prefer a "no flow" prepreg, a prepreg with the tendency not to expand during flow region.

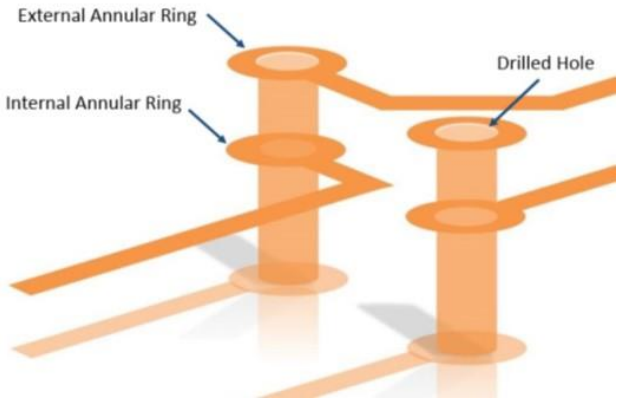

Figure 2 Schematic illustration of a printed circuit board showing internal annular rings[13].

Additional drivers include size of the panel or individual boards before the lamination process, which can vary greatly. From industry experience, after a board undergoes a lamination process it shrinks. So typical manufacture make boards slightly larger than usual in order to correct for the shrinkage. Special attention is given to the glass/resin ratio of the prepreg - the heavier the glass, the more likely drill bit deflection will occur. As a common practice, a thinner glass is recommended.

Experimental

The goal of the test plan is to design in variations in the printed circuit board(PCB) internal annular ring (IAR) geometries and correlate the effects of these variations as a source of risk for PCB failure in the test and mission environments. Reliability tests such as temperature cycling, and mechanical flexure will be conducted on test samples constructed with controlled IAR widths, sub-optimal IAR widths and other configurations such as teardrops. Part of this study is to demonstrate that internal annular rings with sub optimum dimensions exhibit a similar level of reliability as the internal annular rings with the dimensions as per specifications.

Two geographical sites of the same printed circuit board supplier (named supplier A and supplier B) were contracted to fabricate printed circuit board test samples. Each site was contracted to fabricate twenty test boards, for a total of forty test boards. Although the primary features on the test samples were internal annular rings intended for a study unrelated to the current research paper, the test boards also included test features, examples of which are shown in Figure 3.

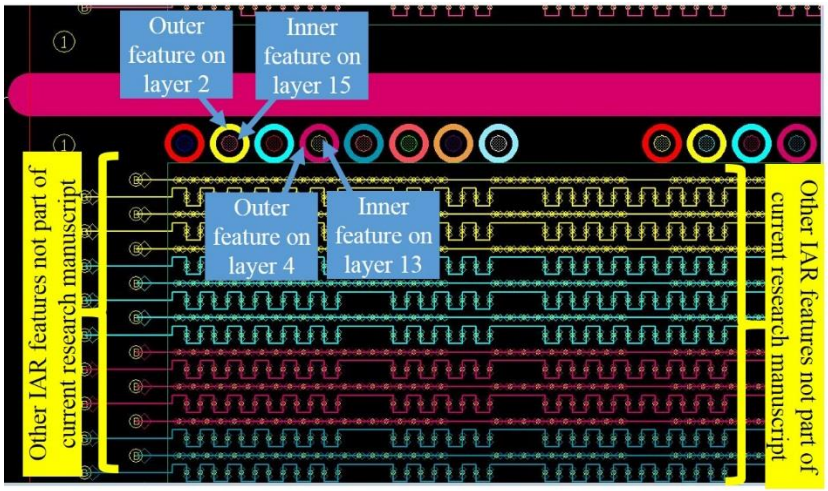

Figure 3 A screen snapshot of the design file used in test board fabrication. The snapshot shows the location and shape of the test features discussed in this research manuscript.

The test patterns used for this study consisted of an outer "donut" shaped circular feature placed on a single plane of the sixteen-layer board, and a second "solid" feature which was designed to be oriented at the center of the first feature but placed at a different plane than the first "donut" shaped feature. As shown in Figure 3, the second (annotated) feature from the left contains the donut feature on layer two of the sixteen-layer board, and the solid feature location on layer fifteen of the board. The fourth (annotated) feature from the left contains the donut feature on layer four of the sixteen layered board, and the solid feature is location on layer thirteen of the test board. These test patterns were repeated along the entire board, with the donut and solid feature placed on varying layers.

Measurements of the annular ring separation between layers in the board, were conducted three times. The first process started by taking misregistration measurements between the outer most layers, top and bottom layer. The next measurement was between one layer below the top layer and one layer above the bottom layer. This pattern of a step size increase of one layer for the next measurements continued until the separation between layers became one or the center of the PCB was reached (1-16, 2-15, etc.). The second process took measurements between the top layer and the adjacent layer below, which continued for subsequent layers (1-2, 2-3, etc.). The third process took measurements between every other layers starting from the top-most layer and concluded at the bottom-most layer(1-3, 2-4, etc.).As shown in Figure 3, there are other internal annular ring and daisy chain features on this test board; however, the applicability or testing of test features will not be discussed in this manuscript.

All as-received test board samples from both the suppliers were inspected and checked for electrical continuity with two-wire resistance measurement method. An external optical inspection was also performed on the test boards. After the boards were checked and accepted, x-ray inspection was performed on the test patterns. X-ray microscopy is used to conduct internal inspection on the test boards to verify the attributes of the test patterns and conduct dimensional measurements that can help in establishing the degree of misregistration. A production X-ray system capable of performing 2D and Computed Tomography (CT, 3D) inspection, with a resolution of 0.3 mm, a magnification of up to 10,000X, and a maximum tube voltage of 160 kV was used for this study[8]. The x-ray inspection consisted of a top-down view x-ray radiograph acquisition of all test boards at the highest magnification achieved by the system. Each test board contained twenty to thirty sites of interest. As each pattern was inspected, the corresponding image in jpeg standard format was saved to the computer. A sample x-ray radiograph is shown in Figure 4. In Figure 4, radiograph (a) shows a donut pattern, which was designed on layer 2 and an inner solid pattern on layer 15. Radiograph (b) shows a similar pattern where the outer donut is designed on layer 15 and the inner solid pattern is designed on layer 2.

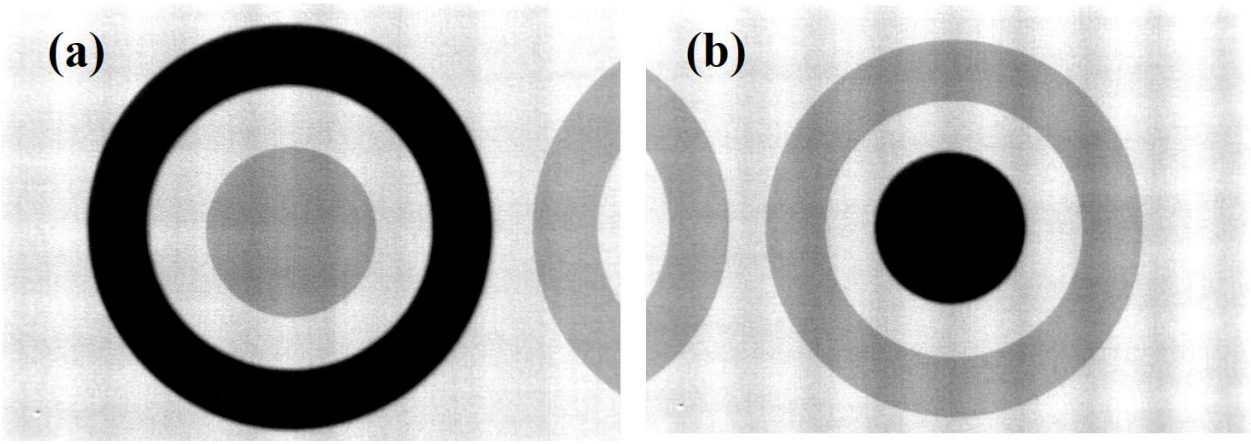

Figure 4 Sample x-ray radiographs obtained on the test boards. Similar radiographs were observed at each test pattern location on each of the forty test boards. Radiograph (a) shows a donut pattern that was designed on layer 2 and an inner solid pattern on layer 15. Radiograph (b) shows a similar pattern where the outer donut is designed on layer 15 and the inner solid pattern is designed on layer 2.

After the x-ray radiographs were acquired for each test pattern location, image analysis was performed. The analysis was performed using production software[9].The image analysis software allowed for the measurement of the relative separation between the centers of the donut shaped feature and the solid circular feature. Also, for the documentation of the variations in layer-to-layer registration observed by means of the test patterns designed in the test boards. The results were recorded and documented in production spreadsheet format. A box and whisker plot of the calculated misregistration between supplier A and supplier B is shown in Figure 5.

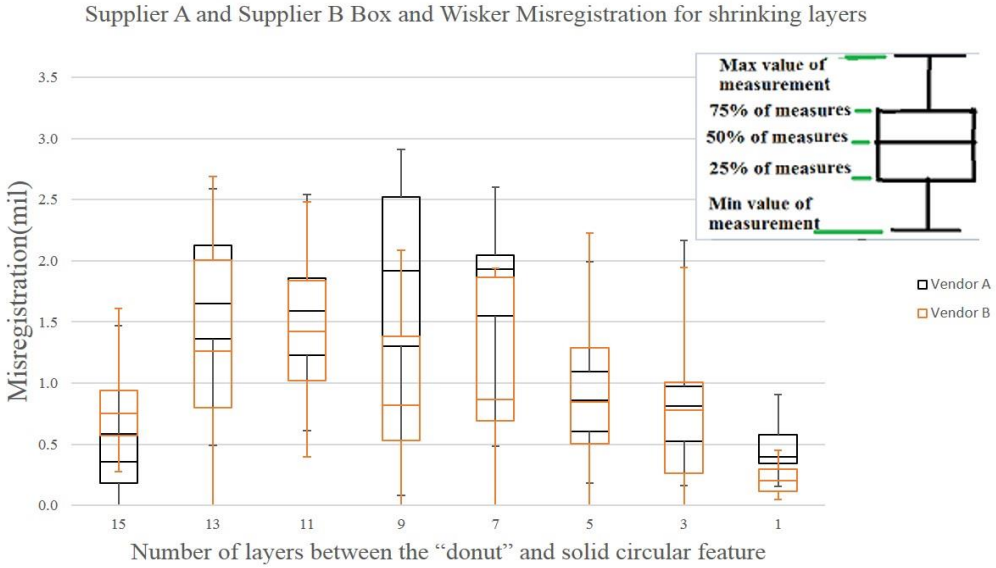

Figure 5 A box and whisker plot showing calculated misregistration between supplier A and supplier B for shrinking layers.

From Figure 5**,** the largest misregistration is observed to occur toward the center of the plot. Mostly at a layer separation (or delta) between seven and nine. It will be necessary to monitor the layers associated with these deltas in the lamination process because it may provide some clues as to why misregistration is so large. Another situation that was observed is at a delta of 1 and 15, where the misregistration is the smallest. A delta of 1 refers to the two layers in the center of the board that lie on top of each other and a delta of 15 corresponds with the two outermost layers. With this evidence, a preliminary conclusion can be made about the relative displacement of the layers. The lateral displacement at the topmost and bottommost layer was almost identical. At the center layers, the same concept applies, which caused misregistration between the layers in question to be small.

An effort was made to mathematically fit polynomial functions to the observed misregistration. When the calculated misregistration data were selected for the layer separation between one and seven, it was found to fit the3rd order polynomial equation.

$$y = 0.024x^3 - 0.2546x^2 + 0.8893x - 0.1887 \quad [1]$$

When the number of layers separating the donut and solid feature was selected to be between seven and eleven, the following 2nd order polynomial equation was best suited.

$$y = -0.0431x^2 + 0.7159x - 1.0915 \quad [2]$$

When the number of layers separating the donut and solid feature was selected to be between eleven and fifteen, the following 2nd order polynomial equation was best suited.

$$y = -0.1723x^2 + 4.2039x - 23.823 \quad [3]$$

The functions have some limited applicability for calculating an upper bound of misregistration between layers with a given amount of separation; however these calculations will have to be conducted with numerous assumptions about the materials, geometries and the processes used for manufacturing the printed circuit boards, since there are many factors that influence misregistration including the number of layers, board thickness, prepreg materials, etc., the equations can be further developed by more testing to identify additional factors in the functions.

In Figure**,** a box and whisker plot represents the data from measurements taken between separations of a single layer. What is clear across multiple layers is that the test samples from Supplier A exhibit larger misregistration when compared with Supplier B. This separation is the highest between layers 3 and 4, where Supplier A has a significantly higher misregistration. This may be attributed to an anomaly within those layers during the lamination process at Supplier A. No clear conclusion can be made as to what occurred in order for the misregistration to be so large. However, to determine the cause of the anomaly, a more in-depth analysis, including failure analysis and destructive physical analysis would need to be performed, with discussions are ongoing with this site. A phenomenon that is observed when representing the data in this form shown in Figure 6, is a sinusoidal oscillating behavior. Taking a look at Figure 6 between layers 1 and 2 the misregistration is large, which then decreases between layers 2 and 3. This pattern of increasing then decreasing misregistration repeats from the top side of the board until the last layer is reached. A visual inspection of the plot is insufficient to attribute this oscillatory behavior to a root cause. One contributor could be the type of prepreg selected and the core material associated with it. A combination of the prepreg expansion and the core material constraining its expansion by expanding very little creates a stress concentration between the layers. This is a shear stress region between the layers with the prepreg and the layers with the core material. Since the prepreg and the core material are located right next to each other throughout the board this region affects all the layers in the board.

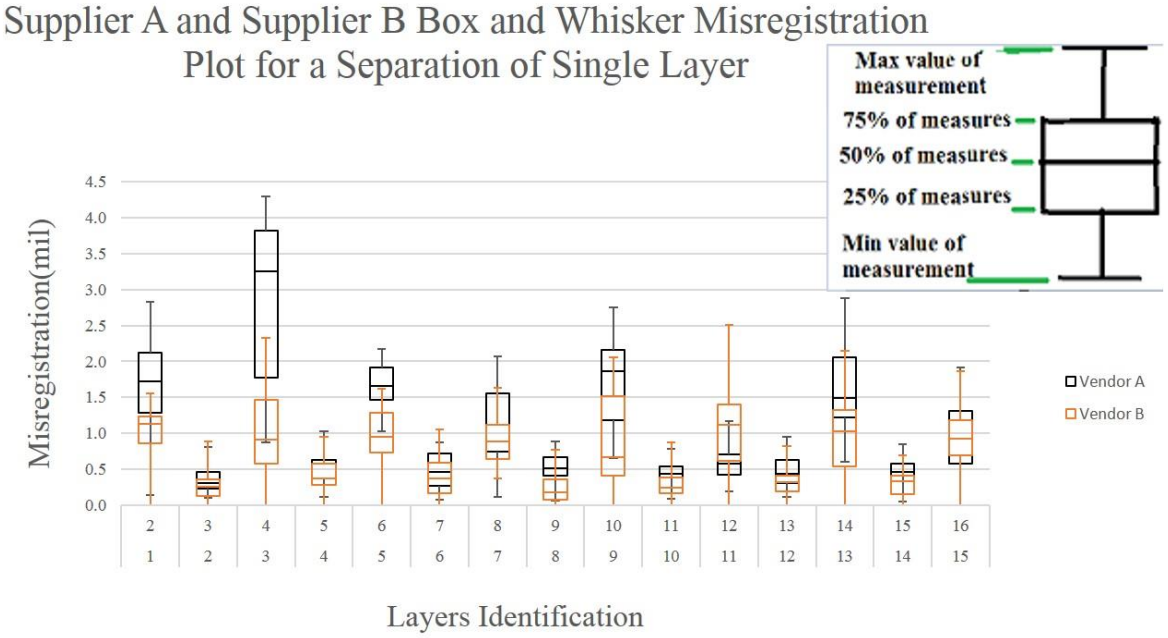

Figure 6 Box and Whisker misregistration plot for separations of a single layer.

The calculated misregistration data from both suppliers was fitted to a normal distribution to observe the mean and the variations associated with misregistration. Figure 7 shows that for Supplier B, the highest probability (0.85) exists that the average misregistration between the layers will be at 0.75 mils. The standard deviation is about 0.75 mils assuming that the center of the distribution is at 0.75 mils. Since Supplier B has a narrower range and larger peak than Supplier A, it implies

that Supplier B may have a better process control. For the Supplier B case, it is very likely to obtain a misregistration closer to the center of the distribution than in the case of Supplier A because its distribution has a larger spread. The larger spread of Supplier A means there is more uncertainty in the measure of misregistration. According to the plot, the Supplier A misregistration highest probability is at 1.25 mils. This is a much higher value than Supplier B, possibly implying that PCBs from Supplier A may carry a larger misregistration. Another way of thinking about the use of this plot is observing the chance of misregistration being 0.75 mils, Supplier A best case value, for Supplier B is about 50%. That is a 35% drop in uncertainty from Supplier A and as a consequence, there is a higher risk of boards from Supplier B of having shorts or opens within the layers. A short is a defect where the copper path in a PCB is connected at an undesignated point; while an open is an area on a copper path where copper is missing when it is not supposed to. The downside of Supplier A distribution is that it may be harder to implement new solutions that have an effect of reduced misregistration, hence, based on this assessment, working with supplier B to improve their process controls may provide substantial results.

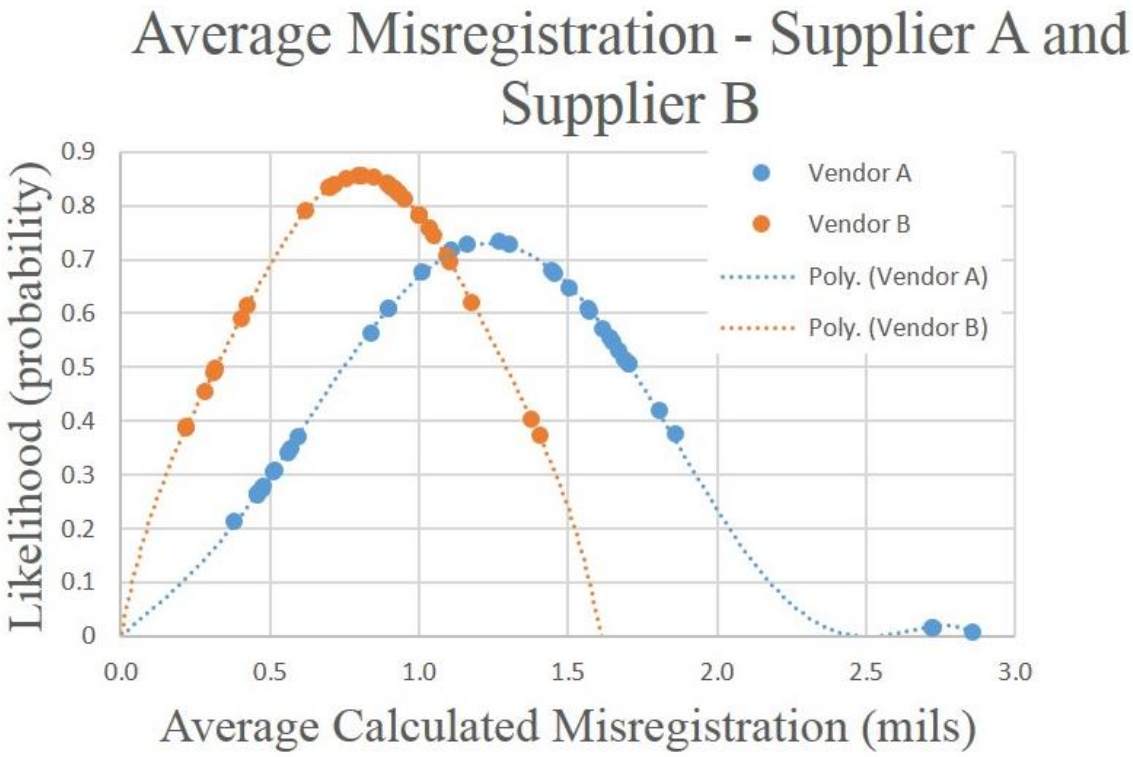

Figure 7 Average misregistration between supplier A and supplier B.

Results and Discussion

Supplier A and B are located in geographically separated locations, and the lamination processes and other parameters are markedly different as well. Because the laminate materials used were different, the corresponding lamination temperature and pressure profile from both location were very different from one another as well. In conjunction with the physical inspection of the test samples, image analysis and the comparative analysis on the test coupons, a finite element analysis methodology was also adopted. The FEA simulations helped in supplementing and providing a greater understanding of the test results. FEA modeling is a way to confirm whether the cause of misregistration is due to familiar factors identified in the lamination process. If the model and the experimental results converge, then the cause of misregistration is better understood and future effects may be predicted. Modeling also helps implement different solutions to stop large misregistration from occurring. Production simulation software was used to re-create the conditions the printed circuit board stack experiences during the lamination process as a way to observe misregistration. Modeling shows the change in misregistration between the selections of different prepreg material and lamination process parameters. The FEA model also provides an insight into the susceptibility of each prepreg to misregistration and what material property of the prepreg is of utmost importance for understanding misregistration. Another benefit of the FEA modeling is to determine how sensitive misregistration is to the pressure and temperature parameters that were discussed earlier. Overall the information gathered provides a guidance to the decisions on what should be done in order to prevent a heavy influence of misregistration in PCBs.

The model used to represent the PCB lamination process was a 2D model. A 2D model was chosen because the geometry of the test boards was relatively simple, additionally, there are no plated through holes or other features on the test boards. The accuracy of the FEA model is of concern, but more emphasis is directed at the location of the PCB misregistration. As an added benefit, the solving time for a 2D model is much shorter which is essential in running multiple iterations of the model

with different variations. Compared to a 3D model, where the benefits include modeling complex geometry and higher accuracy, a 2D model achieves the goal it is intended to do at a much quicker and simpler tempo. Some assumptions about the FEA model was made. The primary assumption is that the printed board test samples had no defects associated with them before they underwent the lamination process. It was assumed that both supplier site A and site B were able to fabricate defect-free laminates, which, in reality may not be the case. The prepreg and the core material were input with similar material properties. Another assumption is that the pressure force and temperature profile that a panel receives during the lamination process is identical to what a single board receives. During the lamination process, the top and bottom edges of the outer most layer is held to a fixed constraint. A vertical negative pressure force is applied only to the top-most layer and a vertical positive pressure force is applied only to the bottom layer. This represents a compressive load only in the vertical direction. The variable kept constant is lamination cycle time while only the lamination pressure and temperature were varied.

The input for this model started with the external and internal dimensions of a PCB, and layer count. Since the model is in 2D, only the length, 77.25 mm, and overall height, 2.293 mm, was taken into account. These inputs are the same inputs as the test boards. Each layer has a certain thickness depending on whether it is assigned the material property of a prepreg or copper foil and its location in the stack-up of the PCB.

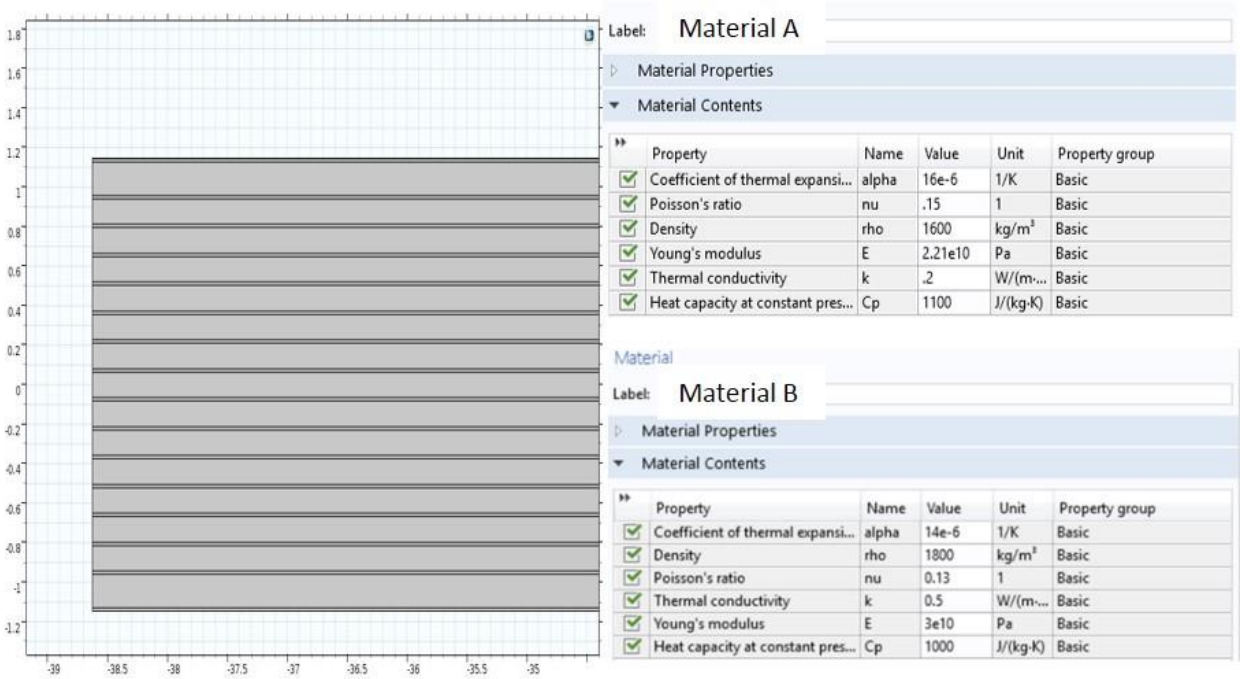

Figure 8 Geometry of the test sample and model input parameters.

The layers with copper foil in the model had the lowest thickness while the layers with prepreg have the larger thickness as can be seen in Figure 8. Associated with the prepreg and copper foil are material properties which includes Poisson ratio, Young's modulus, density, the coefficient of thermal expansion (CTE), and specific heat capacity found in Figure 8. Although Copper foil material properties are not displayed, they can be found from open literature. The numeric value of the material property is different for each prepreg. It is important to recognize the differences and how misregistration is affected. The final inputs are pressure and force, the period of time this pressure is applied, and the temperature profile applied. It is necessary to have those final inputs to recreate the lamination process that a laminate stackup undergoes. A classic lamination process starts with the PCB placed in a vacuum. Then a combined pressure and temperature gradient is applied for a limited period of time. At the end, the PCB is taken out of the vacuum and moves on to the laser plotter machine.

Figure 9 shows the FEA model displacements (in units of mil) experienced by the laminate stackup due to inputs of this model. A benefit to the model is understanding that there is expansion not only in the horizontal direction, the x-plane, but also in the vertical direction, z-plane. The focus of the results of the model will be only on expansion in the x-plane (because misregistration is primarily an in-plane phenomenon) and not z-plane, although the expansion in the out-of-plane direction is important for PCB reliability and its application environment. In the experimental results section, data on misregistration came from the horizontal plane so it is reasonable to follow the same practice.

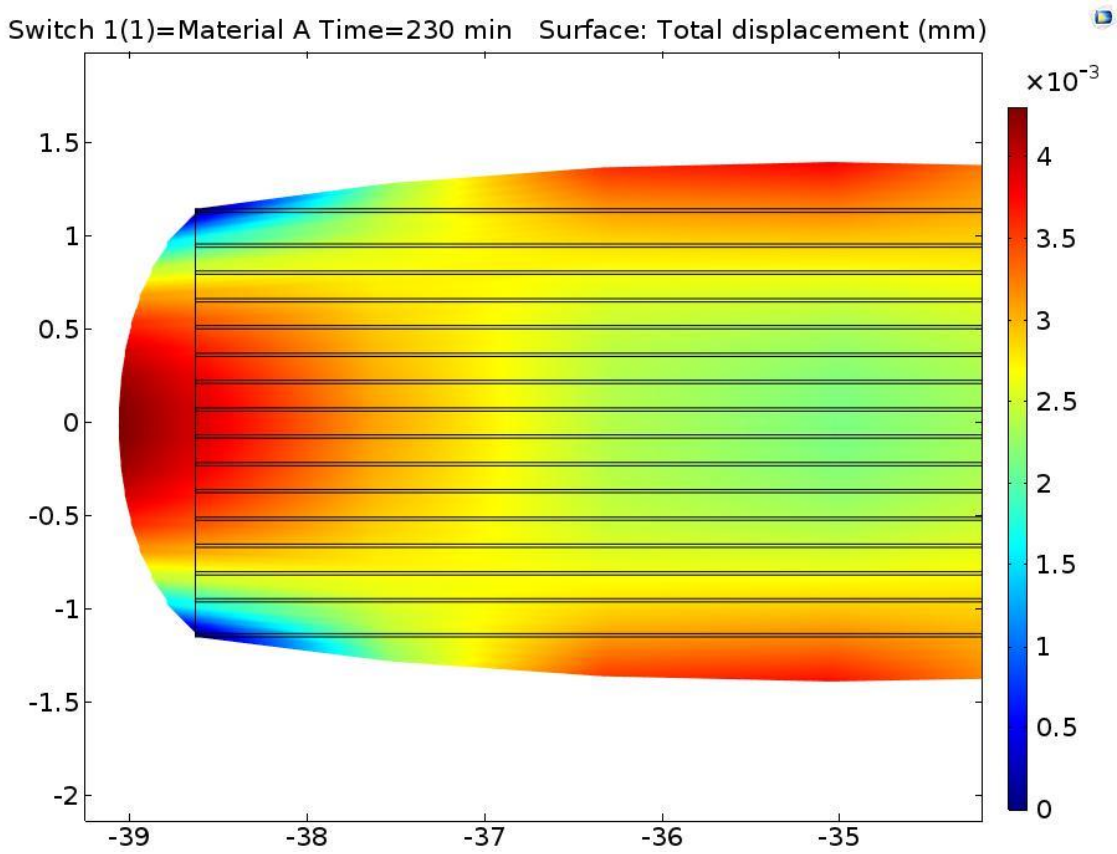

Figure 9 FEA model output showing calculated displacements.

The FEA model was first run using a constant pressure and temperature on the PCB. The temperature and pressure are typical values that are found in the lamination process and are available on the laminate manufacturers' websites. The trial FEA run was to observe the effects of different prepreg selections between the suppliers on misregistration.

Results from the model replicated the experimental results in the manner that Supplier A (material A) lateral displacement is higher than Supplier B (material B). This is shown in Figure 10 below. Layer 1T represents the top outermost layer while Layer 16 B is the bottom-most layer.

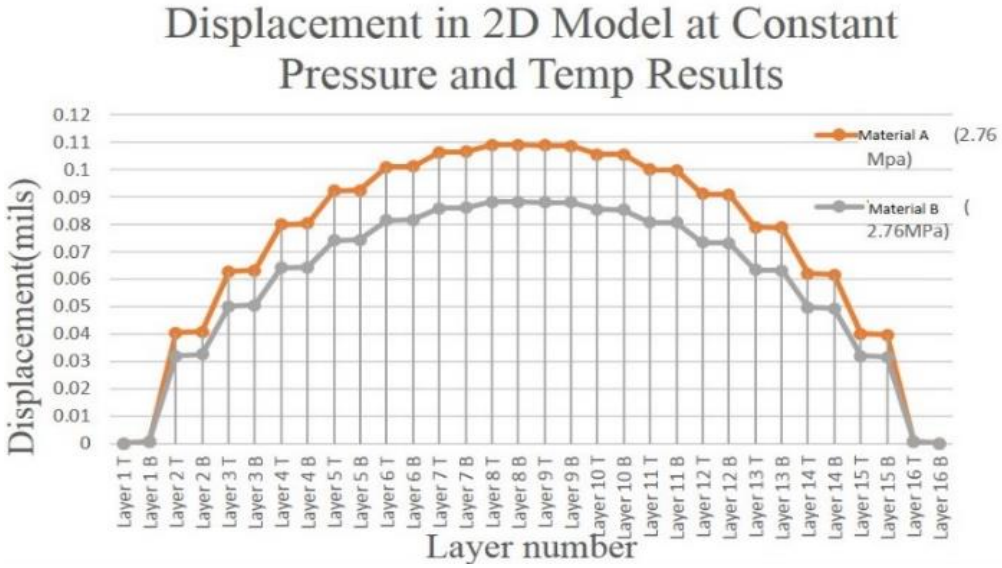

Figure 10 Displacement in 2D at constant pressure and temperature.

The region between the two markers represents the layer between the top and bottom layers. A key note is the letter "T" represents the top surface of that specific layer and "B" represents the bottom surface. This was to track internal displacement within the layer. According to Figure 10, there is some internal displacement within the layers which is minuscule compared with the intra-layer displacement. What is revealed by the figure is the largest displacement occurs at the center layers while the smallest is at the outer layers or in the layers closest to the outermost layers. Another influencing factor of displacement is the prepreg. Each layer is made of copper but in between each layer is prepreg and core materials for others. For example, in between layer 1 and layer 2, the prepreg has its largest displacement of 0.032 mils. The prepreg expands more than the copper so can be deemed as the most influential factor when it comes to misregistration and re-affirms the observations section.

The next step of the modeling was to change the material properties of the prepreg by fifteen percent with a step size of three percent for each trial. After numerous simulations, it was found that Young's modulus was the most dominant factor in the model to prepreg misregistration. This suggests that Young's modulus heavily influences viscosity as well. The larger the Young's modulus the less viscous the prepreg, which means a decrease in misregistration. So compared to other studies in the literature that focus on other factors of viscosity, it may prove significant to have an in-depth study of the relationship between viscosity and Young's modulus as it relates to prepreg selection. The goal will be to see if it can be possible to describe the behavior of the prepreg from one or multiple key properties and attain a physics of failure model. The use of Supplier A processing guidelines for lamination, shown in Figure 11 was used in an attempt to replicate the experiment results from Supplier A.

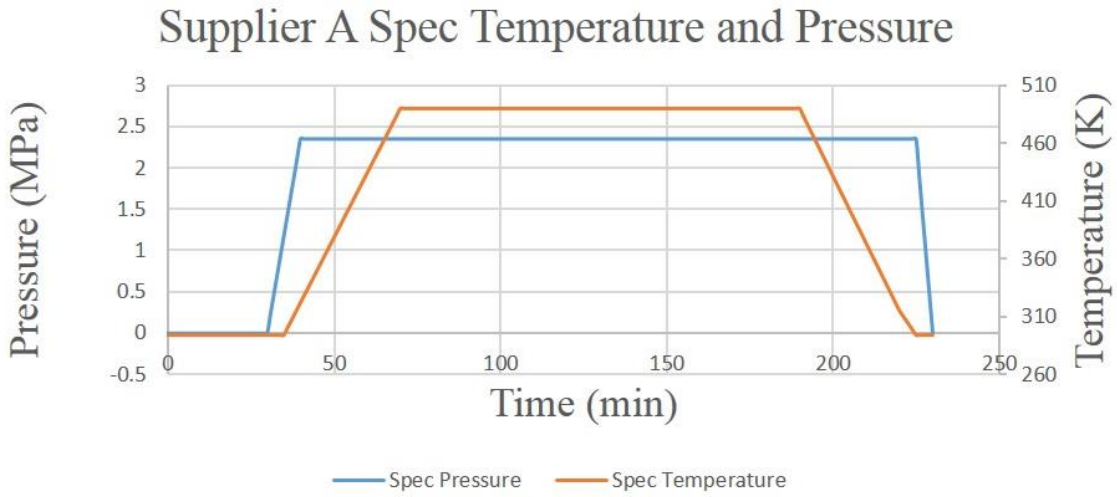

Figure 11 Lamination profile proposed by manufacturer of material A.

It was assumed that Supplier A, which had used material A, used these guidelines to laminate the PCB. The goal of this exercise was that by using the profile, the FEA model would be able to simulate similar experimental results. The next two figures display the FEA results from using the guidelines. Each bar in Figure 12 represent the displacements that were measured at that point in time.

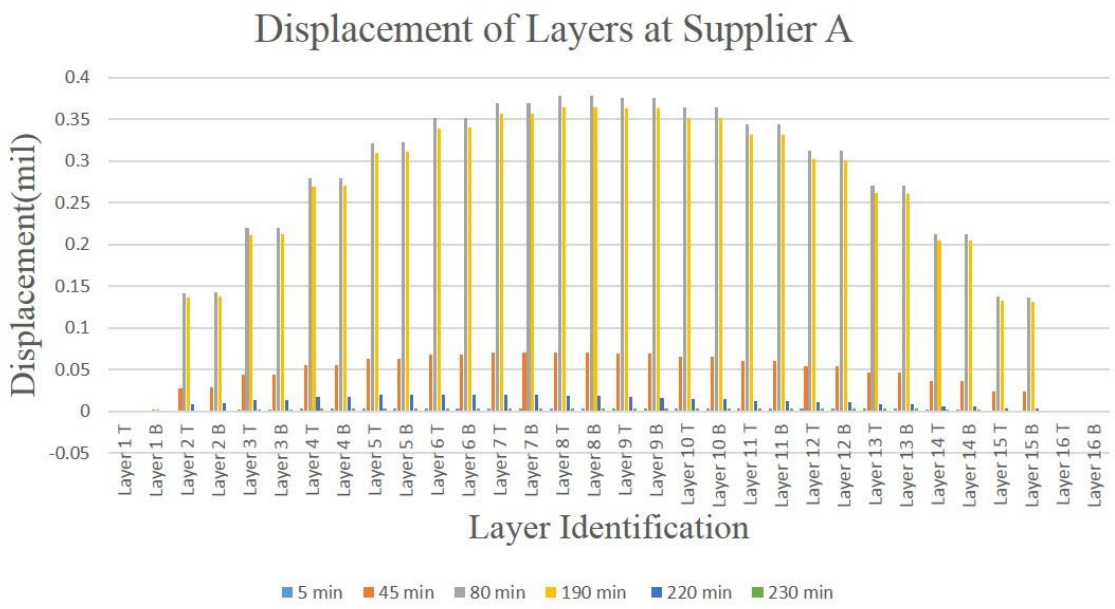

Figure 12 Displacements obtained from the FEA model after inputting the lamination profile suggested by the laminate supplier for material A.

Six periods in times were chosen in order to observe the change in displacement. The model started at a time equal to 0 minutes and ended at a time of 230 minutes. According to the FEA model results, using the processing guidelines does not replicate the magnitude of misregistration seen by the experimental results. At the final displacement time 230 minute, the displacement is so small that it is barely visible on the plot. As observed by the analysis and shown in Figure 12, maximum displacement occurred at around 80 minutes in running time. This displacement is six times larger than at 45 minutes and a hundred times larger than at 5 minutes. At 110 minutes to 190 minutes later, a slight decrease in displacement occurs but it is very small. The displacements at 5 minutes and at 230 minutes are almost identical. The situation was interesting because the initial displacement and final displacement was initially expected to be different from one another.Figure 13 shows the FEA calculated displacement at the center of the PCB with respect to time for boards from Location A.

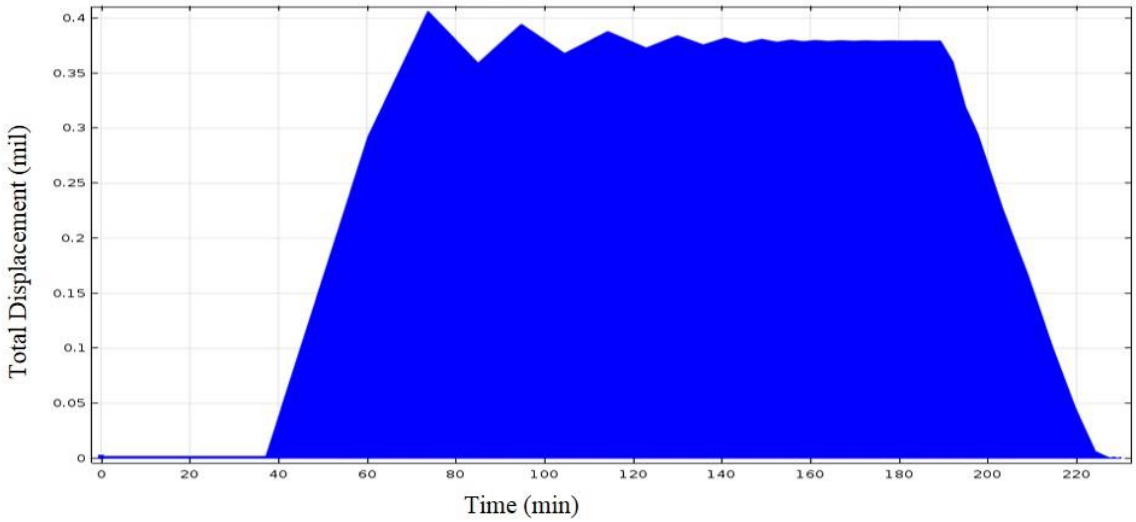

Figure 13 Displacements within the PCB layer, observed in the FEA model.

As seen in Figure 13, there is a sharp change in the displacement due to a combined effect of increasing temperature and pressure profile at close to 40 minutes into the lamination process (also shown in Figure 11). Once at 70 minutes, the pressure and temperature are at the peak. For the duration of 70 minutes to 190 minutes, the temperature and pressure are held constant. This brings displacement to equilibrium at 0.37 mils. Then after 190 minutes, the temperature undergoes a sharp decrease, which quickly returns displacement to measurements experienced at 5 minutes. This was very unusual because as temperature decreases it was expected that the PCB will have a harder time regaining its original state due to material

hardening. The assumption was at the end of the process the displacement should be significantly higher than the displacement at the beginning. A maximum misregistration of 3x 10^{-3} mils was observed compared to a typical misregistration of 0.75 mils, which was seen in the experiment. There is a factor of two hundred difference between the experimental data and FEA model with the supplier-recommended guidelines. This solicits the question of why is the difference is so large? A conclusion that can be drawn from the supplier's guidelines lamination process is that they do not follow the protocols defined by the laminate manufacturers. Therefore, by replicating the experimental results in the model will offer some clues as to which steps in the process contributed towards the misregistration observed in the experiments.

The next step in the model is to attempt to re-create the experimental results by adjusting the pressure profile and the temperature profile. After ten iterations, the profile that came closest to the experimental results was reached. Table 1 displays the pressure and temperature factors that were adjusted to recreate misregistration observed in the x-ray radiographs and calculated misregistration from the x-ray experiments. The first iteration are the values represented in Figure 12 and the last iteration are values represented in Figure 14. In between the two are the test runs with different outcomes.

Table 1 Pressure and temperature factors adjusted to obtain close correlation with experimental results.

Iterations	1(start)	10(end)
Max Pressure	1 MPa	2.41 MPa
Ramp-up Temp. Rate	3 K/min	8 K/min
Peak Temp.	180 K	510 K
Time Duration Peak Temp.	1.8 hours	2.75 Hour
Ramp down Temp. Rate	-3 K/min	-9.75 K/min
Initial Temp.	294 K	305 K
Final Temp.	295 K	315 K

Compared to the previous profile, in the profile shown in Figure 14, the maximum pressure was increased from 2.3 MPa to 2.41 MPa. As for the temperature, the time duration held at room temperature in the beginning portion of the profile was shortened by a half. The temperature ramp up rate increased by a factor of 1.5 and the peak temperature changed from 220℃ to 240℃. The duration the peak temperature was held increased from 2 hours to 2.75 hours. The ramp down rate increased by a factor of 1.5 and the final temperature of model change from 24℃ to 45℃. Reasons for the final temperature not being room temperature is an assumption that PCB suppliers may remove the PCB from lamination chamber and let natural convection cool the finished laminate board.

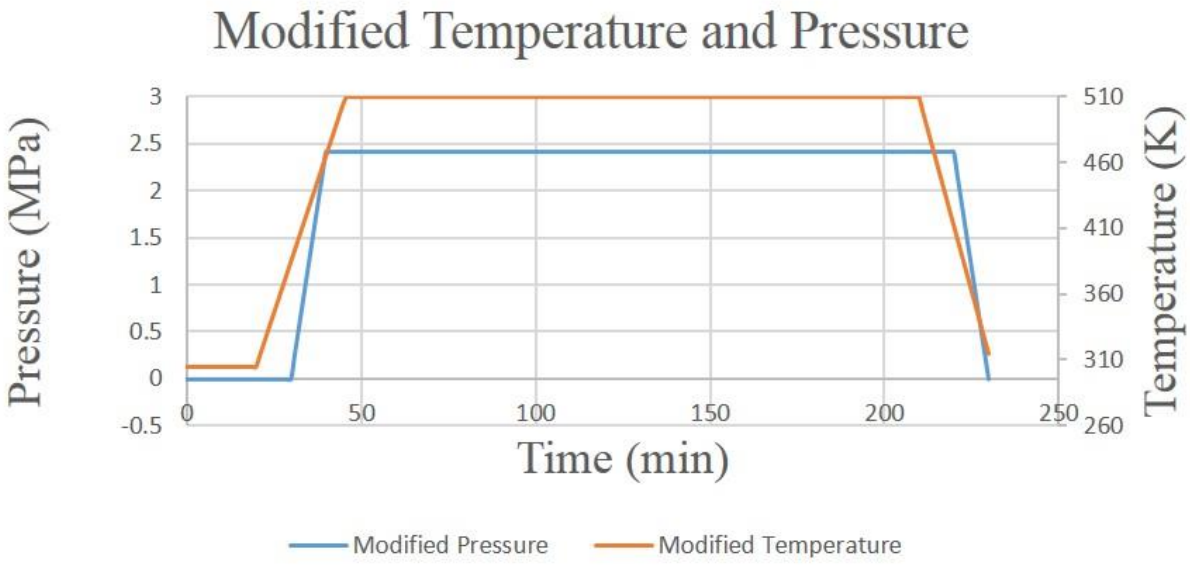

Figure 14 A modified lamination profile.

In Figure 15, the previous FEA results are represented by "230 min" and the modified profile is shown as "Replicate Experiment." Results from Figure 15show a higher misregistration compared to using the Supplier A guidelines. The difference between the two is about 0.15 mils larger at the center of the board. One conclusion that can be obtained is that Supplier A may have followed a profile very similar to that in Figure 14 in order to obtain the results observed from the x-ray study. Results show Supplier A may have in practice or through experiences increased the ramp-up rate, ramp down rate, and have a longer peak curing time for PCBs in lamination. These factors were identified from the model to have the most

sensitivity to misregistration. Adjusting even one factor in the temperature profile causes misregistration to shift dramatically. The pressure was found to have little influence on final misregistration. The results are still a 0.6 mils reduced from the experimental results. Additional factors need to be included into the model to obtain results that exactly match the results of the x-ray study.

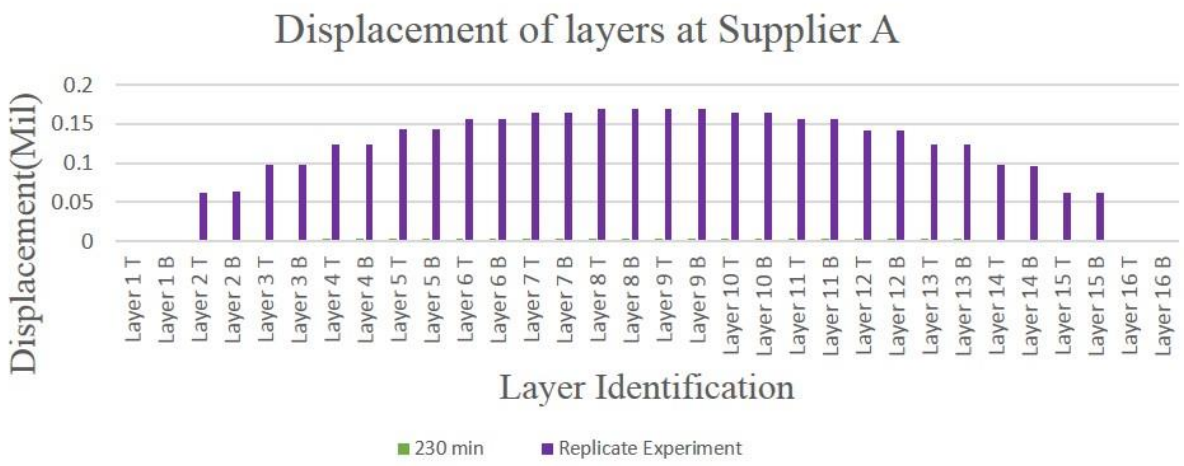

Figure 15 Displacements observed after modifying the simulated lamination profiles used in the FEA model.

Figure 16 shows the displacement of the modified profile from 0 to 230 minutes. As expected, the displacement seen using this profile is much different than the previous profile. The maximum displacement is 0.43 mils and an equilibrium at this point is achieved much faster.

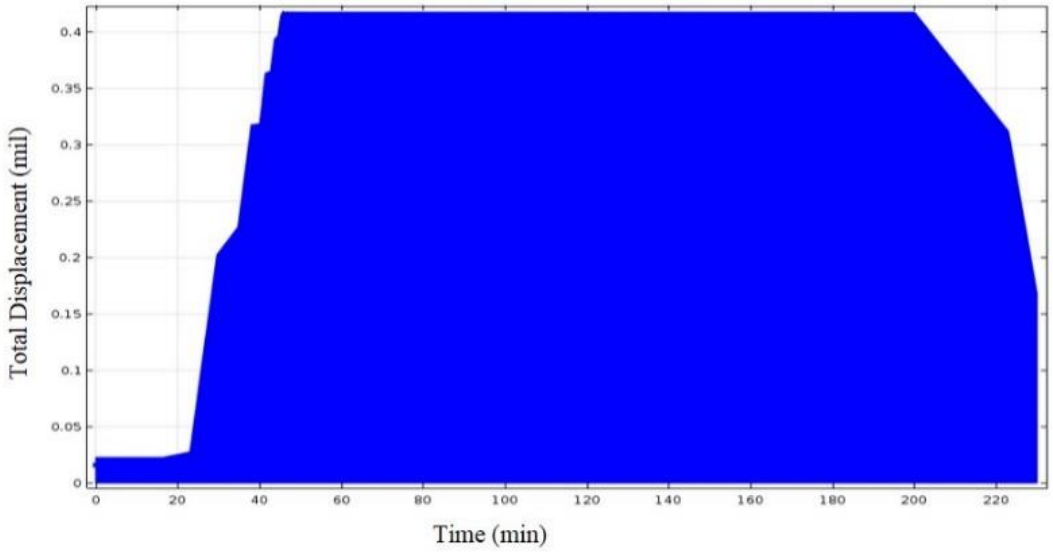

Figure 16 Displacements within the PCB layer, observed after the inputs into the FEA model were adjusted.

Of note is that the increase of ramp-up rate and ramp down rate caused a gradual influence on displacement. The relationship was quite an unexpected development and can be used to create a new assumption about future finite element analysis (FEA) models and PCB behavior during lamination. According to the model results, the initial displacement at the beginning of the lamination process and final displacement at the end was much different which agreed with an assumption about the behavior of the boards. The final displacement was about 0.10 mils larger than the initial displacement. In the figure, the final displacement reached at 230 minutes is 0.16 mils.

Conclusions

The continued fast pace towards miniaturization is leading printed board designers to advance integration density. The impacts of misregistration can be very serious due to possible electrical opens caused by breakouts or a short or intermittent connection due to a violation of the minimum clearance. Specialized test patterns were fabricated into test PCBs and used for calculating the amount of misregistration observed. The calculations were made on test PCBs fabricated at two

manufacturing sites of the same PCB vendor. The test samples, after fabrication, were inspected in x-ray and the radiographs were examined using image analysis techniques. A degree of misregistration was calculated from the radiographs. FEA simulations helped in supplementing and providing a greater understanding of the radiography and image analysis results obtained from the tests. FEA modeling is a way to confirm whether the cause of misregistration is due to familiar factors identified in the lamination process. The FEA model provides new relationships that previously were not reported in open literature and new factors to take into account that could not be observed by the experimental x-ray inspection or observed in destructive physical analysis (which was not discussed in the paper). This study represented the PCB lamination process and helped to provide an understanding of many assumptions. However, it is necessary to perform additional experiments and FEA models by varying factors such as ramp up, ramp down rate, peak temperature, etc.

This study highlights the difference in registration of PCB samples made by the same supplier at two geographical locations. The study compared between the samples made at both locations, however, the focus of the comparison was studying whether both populations are subjected to the same statistical results, trying to understand where the difference in population occurred and identified the population which has the lower misregistration between layers.

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A Comparison of Registration Errors Amongst Suppliers of Printed Circuit Boards

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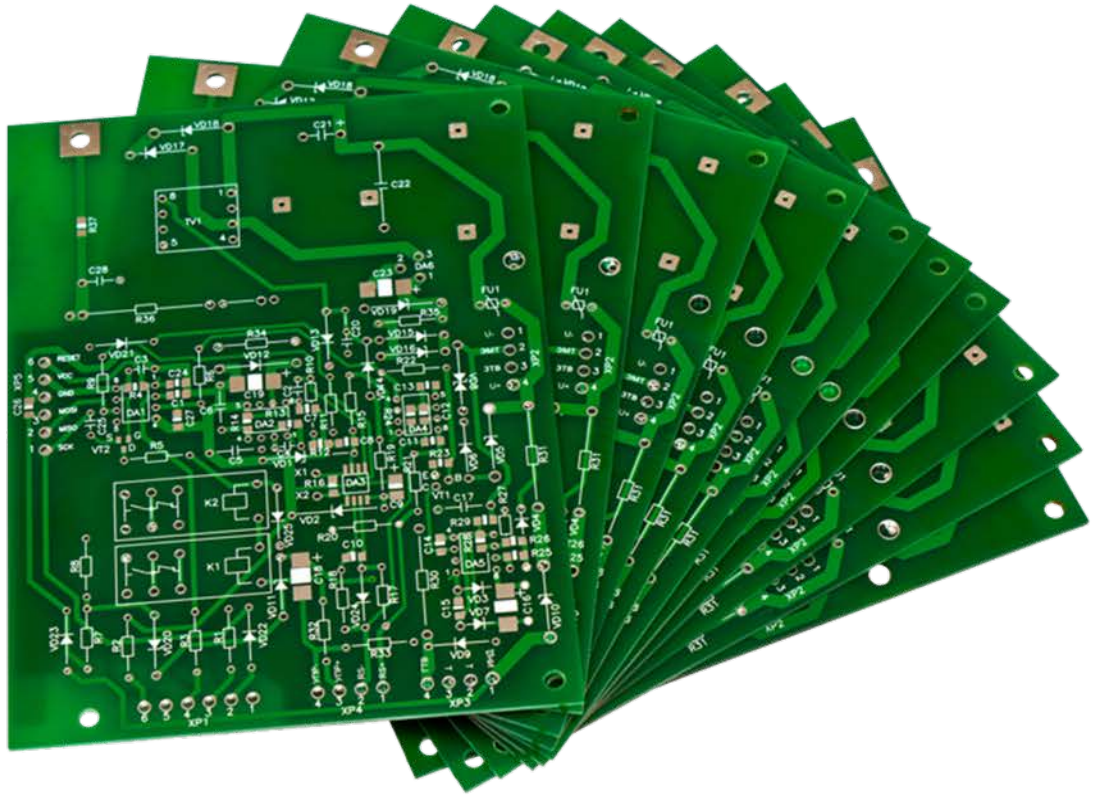
Overview and Goals

- The goal of the test plan is to design in variations in the PCB internal annular ring (IAR) geometries and correlate the effects of these variations as a source of risk for PCB failure in test and mission environments.
- Two geographical sites of the same printed circuit board supplier were contracted to fabricate printed circuit board test samples.
- The test patterns for this study consisted of an outer “donut” shaped circular feature and a “solid” feature which was designed to be oriented at the center of the donut shape.
- X-ray inspection was performed on the test patterns in order to reveal amount of misregistration that occurred.
- The study highlights the variations in PCB (Printed Circuit Board) layer-to-layer registration.
  - *The intent is to determine a statistical correlation between the populations of registration error measurements taken on samples, from layer-to-layer or across layers.*
  - *Provides a method to study the effects of PCB material properties and lamination profiles on misregistration.*
  - *Identify parameters not observed physically than can also effect misregistration.*
  - *Learn how important misregistration is to PCB manufacturing.*

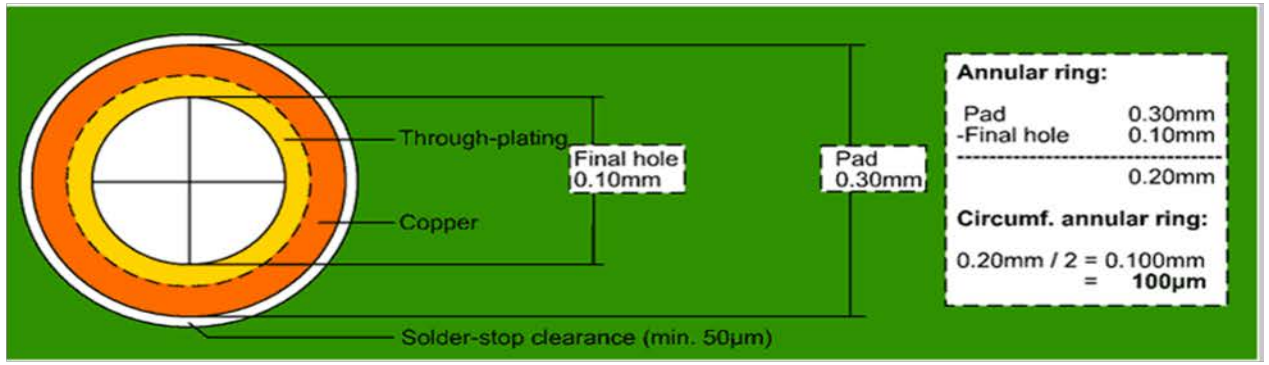
Changing PCB Requirements

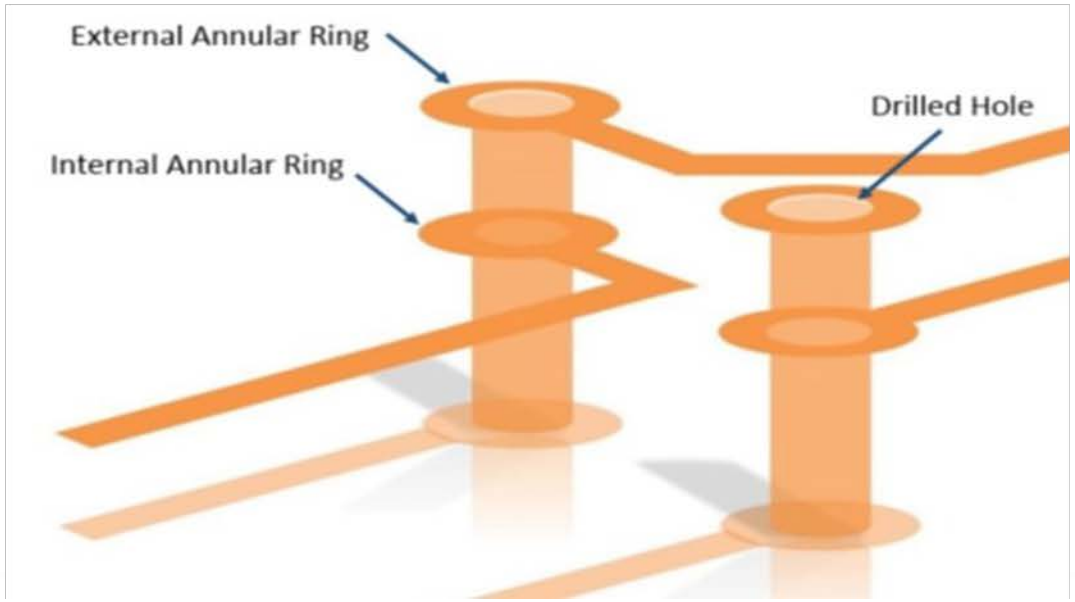
- PCBs are used in a variety of electronic circuits from simple one-transistor amplifiers to large super computers.
- As performance requirements increases, chip and package designers design for factors such as higher density, reduced real estate, and higher functionality.
- With increased complexity comes increased I/O count and reduced I/O and pad pitch in packages.
- This in-turn makes PCBs more sensitive to disturbances during board fabrication.



Misregistration

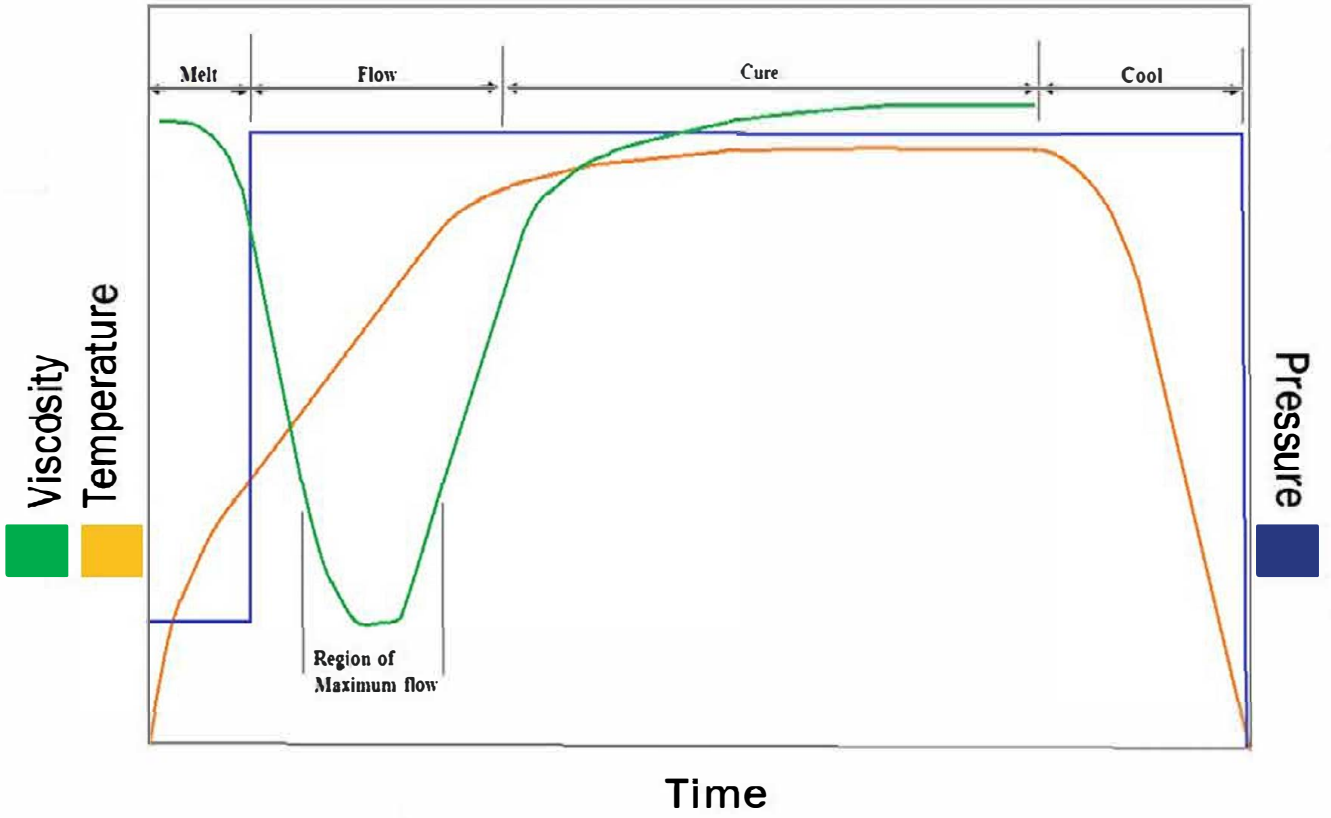
- Misregistration is the maximum amount of variation between the centerlines of all terminal pads within one plated through hole (PTH).
- The impacts of misregistration can be electrical opens caused by breakouts or a short or intermittent connection due to a violation of the minimum clearance.
- The most critical part of PCB assembly is in the lamination process and that is where the role of misregistration is substantial.





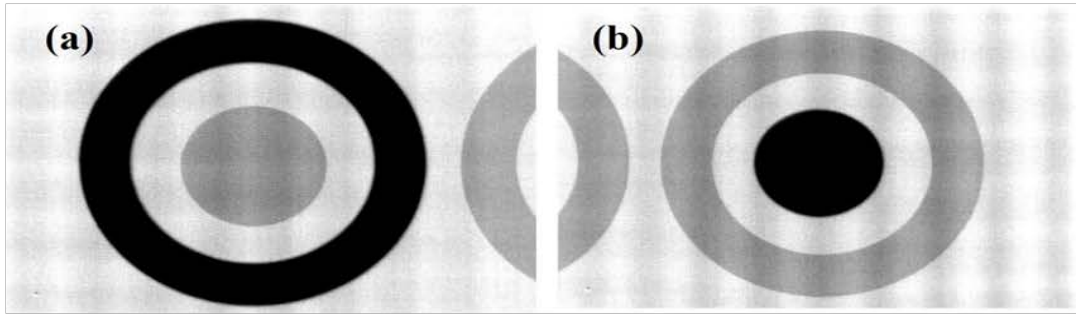
Lamination Process: An Overview

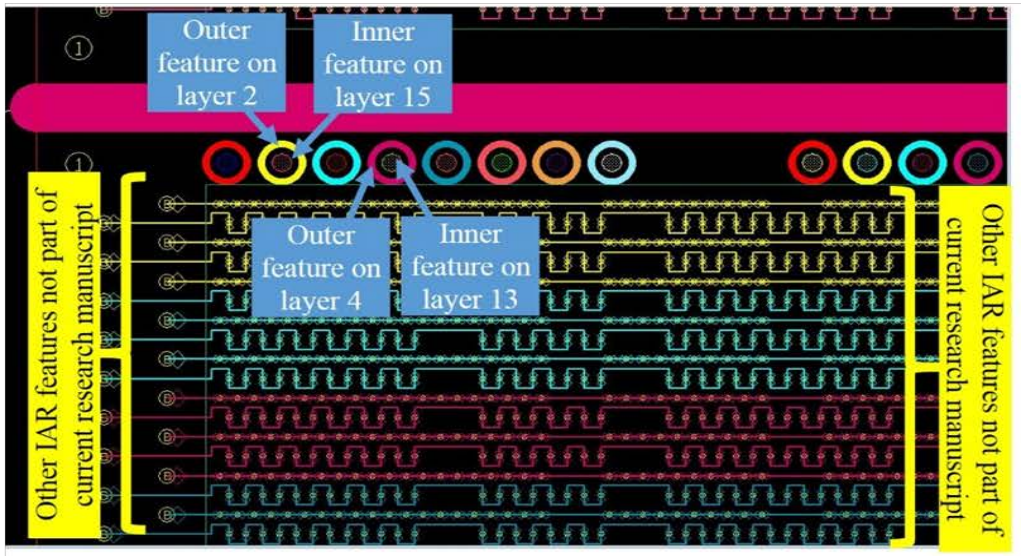
- Main types of lamination processes
  - *A Standard Hydraulic Lamination uses steam press, hot oil press, or electrical resistance heaters.*
  - *The Vacuum-Assisted Hydraulic Lamination (VAHL). Before the lamination process occurs a vacuum cycle of 15 to 60 minutes occurs where moisture, air, and other volatiles are pulled out from the PCB stack.*
  - *Autoclave lamination where the stack is sealed in a vacuum chamber with high pressure heated gas.*
- The type of lamination process is driven by the main structure of the boards (ex. FR4, HDI-FC film, etc)



Test Pattern Design and X-ray Inspection

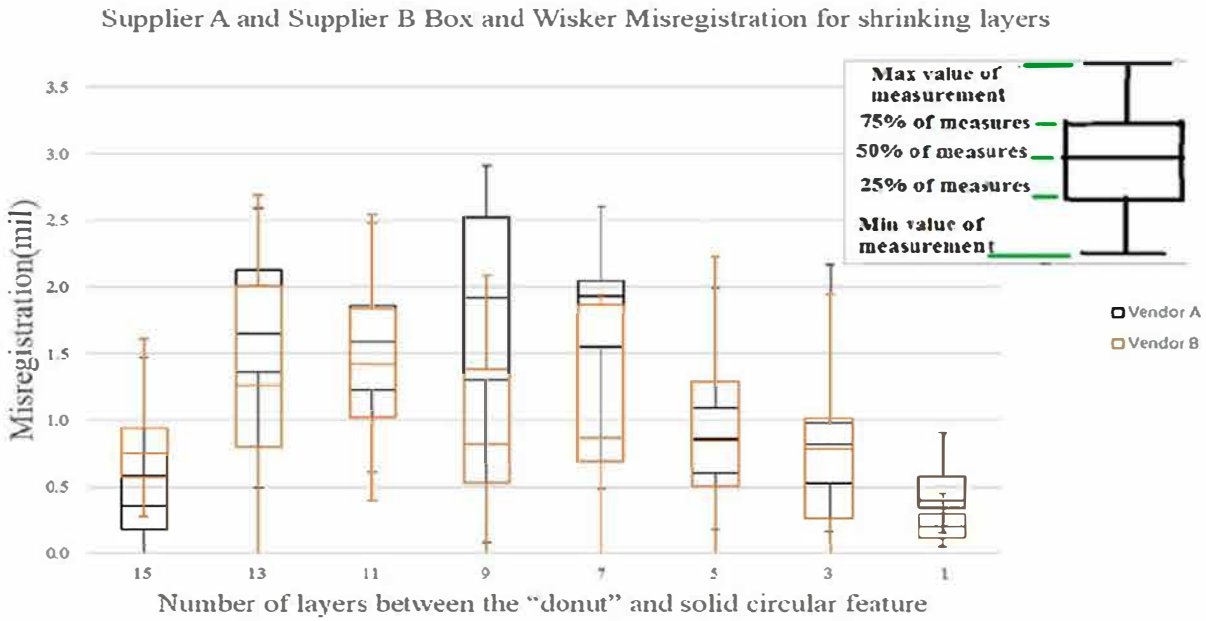
- Test patterns consist of an outer "donut" shaped circular feature and a solid feature which was designed to be oriented at the center of the first feature (different layer).
- Sixteen layered board, thirty sites of interest per board.
- X-ray was used to capture top down images of patterns.
- Measurements of the annular ring separation between layers in the board, were conducted three times.
  - *First: measurements between the outer most layers*
  - *Second: between one layer below the top layer and one layer above the bottom layer.*
  - *Third: between every other layers starting from the top-most layer and concluded at the bottom-most layer.*





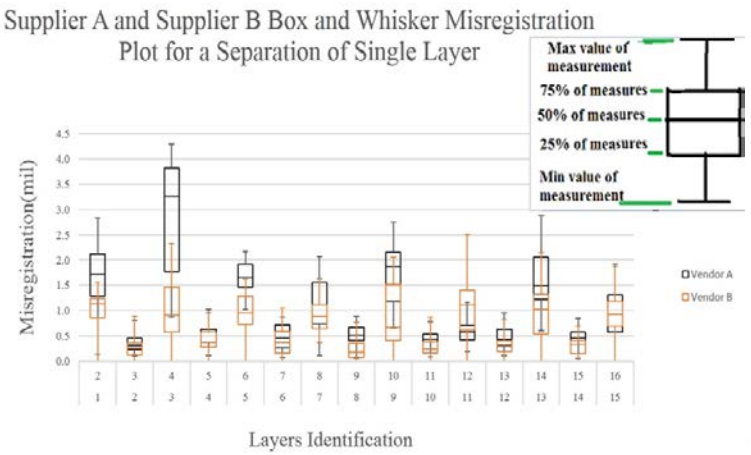
Measurements 1 Box and Whisker plot

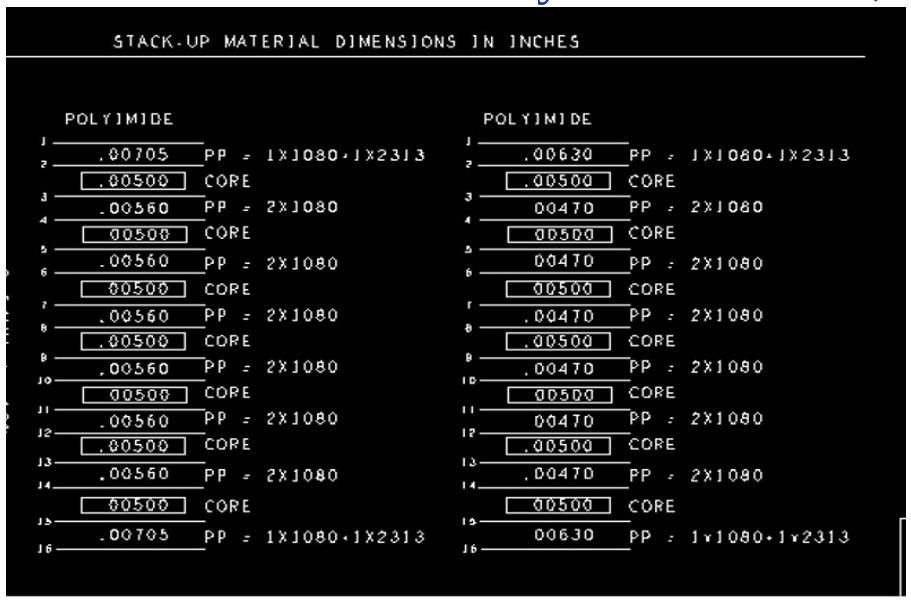
- Image analysis was performed on the X-rays images to get measurements of the misregistration.
- An effort was made to mathematically fit polynomial functions to the observed misregistration.
- Between one and seven followed (1), seven and eleven (2), between eleven and fifteen (3).
  - *1. $y = 0.024x^3 - 0.2546x^2 + 0.8893x - 0.1887$*
  - *2. $y = -0.0431x^2 + 0.7159x - 1.0915$*
  - *3. $y = -0.1723x^2 + 4.2039x - 23.823$*
  - *All the curves had an $R^2 > 0.92$ which signifies that the curves are a very good fit for the data.*



Measurement 2 Box and Whisker plot

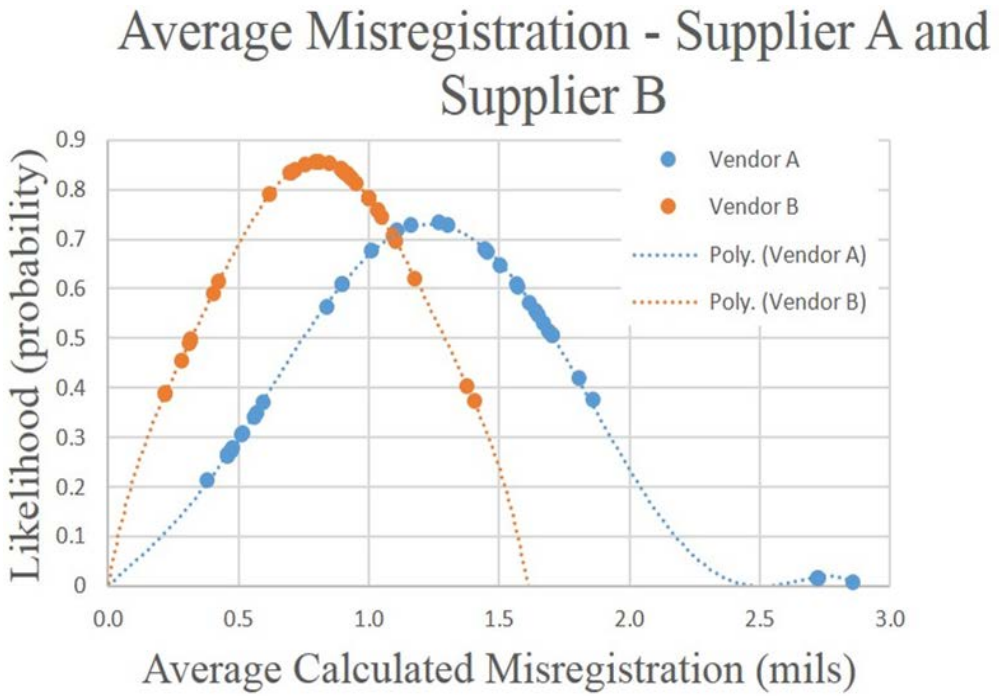
- A sinusoidal oscillating motion is observed.
- The oscillatory behavior root cause is due to the type of prepreg selected and the core material associated with it.
- A combination of the prepreg expansion and the core material constraining its expansion by expanding very little creates a shear stress concentration region between the layers.
- Since the prepreg and core repeat each other as you move further down the layers in the PCB, it means that the entire PCB is subjected to a shear stress.





Normal Distribution Fit

- The calculated misregistration data from both suppliers was fitted to a normal distribution to observe the mean and the variations associated with misregistration.
- For Supplier B, the highest probability (0.85) of average misregistration between the layers will be at 0.75 mils.
- According to the plot, Supplier A's misregistration highest probability is at 1.25 mils.
- Supplier A's PCB manufacturing process has a better tolerance and has a reduced effect of misregistration than Supplier B.

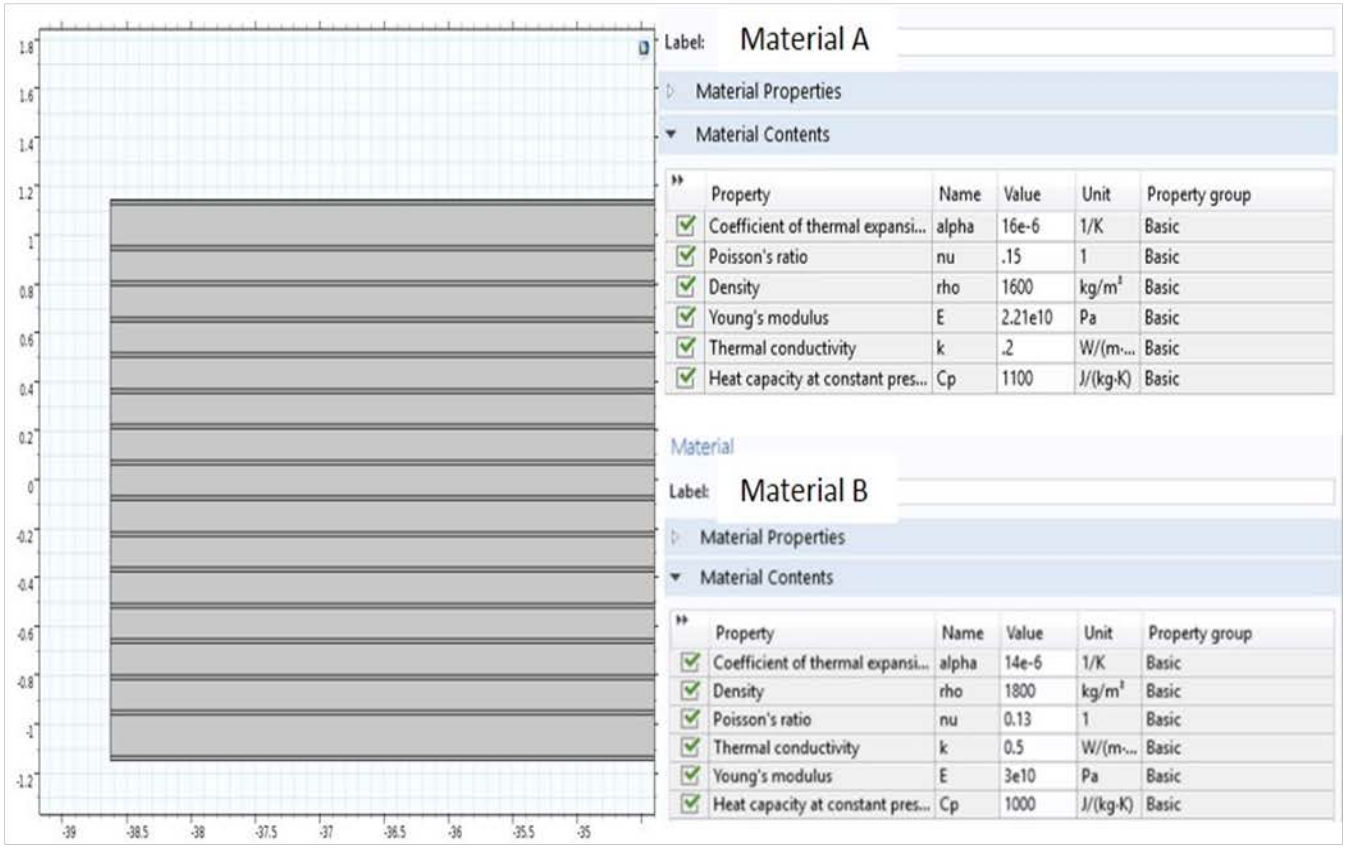


Finite Element Analysis (FEA): Overview

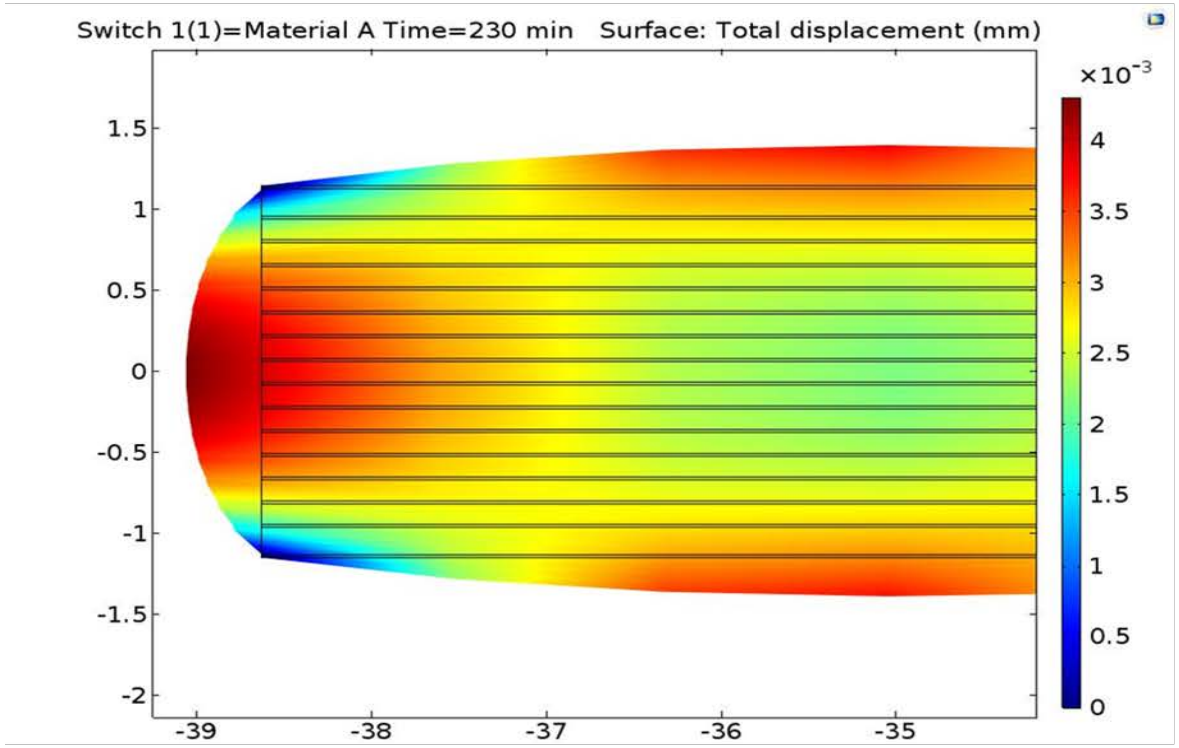
- A 2-D FEA, production simulation software was chosen because of its ability to re-create the conditions the printed circuit board stack experiences during the lamination process and display those results quickly.
- Assumptions of the 2D model was the test boards was relatively simple, additionally, there were no plated through holes or other features on the test boards.
- FEA results shows the change in misregistration between the selections of different prepreg material and lamination process parameters.
- The FEA model also provides an insight into the susceptibility of each prepreg to misregistration and what material property of the prepreg is of utmost importance for understanding misregistration.
- The FEA simulations helped in supplementing a greater understanding of the test results.

Geometry Build & Material Properties (FEA)

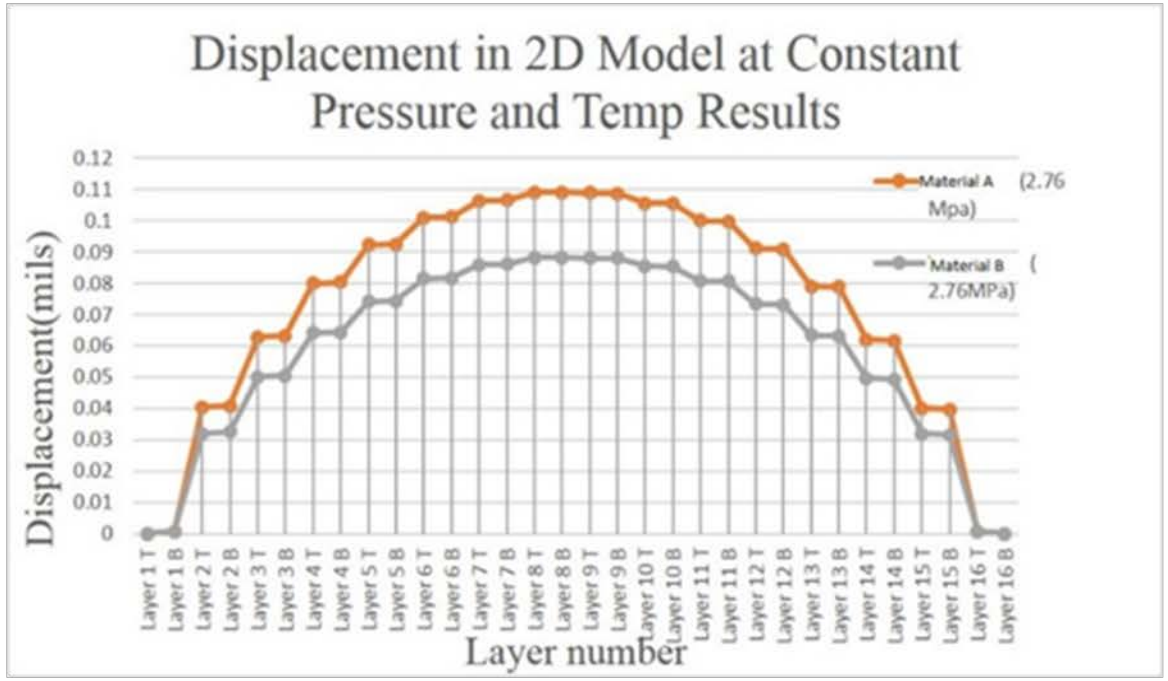
- Since the model is in 2D, length, 77.25 mm, and overall height, 2.293 mm, was taken into account.
- Each layer has a certain thickness and was assigned the material property of a prepreg (Material A or Material B) or copper foil.
- Although Copper foil material properties are not displayed, it can be found from open literature.
- Simulations varying the pressure and the temperature were run.



Lamination Simulation – FEA Results



FEA model output showing calculated displacements.



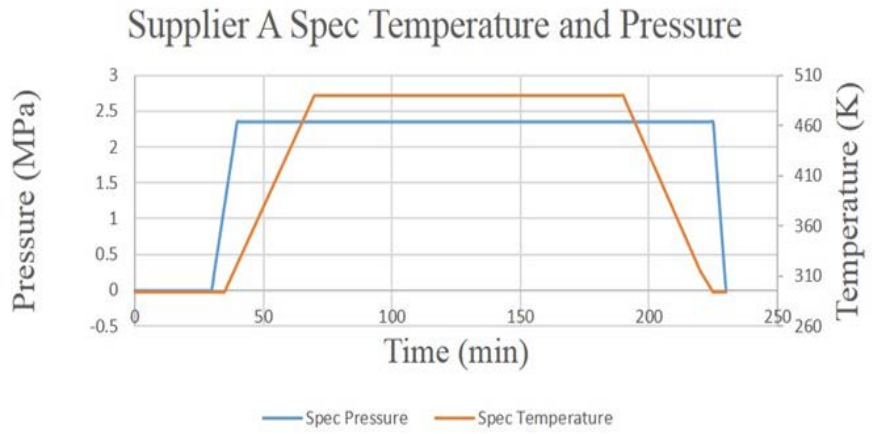
Displacement in 2D at constant pressure and temperature.

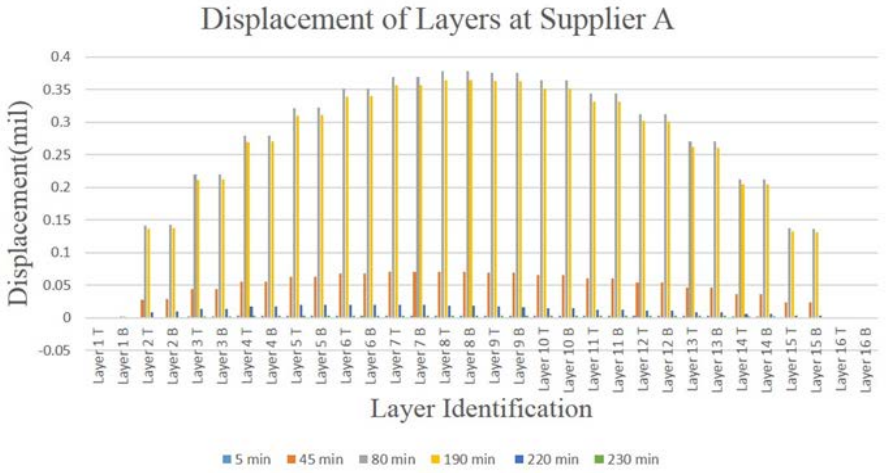
FEA Results and Discussion

- The focus of the results of the model will be only on expansion in the x-plane (because misregistration is primarily an in-plane phenomenon) and not z-plane, although the expansion in the out-of-plane direction is important for PCB reliability and its application environment.
- After numerous simulations, it was found that Young's modulus was the most dominant factor in displacement of the prepreg which in turn induce misregistration.
  - *Larger Young's modulus translates to a lower viscousity of the prepreg which means a lower misregistration.*
- The next step was to run a simulation of the lamination process.

Displacements Using Laminate Suppliers Recommended Profile

- It was assumed that Supplier A, which had used material A, used these guidelines to laminate the PCB.
- Six periods in times were chosen in order to observe the change in displacement.
- The largest displacement was found at the center of the PCB. Maximum displacement occurred between 80 and 190 minutes in running time.
- Results showed displacements at 5 minutes (initial displacement) and at 230 minutes (final displacement) are almost identical. Initially it was assumed that due material hardening(strain hardening) there would be a slight permanent change in shape and the layers would not be able to recover its initial displacements.
- Supplier A did not follow guidelines or else the results would have shown a higher change in displacement which would indicate misregistration and values similar to the experiment runs (0.75 mils).





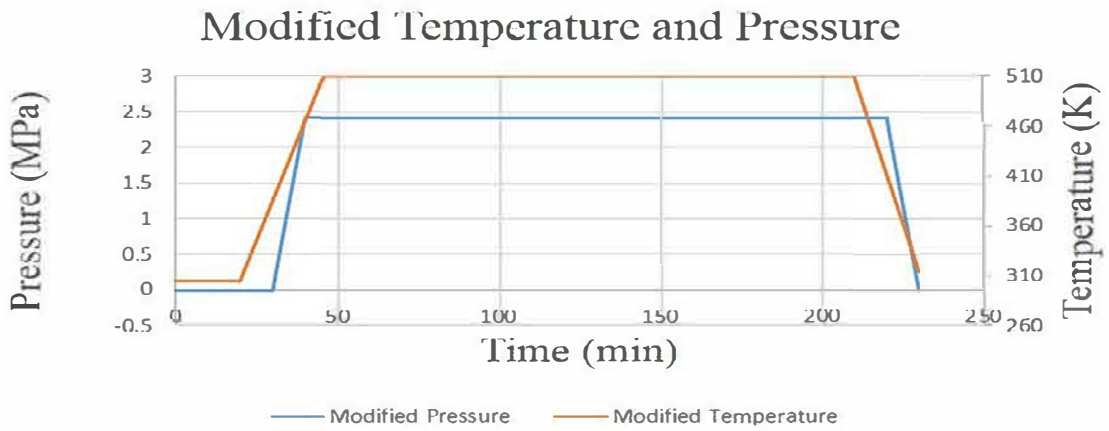
Lamination Parameters

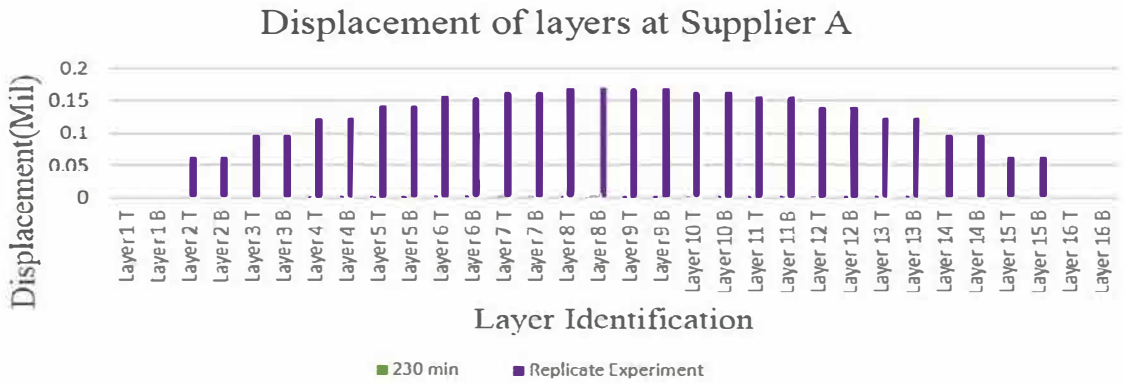
- The next step in the model is to attempt to re-create the experimental results by adjusting the pressure profile and the temperature profile.
- The table displays the pressure and temperature factors that were adjusted to recreate misregistration observed in the x-ray radiographs and calculated misregistration from the x-ray experiments.
- After ten iterations, the profile that came closest to the experimental results was reached.
- This hinted a strong possibility that the supplier could have used these lamination parameters value for their process.

Iterations	1(start)	10(end)
Max Pressure	1 MPa	2.41 MPa
Ramp-up Temp. Rate	3 K/min	8 K/min
Peak Temp.	180 K	510 K
Time Duration Peak Temp.	1.8 hours	2.75 Hour
Ramp down Temp. Rate	-3 K/min	-9.75 K/min
Initial Temp.	294 K	305 K
Final Temp.	295 K	315 K

Displacements using Modified Lamination Profile

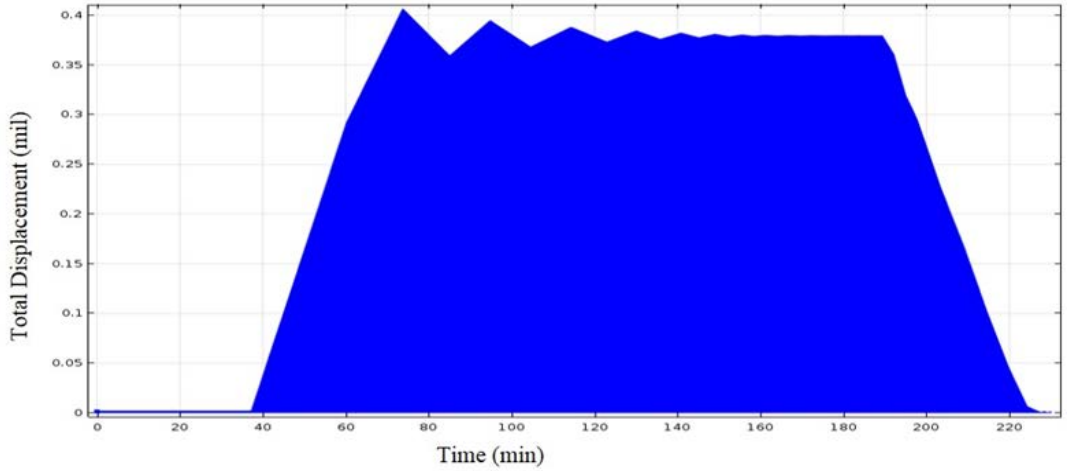
- The most recent iteration profile is shown on the left.
- The difference between Supplier A specs-results and the new results is about 0.15 mils larger at the center of the board.
- Supplier A may have followed a profile very similar to modified figure profile in order to obtain the results observed from the x-ray study.
- Although best case scenario misregistration in the experiment is about 0.75 mils, the FEA results are still 0.6 mils reduced from the experimental results. Additional factors need to be included in FEA study to be more accurate.
- Results show Supplier A may have in practice or through experiences increased the ramp up rate, ramp down rate, and have a longer peak curing time for PCBs in lamination.
- These factors were identified from the model to have the most sensitivity to misregistration.

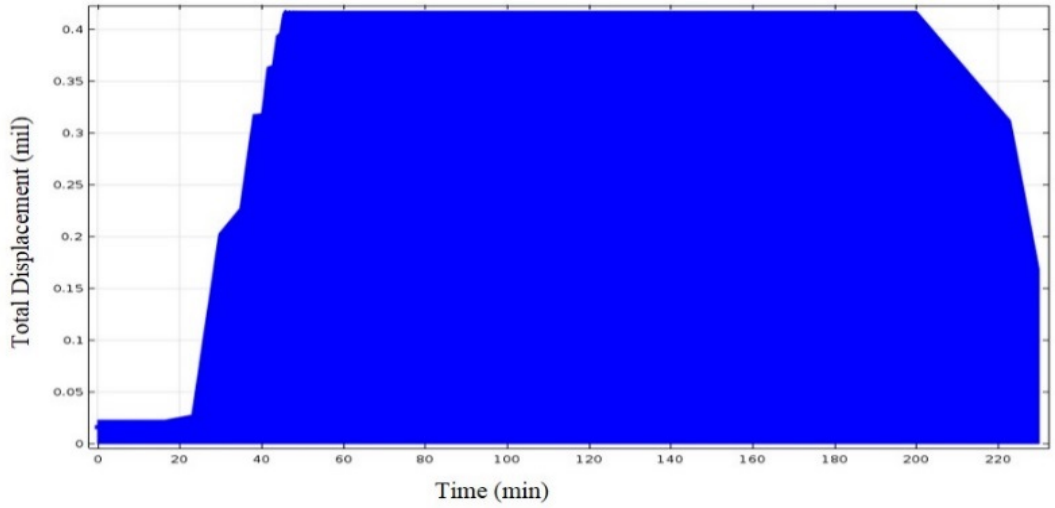




Internal Displacement Comparison

- Of note is that the change of ramp up rate and ramp down rate caused a gradual influence on displacement.
- In the new profile(bottom figure) the maximum displacement is at 0.43 mils and an equilibrium at this point is achieved much faster.
- The final displacement reached at 230 minutes is 0.16 mils
- The assumption that displacement at the beginning of the lamination process and at the end was much different from one another was proven true.





Conclusion

- This study highlights the difference in registration of PCB samples made by the same supplier at two geographical locations.
- The study compared between the samples made at both locations, however, the focus of the comparison was studying whether both populations are subjected to the same statistical results, trying to understand where the difference in population occurred and identified the population which has the lower misregistration between layers.
- FEA simulations helped in providing a greater understanding of the radiography and image analysis results obtained from the tests.
  - *New relationships that previously were not reported in open literature and new factors to take into account that could not be observed by the experimental X-ray inspection or observed in destructive physical analysis (which was not discussed in the paper).*
- However it is necessary to perform additional experiments and FEA models by varying factors such as ramp up, ramp down rate, peak temperature, etc.

Questions?

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