Residue Analysis of Masking Alternatives for Advanced Electronics

Dave Edwards and Callum Poole Henkel Electronic Materials LLC Irvine, CA

Abstract

Prior to any conformal or chemically vapor deposited coating process, specific areas and components -often called "keep out zones"- on the printed circuit board (PCB) assembly are generally masked to shield them from exposure to coating materials. There are several approaches to masking and, traditionally, this has been achieved through the use of tapes (applied manually), UV curable masking materials, latex-based products and, more recently, a dispensable, peelable hotmelt material. Masking materials, however, can leave residues. These residues may have to be cleaned as there could be a risk of corrosion, electrochemical migration and/or parasitic current leakage. This paper will evaluate polyimide tape, UV curable, latex-based, and hotmelt masking materials and compare residue production of each, in addition to testing the products in relation to performance with no-clean solder paste residues. Results of surface insulation testing (SIR) per IPC TM-650 2.6.3.3 along with Fourier Transformed Infrared Spectroscopy (FTIR) analysis of material residues will be presented.

Introduction

In many electronic applications, PCB assemblies require some type of protective method to increase its reliability in deleterious environments. One method is the use of conformal coatings. Conformal coatings are thin layers of insulting material applied to the surface of a PCB to protect sensitive components from thermal shock, humidity, moisture, corrosion, dust, dirt and other damaging elements. Conformal coatings can also provide dielectric resistance to protect against stray electrical currents both internal to the assembly and externally. In some cases conformal coatings are applied to mitigate against tin whisker growth.

In many applications, the entire PCB is not coated due to the existence of areas or components that cannot be coated for various reasons. These are often referred to as 'keep out zones''. Examples include electrical connectors which require a clean surface free of dielectric materials, switches that need to be sealed from masking materials not to flow into them and through holes or solder pads may need to be left uncoated for subsequent soldering or processing.

For these "keep out area" some sort of masking material may be applied. These masks are used to cover and seal components and areas from ingress of conformal coatings. These masking materials can include but are not limited to tapes, peelable liquid masks, boots or shields. These masks can be applied manually or via an automated XYZ dispense system. For the peelable liquid mask they would require some type of curing or other process to solidify them. For tapes and boots/shields, no cure is required.

These temporary masking materials may leave some form of residue behind after removal. It is important to evaluate whether these residues will have any adverse effects on the PCB. These may include but not limited to poor adhesion, cure inhibition, corrosion, electrochemical migration or parasitic current leakage. Compatibility between the masking material and other materials on the PCB should also be evaluated. Flux residues are one of these materials that may be present on the PCB. Compatibility between flux residues and masking materials should be evaluated.

The question arises on how to evaluate any negative effects of masking residues on PCBs. Ion chromatography is one method to determine content of residues. Fourier Transformed Infrared Spectroscopy (FTIR) is another method to analyze for surface residues. Both may identify what residues if any present but may not determine whether they are harmful.

Surface Insulation Resistance (SIR) testing can be done to determine harmful effects any residues may cause during the life/operation of the PCB. This testing involves applying material to a test board with copper traces with controlled spacing between traces and exposing the test board to heat, humidity and electrical bias. The test is performed for a determined time and electrical resistance is measured between the copper traces. The presence of ionic active materials on the test pattern from the coating material would result in reduction of electrical resistance, corrosion and/or dendritic growth. These would reduce the long-term reliability of PCB.

This paper will discuss the evaluation of five common masking materials and investigate via SIR whether their residues may have detrimental effects on a PCB. This SIR testing will be performed on both bare test boards and boards with no-clean lead free solder paste residues. FTIR analysis was performed to determine whether any of the masking materials left residues on ceramic test coupons after removal.

Five common masking materials were selected to be evaluated. One was high temperature polyimide tape. Two were UV curable peelable masks. One was a latex based masking material. The last one was dispensable peelable hotmelt material. These five materials were tested alone and in conjunction with lead-free no-clean solder paste residues. All materials were applied, cured/processed per parameters outlined on their respective technical data sheets. Table 1 list the materials used.

Table 1- Material Description	
Material Label	Description
Таре	High temperature polyimide tape
UV-Blue	UV curable temporary mask from Supplier A
UV-White	UV curable temporary mask from Supplier B
Latex	Latex based temporary mask for Supplier C
Hotmelt	Dispensable peelable hotmelt mask from Supplier C
Solder paste	Lead-free no-clean solder paste from Supplier D

Surface Insulation Resistance was performed used IPC-B-24 Rev. D test boards. Figure 1 shows a representation of the test board.



Figure 1- SIR Test Board

SIR boards were cleaned before use. The cleaning process involved soaking the SIR boards in a solution of 75:25 IPA:DIwater for at least 5 minutes. A soft non-contaminating scouring pad was used to gently clean the comb pattern of any debris. The coupons were then rinsed with 100% IPA and dried in 110C oven for 1 hour.

Ceramic substrates for FTIR analysis were cleaned with 100% IPA and dried at 110C for 1 hour.

One set of SIR was left alone and one set was printed with lead-free no-clean solder paste. Solder paste was reflowed per the manufacturers recommended reflow process.

Masking material was applied to all four test patterns and processed accordingly.

The masking materials were then applied to cleaned ceramic coupons for FTIR analysis of potential residues.

Figures 2, 3 and 4 shows examples of applied masking materials to bare SIR test patterns, reflowed SIR test patterns and ceramic substrates.



Figure 2-Masking Material Applied to Bare SIR boards



Figure 3- Masking Material Applied to Soldered SIR Boards



Figure 4- Masking Material Applied to bare ceramic

In addition to recommended cure/processing parameters, coated boards and coupons were heated for 1 hour at 100C to simulate potential drying/curing process from a conformal coating process. After boards and coupons were cooled to ambient temperature, the masking material was peeled off by hand and boards examined.

Surface Insulation Resistance testing parameters were based on IPC-TM-650 2.6.3.3. Coated test boards were subjected to temperature and humidity of 85C and 85% RH for 168 hours. A voltage bias of 50V was applied during the test period. Testing voltage was -100V. Measurements were taken at 24 hours, 96 hours and 168 hours. Test boards were visually examined after the 168 hours testing.

Ceramic coupons were submitted to an analytical department and Fourier Transformed Infrared Spectroscopy was used to examine for any residues. A blank used ceramic coupon was also analyzed for a base line.

Results

Figure 5 shows the graph of the average resistance values from SIR testing of the five materials on bare test boards. A 'pass' mark would be values of 1.0E+08 or higher. All samples exceeded this value for the duration of the test.







Figure 6 shows a graph of the average resistance values from SIR testing of the five materials on test boards reflowed with the no-clean lead-free solder paste. All values exceeded the pass mark of 1.0E+08 for the duration of the test.

Figure 6-Mask Material and Solder Paste Residue on SIR Board

Figures 7, 8, 9, 10 and 11 show FTIR spectra of the ceramic samples from the five masking materials that were applied and then removed. A spectrum of the bare unprocessed ceramic sample was included as a baseline.

FTIR spectra of all samples could detect little or no residues present after maskants were removed for all five materials.



Figure 7- FTIR Spectrum of Tape







Figure 11-FTIR Spectrum of Hotmelt

Figure 12 shows images of test patterns from four of the SIR test boards after SIR testing that showed staining of the copper traces. The samples from the latex samples showed staining on the test pattern on both the bare boards and solder boards. UV Blue and UV White also showed staining on the bare SIR boards. No staining was evident on the tape or hotmelt samples.



Figure 12- Test Patterns after SIR testing of Latex (upper left), UV Blue (upper right), UV White (lower left) and Latex+Solder (lower right)

Discussion/Conclusions

In this study, we evaluated five common masking materials used in the conformal coating process. We investigated using FTIR analysis whether there were any detectable residues present after removal of the masking materials. We also evaluated via SIR whether any residues may have deleterious effects on PCB functionality. This SIR testing was performed on both bare test boards and boards with no-clean lead free solder paste and associated flux residues to investigate for any interactions between masking material and solder paste flux residues.

Based on the results from SIR testing of the five materials on both bare test boards and boards reflowed with solder, any residues that may be present should have no effect on electrical reliability. No resistance loss, corrosion or dendritic growth

was observed on any of the samples. Three of the materials (latex, UV blue and UV white) showed staining of the bare copper. This staining is limited purely to cosmetic defects and does not appear to affect electrical reliability.

FTIR analysis of ceramic test samples with the five materials applied and then removed resulted in no significant residues found to be present. From this testing, it appears little or no residues are left after the five masking material were removed. This absence of detected residues removes one potential source of coating defects like cure inhibition, poor wetting and adhesion loss.

Further work may be desired to expand on this testing, with some of the following as potential studies. Evaluation on other PCB finishes like OSP, ENIG and immersion Ag and immersion Sn may be done. Also evaluation with other no-clean lead-free solder pastes, as well as studies with tin-lead solder paste may also be performed.

Acknowledgements

The authors would like to acknowledge Cristina Gomez from the company for her assistance in printing and reflowing soldered SIR test boards. In addition, David Jackson and Nanette Tran at the company for the FTIR analysis.



Residual Analysis of Masking Alternatives for Advanced Electronics

Dave Edwards and Callum Poole

Henkel Electronic Materials LLC

Irvine, CA



AGENDA

- Introduction
- Experimental Procedure
- Results
- Conclusion/Discussion



Introduction

- In many electronic applications, PCBAs require some type of protective method to increase reliability.
- One method is conformal coatings.
- Of the conformal coating applications, many require 'keep out' areas in which sections of PCB are masked to prevent coating.
- The questions arises on whether these masking materials and techniques leave any residues that may have deleterious effects on the assembly.
- Fourier Transformed Infrared Spectroscopy (FTIR) is a method to analyze for surface residues. This may determine if a residue is present but can not determine whether residues are harmful. It may also not detect some contaminates.
- Surface Insulation Resistance (SIR) is a method to determine harmful effects any residues may present during operation of PCB.

Introduction

SUCCEED VELTETY

TECHNOLOGY

AT THE

- Four common masking materials were evaluated along with a more recently introduced peelable hotmelt masking material were evaluated.
- SIR was tested on bare IPC-B-24 test boards along with test boards reflowed with no-clean lead free solder paste.
- FTIR was performed on bare ceramic test coupons.



Table 1 shows what materials were evaluated

Material Label	Description
Таре	High temperature polyimide tape
UV-Blue	UV curable temporary mask from Supplier A
UV-White	UV curable temporary mask from Supplier B
Latex	Latex based temporary mask from Supplier C
Hotmelt	Dispensable peelable hotmelt mask from Supplier C
Solder Paste	Lead-free no-clean solder paste from Supplier D



- Figure 1 shows a representation of IPC-B-24 Rev. D test board used for SIR testing.
- Boards cleaned prior to use
 - 75:25 IPA:DI-water
 - Dried 1 hour at 110C
- One set of test boards were left bare and one reflowed with solder paste processed per supplier's recommended parameters.





 Ceramic substrates for FTIR were cleaned with 100% IPA and dried at 110C for 1 hour.

TECHNOLOGY

SUCCEED VELDEITY

AT THE

- Masking materials were applied to SIR test boards and ceramic coupons and processed according to parameter listed on their technical data sheets.
- The next slides shows examples of applied masking materials.





Figure 2-Masking Material Applied to Bare SIR boards





Figure 3- Masking Material Applied to Soldered SIR Boards





Figure 4- Masking Material Applied to bare ceramic.

TECHNOLOGY

SUCCEED VELDEITY

AT THE

- In addition to recommended cure/processing parameters, coated boards and coupons were heated to 100C for 1 hour to simulate potential drying/curing process of conformal coating.
- Surface Insulation Resistance testing parameters were based on IPC-TM-650 2.6.3.3.
 - 85C and 85% RH for 168 hours
 - Bias voltage of 50V. Testing voltage of -100V.
 - Measurements taken at 24 hours, 96 hours and 168 hours
 - Boards were visually inspected after testing.
- Ceramic coupons were submitted for FTIR. A blank unused ceramic coupon was used as reference.

AT THE

SUCCEED VELDEITY

TECHNOLOGY

- The next slide shows graphs of average resistance values of the five materials on both bare test boards and soldered test boards.
- A pass mark of 1.0E+08 or higher was used.
- All samples exceed this pass mark for all five materials throughout the test.





Figure 5- Mask Material on bare SIR board



Figure 6-Mask Material and Solder Paste Residue on SIR Board

AT THE

SUCCEED VELDEITY

TECHNOLOGY

- Examination of the test boards after SIR testing showed staining on four of the test boards.
- Test patterns from Latex sample showed staining on both bare test boards and soldered test boards
- Test patterns from UV-Blue and UV-White showed staining on bare SIR boards.
- The next slide have images of this.
- No other defects were seen.





Figure 12- Test Patterns after SIR testing of Latex (upper left), UV Blue (upper right), UV White (lower left) and Latex+Solder (lower right)



- Examination of FTIR spectra of all samples resulted in little or no residues detected on ceramic coupons after masking material was removed.
- The next slides contain the represented spectra.





Figure 7- FTIR Spectrum of Tape



Figure 8- FTIR Spectrum of UV Blue



Figure 9- FTIR Spectrum of UV White

SUCCEED VELOCITY AT THE OF TECHNOLOGY



Figure 10- FTIR Spectrum of Latex



Figure 11- FTIR Spectrum of Hotmelt

Discussion/ Conclusions

TECHNOLOGY

SUCCEED VELDEITY

AT THE

- All five masking materials resulted in no issues with surface insulation resistance testing at 85C/85%RH under bias.
- FTIR analysis of ceramic coupons coated then removed of the five masking materials showed little or no residue.
- All masking materials left behind no deleterious residues on test boards and coupons as determined by SIR testing.
- Masking material Latex along with UV-Blue and UV-White showed staining of copper traces.
- Further work may be desired to expand on this testing
 - Evaluation on other PCB finishes like OSP, ENIG, immersion Ag and immersion Sn may done along with other lead-free and tin-lead solder pastes.



QUESTIONS?