Novel Approach to Void Reduction Using Microflux Coated Solder Preforms for QFN/BTC Packages that Generate Heat

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Abstract

The requirement to reconsider traditional soldering methods is becoming more relevant as the demand for bottom terminated components (QFN/BTC) increases. Thermal pads under said components are designed to enhance the thermal and electrical performance of the component and ultimately allow the component to run more efficiently. Additionally, low voiding is important in decreasing the current path of the circuit to maximize high speed and RF performances. The demand to develop smaller, more reliable, packages has seen voiding requirements decrease below 15 percent and in some instances, below 10 percent.

Earlier work has demonstrated the use of micro-fluxed solder preforms as a mechanism to reduce voiding. The current work builds upon these results to focus on developing an engineered approach to void reduction in leadless components (QFN) through increasing understanding of how processing parameters and a use of custom designed micro-fluxed preforms interact. Leveraging the use of a micro-fluxed solder preform in conjunction with low voiding solder paste, stencil design, and application knowhow are critical factors in determining voiding in QFN packages. The study presented seeks to understand the vectors that can contribute to voiding such as PCB pad finish, reflow profile, reflow atmosphere, via configuration, and ultimately solder design.

A collaboration between three companies consisting of solder materials supplier, a power semiconductor supplier, and an electronic assembly manufacturer worked together for an in-depth study into the effectiveness of solder preforms at reducing voiding under some of the most prevalent bottom terminated components packages. The effects of factors such as thermal pad size, finish on PCB, preform types, stencil design, reflow profile and atmosphere, have been evaluated using lead-free SAC305 low voiding solder paste and micro-fluxed preforms. Design and manufacturing rules developed from this work will be discussed.

Key words: bottom termination components; preforms in paste; voiding; tape and reel preforms; flux coated preforms.

Introduction

Bottom terminated component packages, such as QFN, are becoming increasingly relevant due to their ability to carry high power dies in a small form factor. With increasing reliability performance requirements, power management components in packages like QFNs are critical to optimizing thermal and electrical performance. Additionally, low voiding is important for decreasing the current path of the circuit to maximize high speed and RF performances (1). The market demand for void reduction under thermal pads of QFN components due to shrinking package sizes and increasing power requirements has generated the need to evaluate key process factors that contribute to voiding to design an optimal solution.

The addition of a micro-fluxed preform in conjunction with a low voiding solder paste and process knowhow is seen to create ideal solder volume with minimal voiding. As IPC 7093 specification acknowledges, one of the key concerns with bottom termination components (BTC) such as QFNs is achieving the solder volume required for a high reliability solder joint (2). A multitude of processing factors such as reflow profile, reflow atmosphere, pad finish, and stencil design have been assessed in this study to develop a solution for achieving a high reliability solder joint with low voiding for QFN packages.

Experimental Procedure

A full factorial DOE was designed based on key factors contributing to voiding under bottom termination components. The use of a solder preform was investigated compared to a solder paste only benchmark sample. The key factors in this DOE were identified and selected by subject matter experts from a leader in semiconductor manufacturing, an OEM of specialized test and measurement equipment for radio communications, and a solder manufacturer.

A custom single layer 1.6mm thick PCB test vehicle was designed specifically for this investigation that encompassed numerous variables that can contribute to voiding in bottom termination components.

A single layer PCB design (**Figure 1**) was chosen so that other factors (i.e. multilayer board and ground planes) would not influence the key factors being addressed in this study. QFN components of various sizes and pin configurations were among the variables addressed and further defined. In this particular study only QFN components was selected (details in **Table 1**).



Figure 1. Image of the PCB test vehicle (TV) and some of the components used in this DOE.

Туре	Pin	ID	# of Comp. per TV	Exposed Ground Pad (LxW, mm)
QFN	32	QFN 32	18	3.6x3.6
QFN	20	LCS 20	18	2.1x2.1
QFN	48	LCS 48	18	5.4x5.4

Table 1. Components Detail	Table 1.	Components Details
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There were 2 types of test boards generated: one with an Immersion tin (ImmSn) plating which is widely used in automotive application and another with an Immersion silver (ImmAg) plating which is used in high reliability and high power application.

The test board also addressed via design including through hole via, no via, and plugged via configurations under the QFN and LCS components. The through hole via had a 0.3mm diameter with and 0.5mm diameter resist on top and bottom. The plugged via maintained the same 0.3mm diameter hole and depth of 0.4mm with 0.7mm diameter resist on top and bottom. Vias were configured in a pattern as indicated in **Figure 2**.

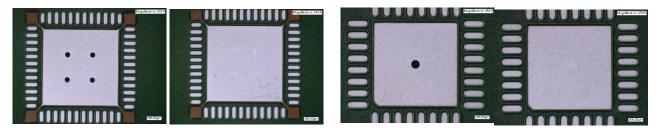
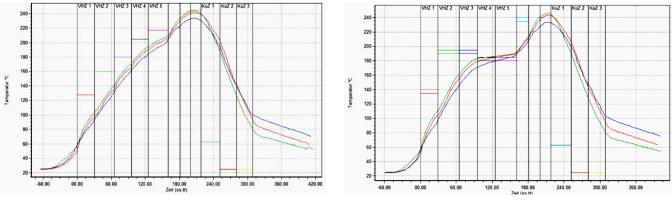


Figure 2. Via design and configuration on the test vehicle (TV)

The investigation also addressed reflow profile and reflow atmosphere. A low voiding SAC305, type 4 solder paste was used for this study with solidus temperature of 217°C and liquidus temperature 220°C. Thermocouples were strategically placed on the QFN32, and QFN64 component locations on the test vehicle. Proven straight ramp and high soak reflow profiles were evaluated as shown in **Figure 3**.



Straight Ramp Reflow Profile.

High Soak Reflow Profile

Figure 3. Reflow profiles using in this study

The straight ramp profile increased at a rate of 1° C/s until reaching liquidus temperature of 220° C. The test vehicle was subjected to 65 seconds above liquidus (TAL) with peak temperature on the test vehicle reaching 240° C. The high soak reflow profile increased temperature at a rate of 1° C/s up to 150° C before slowing to a rate of 0.5° C/s up to 200° C to allow more time for the flux to activate the surfaces.

The high soak profile subjected the test vehicle to 50 seconds above liquidus (220°C) with a peak temperature of 240°C on the test vehicle. Finally, both Air and nitrogen reflow atmospheres were evaluated in this investigation to further understand the effect of voiding under bottom termination components.

The focus of the investigation involved the use of the micro-flux coated solder preform to increase solder volume relative to fluxing agent and reduce voiding. The use of a SAC305 micro-flux coated solder preform in conjunction with paste was benchmarked against a solder paste only test vehicle for each of the configurations summarized in **Table 2.** Four replicate boards of each iteration were processed in order to ensure statistically viable data.

ID	PCB finish	Reflow Profile	Atmosphere
1	ImmSn	High Soak	Air
2		High Soak	Nitrogen
3	-	St. Ramp	Air
4		St. Ramp	Nitrogen
5	ImmAg	High Soak	Air
6]	High Soak	Nitrogen
7]	St. Ramp	Air
8		St. Ramp	Nitrogen

 Table 2. Assemblies configuration details.

Close to 2,000 data points were generated combining 54 components on each test vehicle and four replicates of each configuration. The solder paste only benchmark samples were printed in a window pane configuration commonly used in the industry for void reduction and shown in **Figure 4**.

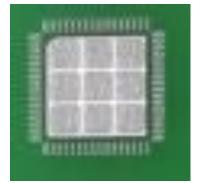


Figure 4. Solder Paste Print Configuration (Examples of window pane solder prints on QFN components used in benchmark samples)

The design of a solder preforms to allow intimate contact with the thermal pad of the component and increase solder volume played a significant role in the results presented in this investigation. **Figure 5** represents an example of the use of solder paste only in window pane format on a QFN where mechanical stack-up issues on the component and reflow characteristics of solder paste make it difficult to achieve good voiding.

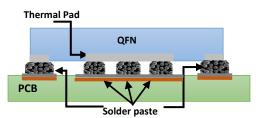


Figure 5. Solder Paste Print design for QFN.

Trials were conducted using a fully automated in-line system. Use of such a world-class facility helped to maintain control and ensure consistent process repeatability among test vehicles. A production printer was used to print 5 mil thick paste layouts on both the solder paste only and solder paste and preform configurations under investigation. Paste was printed at a 65° squeegee angle at a rate of 30mm/s and 80N pressure using a 5mil stencil. Components and solder preforms were placed from tape and reel using a production component placement machine with Twin-head and 2N force. Samples were then inspected for skew prior to reflow in a production belt driven reflow oven per the reflow profiles defined in **Figure 3**. Finally, upon reflow, every component was subjected to X-ray voiding analysis capturing its largest single void size and total void percent under the thermal pad.

Results and Discussion

Voiding analysis was performed on all test assemblies. Statistical software was used to compare voiding performance and processing factors to generate a main effect plot to understand QFN voiding. The plot of the main effects on the voiding of the built assemblies are shown in **Figure 6**. Reviewing data, it was observed that no significant difference was observed between the two surface finishes (ImmSn and ImmAg) evaluated in this study. A very small effect of the reflow profile type was observed when all data was analyzed. As expected, the lower voiding percentage was achieved with a high soak reflow profile compare to the straight ramp. Typically, higher soak profile allows more outgassing of volatiles during reflow, which could result in lower voiding. Reflow in nitrogen atmosphere resulted in lower voiding. Higher voiding levels were observed on the larger QFN component with thermal pad 5.4x5.4mm. The results for the small and medium sized LCS and QFN packages were similar even though components' thermal pads were very different (3.6x3.6 mm and 2.1x2.1mm). Assemblies without vias and with through hole vias produced the least amount of voiding overall; whereas, plugged vias showed higher voiding level. The biggest effect contributing to the reduction in voiding was the use of the solder paste and preform (PF+Paste) configuration versus Solder Paste Only (SPO) configuration.

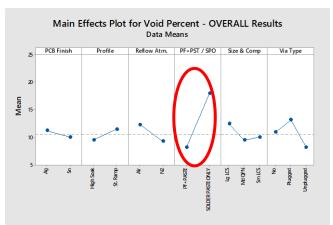


Figure 6. The Main Effects % Void – Overall plot

The solder paste only configuration was used as a benchmarking factor for the remainder of the analysis. The average voiding for the contributing factors for Solder Paste Only (SPO) configuration shown in **Figure 7.** The resultant voiding was approximately in 22% average range.

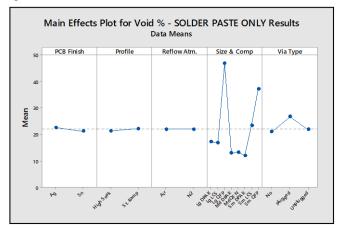


Figure 7. The Main Effects for SOLDER PASTE ONLY (SPO) configuration

ImmSn board finish and the high soak profile marginally drove to lesser voiding. Reflow atmosphere had very little impact on the voiding results overall. Unplugged vias were the most problematic of the three vias design in this study.

Focusing on the results for PREFORM AND PASTE (PF+Paste) configuration only, an average voiding of 9% was measured. The overall average voiding for PF+Paste configuration was more than two times lower relative to the SPO configuration. **Figure 8** shows the main effect of various parameters on the voiding of the PF+Paste configuration. Unlike the SPO configuration, the primary contributor to voiding in the PF+Paste configuration was the reflow atmosphere. Reflow in nitrogen reduces voiding nearly to 5%. Clear correlation with component size and voiding performance was observed. Voiding levels of about 12% were observed on the larger QFN component with thermal pad 5.4x5.4mm. Reduction in the size of the thermal pad down to 3.6x3.6mm reduced voiding level down to around 9%. As expected, the smallest package with the thermal pad of 2.1x2.1mm showed the lowest voiding level and it was about 5%. Similar to SPO configuration, assemblies with unplugged vias were the most problematic and produced higher voiding levels compared to other pad design.

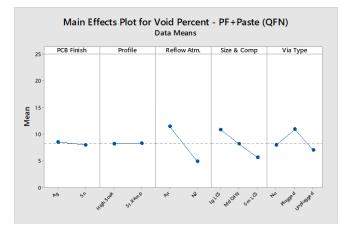


Figure 8. The Main Effects for PREFORM AND PASTE (PF+Paste) configuration

Earlier conducted studies were undertaken to understand the effects of micro-flux coated solder preforms and voiding for Bottom Termination Components (BTC). In the last several years a lot of advancement was achieved in flux chemistry development to improve voiding performance significantly. In the previous voiding studies (3,4) it was identified that the higher preform-to-paste volume ratio on the pad contributed to lower voiding, specifically in nitrogen. It is evident that the increased solder volume from the preforms plays a critical role in void reduction.

Voiding of QFN Packages (Small, Medium and Large Pads) Results

A QFN is a bottom termination component in which both thermal pad and signal leads terminate under the body of the component. **Figure 9** summarizes the results of the voiding of those components based on the combination of PF+Paste and Solder Paste Only configuration as well as types of vias on the board. The PF+Paste configuration with no vias or unplugged vias provide excellent voiding results below 5%. Plugged vias had slightly higher voiding but remained lower than Solder Paste Only configuration. The PF+Paste configuration reflowed in nitrogen environment produced the most impressive voiding results, averaging between 5%-10% under all 3 package sizes.

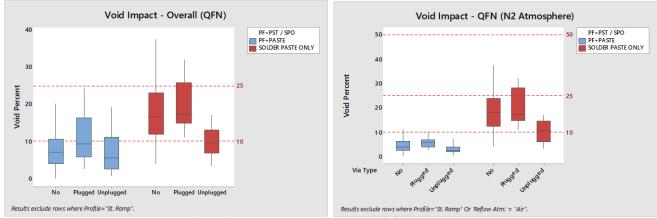
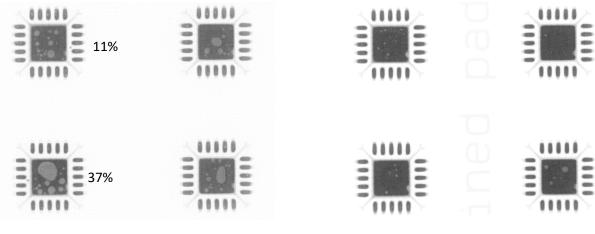


Figure 9. The overall void results of QFN packages

It was observed during X-Ray analysis that assemblies built with PF+Paste configuration had a greater consistency in voiding and pad coverage from one component to another. Void distribution was much tighter for the PF+Paste configurations compared to SOLDER PASTE ONLY (SPO) configuration. Those differences could be clearly observed in **Figure 10**.



SOLDER PASTE ONLY

PREFORM AND PASTE.

Figure 10. X-Ray images of the QFN components assemblies built with different solder material configurations.

In the solder paste only example, a wider distribution of voids was present in which voiding between 11% and 37% was present on the same board for like components in similar board locations. As evident in **Figure 10**, a greater consistency void percent was achieved for the same situation when a micro-flux preform was used. This consistency will result in a reduction in defect rate and would eliminate the need for assembly rework.

Another focus of the analysis was evaluating the influence of the via design on to the void percentage. The complexity and functionality of the boards' vias in a PCB are important components. In this study two types of vias were evaluated: (1) through hole vias and (2) plugged vias. All vias were 0.3mm diameter. Plugged vias were 0.3mm diameter through hole vias with 0.5mm diameter resist on top and bottom. **Figure 11** shows the optical profile of the plugged via. It appears that resist had some curvature (depression) which could contribute to increased voiding due to air entrapment.

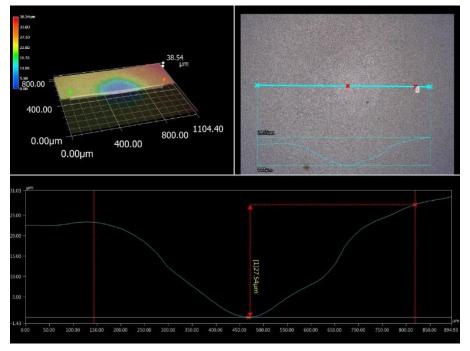


Figure 11. Optical image and profile of the surface of the plugged via.

Solder material selection is an important factor when setting up a process for QFN or any other BTC. Voiding is a problem for bottom termination components, especially for QFN packages that have a thermal pad to conduct heat away from the integrated circuit (IC). Excess voiding will increase the thermal resistance of the thermal interface. It is common practice to design pad and vias to increase propensity for volatiles to escape during reflow process in order to minimize voiding under the Bottom Termination Component. X-Ray images of the assemblies built with SOLDER PASTE ONLY and PF+Paste Configurations are shown in **Figure 12.** Again the same consistency between voiding of the assemblies was observed when PF+Paste was examined. For plugged vias, voiding was observed around vias. As it was stated earlier, curvature in the solder resist might be contributing factor in higher voiding in the via area. Much lower and smaller voids were observed with PF+Paste configuration.

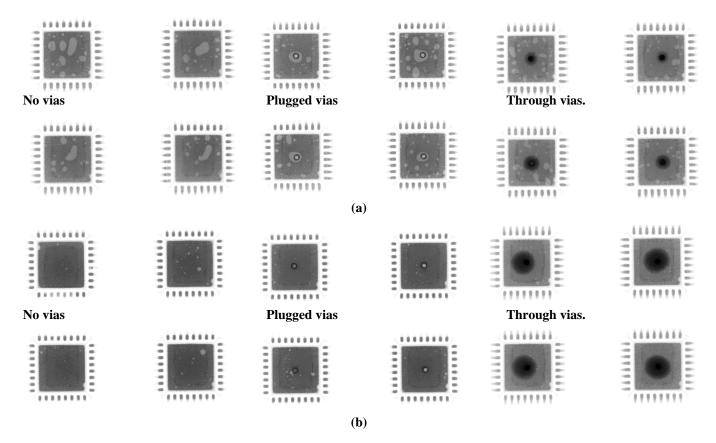


Figure 12. X-Ray images of different via design the medium QFN components assemblies built with (a) SOLDER PASTE ONLY and (b) PREFORM AND PASTE with different via design.

In all cases when through hole or unplugged vias were assessed, solder overfills the hole leading to the bumps on the bottom of the board (**Figure 13**). This uncontrolled solder wicking could result in insufficient thermal connection between PCB and heat sink. Reduced via diameter could limit the amount of solder wicking. With smaller vias, the surface tension of the liquid solder inside the via could oppose gravity and minimize solder wicking. However, the reduction in via diameter will result in higher overall thermal resistance, which could be one of the downsides of this approach.

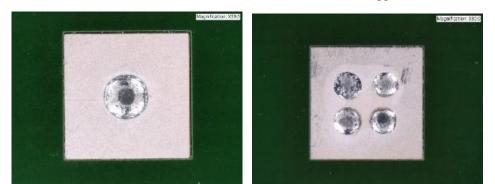
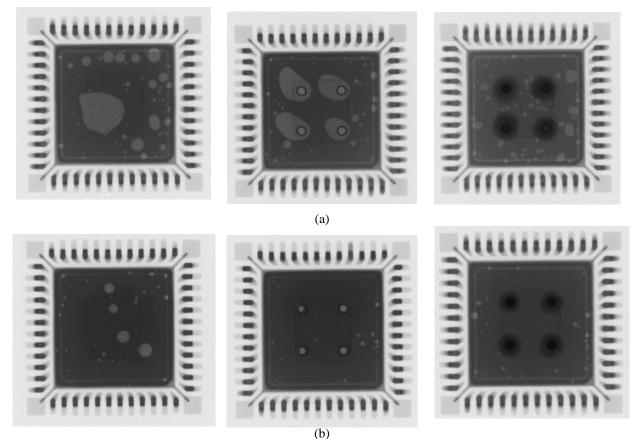


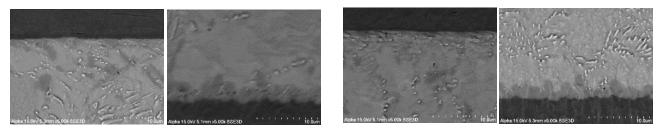
Figure 13. Optical images of the back side of the PCB. Pads with through vias.

In the case of the 5.4x5.4mm thermal pad, 48 pin component, board was designed with four vias per pad. Results similar to the single via design was observed (**Figure 14**). The vast majority of the voids on filled via pads were on the top of the vias. Void percent in the pads with unfilled vias were lower but based on the X-Ray and optical analysis, solder wicking to the bottom of the board was observed in all cases. Joints with filled vias demonstrated larger and more frequent voids.



No viasPlugged viasThrough vias.Figure 14. X-Ray images of different via design the larger QFN components assemblies built with (a) SOLDER
PASTE ONLY and (b) PREFORM AND PASTE with different via design.

Some of the assemblies were metallographically prepared for microstructural evaluation. Interfacial reaction between the component thermal pad and solder as well as solder and board pad was examined. Uniform and continuous IMC (Inter Metallic Compound) layer was formed at all interfaces, Acceptable solder joints were built using both configurations (SPO and PF+Paste). SEM images of the cross sectioned assemblies are shown in **Figure 15**.



(a) (b) Figure 15. SEM images of the interfacial reaction of the assemblies built using (a) SOLDER PASTE ONLY and (b) PF+Paste configuration.

Summary and Conclusions

The previous work and the work presented in this study, demonstrates the advancement of QFN and other Bottom Termination Component (BTC) assembly through the use of low voiding micro-flux solder preform and optimized process parameters such as stencil design, pad design and reflow parameters.

Design of the preform, selecting specific flux amount, and optimizing soldering conditions resulted in significant reduction in voiding. For various component sizes, consistent sub-10% voiding was achieved. The use of preforms in conjunction with micro-flux coating technology ensures low voiding in both air and nitrogen reflow environments. Reduction in solder paste volume and controlled amount of the flux on the micro-flux preform generates low residue and ensures high electrochemical reliability of the BTC. Low voiding micro-flux technology is compatible with finishes such as immersion Sn and immersion Ag commonly used in industry. Via design is an important factor in BTC assembly. Via type and diameter could be a critical factor to achieve low voiding and reliable solder assembly.

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References

(1) IPC- Association Connecting Electronics Industries. "IPC-7093 – Design and Assembly process implementation for Bottom Termination Components." 2011.

(2) Reza Ghaffarian / Nasa. "Body of Knowledge (BOK) for Leadless Quad Flat No-Lead/Bottom Termination Components (QFN/BTC) Package Trends and Reliability." Jet Propulsion Lab - California Institute of Technology (10/2014): 14-15. Print.
(3) Tormey/Sidone/Bent/Tellefsen/Koep/Raut, 2012. "The Effects of Preforms in Paste on Voiding Under Bottom Terminate Components", SMTAI, Orlando, FL, Oct. 16-17, 2012.

(4) Lifton/Salerno/Sidone/Khaselev/Marczi, 2017 "Void Reduction strategy for bottom termination components (BTC) using flux coated preforms", SMTAI, Chicago, IL Sept.19-21, 2017.

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NOVEL APPROACH TO VOID REDUCTION USING MICROFLUX COATED SOLDER PREFORMS FOR QFN/BTC PACKAGES THAT GENERATE HEAT

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Outline/Agenda

Introduction

- Experimental Procedure
- Results and Discussion
- Conclusions
- ■Q & A



Introduction

Markets increasing demand for higher power density components require low voiding solder joints.

Concerns with bottom termination components (BTC) to achieve the solder joint quality required for a high reliability solder joint.

The aim of the project was to develop technology for managing low voiding under BTC.

BTC Definition and Considerations:

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- IPC T-50 BTC definition: SMT electronic components whose external connection consists of metalized termination that are a part of the component body.
- Large variation in component design results in large variation in stencil and manufacturing strategy.

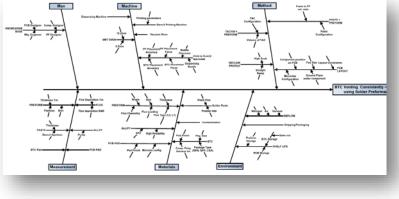
- Discrepancies and inconsistencies exist in standardized packages.
- Devices are more sensitive to warpage of the PCB or component.
- Not achieving the correct standoff height could be reliability issue.

Low Voiding Technology Development :

- Voiding is complex issue with many factors contributing to excessive voiding
- Low Voiding Technology uses a combination of processing considerations, solder paste, uniquely designed microfluxed preforms and stencil design.
- The power semiconductor supplier and an electronic assembly manufacturer partnered on this development.
- DOE generating over 4000 data points

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Experimental Procedure:

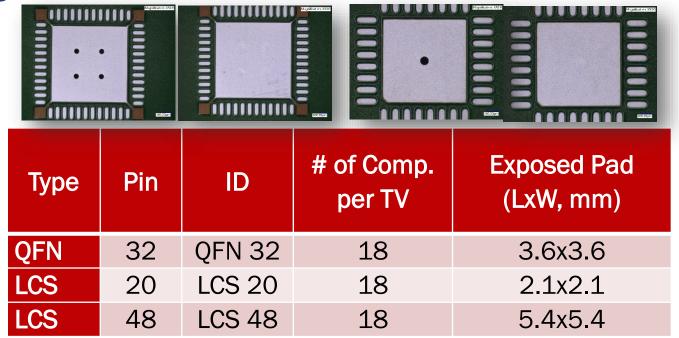
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- Components:
- QFN packages.

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- Large, Medium and Small packages sizes.
- PCB Configuration:
- Ag and Sn finishes
- Via configurations
- Solder Configuration:
- Benchmark: Solder paste
- Microfluxed Preform + Paste



Electroless Silver

FN32P505-3.

Experimental Procedure:

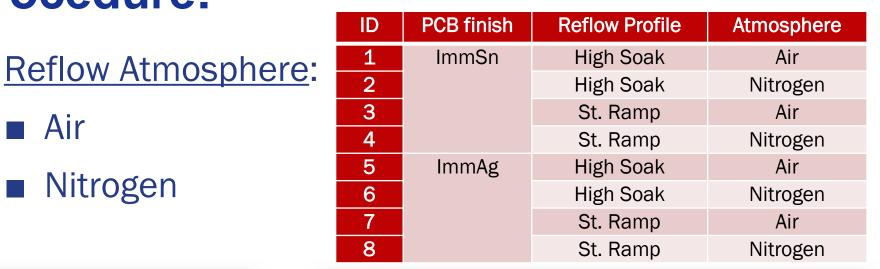
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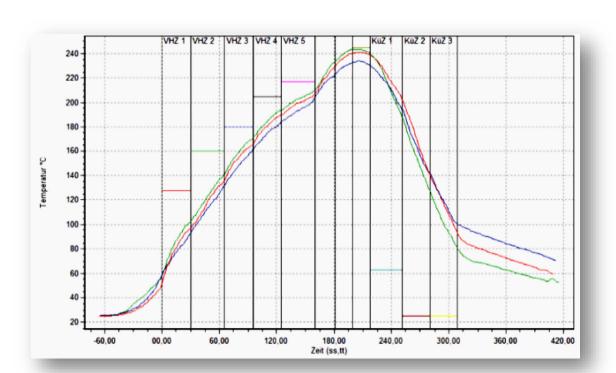
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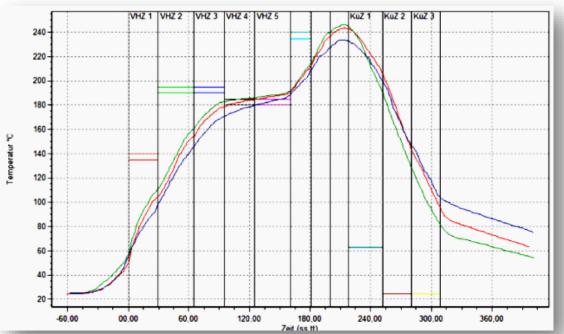
- **Reflow Profiles:**
- Straight Ramp
- High Soak



Air





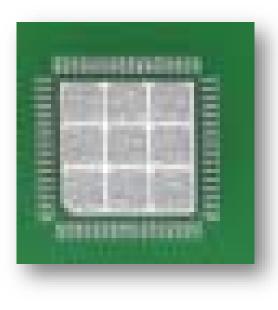


 A proven low voiding solder paste solution was used for benchmarking.

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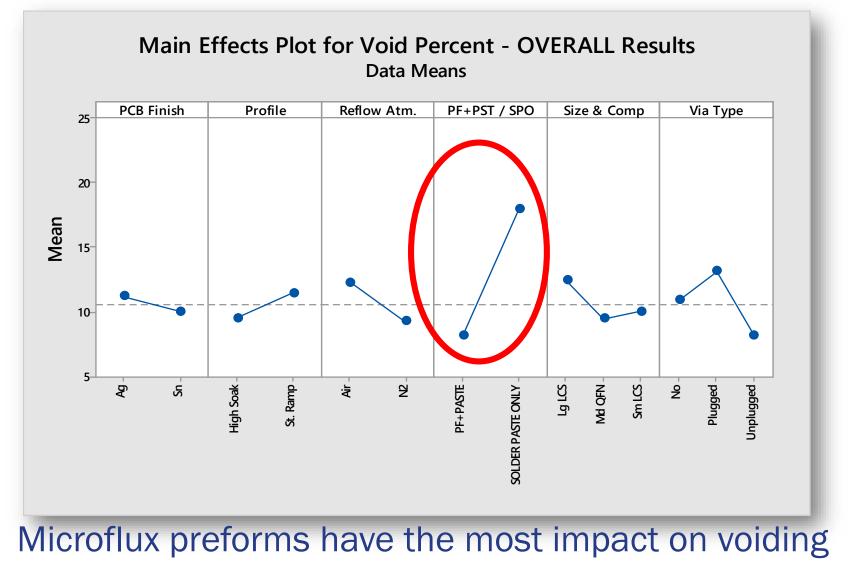
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 Average voiding overall is 20%-23%



BENCHMARK (Solder Paste Only) Void Amount (%) 40 30 20 10 0 Highsoat High Soat St. Ramp High Soat St. Ramp St Ramp High Soat Ramp **Reflow Profile** PCB Finish 5 20) 20) 5 **Reflow Atmosphere** pit 22



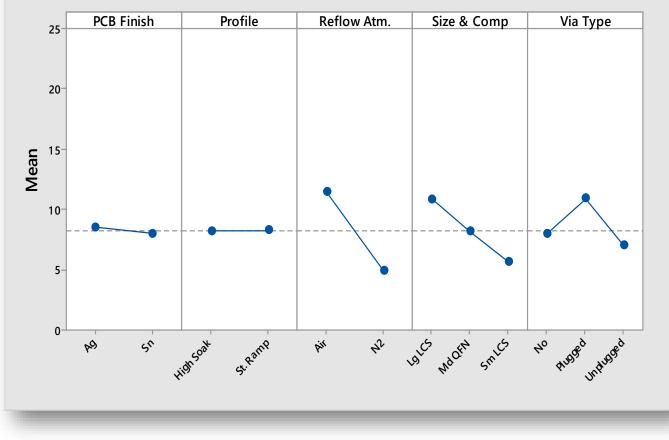


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- Surface finish and reflow profile did not play significant role in affecting voiding for QFN components.
- Reflow atmosphere and component size had significant effect on resulted voiding
- Via type affected voiding
- The average voiding for Microfluxed Preform+ Paste Assemblies was <15%</p>

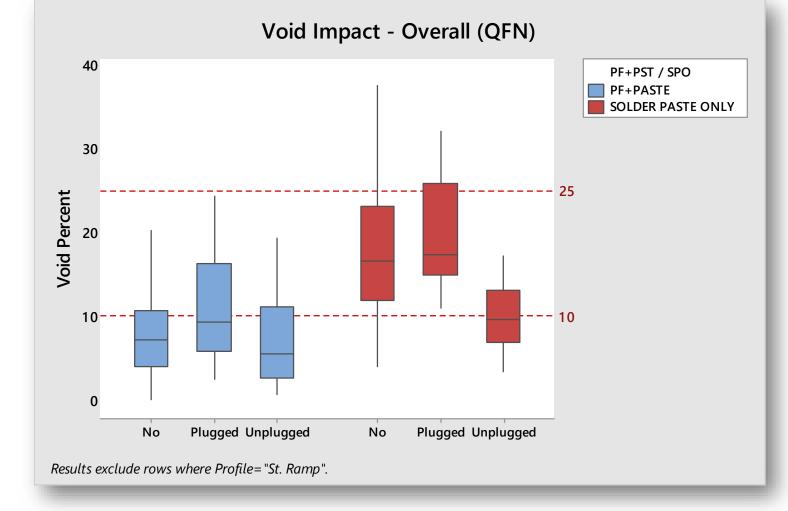
Main Effects Plot for Void Percent - PF+Paste (QFN) Data Means



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The average voiding for Microfluxed Preform+ Paste Assemblies was almost half of the voiding for SPO (except for unplugged vias).

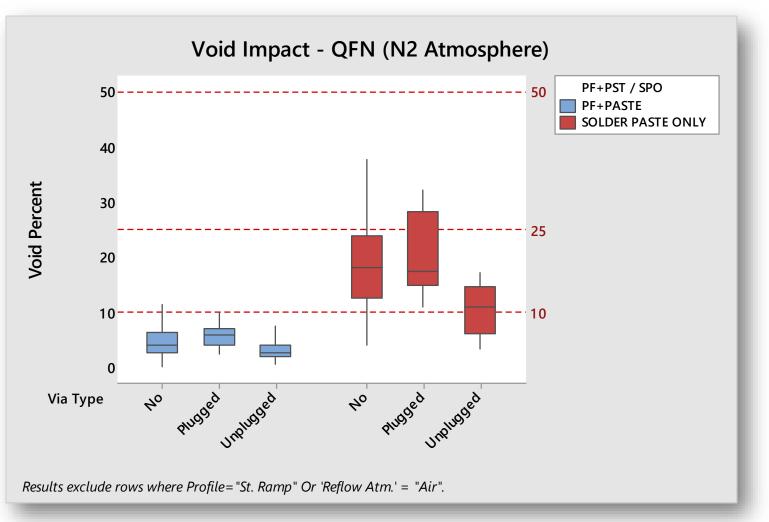


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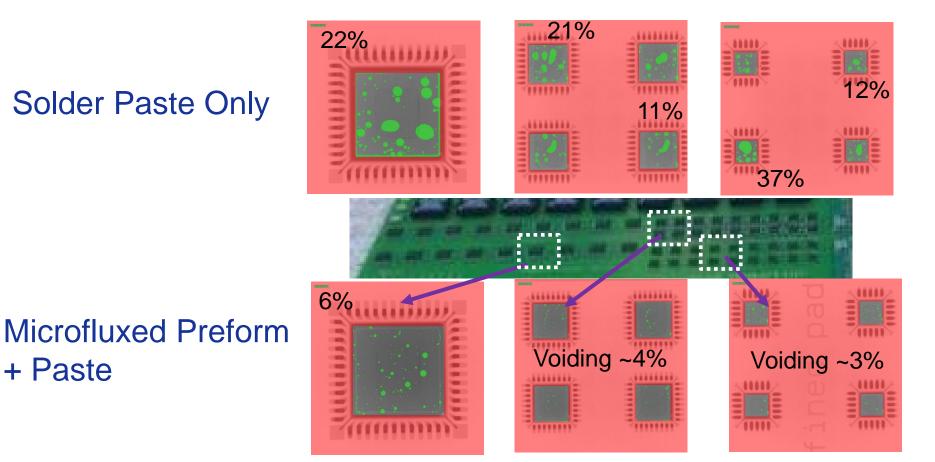
- The average voiding for Microfluxed Preform+ Paste
 Assemblies reflowed in
 Nitrogen was well below
 10%.
- No significant improvement in voiding for Solder Paste Only configuration was observed.



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Consistent low voiding of QFN components was achieved using LVT versus Solder Paste Only approach



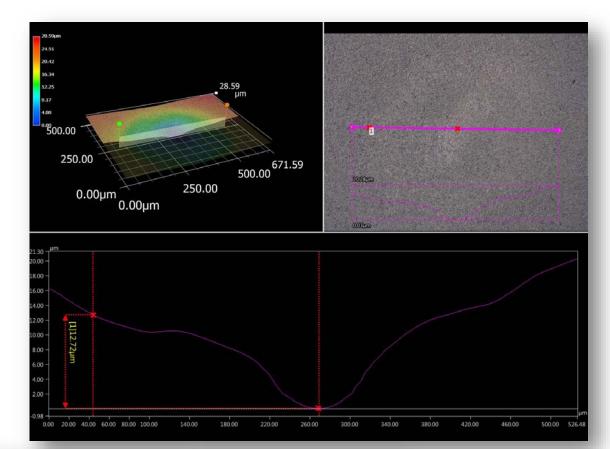
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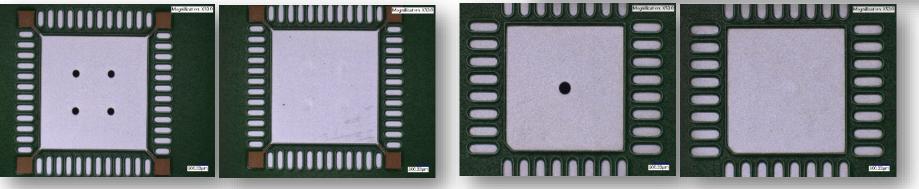
- Three types of pad design was used in this study:
 - -No via

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- -Plugged vias
- -Unplugged (through) vias
- Depending on the pad size, one or four vias were used per pad.



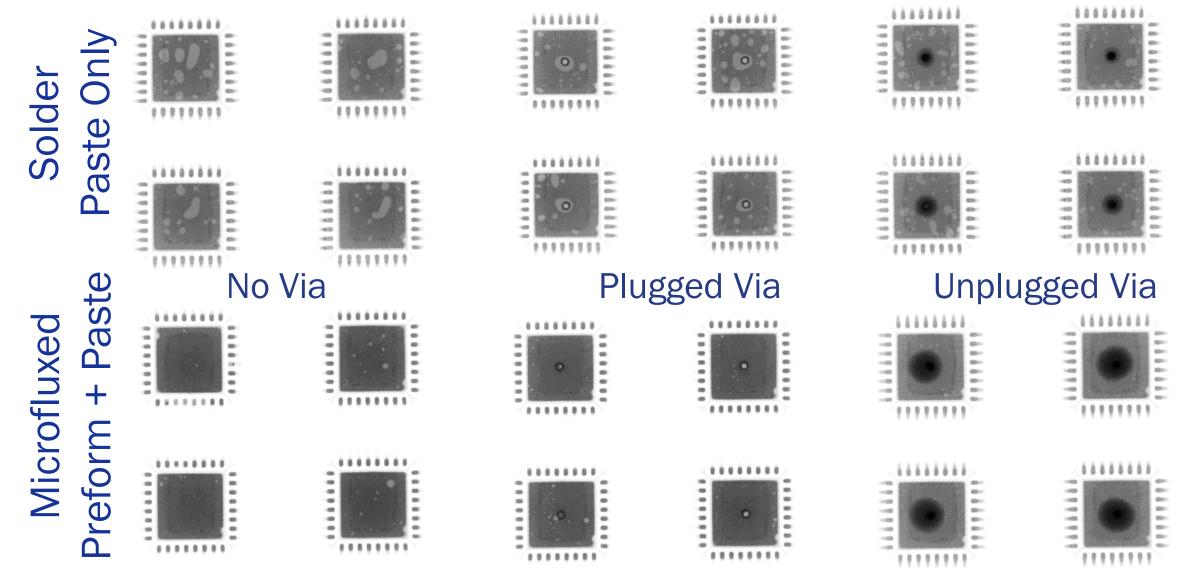


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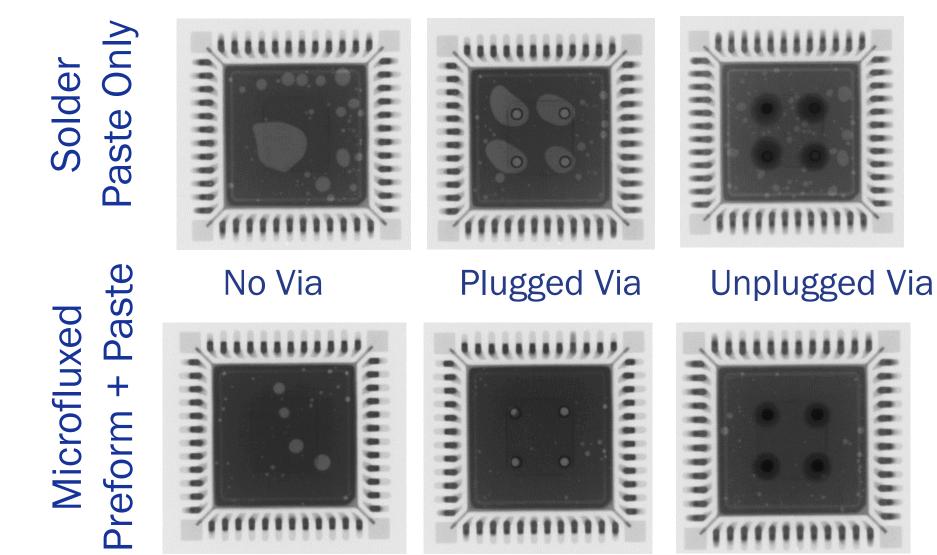
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- Solder overfills the hole leading to the bump formation on the back side of the PCB.
- Those bumps could result in insufficient thermal connection with heat sink.
- Solder wicking was observed both with Solder Paste Only and PF+Paste configurations.



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Summary/ Conclusions:

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- Low Voiding Technology using microfluxed preforms has the highest impact:
 - Significant reduction in voiding
 - Tighter distribution of voiding
- Interaction of assembly process factors impacts voiding performance
- Additional Benefits:
 - Higher reliability
 - Reduced flux residue
 - Eliminates rework
 - Enhances electrical and thermal performance



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- Alan Plant
- Frank Andres
- Karen Tellefsen
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Thank You!

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