Flex Based 3D Package Innovations for Enabling Low Cost System Level Integration and Miniaturization

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Abstract
Hand-held communication and entertainment products continue to dominate the consumer markets worldwide and, with each generation, offering more and more features and/or capability. And even though the actual functionality of the new product offering expands, the customer is expecting each generation to be smaller and lighter that its predecessor. More functionality typically requires additional or more complex electronics and greater memory capacity. Increasing functional capability, however, can adversely impact the products size as well as manufacturing cost. The challenge manufactures face when competing in the world marketplace is to offer a product that will meet all performance and functionality expectations within budget and without increasing product size.

Increased electronic functionality can be achieved through the development of more complex silicon integration (system-on-chip) but that route generally requires a great deal of capital resources and time. With the rapid deployment of new products from an ever growing number of competing companies', time-to-market can be the difference between leading and following. For that reason, many manufacturers will rely heavily on more innovative IC package solutions, solutions for integrating a number of already proven functional elements within a single-package outline. When adapting multiple die configurations, each package becomes a fully tested subsystem that can be certified by the supplier before board or module level assembly. To achieve system level integration and miniaturization goals, companies' can now rely on a combination of multiple-die package solutions and high-density flexible film based substrate methodology. For many applications, the multiple-die package is actually proving superior to the system-on-chip alternative because it minimizes risk and economically integrates several different but complementary functions. In the case of memory for example, multiples of the same function can be vertically stacked for increased density.

This paper will explore three flexible film based multiple die system level applications developed within Tessera's Package Engineering Service Laboratories.

Introduction
The motivation for developing higher density IC packaging continues to be the market, the consumers' expectation that each new generation of products furnish greater functionality, be smaller than its predecessor's and provide higher performance. To address functionality and size, a number of companies have already shifted away from simple single-die IC packaging and are adapting various forms of multiple-die 3D packaging. A 3D package is a component that incases multiple devices. The bare die can be grouped into a single package or individually packaged and electrically tested before joining together in a vertically configured format. Applications requiring more complex mixed-technology functions can be produced economically as well. Microprocessors and memory, for example, have very different wafer process flows and functionality. Developing an electrical test for a single package assembly that combines both technologies is difficult, but, by using a combination of stackable pre-tested ICs packages there are never any compromises made that would impact their subsequent board level functionality.

Ball Stack Packaging
The ball-stack methodology has proved to be one of the most practical solutions for packaging several die within a single package footprint and is probably the most economical approach for developing a multiple-die component as well. The final 3D configuration is accomplished by vertically joining two or more pre-tested single package units into a low-profile multi-tiered µZ™-Ball Stack package assembly (see Figure 1). The stacked packaged die methodology has proved to have less risk for memory because the individual package units can be pre-tested at high temperature, sorted and graded before conversion into the final vertical format. This methodology has proved ideal for a number of high speed SDRAM applications. And, by mounting the two-level ball stack packages onto single DIMM or SO-DIMM substrate it will furnish double the memory capacity and saves the expense associated with additional circuit board modules, the connectors needed for interface and the additional area on the host board.

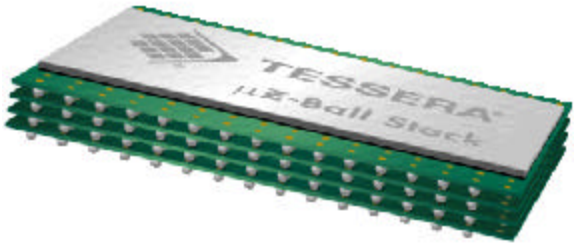


Figure 1 - The Stacking of Pre-packaged and Tested Die provides a Low Cost and Low Risk 3D Solution for Enabling Higher Component Density

In preparation for package stacking, individual package sections are first assembled using a single or two metal layer, non reinforced polyimide film substrate. To accommodate efficient package assembly processing, several package sites are uniformly arranged onto a common rectangular strip format. One of the more mature processes for interconnecting the semiconductor die and package substrate is wire-bonding. The process can be applied when the die is mounted 'face-up', away from the package substrate surface; however, wire-bond can also be applied to the die when mounted 'face-down' against the package substrate. While most die are designed with the bond pads at the outer perimeter, the newer generations of high performance memory have bond sites positioned though the center. To accommodate face-down wire-bond termination for the center-bond memory die, a slot is provided in the substrate to access the bond pads on the die as shown in Figure 2. Following die attach, wire-bond and encapsulation, the ball contacts are attached to the bottom surface of the substrate and finally separated into single package units. Electrical testing may be performed before or following package singulation.

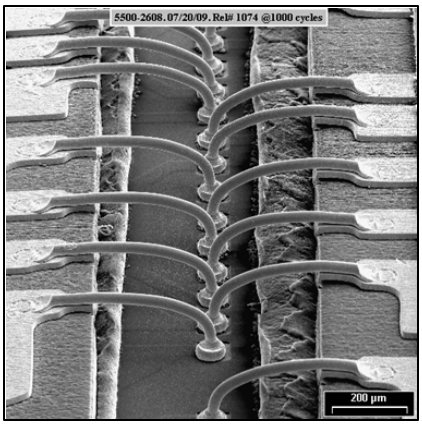


Figure 2 - Ideal for High Performance Memory Applications, the Through-Slot Wire-Bond Enables a Very Short Interface between the Die Bond Pads and the Package Substrate

Folded Multiple-Die Package Technology

The µZ™-Folded package technology enables a number of die to be attached in series onto a common multiple site substrate (typical of the three die, mixed memory package shown in Figure 3). To retain the folded format, a thin polymer film is applied to the top surface of one row of die. The extended area is then folded over and repeated for the remaining extension and secured in a clamp fixture to complete the bonding process. Following a cure cycle, the solder ball contacts are applied, the folded strip is cleaned and unit parts are finally singulated and made ready for testing. After testing the finished package is ready for board level assembly. The benefit to the user is that when the finished package is mounted to the host board or module, the die set will require no more area than a single die package.

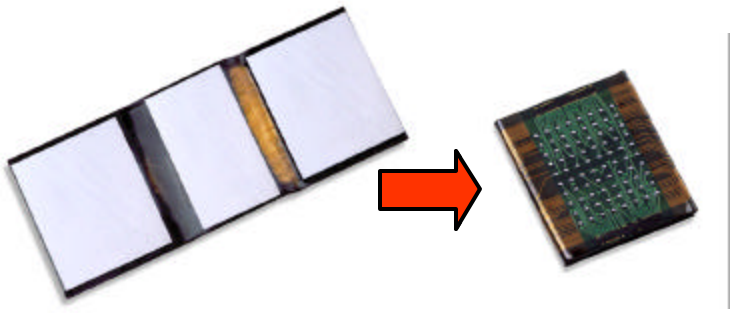


Figure 3 - The Three Die Package includes Two Flash Die and One SRAM Die but, the Finished Outline is only Slightly Larger than the Largest Die in the Set

The enabling technology for the multiple-die foldable package is the flexible film substrate. The base material shown in Figure 4 uses a 25 µm thick polyimide film having copper-foil on two sides. The multiple-die package assembly process begins with die attach, lead termination and encapsulation. The package adapts one of the most reliable package interconnect methods available, the lead-bond process. The technology provides a very close, low-profile coupling between die and substrate. This methodology minimizes both signal inductance and resistance because the lead is an integral part of the package substrate. During the lead termination process each lead is reshaped from its planer profile into an '*S*' configuration (Figure 5). The encapsulation of the die and lead-bond area follows. The encapsulation material has been formulated so that after curing it will allow a controlled movement of the 'S' shaped lead during thermal excursions to buffer the physical strain of the solder joint at the board level interface. Although the lead-bond methodology was originally developed for single die packaging, it has also proved to be successful for a broad number of multiple die package applications needing a small outline and low profile.

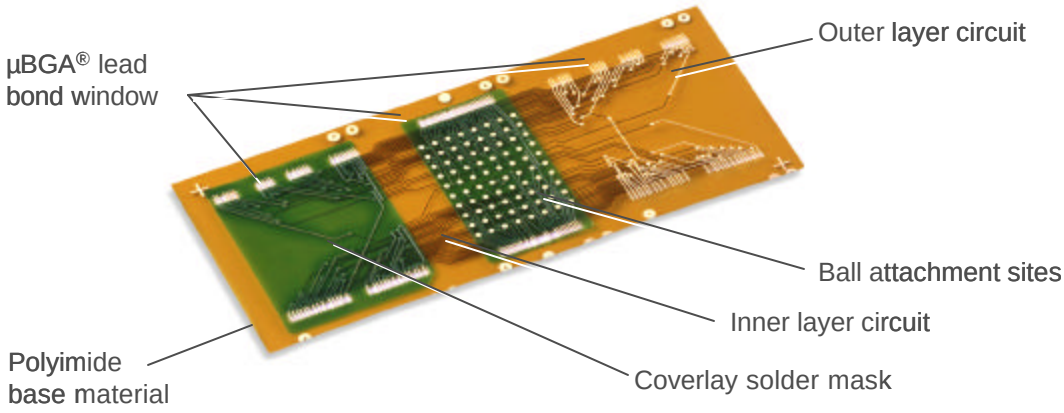


Figure 4 - Three Die Substrate adapts 25 µm Wide Circuit Layers on Two Sides, Interconnected with laser Ablated and Plated Micro-Vias

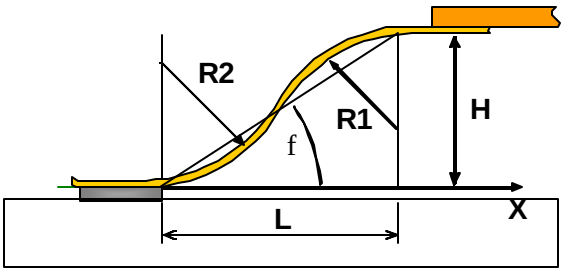


Figure 5 - The Symmetrical 'S' Profile of the µBGA® Lead, when Encapsulated, absorbs Physical Stress and Strain that can occur between Dissimilar Materials when Exposed to High and Low Operating Temperature

Fold-Over and Stacked Packaging

There are a number of multiple function package applications that will require the sequential assembly of separately processed die. A case in point is the package shown in Figure 6 that was developed as a base unit, providing a mounting site on its top surface for ICs with complimentary but very different functions. Through a process of folding and package stacking, two or more pre-tested parts become a single, high yielding multiple-function component. The finished stacked package configuration can be performed by the supplier or at the board level assembly stage. If the decision is to join the two sections at the board-level assembly, the base fold-over package can be placed onto the board and additional packaged devices placed sequentially onto the mating contact matrix of the base for simultaneous reflow soldering.

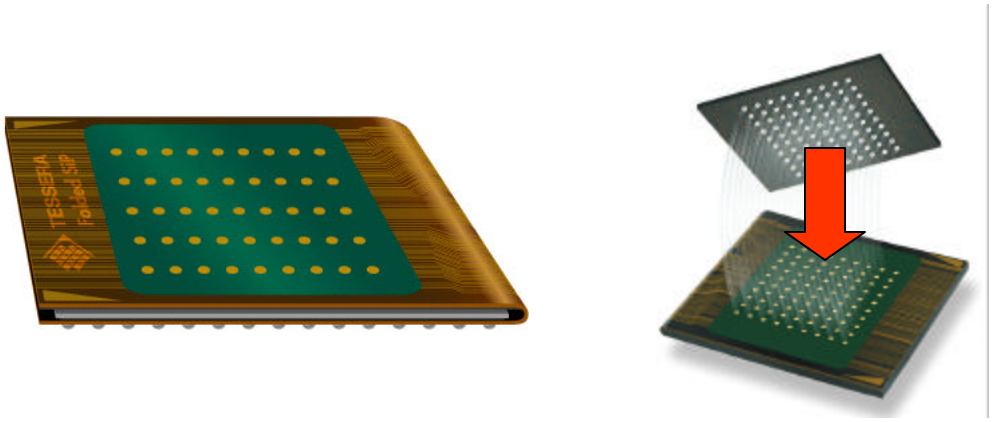


Figure 6 – This Technology provides a Land Pattern on its Top Surface to accommodate the Stacking of Additional Packaged IC Devices

The fold-over base section substrate (Figure 7) is designed to accommodate a single die interface to an array matrix for PCB mounting and, by extending the base material from one edge of the package; a second array-mounting site is provided. The extension will eventually be folded over and onto the die encapsulation to accommodate a second package. For this application the die is mounted to the substrate with its active surface facing away from the substrate surface (face-up). The substrate is designed so that the bond-wire interface from the die is as direct as possible.

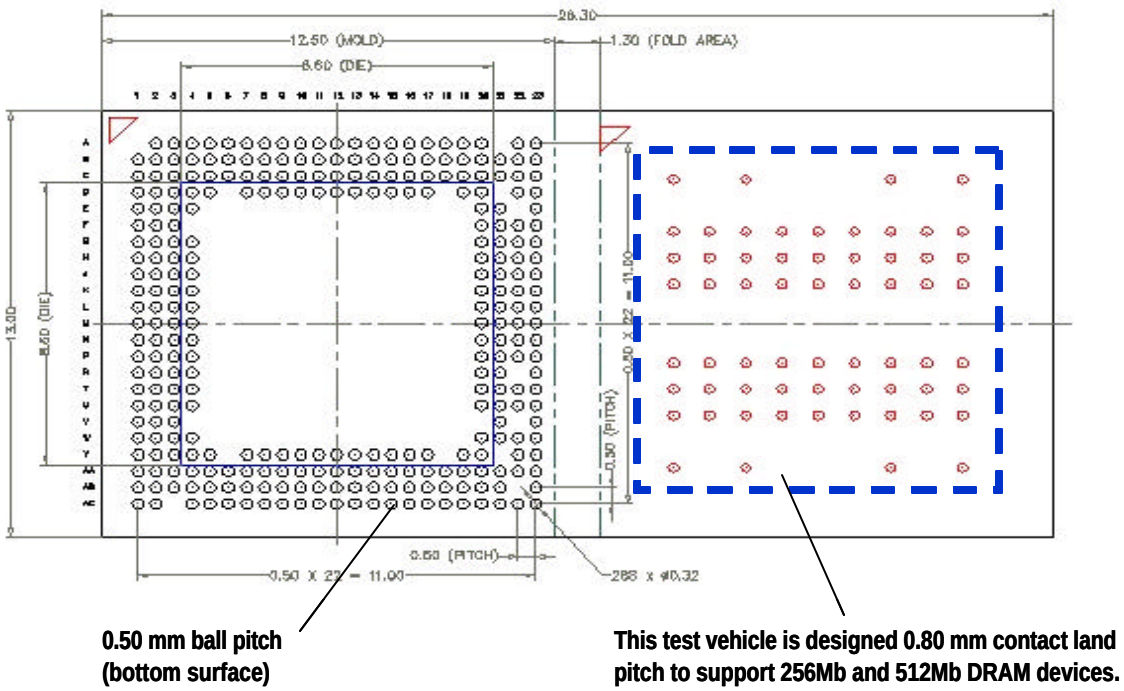


Figure 7 - Fold-Over Package Substrate is Designed with an Extended Section that, when Folded, Accommodates the Stack Mounting of Additional Packaged ICs

The actual interface between the base die and the package attachment site on the top of the finished package requires two circuit layers to provide for higher wiring density. The two metal layer fabrication process used for the µZ package substrate is very similar to that described for the folded package, enabling very narrow circuit routing features. The base material selected for the fold-over base package is also a 25 µm thick polyimide film having copper deposition on two sides. Spacing between the wire-bond lands on the substrate can be greater, but it is critical that the land be arranged so that the wires length can be minimized. Although both sides of the substrate are utilized for interconnect, the circuit path between die and the stacked package mounting site is routed only on what will become the inside surface of the flex material. With the exception of the 'fold zone', the circuit pattern remaining on the outer surface is coated with a photo-imaged dielectric mask material.

Prior to die attachment and wire-bonding operations, an adhesive pattern is applied to the substrate surface. This adhesive can be dispensed as a liquid, pattern printed or, pre-applied to the substrate as a die cut dry film composite. The silicon die is then aligned and placed onto the prepared site followed by a short cure cycle. After curing the die-attach material the substrate carrier is transferred to the wire-bond system to complete the electrical interface between die and substrate. The wire-bond land shown in Figure 8 is a staggered oval shape with 100 µm pitch to furnish wider clearance for the wire-bond process. Limiting the wire loop height is vital to maintaining a lower package profile. To accomplish this, a combination of wedge and ball bonding methods are employed as shown in Figure 9. The relatively low (75 µm) loop height of the wire must be maintained in order to provide the thin encapsulated package height requirement established. The attachment and wire-bond sequence completed, the assembly is inspected and transferred to a transfer-mold system for encapsulation.

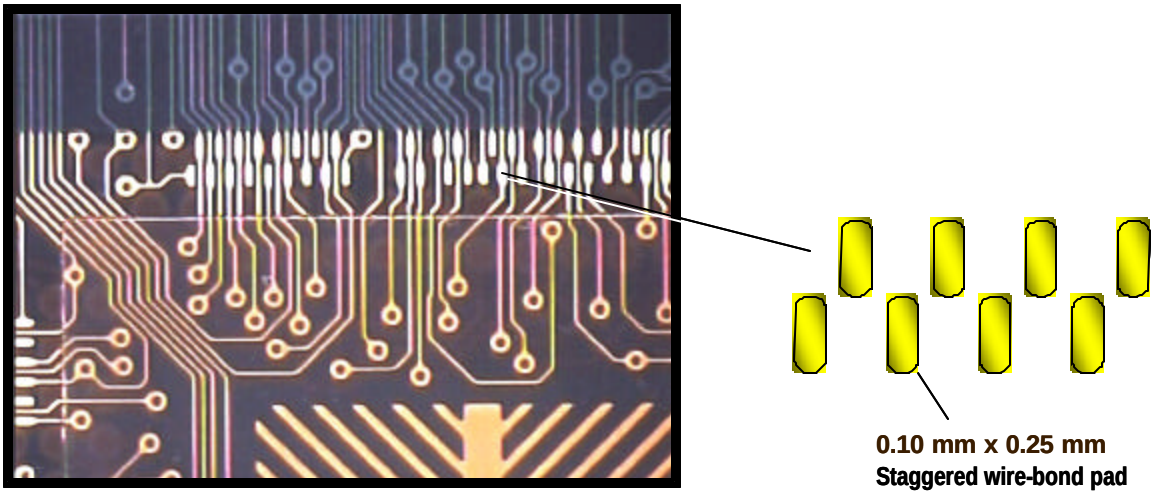
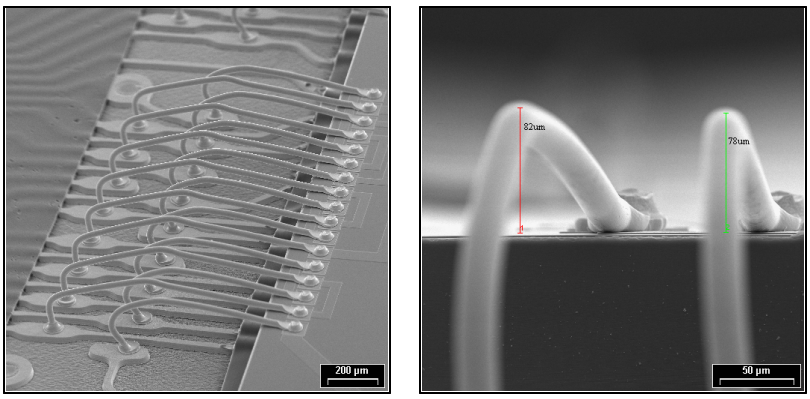


Figure 8 - The Staggered Land Pattern is Designed to Maximize the Side-By-Side Wire-Bond Requirements of Higher I/O Die



Reverse bond enables a lower wire loop profile

Reduced loop height is 75 - 80 microns

Figure 9 - A reverse-Bond Substrate-to-Die Process is applied to enable the Lowest Possible Loop Height after Wire-Bonding

The final phase of the base package assembly is performed in a sequence that first applies an adhesive composition to the top surface of the molding compound followed by precise mechanical folding and clamping operation. When the bonding material completes its curing cycle, the finished base package is ready for ball contact attachment, singulation and electrical testing. Singulation of the packaged devices from the strip is also very precise. A precision saw developed for wafer level processing has proved efficient for cutting through the substrate and mold material. Both sawing and laser ablation are viable methods for package singulation, requiring minimal dedicated tooling and each can be programmed to accommodate several package outline variations.

Building the package in stackable sections typical of that shown in Figure 10 has two benefits. It allows the user to specify multiple variations (different memory functions, data rate and so on) as well as accommodating secondary sources of supply. Whether or not to join one package to the other before or during the board level assembly process is a decision that may be influenced by the requirement for in-process configuration flexibility. For example, the base fold-over package can be furnished by vendor 'A' while the memory sections of the stack are supplied by vendor 'B', 'C' or 'D'.

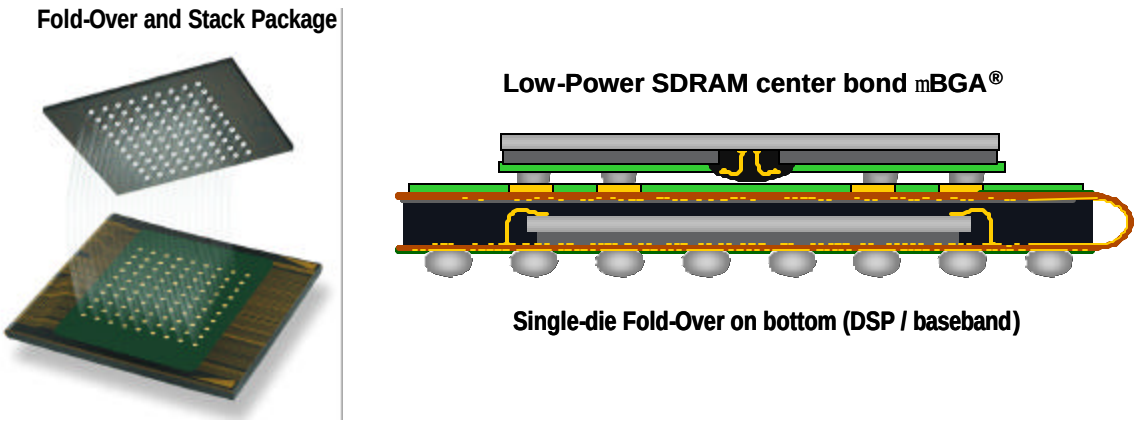


Figure 10 - Fold-Over and Stacked Package enables Board Level Sequential Assembly of Components supplied from Multiple Sources

Substrate Material Selection and Fabrication Methodology

The non reinforced polyimide film dielectric has proved to be excellent for high-performance applications and is often selected for products that must operate in more hazardous environments. The physical elements of the polyimide flex-film are detailed in Table 1. For single side circuits (one metal layer) the copper is typically applied to the flexible base dielectric as a foil with adhesive as illustrated in Figure 11. An alternative process casts a polymer dielectric directly onto the copper foil without adhesive. In both single metal material variations, holes and other features are drilled or punched through the composite structure; circuit features are imaged using photo resists and chemically etched to provide the finished circuit pattern.

Table 1 - Flexible Polyimide Film Materials

	Polyimide Film (w / adhesive)	Polyimide Film (adhesiveless)
Glass transition temp.	270°C	270°C
Oper. temp. range	85-160°C	105-200°C
TCE (ppm/°C)	13-15	15-15
Dielectric constant	3.5	3.3
Dielectric strength	3-5Kv / 25µm	5Kv / 25µm
Insulation Resistance	10^3 O-cm	10^3 O-cm
Modulus (MPa)	2500	4000
Tear resistance	500g	500g
Cu peel strength	1740 N/M	1225 N/M

Data source: IPC-2223

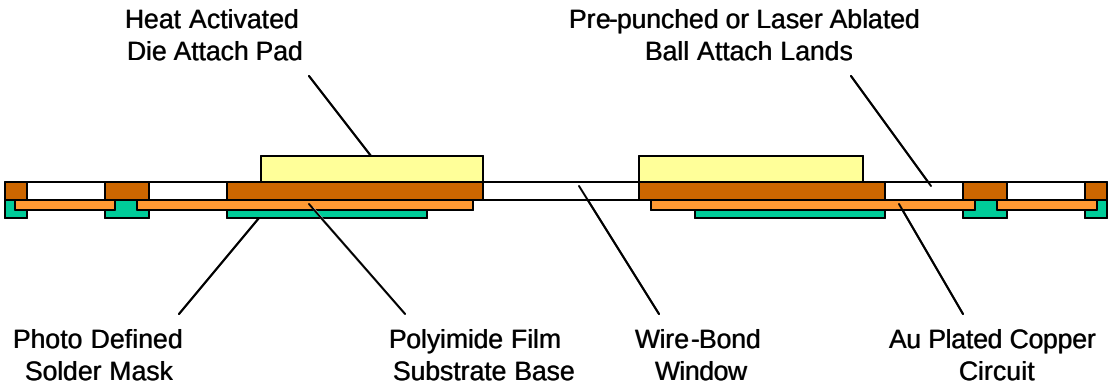


Figure 11 - The Single Metal Flexible Film Substrate developed for the Ball Stack Package is the Most Economical Package Base but it has Limited In-Package Circuit Routing Capability

Two metal flex based substrates can be furnished using adhesives as well but adhesive-less copper is preferred, especially for fine-line circuit design. For this application, a seed layer is first applied to the polyimide film consisting of a sputtered 'tie-coat' of nickel, chrome or nickel/copper alloy of approximately 200-300 angstroms thick followed by copper sputtered to ¼ micron. The sputtered copper layer is then electroplated to approximately 2to 3 µm thick providing a sufficient conductive base for the subsequent electroplating of the circuit conductors. This methodology is referred to as a semi-additive plating, where holes and features are first drilled or punched through the metalized substrate, photo-resist materials are applied over the base-copper, the circuit pattern is then imaged and developed and made ready for the plating process. During the electro-plating process, copper is 'built-up' onto the exposed circuit pattern and into the connecting via holes. After stripping the resist, the remaining thin base alloy layer remaining on the substrate surface is etched away leaving only the finished copper conductor pattern.

To insulate and protect the polyimide based substrate after circuit fabrication, permanent coatings or films are generally applied over the circuit conductors as illustrated in Figure 12. The openings in the coating provide access to the copper features designated for component attachment during the assembly process. Photo-imagable materials have been developed for surface insulation as well, available in dry film and wet applied variations, the photo-imaged material requires no pre-processing or hard tooling (other than photo-tools).

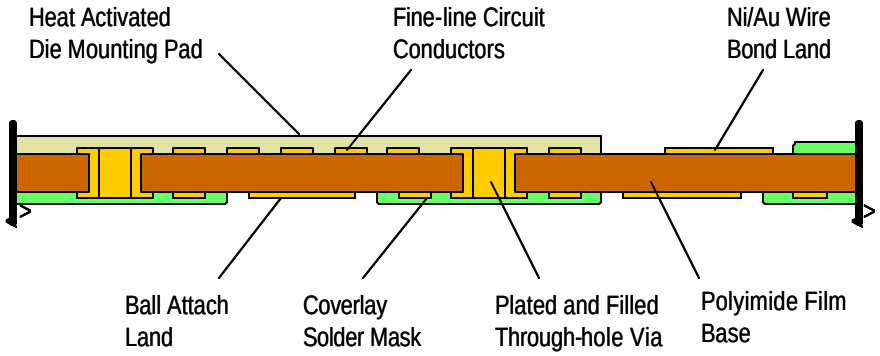


Figure 12 - The Two Metal Layer Flexible Film Substrate with Semi-Additive Plating and Plated and Filled Micro-Via Interconnect Enables Higher In-Package Circuit Routing Density

Conclusion

Although this paper illustrates a number of practical package solutions for multiple die, there are still challenges that need to be addressed. Many of these involve logistical and business issues that some in the industry are already solving. These include: cost reduction strategies, reliability improvement strategies, design and analysis capabilities, cost of design, system test and access to known (fully tested) good die (KGD). To obtain packaged part die quality and reliability, some sort of electrical testing must be done on the bare die prior to package level assembly. ASIC, simple logic circuits, some processors and linear circuits, at some point, tend to stabilize but testing is the only way to guarantee quality and reliability. The multiple die packages shown allow package level testing and have already proved to be a practical solution for system level integration and miniaturization. In the future, it may be practical to combine both SoC and 3D packaging to achieve specific economical goals. Another issue is the acknowledgement and respect of the

developing companies' innovative intellectual property (IP) and the need for improved cooperation among the package manufacturers, semiconductor device suppliers, and the systems companies.

As the multiple die package sectors continue to grow, all of the parties involved must find ways to work with each other to make sure that they minimize risk to the user and ensure rapid deployment into the marketplace. And, although some have defined the multiple die 3D packages as an "interim" solution to fill gaps while an SoC product is developed. It is certainly true that 3D packaging is a way to get into the marketplace quickly, long before complex mixed function silicon can be created. Many believe that the real advantage to the multiple die approach is flexibility in developing and manufacturing specialized package combinations quickly and with minimal risk of resources.

References

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