PWB Design: Beyond Copper Interconnects

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Abstract
Two emerging board technologies, embedded passives and embedded optical waveguides, have the potential to change the way that printed wiring boards operate. No longer will interconnects be relegated to copper, but true passive electrical functionality will be incorporated into the board. Some high speed electrical interconnects may actually be replaced with pulses of light guided through transparent optical materials built into the board. These technologies are reviewed in simplified form, and the implications for board designers are examined.

Introduction
Today's Printed Wiring Board (PWB) designer practices the routing of metal lines over the surfaces of glass-epoxy or perhaps more exotic dielectic materials. Perhaps that designer works on boards with 8, 12, 20, 36, or more layers. Perhaps the designer works with a shop that pushes the design envelope, shrinking lines and space dimensions to 3, 2, or even sub-1 mil dimensions. Perhaps the designer is working on the latest 0.4 mm pitch BGA chip attachments with multiple layers of HDI or similar technologies to route it. Even in the compilation of all of these cases, it is still a game of putting metal on multiple layers of a dielectric material. The game has not changed since the introduction of the PWB decades ago.

That game is now changing. Today, two major technologies are being brought to bear on the PWB. The first of these is Embedded Passives (EP), a thrust to place other materials inside the PWB to replace surface mount technology (SMT) resistors, capacitors, and inductors on the surface of the board. This pulls electrical functions into the board, requiring the designer to be aware of more of the electrical aspects of the passive designs. Many of these materials are available to board shops today, and Motorola, for instance, has shipped millions of functional modules with various EP technologies. The second technology is polymer optical waveguides. Imagine the possibility of conducting high speed interconnects in a technology that is not susceptible to crosstalk or the parasitic losses of the typical PWB. That is the promise of embedded optical waveguides; yet, there are many challenges to be resolved in this area.

The purpose of this paper is to review the essential technology elements of each of these emerging advances with the perspective of what is important to the CAD designer. Basically, how do these things work in layman's terms? How are passives sized? What will be new in the design of waveguides? These, along with other questions, will be addressed for both of these emerging technologies.

Technology #1: Embedded Passives
The first revolutionary technology to be examined is Embedded Passive (EP) components. EP utilizes new material sets to embed the functionality of surface mount passives into layers of the PWB substrate. Passives, in general, are divided into three categories: inductors, which store electrical energy in magnetic fields; capacitors, which store electrical energy in electric fields; and resistors, which dissipate electrical energy. Each of these devices is typically packaged into extremely small form factor SMT parts, such as the ubiquitous 0402 and the relatively new 0201 EIA case sizes. Even smaller case sizes are on the implementation horizon. However, SMT devices always take up more area than their own surface area because of pad geometries and required keepouts. It is very desirable to move at least a portion of these into the board, which is accomplished with the advent of embedded passives.

Inductors. In actuality, RF board designers have been creating at least one form of embedded passive for some time. Transmission lines are effectively inductor structures. An inductor is formed whenever a current loop exists in a circuit. Current loops induce a magnetic field in accordance with the right hand rule, thereby storing energy in a magnetic field. Transmission lines have been utilized for a few nanohenries (nH) of inductance. Single layer copper spirals are also used to reach about 10nH. Multi-layer spirals in HDI designs are becoming more prevalent, reaching up to about 25nH for a maximum value. The sizing of inductors is dependent on a number of parameters, including line width and spacing, diameter of any circular geometries, dielectric gaps for multi-layer structures, etc. The bottom line is that these parts have been created by designers for some time with input from their electrical engineering counterparts.

One possible extension of the inductor designs up to the 100nH range would utilize a ferromagnetic material either as a core within loops of copper or lying beneath or sandwiching a spiral. These ferromagnetic materials are potentially screen-

printable. From a board design standpoint, there would likely be only one additional mask or screen to design. However, the cost of integrating a ferromagnetic material makes implementation unlikely. This can be explained by looking at the relative percentage of inductors for a typical product. A typical distribution of passives in a cell phone (early 2G or early 3G) is shown in Figure 1. Note that inductors comprise less than 10% of the number of passives, and the number that can be embedded is only a fraction of that percentage. For most manufacturers, it does not make economic sense to work on embedding such a small fraction of typical devices. Some applications though, such as switching power supplies, might benefit from such constructions. Universities, such as Georgia Tech, continue to work on high value inductors with ferromagnetic cores.[1, 2]

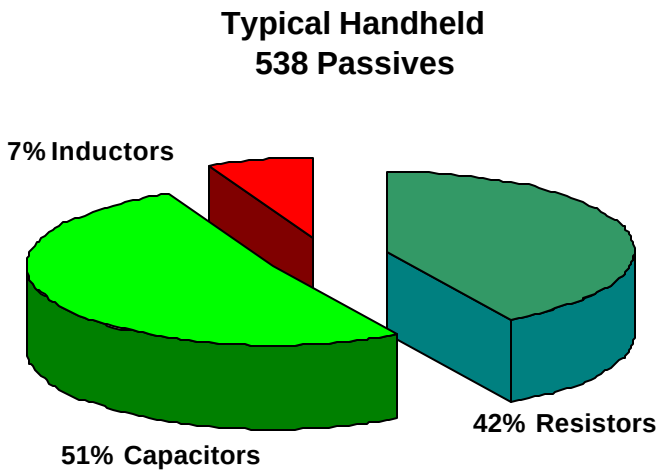

Figure 1 - Typical Passive Count for a 2G Cell Phone

In summary for inductors, no new masks are required to make the typical inductor. Inductor designs are limited by the size of the devices and the electrical properties of the resulting structures. Expansion of embedded inductor range is unlikely because of the need for expensive advanced materials (ferromagnetics) with limited impact.

Capacitors. Capacitors are elements that store energy in electric fields. The simplest form of capacitor, which is also the simplest embeddable form, is the parallel plate capacitor. The capacitance, or the charge storage capability, of the structure is related by the following equation:

$$C = \frac{e_0 e_r A}{d} \qquad (1)$$

where C is the capacitance in Farads (F), $\varepsilon_0 = 8.854 \cdot 10^{-14}$ F/cm^2, ε_r is the unitless dielectric constant of the insulating medium separating the two parallel metal plates, A is the area of the smaller plate (if they are not equal), and d is the distance between the inner surfaces of the two conductive plates. The dielectric material influences the relative dielectric constant, which may also be denoted as D_k or κ. The physical parameters that can be varied are the thickness of the dielectric and the area of the capacitor plates. Obviously, the smaller the embedded capacitor, the better, which implies that higher D_k and thinner dielectrics are preferred.

The key to higher capacitance is the dielectric. There are basically two types of dielectrics, as illustrated in Figure 2. They are organics and ceramics. Ceramics are preferable in terms of dielectric constant, as they possess dielectric constants from the 10's to the 1000's. Moreover, ceramics can be coated very thin, another advantage to an embedded capacitor. Organics tend to have dielectric constants below 10, and thickness is often greater than 10 microns. However, organics are more easily processed than ceramics. In fact, ceramic materials usually require firing temperatures beyond what can be tolerated by the organic substrates which they are to be mounted upon. A third possibility, as illustrated in the middle of Figure 2, is the combination of a ceramic material dispersed in a polymer medium. These materials have improved dielectric constants compared to organics, but the result is an effective-medium calculation rather than an average. The result is a dielectric constant improved to about 20 to 50 from the polymer dielectric constant of about 4. The bulk dielelctric constant of the dispersed ceramic particles is typically 200-2000. Still, the material gains processability while retaining an elevated dielectric constant. Several of the materials currently shipping from various suppliers are based upon ceramic-loaded epoxy compositions.

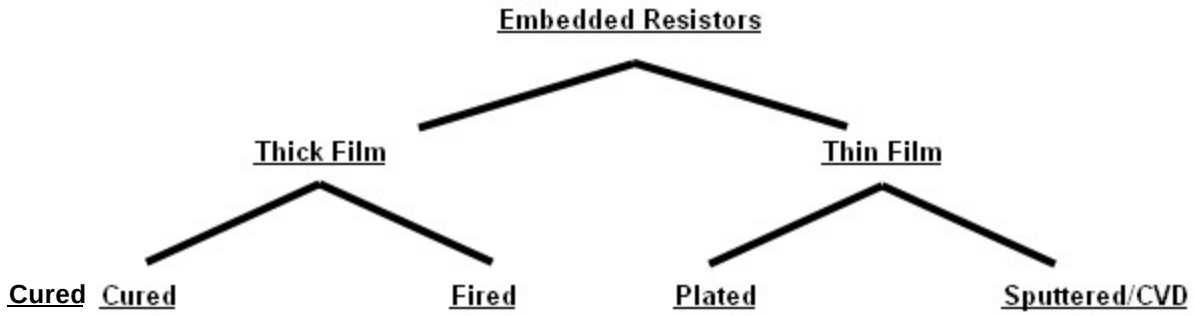

Figure 2 - EP Capacitor Dielectric Compositions

Embedded capacitors can exist in two means: 1) distributed (or sheet) capacitance or 2) singulated (or discrete) capacitance. In the first case, the capacitor is a full plane, encompassing the entire board. Typically, the laminate separates power and ground planes, providing decoupling of the power supply. The record is already well populated with art related to distributed capacitance and the expected necessity of these materials for high frequency, power-hungry boards.[3-5] For the designer, an embedded distributed capacitance plane should be treated the same as a normal power-ground plane. The number of clearance annuli per unit area should be kept reasonably low, as many of these materials are brittle from high ceramic loading. Otherwise, the accounting for the capacitance is merely in the specifications for the build notes and the manufacturing drawing.

The second type of embedded capacitors, singulated embedded capacitors, is formed by patterning both the capacitor plates and the dielectric material. The dielectric may be selectively deposited or removed after a blanket deposition. A cross-sectional example of a singulated embedded capacitor used by Motorola appears in Figure 3. In the case of distributed capacitance, only capacitors from the power line to ground can be embedded. For singulated embedded capacitors, any circuit topology, series or parallel, can be replaced. Two of the main materials for this type of capacitor are DuPont's Interra™ pastes[6, 7] and Huntsman Advanced Materials Probelec™ 81 CFP (ceramic-filled photopolymer).[8] Methods of forming the singulated capacitors varies with the material class, but suffice it to say that new artwork layers will be required to define the dielectric and the capacitor plate geometries.

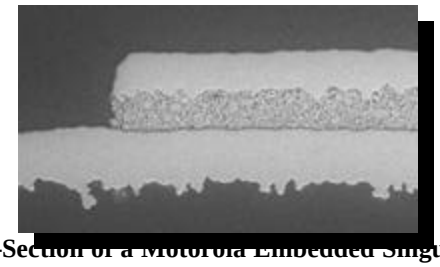

Figure 3 - Cross-Section of a Motorola Embedded Singulated Capacitor

Resistors. The third type of embedded passive is the resistor, arguably the most easily replaced component. Referring back to Figure 1, greater than 40% of passives in typical phone constructions are resistors. More importantly, materials exist such that virtually all resistor values can be embedded (as opposed to capacitors, which require more exotic dielectrics for moderate value capacitors). The processes involved in resistor formation tend to be less expensive than capacitor processes as well. The economics favor resistors for the primary economic driver for first implementations of embedded passives.

Resistors dissipate energy and drop voltage in accordance with the familiar Ohm's Law (V=IR). A typical rectilinear construction of a resistor in Polymer Thick Film (PTF) is shown in diagram in Figure 4. The resistance of such a resistor is given by equation 2

$$R = r\frac{L}{W \cdot t} \qquad (2)$$

where R is resistance (Ω), ρ is the resistivity of the material (Ω·cm), L is the length, W is the width, and t is the material thickness. However, thickness is typically not an easily measured parameter, while resistance is easily measured. Equation (2) can be simplified by substituting a new parameter, ρ_s, sheet resistivity (Ω/square), which is defined as ρ/t. Substituting yields equation 3:

$$R = r_s \frac{L}{W} \qquad (3)$$

The beauty of this equation and the parameter ρ_s is that the aspect ratio (L/W) defines the resistance. In other words, if L=40mils and W=10 mils, then there are 4 squares. Therefore, if the sheet resisitivity is 100 Ω/square, then the resistance is 400Ω. Note that if L=400mils and W=100mils, then there are still 4 squares, and resistance is still 400Ω.

Although rectilinear resistors are widely used in straight lines and serpentines, an additional form used for small effective ratios is the annular resistor. Additional material on this resistor geometry can be found in the literature.[9]

Resistors are formed by either additive or subtractive processes. In the additive case, a paste or ink is typically screened or plated in desired locations. Different termination materials are often required to protect the copper-resistor interface from corrosion and, therefore, changes in contact resistance. Additive materials are typically available in a wide range of sheet resistivities, though this varies by supplier. Motorola's choice for reisitors is an additive ink, dubbed Polymer Thick Film (PTF). The PTF ink is screen printed onto previously etched termination pads, which define the length of the resistor. The screen printing process defines the width (and the thickness). The termination pads are selectively coated with silver to promote stability by avoiding contact corrosion. The PTF ink is available from about 30Ω/square up to over 100,000Ω/square. Three to five decades of resistance values can be addressed by printing up to 3 PTF inks. More information on this process is available in published works[10,11]

In the subtractive process, a sheet material is used, typically copper with a thin coating of some other material, such as NiP, which has higher resistivity and is selectively etchable compared to the copper. The foil is placed with the resistor material down. Typically, the resistor width and length are defined in two etch steps: one to define the width of the resistor, removing all material, and a second to define the length, removing the copper only and leaving behind the thin, high-resistivity material. Typically, these materials are available in the range from 25Ω/square[12] up to 1000Ω/square.[12]

On top of the types of processes, there are additionally a number of materials choices by the type of process that is used. A chart illustrating the variations for commercially-available resistor materials appears in Figure 4.

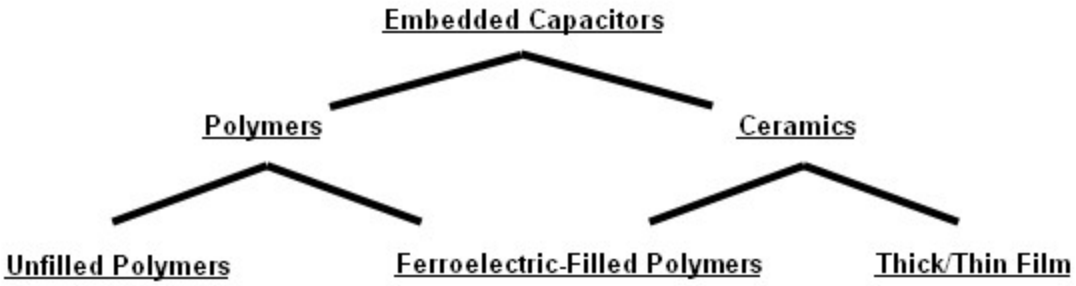

Figure 4 - Commercially-available Embedded Resistor Materials

Implications for the Designer. So, what are the implications of EP on the work done by the board designer? First of all, designers will be responsible for creating specific values of components. Secondly, designers will be responsible for implementing the required design rules for a variety of EP processes. Finally, designers will be responsible for understanding the cost ramifications for the embedded processes they use.

Designers have historically been responsible for interconnecting components with copper lines. The lines might have specific geometries in certain cases, such as RF transmission lines (stripline, microstrip line, or coplanar waveguides) or phase-matched differential pairs. Designers have never been responsible for calculating and implementing a specific value for a component. Now, designers may be responsible for creating embedded components with specific values, such as a 25pF series capacitor or a 1500Ω resistor. Creating a specific component value will require an understanding of the basic physical equations, the parameters of the chosen materials system, and the design rules appropriate for the chosen materials system. For instance, to create a 1500Ω PTF resistor requires the knowledge of the sheet resistivity used, the allowable aspect ratios,

and the overprint geometries required for a good termination. Additionally, the designer must know that a selective surface finish is required on the inner layer, and must provide for this facility as a separate mask layer in the artwork files.

Secondly, designers will be responsible for implementing the design rules associated with each EP process/material choice. Currently, the major EDA tools for the PWB industry do not handle EP components very well—much of the customization is left to the designer in a manual sense. The designer must be aware of keepouts associated with the parts, as these are often more restrictive than the line and space requirements on the inner layers. The designer will have to be aware of the build process and how separate layers should overlap. For instance, in DuPont's Interra™ paste capacitors, the dielectric must overlap the bottom plate, especially on one edge. The top conductor is then printed across the dielectric step. If the dielectric is not printed out far enough, then the capacitor could potentially be shorted. In the Motorola mezzanine process with Probelec™ 81 CFP, the dielectric is photoimaged with the top electrode as a mask. The bottom electrode is then formed, but it must be at least 3 mils larger than the upper electrode on all sides to allow a good photomask seal. Additionally, a microvia is required to contact the upper capacitor plate. The details for creation of the components are essential, and the designer must be aware of the strengths and weaknesses of all the approved processes/materials at his or her disposal. It should be noted that much of this work can be automatically handled by software, and the major EDA tool suppliers are moving towards supporting embedded passives in their mainline toolsets, along with the appropriate toolkits to manage the differences between processes.

Finally, designers must understand the cost implications with their materials and layer choices. Since EP processes are "mass-forming," which is to say that the cost of forming one component is the same as the cost of forming one million, care must be taken to maximize the use of a given process to produce the greatest number of components. However, part selection is often out of the designer's control. An engineer will specify a list of parts to be embedded. What the designer might be able to influence are the parameters (such as sheet resistivity) and the location of the specified components. Examining Motorola's processes shows two excellent examples. Multiple prints of PTF resistor inks are possible. However, printing the same ink on two layers costs twice as much as a single print. If a designer can co-locate all resistors requiring one sheet resistivity on a single layer, an optimum cost design can be achieved. (Note, this does *not* mean that all resistors must be on one layer.) In the case of the Motorola mezzanine capacitor process, capacitors are formed on two layers symmetric around the substrate at the same time. A knowledgeable designer can take advantage of these two layers, realizing that no additional cost is attained by utilizing the second layer. Each embedded passive process has its own idiosyncrasies for cost, and these must be understood by the designer to achieve an optimal cost design.

Embedded passives present new problems and opportunities for designers. Still, these components are *electrical* parts—not all that different from the copper traces that designers commonly create. However, a new interconnect technology is shifting PWB technology away from the electrical realm.

Technology #2: Polymer Optical Waveguides

A looming problem for high-speed copper interconnects is the inherent parasitic reactances and the finite conductance of the conductor material. The small resistance and the parasitic inductance generated in the lines sets up an RC-time constant that limits the capability for signals to rise and fall in time, thereby setting up limits in speeds of switched signals on those lines. Electrical design can minimize the problem, but it cannot eliminate it. Another medium (and another transmission mode) is required to simplify interconnects and again push the speed envelope beyond copper. That medium is optics.

For some time, many companies have been examining optical materials for integration into the printed circuit board.[13] To understand the workings of these materials and the associated processes, one must understand the principle of optical fiber transmission. The governing equation is Snell's Law, which is expressed in equation 4:

$$n_1 \cdot \sin q_1 = n_2 \cdot \sin q_2 \qquad (4)$$

where n_1 and n_2 are the indices of refraction for the two mediums, and θ_1 and θ_2 are the angles of incidence to the respective mediums as measured from the normal line to the interface of the surfaces as light passes from medium 1 to medium 2. If plotted, then this shows that light is bent away from the normal line when $n_1 > n_2$. In the extreme case, the light is bent at 90º, or along the surface. At this angle or higher, total internal reflection occurs, trapping all of the light inside the first medium. Defining this angle as the critical angle, θ_c, equation 4 can be solved for the critical angle as follows in equation 5:

$$q_c = \sin^{-1} \frac{n_2}{n_1} \qquad (5)$$

Thus, a very small change in index of refraction yields the higher critical angle. For instance, if n_2 is 1.467 and n_1 is 1.462, the critical angle is 85.3º. A controllable change in the thousandths place in index of refraction is ideal for setting up total internal reflection in an optical fiber.

In an optical fiber, the high index center material is typically called the core, and the lower index surrounding material is called the cladding. These definitions will be used in the rest of the discussion for the high and low index materials for embedded waveguides.

A number of material systems have been explored for embedding optical waveguides into PWBs. A table of these chemistries along with the companies pursuing them appears in Table 1.[14]

Table 1 - Polymer Waveguide Materials

Manufacturer or Research Organization	Polymer Type	Patterning Techniques
Allied Signal	Halogenated Acrylate, Acrylate	Lithographic, RIE, Laser Lithographic, RIE, Laser
Dow Chemical	Benzocyclobutene Perfluorocyclobutene	RIE RIE
DuPont	Acrylate Teflon AF	Lithographic, RIE RIE
Amoco	Fluorinated polyimide	Lithogaphic
BF Goodrich	Polynorbornenes	RIE, Laser
TeraHertz	Fluorinated Acrylate	Lithographic
NTT	Halogenated Acrylate Polysiloxane	RIE RIE
Optical Crosslinks [15]	Proprietary Polymer/Monomer	Photobleaching
Nippon Paint	Polysilane	Lithographic, Photobleaching
Fraunhofer Institute, others [16]	Ormocer (ceramic-organic hybrid)	Lithographic

An example of a polymer waveguide, in this case, an optical reflection sensor from Optical Crosslinks [15] appears in Figure 5.

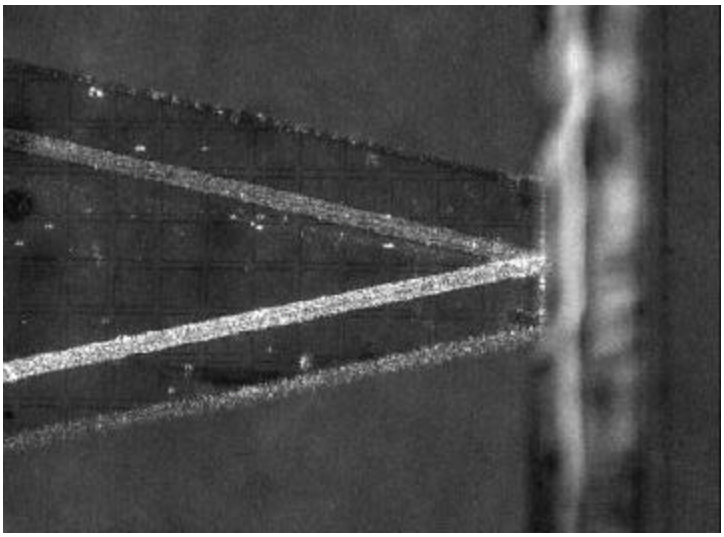

Figure 5 - Polymer waveguide used as a Reflectivity Sensor

From Table 1, it is obvious that there are a number of groups working on a materials solution, and there is great interest in the field. Unfortunately, this technology is not quite as far along as EP. There are still a few problems to be solved related to waveguide fabrication. First of all, there must be an index of refraction gradient generated. Most of the material systems provide two materials, each with a slightly different index. Typically a cladding layer is coated, the core layer is coated and imaged, and a second cladding layer is coated. The problem lies in the definition of the core layer, and each material set has its own method. Wet etching is not a good solution, because side-walls should be nearly vertical. Reactive Ion Etching (RIE) is possible, but this is an expensive vacuum process, and it should be avoided if fabrication is desired on-board. Some systems are photodefinable, which means that exposed material can be developed away. Other systems are photobleachable, which means that the index of refraction of the material can be selectively shifted a few thousandths by exposure to certain wavelengths of radiation prior to cure. In each case, well-defined edge gradients are required for good waveguide operation.

Compounding the problem, many of these systems degrade in their optical properties—or completely fail—when put through the temperatures of a typical lamination cycle. This fact will limit some systems to a surface layer of the board, which in many cases is not optimal.

The other major hurdle is the development of good structures to couple the light into the waveguides. Most of the concepts have a surface mounted laser or LED firing down into the board, usually through a hole, and hitting the plane of optical material. However, light at this angle does not satisfy the critical angle for total internal reflection. Some means must be provided to shift the beam from a vertical to a horizontal orientation. The only solution that is routinely mentioned is a 45º mirror in plane. It is formed either in an embossing step or by imaging the waveguide core at a 45º angle. Metallization of the back edge of the reflector may or may not be required, depending on the loss with the surface and the loss budget available. Creating this structure will be a new task for the designer, as it is definitely a 3-D object rather than the 2-D projection the designer is accustomed to drawing.

What does this mean for the board designer? For now, not much. A few rack backplane makers are examining optical waveguides on the backplane rather than patching in a network of fiber optics. This is a very small percentage of board designs, though. Most designers will not see this technology on their terminals in the near term. However, it is coming, and a few extra considerations will have to be made. First of all, there is a new materials set to specify in the manufacturing drawings. Distinctions will have to be made between the core and cladding layers, and the core patterning must be done in the artwork according to the manufacturers specification. The appropriate beam-shift (from vertical-to-horizontal) must be provided. Also, another layer of design verification must be implemented in the EDA tools…no longer will all signals be routed by copper. These are but a few of the designer's issues as embedded waveguides begin to appear in PWBs.

Conclusion

Two new technologies are making an appearance in the PWB arena. Embedded passives have been around for decades in niche applications, but new, inexpensive materials and processes, along with some new requirements for high-speed decoupling, are moving the technology into production in a growing number of applications. Embedded polymer waveguides, although a little further out on the horizon, are a burgeoning field, poised to carry even greater bandwidths of data through the circuit board, both in backplane and, potentially, handheld applications. Designers are now faced with the challenge of understanding not only the design rules for the given technologies, but also how their design choices impact the cost of the circuit boards. Moreover, in the case of embedded passives, designers will now be responsible for designing specific component values rather than simply supplying pads for components. In the case of embedded polymer waveguides, designers will be responsible for providing truly 3-D structures in layout rather than the typical 2-D projections constructed in CAD tools.

With both of these technologies, new functionality is being incorporated into the PWB substrate. Truly, these technologies are taking the PWB design beyond copper interconnects.

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