Principles for Implementing BGA and CSP Technology

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Abstract
As IC technology advances, electronic packaging for the ICs has had to advance as well. The package methodology has become technically more sophisticated and physically more complex. For many IC package applications, the lead-frame package technology of the past is not adequate. The Ball Grid Array (BGA) and Chip-Scale Package (CSP), on the other hand, are seen by many as the most viable solution for improving both functionality and performance. Array package technology is well established in the industry and the market growth for the BGA families has exceeded forecast. The array package technology and methodology has evolved throughout the past decade and many of the newer generations of BGA and CSP devices have become smaller and adapted finer contact pitch than their predecessors. The finer contact pitch BGA package enables the IC manufacture to meet the demand for higher I/O need for the more complex applications while maintaining a relatively small package outline.

By adapting a finer contact pitch, however, can dramatically affect the methodology used in board design and assembly. Because of the higher contact density made possible by array type packaging, design specialists have realized that the higher density land pattern geometry significantly effects PC board routing efficiency and can definitely impact fabrication cost. When adapting BGA and chip-scale BGA packaging in particular, one must consider board fabrication tolerances and provide the necessary physical features needed for assembly machine processing. For assembly process control, land pattern geometry is of primary concern because it is directly related to solder attachment uniformity. This paper will review BGA/CSP applications, packaging standards and package assembly methodology, furnish circuit routing guidelines for array packaged devices and review recommendations for design defined in IPC-7095A, the *Standard Guideline for Design and Assembly Process Implementation for BGAs.*

BGA/CSP Applications
Array packaging has evolved as one of the more versatile solutions for high performance and high I/O semiconductor packaging. Ideal for board level assembly processing, the physically robust components have proved to be less prone to damage than their lead-frame packaged predecessors and enabled a more efficient utilization of the ever shrinking circuit board. Reducing product size is a high priority for many companies, especially those developing portable and hand-held electronic products. Such companies are always seeking solutions for the next product generation to enable them to furnish more functional enhancements without increasing product size or weight. Consumer products such as wireless telephones, pagers, personal communicators, palm top computers, personal GPS, digital cameras and camcorders are key targets for product miniaturization. In addition, industrial and automotive electronics, medical and diagnostic products are targets for size reduction.

Because more and more components are being made available in the array package format, sources for BGA and CSP have become more plentiful. For high performance processor applications, for example, the lead-frame package has been abandoned altogether. The array format has become the most flexible package solution because it allows the design engineer to be more involved in the actual substrate development, ensuring that the finished product will more likely achieve its criteria for optimum performance. Power and ground distribution and clock lines, for example, can be incorporated within the package substrate. This greatly simplifies the package-to-board interface and, with selective in-package circuit routing of critical signals, it further optimizes functional performance.

Package Standards

Ball grid array packaging includes both plastic and ceramic package outlines and is divided up into to two groups based on their contact pitch. The carrier body or substrate for the BGA package is typically a dielectric structure with a metalized circuit pattern interconnecting the die to a uniform contact array pattern. One or more semiconductor devices can be attached to either the top or the bottom surface of this dielectric carrier. The array pattern on the underside of the substrate can be furnished with a land area contact or alloy ball contact. The contacts form the mechanical and electrical connection from the package body to a mating land pattern feature on the host printed circuit board. The first group to be standardized in JEDEC established three optional contact pitch variations; 1.50 mm, 1.27 mm, and 1.00 mm. While only a few component manufacturers are currently providing BGA parts with 1.5 mm pitch, BGA packaging with 1.27 mm and 1.00 mm pitch are quite common throughout the industry. An increasing number of BGA components are being furnished with fine-pitch contacts. The contact pitch plays a large role in the determination of what ball diameters can be used in various combinations. Table 1 shows the physical characteristics of the BGA contacts as they apply to array devices having 0.50 mm through 1.50 mm pitch.

Table 1 - Ball Contact Diameters, Allowable Contact Size Range and Contact Pitch Variations Specified in JEDEC Standards

Nominal Ball Dia.	Max - Min Diameter	Pitch
0.75	0.90 - 0.65	1.5, 1.27
0.60	0.70 - 0.50	1.0
0.50	0.55 - 0.45	1.0, 0.8
0.45	0.50 - 0.40	1.0, 0.8, 0.75
0.40	0.45 - 0.35	0.80, 0.75, 0.65
0.30	0.35 - 0.25	0.80, 0.75, 0.65, 0.50

JEDEC Publication JEP95-1 Section 4.5 and Section 5 define the physical attributes for a Fine-pitch Ball Grid Array (FBGA) package family. The package family is a reduced-pitch version of a wider pitch (<1.0 mm) Ball-Grid-Array (BGA) package. The total profile height, of the FBGA as measured from the seating plane to the top of the component, is >1.70 mm. The Low-Profile Fine-Pitch Ball-Grid-Array (LFBGA) and is a *reduced-height* version of an FBGA. The total profile height of the LFBGA as measured from the seating plane to the top of the component, is no greater than 1.20 mm. Thin-Profile Fine-Pitch Ball-Grid-Array (TFBGA) is a *reduced-height* version of an FBGA with a total profile that does not exceed 1.00 mm and the Very-Thin-Profile Fine-Pitch Ball-Grid-Array (VFBGA) is a *reduced-height* version of an FBGA with a total profile height that is no greater than 0.80 mm.

The JEDEC design guide for FBGA allows the manufacturer the option to increase ball diameter as the spacing or pitch between ball contact centers increase as compared in Table 2. The surface that contains the die may be encapsulated by various techniques to protect the semiconductor, however, the JEDEC standard guidelines will only define the general size and physical tolerance limits of the package outline and is careful not to influence or favor any package process or assembly methodology.

Table 2 - Ball Contact Variations for Fine-Pitch (FBGA) and Die-size (DSBGA) Package Families

Ball Pitch	Ball Diameter		
	Min	Nom.	Max
0.80	0.25	0.30	0.35
0.80	0.35	0.40	0.45
0.80	0.45	0.50	0.55
0.65	0.25	0.30	0.35
0.65	0.35	0.40	0.45
0.50	0.25	0.30	0.35

Array Package Assembly Methodology

The package assembly process for BGA will vary somewhat do in part to the components complexity and performance criteria. The illustration shown in Figure 1 compares two common methods for establishing a die-to-substrate interface. The wire-bond method is most common because it typically utilizes the assembly service providers existing systems. For high performance applications the flip-chip (direct die attach) method is often preferred. For this methodology, however, the wafer must be processed to furnish bump contacts for mounting to the package substrate. The actual package substrate is typically fabricated in a rectangular strip format containing multiple packages for more efficient machine handling. Ball contact placement is performed as a final step after die attachment, wire-bonding and plastic molding or encapsulation process steps.

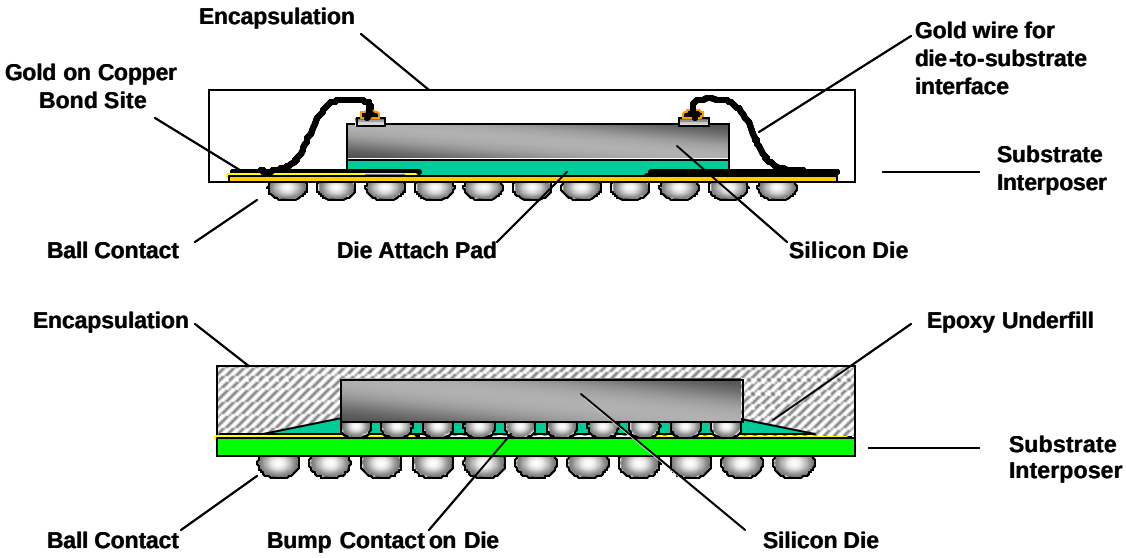

Figure 1 - This Detail Illustrates Two Common Assembly Process Methodologies for Single Die BGA and CSP Packaging

Alloy spheres of the desired size are attached either by gang placement machines or dispensed in mass with a stencil-like fixture. For companies doing development or for low-volume placement, simple template fixtures can be provided for precise ball positioning. The overall ball attachment process, however, is the same. To begin, liquid or paste flux is dispensed or printed onto the contact pattern and the ball contacts are deposited onto the flux material. The flux holds the balls in place during reflow soldering. Reflow soldering of the ball to the substrate is often performed in a nitrogen gas environment. The nitrogen gas environment keeps the solder balls and contact surfaces from oxidizing when heated. The solder balls reach a liquidus state during reflow soldering, promotes self-alignment (compensating for some ball misplacement during assembly).

The process for ball attach is not without some difficulty. BGA packages that adapt a reinforced resin based substrate, for example, are often prone to warping when exposed to temperatures required for solder attachment. The edges of the package tend to lift up or curve down when exposed to the high temperatures of reflow soldering and can severely disturb or interrupt the electrical interface between package and board during assembly. Larger packages (>20.0 mm) are more susceptible to warping than the smaller packages. The package warp is generally influenced by CTE mismatch between the packages' substrate, the mold compound and the silicon die inside. This problem can become more acute when the die is large, or when the package includes a large heat spreader. A number of companies have been able to avoid the material mismatch issue by adopting a package technology (see Figure 2) that allows the stresses to be buffered, reliving the direct strain on the solder ball-to-PCB interface.

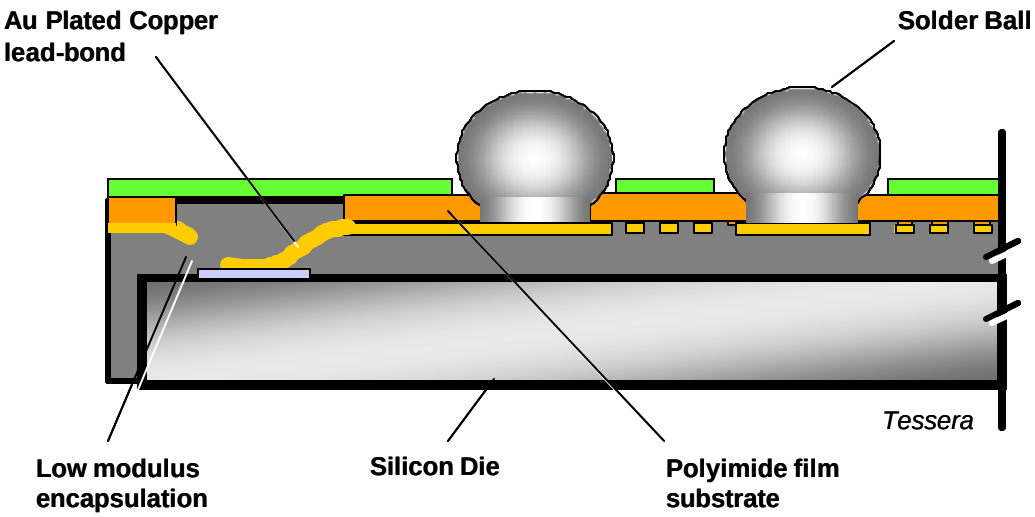

Figure 2 - The Thin, Die-Size µBGA® Lead-Bond Package Technology has been Engineered to Absorb the Physical Stresses Caused when Interfacing Materials With Radically Different Thermal Coefficient of Expansion

Circuit Routing Guidelines

The attachment site or land pattern geometry recommended for BGA devices is typically round, with the diameter adjusted to meet contact pitch and size variation. Establishing the correct land pattern for each device family is critical for assembly process control and finished product reliability. Companies developing products requiring higher component and circuit density may choose to modify or 'tailor' the land pattern geometry to reduce the attachment surface area but, reducing the surface area further may compromise product reliability. The designer may attempt to maximize the land pattern area and provide a land diameter equal to the nominal diameter of the ball contact as illustrated in Figure 3, however, that will contribute to a slightly greater collapse of the solder ball during reflow soldering. Users recommend that the diameter of the land should be no larger than the diameter of the land at the package interface, typically 20% smaller than the nominal diameter specified for the ball contact (see Table 3).

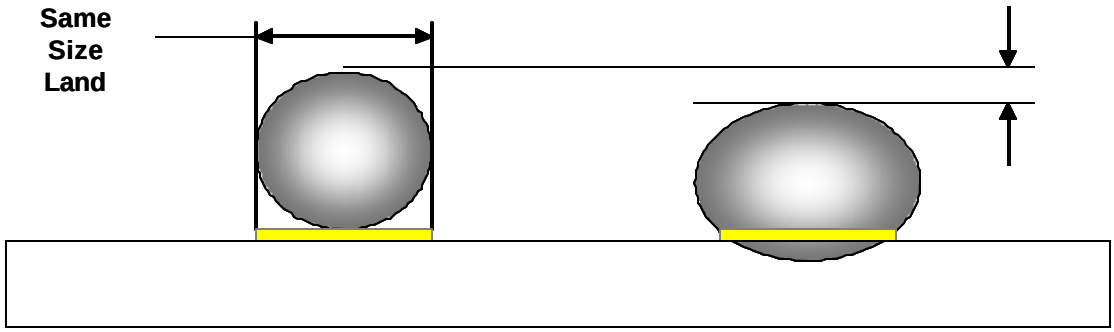

Figure 3 - Post reflow ball collapse between a ball contact on a land pattern that is equal in diameter

Table 3 - Recommended Land Size Reduction and Manufacturing Allowance for Land Size

Nom. Ball Diameter	Land Reduction	Land Diameter	Land Size Variation
0.75	25%	0.55	0.60 - 0.50
0.60	25%	0.45	0.50 - 0.40
0.50	20%	0.40	0.45 - 0.35
0.45	20%	0.35	0.40 - 0.30
0.40	20%	0.30	0.35 - 0.25
0.30	20%	0.25	0.25 - 0.20

Source: IPC-7095

The contact array for each device will typically be furnished with a common pitch and positioned symmetrically within the package outline as illustrated in Figure 4. In addition, the contact spacing dimensions are 'basic' and not subject to progressive tolerance variation. With the land pattern diameter and center-to-center spacing defined, the routing channels, or space between the land patterns can easily be calculated. The designer should not assume, however, that all devices that have the same contact pitch will be furnished with the exact same ball contact diameter. The industry standards allow the manufacturer to select from a range of variations to meet their specific requirements. The variations shown in Table 4, for example, are for the fine-pitch BGA family of packages.

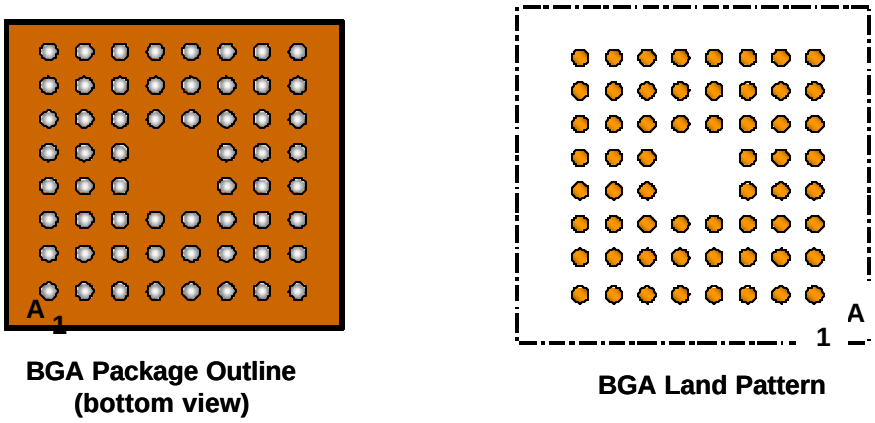

Figure 4 - BGA Package Contact Array will normally be Centered and Arranged in a Symmetrical Pattern within the Package Outline

Table 4 - Comparing the Contact Pitch Variations Allowed for FBGA and DSBGA, the Ball Contact Size Range and Recommended Land Pattern Geometry

Contact Pitch	Ball Diameter			Land Pattern	
(basic)	*Min.*	*Nom.*	*Max.*	*Min.*	*Max.*
0.50	0.25	0.30	0.35	0.25 - 0.30 mm	
0.65	0.25	0.30	0.35	0.25 - 0.30 mm	
0.65	0.35	0.40	0.45	0.35 - 0.40 mm	
0.80	0.25	0.30	0.35	0.25 - 0.30 mm	
0.80	0.35	0.40	0.45	0.35 - 0.40 mm	
0.80	0.45	0.50	0.55	0.40 - 0.50 mm	

After the land pattern has been defined the designer can begin planning the circuit routing strategy. Signal routing channels on the outer surface layers of the PCB are restricted by the space reserved between land pattern sites. Routing circuits to BGA devices with wider contact pitch will, of course, be less difficult and for those devices that are furnished with a depopulated array, circuit paths are less restrictive. For example, many of the lower I/O products (typical of memory devices), the circuit routing can be provided on the outer surface of the mounting structure. Circuit density for the miniature fine-pitch array device, however, is typically higher than that defined for the larger pitch plastic BGA. For the higher I/O devices with fine-pitch contact spacing, the inner or subsurface layer circuit routing should be considered for a majority of the signal paths because it will provide the most efficient interface between these more complex devices.

As a caution, the designer should keep in mind that, although companies furnishing components in a commodity market may supply a component with the same array pattern and pin assignment as another, the ball contact diameter may or may not be consistent. Companies supplying CSP packages have attempted to maintain a constant contact diameter for all fine-pitch applications, but, because the 0.65 mm and 0.80 mm contact pitch devices have been allowed two to three optional ball and contact diameter variations, the designer is advised to refer to the specific supplier specifications before establishing land pattern diameter. The land pattern geometry for some BGA device families may not provide spacing to clear more than one or two circuit paths (see Figure 5). Limiting the outer layers of the circuit board to only the attachment site and closely positioned via lands enables a more uniform routing pattern between devices and maximizes the ground plane area on the outer surface. Adapting finer lines and spaces, although it may reduce the need for added circuit layers, may prove to be more

costly due to the lower PCB fabrication yield. Table 5 compares the circuit routing conditions and limitations for fine-pitch BGA. Higher circuit routing density and micro-via fabrication techniques for manufacturing multilayer circuit boards are available, and, although these technologies are somewhat specialized, they should be considered when planning FBGA component attachment.

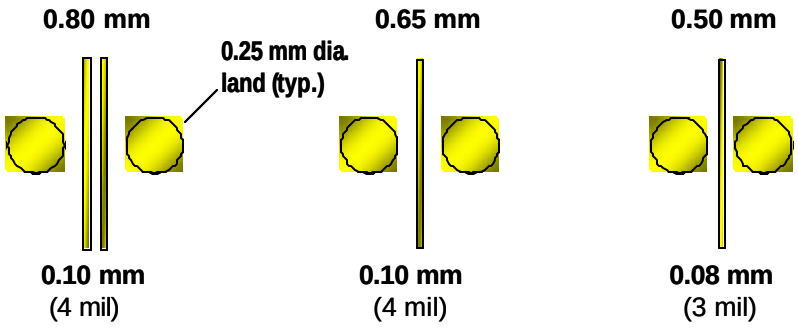

Figure 5 - Circuit Routing on the Outer Surface between Fine-Pitch BGA Lands will be limited to the Remaining Narrow Area between Contact Lands

Table 5 - The Above is based on Outer Layer Surface Routing Capability using 100 µm (4 mil) Lines and Spaces - Subsurface Routing will allow Finer Lines and Spaces

Contact Pitch	Land Diameter	Routing Space	Number of Conductors
0.80	0.40 mm	0.40 mm	1
0.80	0.35 mm	0.45 mm	2 *(tight)*
0.80	0.25 mm	0.55 mm	2
0.65	0.35 mm	0.25 mm	none
0.65	0.25 mm	0.40 mm	1
0.50	0.25 mm	0.25 mm	none

The designer should also be aware that when the BGA attachment site is defined by the etched copper land pattern, solder mask clearance will be a minimum of 0.075 mm from the contact land perimeter. When adapting a solder mask defined land pattern, however, it is necessary to increase land pattern diameter accordingly to ensure uniform mask coverage and will reduce the circuit routing path area significantly as illustrated in Figure 6. Solder mask openings for the FBGA and DSBGA with 0.65mm and 0.8mm contact pitch should be made 0.15 mm (6 mils) greater in size than the land pattern feature. Most user companies are specifying a mask that is clear of the land pattern but the mask material must cover the surface area between lands to help preventing solder bridging between one land and another. Recommended solder mask clearance for BGA and CSP lands are shown in Table 6.

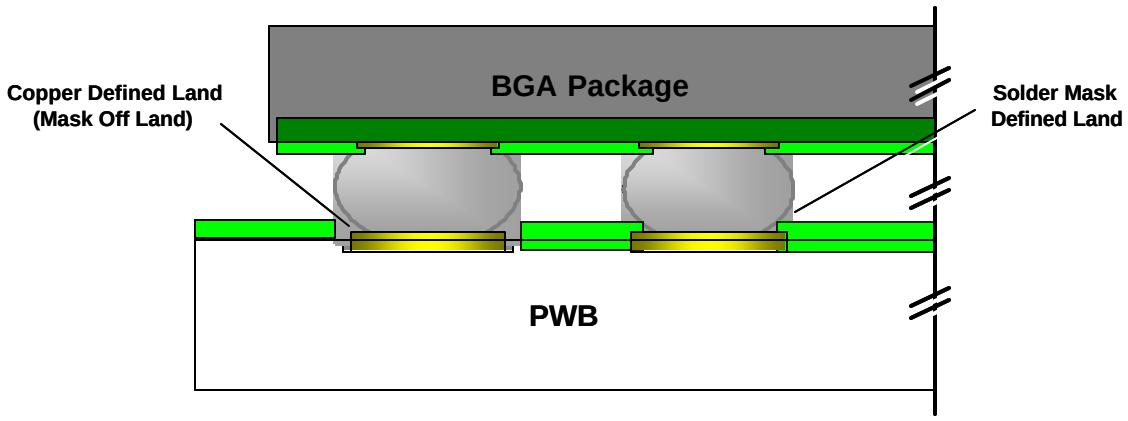

Figure 6 - When the Land Pattern is defined by Soldermask the Land Diameter must be Significantly Larger in Diameter than the Land without Soldermask, Reducing the Space Needed for Circuit Routing between Lands

Table 6 - Recommended Solder Mask Clearance for BGA and CSP Lands

Nominal Ball Diameter	Land Pattern Diameter	Solder Mask Opening
0.75 mm (.027")	0.65 - 0.75 mm	0.85 - 0.90 mm
0.60 mm (.023")	0.55 - 0.60 mm	0.70 - 0.75 mm
0.50 mm (.019")	0.45 - 0.50 mm	0.60 - 0.65 mm
0.45 mm (.018")	0.40 - 0.45 mm	0.55 - 0.60 mm
0.40 mm (.016")	0.35 - 0.40 mm	0.45 - 0.50 mm
0.30 mm (.012")	0.25 - 0.30 mm	0.35 - 0.40 mm

PCB Layout Planning

In regard to requirements and features needed for automated assembly processing, the designer will need to have a clear understanding of the process methodology and sequence. Basically, the surface mount assembly process begins with solder paste printing followed by package placement and mass reflow soldering. In volume assembly, automated systems with conveyor type handlers are used to transfer the board through each phase of the process. Because of the relatively small and often irregular outline of some electronic assemblies the printed circuit board substrate is likely to be furnished in a panel format, maximizing automated assembly efficiency. To accommodate automated assembly and post assembly handling, specific features must be furnished within the design. For vision assisted solder paste printing and component placement, chemically etched fiducials or optical targets must be present on the outer surface of the substrate. Component orientation will be governed by the package-to-package interface criteria, however, spacing between components must allow for inspection, and if warranted, rework and repair. Inspection for array packages is more difficult than lead-frame packaged devices but some capability for limited visual access does exist at each edge of the component. For more detailed recommendations on component clearances and inspection criteria for BGA refer to IPC-7095.

Summary and Conclusion

Array packaging provides the designer with an opportunity to achieve a high level of component density and will likely improve both product performance and assembly efficiency. This is because all of the contacts are within the components outline and the packages can be placed onto the host circuit board with minimal clearance, minimizing circuit routing length. In addition, routing between the array packaged devices can originate from via features within the outline without fanning out to via hole and pad features outside the components perimeter (common for lead-frame packed ICs).

There should be no reservations regarding the use of BGA and CSP devices. The infrastructure is well established to support both the BGA and CSP packaging requirements and most semiconductor and service providers have achieved high yield manufacturing process capability. Assembly processes for attaching the BGA and CSP devices has proved to be repeatable and predictable for both low and high volume manufacturing. Assembly service companies and product developers are successfully utilizing automated SMT assembly, and many have found that when the devices are furnished in tape-and-reel packaging, machine utilization can be further enhanced. Assembly using array packaging is not unlike the processes already widely used for surface mount and fine-pitch technology. If a company is already achieving acceptable assembly yields for SMT, it should not require additional resources or new methodology to implement array package technology.

The choice between BGA and CSP packaging methodologies depends upon the ability of the device to qualify for the specific product use environment criteria. The material system developed for the component will be expected to withstand the physical expansion differential between die and PC board. If the components material set cannot absorb the stresses created within the operating environment, the use of epoxy underfill may be required to stabilize the part after mounting.