





**Mathematical Model** 

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### **Dimensioning Concepts**

Concepts used for this analysis consider the assembly and /attachment requirements as their major goal

Data sheets for components or dimensions for land patterns on boards may use other dimensioning concepts, however, the goal is to combine all concepts into a single system

The system allows for tailoring of these concepts for robust process performance

#### **Dimensioning Requirements**

- All dimensions are basic (nominal)
- Limits of size control form as well as size
- Perfect form is required at maximum dimensions
- Datum reference and position tolerances apply at maximum dimensions and are dependent on feature size

#### **Dimensioning Requirements**

- Position dimensions originate from maximum dimensions
- Tolerances and their datum references other than size and position apply regardless of feature size (rfs)

Interpretations are per ASME Y14.5
(IPC-2615)

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#### **Profile Tolerancing Example**



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### **Component Tolerancing**

 Component manufacturers are responsible for the dimensioning and tolerancing of electronic components

Their concepts have been converted to a functional equivalent using the profile tolerancing method

 All components are shown with their basic dimensions as limit dimensions (maximum or minimum size)



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#### **Component Tolerancing**

Profile tolerances are unilateral, and are described to reflect the best condition for solder joint formation

Component dimensions are evaluated using the surfaces of the termination or component lead involved in the formation of an acceptable solder joint

Component manufactures provide nominal dimensions which are converted to maximum and minimum requirements

### C1206 Capacitor example



3.2 ± 0.2 mm

Manufacturers dimensions and tolerances (maximum length of part is 3.4 mm).

Part shown with length at "least material condition", and profile tolerance to indicate maximum range of component length at 3.4 mm.

Land pattern with dimension  $\mathbb{Z}$  at "maximum material condition". Profile tolerance of part (0.2 X 2), plus profile tolerance of land pattern (0.05 X 2) plus placement accuracy (0.1 diameter of true position) are considered in determining the proper dimension for  $\mathbb{Z}$ , plus the desired toe fillet.



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### Heel to Heel Dimensions

The outer dimensions of leaded or even leadless components are usually easy to determine, these are readily available from the component manufacturer

The inner (heel-to-heel) dimensions are not provided and are more difficult to determine

Inner dimensions must be derived by subtracting the sum of the dimensions of the leads (with their inherent tolerances) from the overall dimensions of the part.

#### **Gull Wing Leaded SOIC**



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Manufacturing dimensions of SOIC's

Manufacturers dimensions and tolerances converted to profile dimensions, with S at "maximum material condition".

Note: if S is not provided by the component manufacturer it may be determined by subtracting T terminal dimensions from the length.

S = [-2] MMC = MMC = LMC O = 0.05 Fabrication tolerance equals 0.1 mm



### **Dimension "S" Determination**

- The inner dimensions between heel fillets on opposing sides are the most important
- Inner dimensions are derived by:
  - establishing the maximum width of the component as measured from lead termination to lead termination. (This dimension is shown as "L," and is provided by the manufacturer).



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#### **Dimension "S" Determination**

establish the minimum amount of the lead length as measured across the component"footprint", from heel to toe for gull-wing leads. (This is "T," and is provided by the manufacturer)

subtract twice the minimum lead length of (T) from the maximum overall component length of (L) to arrive at the maximum length inside the leads across the length of the component (dimension between opposing heels)



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#### **Dimension "S" Determination**

Including the tolerances on dimensions (L) and (T) will yield the minimum dimension between opposing heels. This signifies worstcase tolerance analysis.

 Three sets of tolerances are involved in the analysis described. These include tolerances on the overall component, plus the tolerances for the lead on each end



#### Root Mean Square (RMS)

Recommended method to determine the statistical impact is to summarise the squares of the tolerances and take the square-root of their sum (RMS)

■ RMS tolerance accumulation = where  $\sqrt{(L_{tol})^2 + 2(T_{tol})^2}$ 

 $L_{tol} = L_{max} - L_{min}$ 

 $T_{tol} = T_{max} - T_{min}$ 



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#### System Equations for Z

 System concepts assume target values of parts and land patterns are maximised for solder joint formation
minimum outer dimensions of components
outer dimensions of land patterns at

maximum size







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Total Tolerances

- C is the the unilateral profile tolerance(s) for the component
- F is the the unilateral profile tolerance(s) for the board land pattern
- P is the the diameter of true position placement accuracy to the centre of the land pattern



#### Land Pattern Equations

- $Z_{max} = L_{min} + 2J_T + \sqrt{C_L^2 + F^2 + P^2}$
- $G_{min} = S_{max} 2J_H \sqrt{C_L^2 + F^2 + P^2}$
- $X_{max} = W_{min} + 2J_{S} + \sqrt{C_{L}^{2} + F^{2} + P^{2}}$

#### where

- Z is the overall length of land pattern;
- G is the distance between lands of the pattern;
- *X* is the width of land pattern;



#### Table 3–4 Tolerance Analysis Elements for Chip Devices

<b>Tolerance Element</b>	Detailed Description
Component Tolerance	The difference between the MMC and the LMC of each component dimension, length, width and distance between electrodes or leads. This number is the "C" tolerance in the equations.
Board Tolerance	The difference between the MMC and the LMC of each land pattern dimension. This number is "F" tolerance in the equations.
Positional Accuracy	0.1 – 0.2 mm DTP
Toe Fillet	0.4 – 0.6 mm
Heel Fillet	0.0 – 0.2 mm
Side Fillet Width	-0.02 - 0.02 mm

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#### **Component Characteristics**

- L is the overall length of component;
- S is the distance between component terminations;
- W is the width of the lead or termination;



#### FOR OPTIMUM (BEST) FILLET

• WORSE CASE ANALYSIS CONSIDERS COMPONENT BASIC DIMENSIONS AT MAXIMUM AND THE LAND AT ITS MINIMUM

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### Solder Joint/Land Protrusion

■ J is the desired dimension of solder fillet or land protrusion;

- J<sub>h</sub> is the solder fillet or protrusion at heel;
- J<sub>s</sub> is the solder fillet or protrusion at side;





	Toler	ance		Solder Joint											
RIP	Assum (m	m)		Heel	el 1 and 2 (mm) Toe 1 and 2 (mm)			Side 1 and 2 (mm)							
No.	F	Р	C_	J <sub>∺1</sub> min	J <sub>H1</sub> max	J <sub>∺₂</sub> min	J <sub>H2</sub> max	$C_{\rm s}$	J <sub>⊤1</sub> min	J <sub>⊺1</sub> max	$J_{T_2}$ min	$J_{T_2}max$	Cw	J <sub>s</sub> min	J <sub>s</sub> max
810A	0.10	0.10	0.25	0.53	0.67	0.45	0.60	0.75	-0.48	-0.10	-0.40	-0.02	0.20	0.01	0.14

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#### **RMS Constituents**

#### • C is the component tolerance

- $rac{} C_L$  is the tolerance on component length;
- C<sub>S</sub> is the tolerance on distance between component terminations;
- $rac{\sim} C_W$  is the tolerance on component width;
- F is the printed board fabrication (land pattern geometric) tolerances
- P is the part placement tolerance (placement equipment accuracy)







# Ribbon Leads greater than 0.625



### Flat ribbon L and gull-wing leads (greater than 0,625 mm pitch) (unit: mm)

Land pattern characteristics	Maximum Level 1	Median Level 2	Minimum Level 3
Toe-land protrusion	0,8	0,5	0,2
Heel-land protrusion	0,5	0,35	0,2
Side-land protrusion	0,05	0,05	0,03
Courtyard excess	0,5	0,25	0,05
Round-up factor	Nearest 0,5	Nearest 0,5	Nearest 0,05





### Ribbon Leads less than 0.625



### Flat ribbon L and gullwing leads (less than or equal to 0,625 mm pitch) (unit: mm)

Land pattern characteristics	Maximum Level 1	Median Level 2	Minimum Level 3
Toe-land protrusion	0,8	0,5	0,2
Heel-land protrusion	0,2	0,2	0,2
Side-land protrusion	0,0	0,0	0,0
Courtyard excess	0,5	0,25	0,05
Round-up factor	Nearest 0,5	Nearest 0,05	Nearest 0,05







#### Round or flattened (coined) leads (unit: mm)

Land pattern characteristics	Maximum Level 1	Median Level 2	Minimum Level 3
Toe-land protrusion	1,0	0,65	0,2
Heel-land protrusion	0,5	0,35	0,2
Side-land protrusion	0,1	0,1	0,1
Courtyard excess	0,5	0,25	0,05
Round-up factor	Nearest 0.5	Nearest 0.5	nearest 0.05





J Leaded Parts



J leads (unit: mm)

Land pattern characteristics	Maximum Level 1	Median Level 2	Minimum Level 3
Toe-land protrusion	0,2	0,2	0,2
Heel-land protrusion	0,8	0,6	0,4
Side-land protrusion	0,1	0,05	0,0
Courtyard excess	1,5	0,8	0,2
Round-up factor	Nearest 0,5	Nearest 0,5	Nearest 0,05





### Rectangular Square end Terminations



### Rectangular or square-end components (ceramic capacitors and resistors) (unit: mm)

Land pattern characteristics	Maximum Level 1	Median Level 2	Minimum Level 3
Toe-land protrusion	0,6	0,4	0,2
Heel-land protrusion	0,0	0,0	0,0
Side-land protrusion	0,0	0,0	0,0
Courtyard excess	0,5	0,25	0,05
Round-up factor	Nearest 0,5	Nearest 0,05	Nearest 0,05





#### Metal Electrical Face



#### Cylindrical end cap terminations (MELF) (unit: mm)

Land pattern characteristics	Maximum Level 1	Median Level 2	Minimum Level 3
Toe-land protrusion	1,0	0,4	0,2
Heel-land protrusion	0,2	0,1	0,0
Side-land protrusion	0,2	0,1	0,0
Courtyard excess	0,5	0,25	0,05
Round-up factor	Nearest 0,5	Nearest 0,5	Nearest 0,05





## Bottom Only Terminations



#### Bottom only terminations (unit: mm)

Land pattern characteristics	Maximum Level 1	Median Level 2	Minimum Level 3
Toe-land protrusion	0,2	0,1	0
Heel-land protrusion	0,2	0,1	0
Side-land protrusion	0,2	0,1	0
Courtyard excess	0,25	0,1	0,05
Round-up factor	Nearest 0,5	Nearest 0,05	Nearest 0,05





#### Leadless Chip Carriers



#### Leadless chip carrier with castellated terminations (unit: mm)

Land pattern characteristics	Maximum Level 1	Median Level 2	Minimum Level 3
Toe-land protrusion	1,5	1,25	1,0
Heel-land protrusion	0,4	0,2	0,1
Side-land protrusion	0,0	0,0	0,0
Courtyard excess	1,5	0,8	0,2
Round-up factor	Nearest 0,5	Nearest 0,5	Nearest 0,05





#### **Butt Joints**



#### Butt joints (unit: mm)

Land pattern characteristics	Maximum Level 1	Median Level 2	Minimum Level 3
Toe-land protrusion	1,0	0,8	0,6
Heel-land protrusion	1,0	0,8	0,6
Side-land protrusion	0,3	0,2	0,1
Courtyard excess	1,5	0,8	0,2
Round-up factor	Nearest 0,5	Nearest 0,5	Nearest 0,05





Inward L shaped Leads



#### Inward L shaped ribbon leads (unit: mm)

Land pattern characteristics	Maximum Level 1	Median Level 2	Minimum Level 3
Toe-land protrusion	0,1	0,1	0,0
Heel-land protrusion	1,0	0,5	0,2
Side-land protrusion	0,1	0,1	0,1
Courtyard excess	0,5	0,25	0,05
Round-up factor	Nearest 0,5	Nearest 0,5	nearest 0,05





### Flat Lug Leads



#### Flat lug leads

Land pattern characteristics	Maximum Level 1	Median Level 2	Minimum Level 3
Toe-land protrusion	1,0	0,8	0,5
Heel-land protrusion	0	0	0
Side-land protrusion	1,0	0,5	0,3
Courtyard excess*	2,0	1,5	1,0
Round-up factor	Nearest 0,5	Nearest 0,5	Nearest 0,05
* Depends on thermal rec	nuirements	÷	

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#### **Design Considerations**

- Land pattern concepts
- Component selection
- Mounting substrate design
- Assembly methods
- Method of test
- Phototool generation
- Meeting solder joint requirements
- Stencil fixture requirements
- Providing access for inspection
- Access for rework and repair



#### Manufacturing Allowance

Manufacturing allowance must be considered in the design process

The courtyard represents the starting point of the minimum area needed for the component and the land pattern

Manufacturing, assembly and testing representatives should assist in determining the additional room needed to accommodate placement, testing, modification and repair





#### **BGA Layout Considerations**







#### The BGA Substrate

- Surface redistribution layers require very aggressive layout rules
- Opposing sets of lands must be connected by the package substrate
- One or more interconnecting lines between two adjacent bonding lands
- Must access multiple rows of the interior I/O lands for connection to the vias or PTHs for eventual connection to the solder balls on the bottom side





#### Micro Processor Requirements

- 40 60% of their I/O dedicated to power and ground
- Signal I/O escape wiring, and their interconnection to other high I/O packages, requires HDI Boards
- I/O on a chip increases the body size of the single chip package
- multichip module packaging solution considered as an alternative.



#### Land Patterns and Circuit Board Considerations

Components are soldered to the board on the surface mount lands
 Lands are areas of copper about the shape and size of the lead

- Land pattern design is critical-affects:
  - solder defect rate
  - Cleanability and testability
  - repair/rework
  - solder joint's reliability.



- Two groups of BGAs pitches
   regular 1.50, 1.27, and 1.00 mm
   fine pitch 0.80, 0.75, 0.65, 0.50, 0.40, 0.30 and 0.25 mm
- Most popular pitch is 1.27 followed by 1.00, 0.80, 0.75, and 0.50 mm
- At the moment, very few component manufacturers are providing parts with 1.5 mm pitch, pressure is on form factor
   Pitch plays a large role.

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Ball Diameter Sizes for PBGAs

Nominal Ball Diameter (mm)	<b>Tolerance Variation (mm)</b>	Pitch (mm)
0.75	0.90 - 0.65	1.5, 1.27
0.60	0.70 - 0.50	1.0
0.50	0.55 - 0.45	1.0, 0.8
0.45	0.50 - 0.40	1.0, 0.8, 0.75
0.40	0.45 - 0.35	0.80, 0.75, 0.65
0.30	0.35 - 0.25	0.8, 0.75, 0.65, 0.50
0.25	0.28 - 0.22	0.40
0.20	0.22 - 0.18	0.30
0.15	0.17 - 0.13	0.25

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#### Land Approximation

Component manufacturers and board designers are encouraged to reduce the land size by some percentage of the nominal ball diameter

Reduction is based on the original ball size

 Used to determine the average land
 Manufacturing allowance for land size has been determined to be 0.1 mm between MMC and LMC



#### Big Vs. Small Land and Impact on Routing

Diameter of the solder land can affect reliability of solder joints and also the routing of conductors

Land diameter is usually smaller than the ball diameter of the BGA

Land size reduction of 20 to 25% provides reliable attachment criteria

Larger the lands, the less room for routing between lands.



#### Land Pattern Approximation

Nominal Ball Diameter (mm)	Reduction	Nominal Land Diameter (mm)	Land Variation (mm)
0.75	25%	0.55	0.60 - 0.50
0.60	25%	0.45	0.50 - 0.40
0.50	20%	0.40	0.45 - 0.35
0.45	20%	0.35	0.40 - 0.30
0.40	20%	0.30	0.35 - 0.25
0.30	20%	0.25	0.25 - 0.20





Two basic types of solder lands used for BGA packages Solution Nonsolder mask defined (NSMD) Solder mask defined (SMD) NSMD lands are copper defined solder mask clearance around land SMD lands have solder mask overlapping the copper land

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# **TYPE I - Tented**

Tented Via (Type 1) Via) - A via with a mask material (typically dry film) applied bridging over the via wherein no additional materials are in the hole. It may be applied to A via covered with dry film soldermask; the via is not filled. When tenting from both sides there may be issues with trapped air that expands during mass soldering.



Type 1 Single-Sided



Type 1 Double-Sided



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# <u>TYPE II - Tented and</u> <u>Covered</u>

 Tented and Covered Via (Type II Via) - A Type I via with a secondary covering of mask material applied over the A via covered with dry film and the LPI soldermask; the via is not filled. Just like Type 1 when tenting from both sides there may be issues with trapped air that expands during mass soldering.



**Type II Single-Sided** 



**Type II Double-Sided** 

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# **TYPE III - Plugged**

Plugged Via (Type III Via) - A via with material applied allowing partial penetration into the via. It may be applied from either one side or both sides During soldermask

During soldermask application the via is flooded with soldermask. The via is partially filled. Chemical entrapment is a major concern.



**Type III Single-Sided** 



**Type III Double-Sided** 



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# <u>TYPE IV - Plugged and</u> <u>Covered</u>

Plugged and Covered Via (Type IV Via) - A Type III via with a secondary covering of material applied over the via.



Type IV Single-Sided

An additional operation which is done independent of soldermask application on one or both sides of the via. The via is partially filled. When capping from both sides there may be issues with trapped air that expands during mass soldering.



**Type IV Double-Sided** 



## **TYPE V - Filled**

 Filled Via (Type V Via)
 A via with material applied into the via targeting a full

encapsulation of the

penetration and

hole

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An additional operation which is done independent of soldermask application. The via is filled with a non-conductive material.

# <u>Type VI - Filled and</u> <u>Covered</u>

 Filled and Covered Via (Type VI Via) - A Type V via with a secondary covering of material (liquid or dry film soldermask) applied over the via. It may be applied from either one side or both sides.

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# <u>Type VII - Filled and</u> <u>Capped</u>

Filled and Capped Via (Type VII Via) - A Type V via with a secondary metallized coating covering the via. The metallization is on both sides











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# Effect of Having Solder Mask Relief Around the BGA Lands of the Board

#### Soldermask Relief Around Land

~0 mm

Top view of land illustrating increase of effective land diameter due to trace connections



0.75 mm



Cross-sectional view of land with solder ball joint illustrating the solder wetting down the edge of the land when there is solder mask relief away from the land edge

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# Via-in-Pad and Impact on Reliability

Via-in-Pad (through-hole via, capped on bottom of the board) for BGA Lands cause voids in the BGA solder joints, which may impact reliability.

Current data indicate that, for the standard 25 - 35 mm package with 0.75 mm balls, there is no reliability risk from voids. Accelerated aging tests have been performed and the failure rate was statistically equivalent to standard dog bone designs. It appears that void consistency is

# <u>Cross Section of 0.75mm Ball</u> with Via-in-Pad Structure



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### After Printing Paste, and BGA Placement



## **During Reflow Soldering**









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#### CALCULATION STEPS

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Please enter information in *all* of the open fields. When you are done, press CALCULATE. If numeric information has been filled in all of the fields, press the NEXT button. NOTE: Depending on the size of your screen and your screen settings, you may have to scroll to the right to see all of the data fields.

Land Pattern Calculations																
Z	Z	Z						X	X	X			Clr	C/C	D1	D2
Min	Max	Max	Z Adj	G Max	G Min	G Min	G Adj	Min	Max	Max	X Adj	Y Ref	Ref	Ref	Ref	Ref
Fin	Fin	Cal	Fact	Fin	Fin	Cal	Fact	Fin	Fin	Cal	Fact	Cal	Cal	Cal	Cal	Cal
36.17	36.27	36.27		32.135	32.035	32.035		0.334	0.434	0.434		2.117	0.216	34.152	29.25	29.2

CALCULATE





STEP 3 - Microsoft Internet Explorer		- 8 ×
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If you are satisfied with the measurements listed click FINISH, otherwise click PREVIOUS to go back a step and modify your Adjustment Factors.

Solder Joint Analysis												
	Toe			Heel		Side						
Design Goal	Statis Min	Statis Max	Design Goal	Statis Min	Statis Max	Design Goal	Statis Min	Statis Max				
0.4	0.3	0.56	0.5	0.25	0.585	0	-0.15	-0.043				

PREVIOUS FINISH

🙆 Done

Start

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Z1 (Max)

Z2 (Max)

G1 (Min)

G2 (Min)

X (Max)

Y (Ref)

D1

D2

E

PIN1

PIN2

PLMT GRID (mm)

C/C1 (Ref)

C/C2 (Ref)

Finished Land Pattern Dimensions

IPC

12.80

16.80

9.6

13.6

0.30

1.60

11.20

15.20

12.50

0.50

18

26

14.00 X

18.00

Modify

8.50

elcome to IPC

We connect the electronics industry with ideas, information, and each other **9**2

#### SITE MAP CONTACT US SEARCH

CFP Chip Capacitors Chip Resistors CQFP DIP

Inductors LCC MELF

PLCC (Rectangular)

PLCC (Square) PQFP

SOD 123 SOIC

SOJ SOP

SOT 143 SOT 223

SOT 23 SOT 89 SQFP/QFP

(Rectangular) SQFP/QFP (Square) SSOIC

Tantalum Capacitors TO 252/ TO 268

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Start

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IPC

Min.

12.60

16.60

9.8

13.8

0.35

1.41

11.19

15.19

8.50

12.50

0.50

18

26

12.70 X

16.70

Modify

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Median

13.20

17.20

9.8

13.8

0.35

1.71

11.49

15.49

8.50

0.50

18

26

13.70 X

17.70

Modify

12.50

Max.

13.50

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9.6

13.6

0.50

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11.54

15.54

8.50

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18

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14.50 X

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#### IPC-735x PCB Libraries Navigator Wizard - Version 2.6 [Bld 109]

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IPC







## **Land Patterns**











### **Land Patterns and Courtyards**



<u>Maximum</u>



<u>Nominal</u>







# **Conclusions**

- Mathematical models provide a method for process control
- Development of standards avoid duplication efforts
- New software code provides a neutral format for libraries
- Methodology is transportable for new or unique components
- Standard library concepts will enhance testing capabilities