IPC 2610 – Documentation Package

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Introduction

In the beginning….

There was Gerber. Boards were built. It was good.

Then came Computer Aided Design …

With the advent of CAD and CAM tools, the need arose for a more complete method of data transfer. As layer count increased, the number of files increased. As trace size and spacing began to decrease, the Gerber file size increased. The need for a better method of Data Transfer was recognized. The search for the Data Transfer Solution began.

IPC develop the GenCAM Initiative with a program to address the Data Transfer Solutions (DTS) with DTS '97, DTS'98, DTS'99, DTS'00, DTS '01, DTS '02… The idea behind the DTS was to parse large data files into an ASCII formatted, process oriented segmented file. At the same time, Valor was developing the ODB+ format for its tools. And the industry used Gerber because it was okay.

Oh no - the Data Format Wars ...

The industry press created the image of these two formats battling each other. Lots of articles were written on who would win the war. This caused a lot of the industry to remain in neutral territory waiting to see who would win. But now the inadequacies of Gerber were hurting the PCB industry.

NEMI offered to broker a "peace" plan by bringing together IPC and Valor to develop a plan that would serve the needs of the PCB industry. Both formats, GenCAMX and ODB++(X) were submitted to the NEMI VFIIP committee for the purpose of developing a single XML-based industry standard.

Through an industry effort of cooperation, IPC-2581 was released in February 2004. This format takes the best of its predecessors for a robust XML data transfer solution. It is available with the XML schema for free download from http://webstds.ipc.org/.

The dawning of a new era … Intelligent Data Transfer … and it is good (almost)!

How does a designer document Intelligent Data? If the Data is placed on a formatted drawing, the intelligence is lost. What pieces of the Documentation Package need to be modified? How can the designer prevent sending redundant information?
Since the beginning, documentation packages have included:

- Fabrication Drawings
- Assembly Drawings
- Bill of Materials
- Schematic or Logic Diagrams
- Wiring Diagrams
- Specification Control Drawings
- Electronic Data
- Mechanical Drawings

This will not change now that we are moving into the era of Intelligent Data Transfer. The human still needs to know what is being transferred and to who is it being transferred.

In 2004, IPC approved the creation of a new IPC standard 2610 to deal with the "requirements for the documentation of electronic equipment, and the methodology used for revision control and configuration management of the information. The descriptions apply to the entire document set used to define and maintain the electronic product. The requirements pertain to both hard copy and electronic data descriptions." (From the Proposal for IPC-2611, PIN document, submitted February 2004.)

IPC-D-325 being revised This paper will discuss the current information being included in the IPC-2611 Generic Requirements for Electronic Product Documentation.

Document of Intelligent Data

Minimum Drawing Requirements

The documentation of a printed board assembly consists of several drawing types that are included or referenced in the documentation package.

All drawings are not always supplied to the fabricator or to the assembly company; however, the designer must have a good understanding of the minimum information necessary to convey the design intent.

IPC-2610 Documents

IPC-2611	Generic Requirements for Electronic Product Documentation
IPC-2612	Sectional Requirements for Electronic Diagramming Documentation (Schematic and Logic Descriptions)
IPC-2613	Sectional Requirements for Assembly Documentation (Electronic Printed Board and Module Assembly Descriptions)
IPC-2614	Sectional Requirements for Board Fabrication Documentation (Printed Circuit board Description Including Embedded Passives)
IPC-2615	***Sectional Requirements for Dimensions and Tolerances*** ***(Released July 2000)***
IPC-2616	Sectional Requirements for Electrical and Mechanical Part Descriptions (Specification and Source Control Part Descriptions)
IPC-2617	Sectional Requirements for Discrete Wiring Documentation (Wire harness, Point to Point and Flexible Cable Descriptions)
IPC-2618	Sectional Requirements for Bill of Material Documentation (Complete Listing of Parts, Materials, and Procurement Documents)

Terms & Definitions

Data	Intelligent information used directly by machine in order to accomplish a particular manufacturing event.
Drawings	Hard copy or un-intelligent documentation (example pdf etc.) to which all formatting criteria applies.
Supplier	The organization or company responsible for providing the goods and/or services required to produce an electronic product, which includes physical items as well as intellectual/software characteristics and is documented as either user procurement, supplier data or contractual agreements.
*User	The individual, organization, company or agency responsible for the procurement of electrical/electronic hardware, and having the authority to define the class of equipment and any variation or restrictions (i.e., the originator/custodian of the contract detailing these requirements).
JISSO	This term describes the interface and solution technology between user and suppliers for Interconnecting, assembling, packaging, mounting and integrating system design. Jisso concepts contain both functional and physical technology. It originated in Japan.

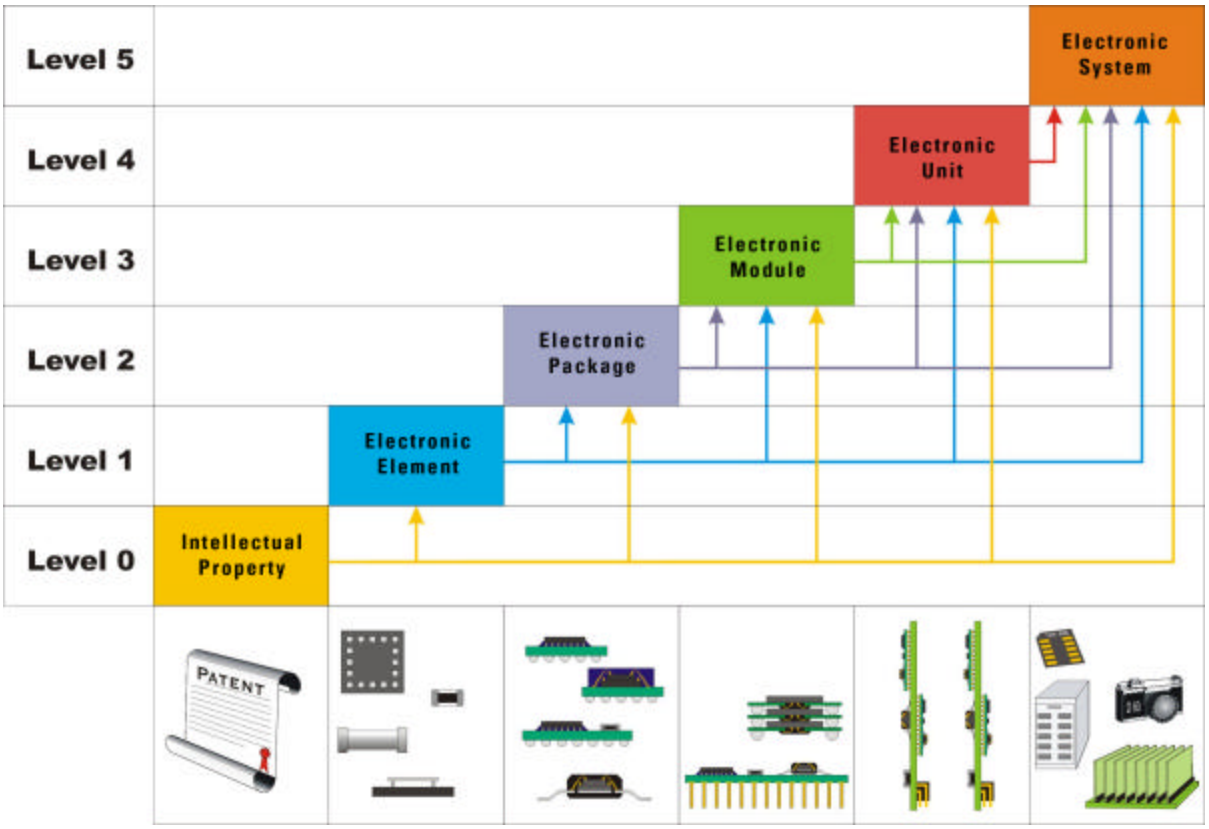

Figure 1 - JISSO Level Hierarchy

Jisso Level 0	Intellectual Property The intellectual property of an item pertains to the idea or intelligence imported or described in a formal document, design entity or patent disclosure. The information may be in hard or soft copy and can include computer code or data format as a part of the descriptive analysis. The characteristics are described as to their physical, chemical, electrical, mechanical, electromechanical, environmental, and/or hazardous properties
Jisso Level 1	Electronic Element Bare die or discrete components (resistor, capacitor, diode, transistor, laser), with metallization or termination ready to be mounted This can be an IC, or discrete electrical, optical or M EMS element. Individual elements cannot be further reduced without destroying their stated function.
Jisso Level 2	Electronic Package A container for an Individual Electronic Element or Elements which protects the contents and provides terminals for making connections to the rest of the circuit. The Component Package outline is generally standardized. The Component Package may function as electronic, optoelectronic, or Micro-Electro-Mechanical- Systems, and may in the future include Bio-electronic sensors.
Jisso Level 3	Electronic Module A sub-assembly with functional blocks which consist of Individual Electronic Elements and /or Component Packages. An individual module having an application specific purpose including Electronic, Optoelectronic or Mechanical (MEMS). The module generally provides protection of its elements and packages, depending on the application.
Jisso Level 4	Electronic Unit A group of functional blocks that have been designed to provide a single or complex function needed by a system in order for the system to serve a specific purpose. The Electrotechnical Assembly may consist of Electronic Elements, Component Packages and/or Application Specific Modules. The function of the Electrotechnical Assembly may be electronic, optoelectronic, electromechanical, or mechanical or any

	combination thereof. The function may in the future include bio-electronic applications.
Jisso Level 5	Electronic System A completed, market ready, unit dedicated to combining and interconnecting functional block(s). The functional block(s) generally consist of Electrotechnical Assemblies, but may also include Application Specific Modules, Component Packages or Electronic Elements. The System Product may include the cabinetry, the backplane into which the Assemblies, Modules, Packages or Elements are inserted and the cabling (electrical, optical, or mechanical) needed to interconnect the total functional block(s) into a configured system.

IPC-D-325 Types of Documentation Packages

In IPC-D-325, there were 3 Classes for the documentation types: A, B and C.

Class A (Minimal Documentation) was intended for internal use. Most of the layout and artwork was in hard copy or NC format. It requires a great deal of coordination between the design and manufacturing teams. Class A documentation requires the use of a manufacturer that can produce a functional product from the information supplied

Class B (Moderate Documentation) contains the complete board description without the manufacturing allowances and includes the parts list and assembly drawing. CAD data on conductor routing describes the interconnectivity of the circuit and is used to derive electrical test data. Class B documentation requires working with a manufacturer and assembly company that has a strong CAD/CAM background and an understanding of what the designer expects.

Class C (Full Documentation) is a complete procurement package that may be sent to multiple suppliers with each producing an identical part. The documentation package includes the master drawing, the assembly drawing; bill of material (BOM); schematic or logic diagram; test specs; artwork in hard copy and electronic form; and an electronic description of the design. An optional panel layout may also be included, especially if the assembly is to be built in panel format

Grades

There are three grades of documentation being defined in the IPC-2610 series. A specific grade shall consist of a letter to define the differences between hard copy and electronic data, and a number that defines the completeness of the documentation procurement package. The following characteristics apply and become a requirement of all the IPC-2610 sectional standards. (See Figure 2)

Grade A documentation is considered Hard Copy Documents and includes dimensionally stable Film.

Grade B documentation is a mixture of Electronic data and hard Copy. The electronic documentation may be intelligent or unintelligent description files such as PDF views. The documentation may be in drawing format and the electronic data may be formatted or unformatted data depending on grade hierarchy.

Grade C documentation consists of intelligent electronic data. The information may be in an industry standard electronic format or an electronic supplier derivative. The completeness of the information is dependant on grade hierarchy.

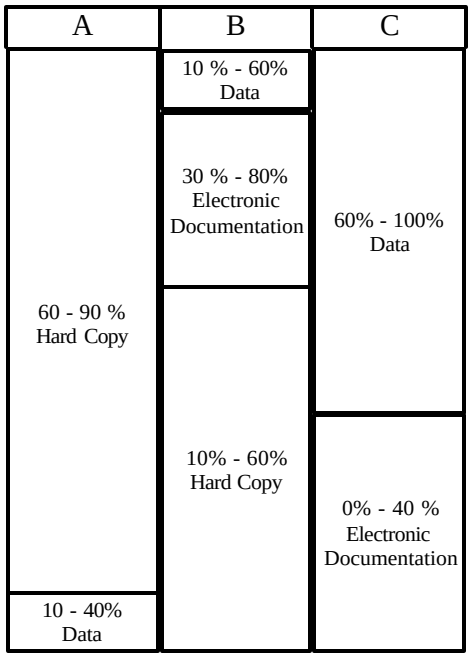

Figure 2 - Documentation Package Grade Requirements

Completeness Criteria

IPC-2611 defines a completeness criterion that corresponds to the IPC-2581 format criteria (See Table 1). Currently most boards are built using documentation packages which are Grade B2 or B3

Two examples of current documentation packages are:

Grade B2: Drawing notes in PDF file, Preliminary Bill of Material (Excel spread sheet or CAD report). Photo description PDF or DXF, IGIS, IDS, Board dimensions PDF, Plotted data descriptions PDF, Hole size information, product description, surface finish, rough draft documentation. Gerber, Drill file

Grade B3: Hard copy or electronic versions in PDF or other printable forms with all document functions addressed in Final documentation form. All files and/or hard copy are completely formatted, and approved. Panelization data or drawing. (PDF file or hard copy)

Name	Full	Design			Fabrication			Assembly			Test		
		1	2	3	1	2	3	1	2	3	1	2	3
Hierarchical layer/stack instance files	Y	N	Y	N	N	N	N	N	N	N	N	N	N
Hierarchical conductor routing files	Y	N	Y	N	N	N	N	N	N	N	N	N	N
BOM (Components and Materials)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y
AVL (Components and Materials)	Y	N	Y	Y	N	Y	Y	Y	Y	Y	N	N	Y
Component Packages	Y	Y	Y	Y	N	N	Y	Y	Y	Y	N	Y	Y
Land Patterns	Y	N	Y	Y	N	N	Y	N	Y	Y	N	Y	Y
Device Descriptions	Y	Y	Y	Y	N	N	N	N	N	Y	N	N	Y
Component Descriptions	Y	Y	Y	Y	N	N	N	Y	Y	Y	N	Y	Y
Soldermask; Solder Paste Legend Layers	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Drilling and Routing Layers	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Documentation Layers	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Net List	Y	Y	Y	Y	N	Y	Y	N	Y	Y	Y	N	Y
Outer Copper Layers	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Inner Layers	Y	N	N	Y	Y	Y	Y	N	Y	Y	N	N	Y
Miscellaneous Image Layers	Y	N	Y	Y	N	Y	Y	N	Y	Y	N	Y	Y
DFX Analysis	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

Table 1 - Completeness Criteria

Revision Control of Data

IPC-D_325 documented the methods for handling revision control of Grade A and B documentation packages. There needs to be a method to handle revision control of data files. The IPC-2611 documents how to handle revision control of data using examples and placeholders from the IPC-2581 format.

Data file revision control follows the same principles as those defined for the hard copy or electronic document release systems. In a structured format the release data element consists of attribute that define the requirements for the release condition. The file Revision ID shall be according to the details defined in table 3-1. The label attribute is useful when applied to a branch head to associate a file that has special significance such as when the file is applicable, (after a number of units). See Figure 3-7. In addition, it may also be useful to populate the Software Package element as some revisions are not always backward compatible.

Next Steps

Encourage your company to migrate from documentation to data for documentation packages. Make requests to your CAD supplier to support automated data export in a supported standard format wherever possible. The preferred method is to provide data in the IPC-2581 convergence format but other documented formats, such as IPC-D-325, IPC-2511(GenCam), can describe the board, assembly and electrical test in complete form. Other forms of electronic data are also useful provided the receiver can read the file. i.e., Gerber plot data or Excellon NC data.

Volunteer to become a member of the 1-14 Documentation Subcommittee and help move the Documentation Package into the new era of Data Exchange.

Documentation Standards

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What's Involved in the Package

- Fabrication Drawings
- Assembly Drawings
- Bill of Materials
- Schematic or Logic Diagrams
- Wiring Diagrams
- Specification Control Drawings
- Electronic Data
- Mechanical Drawings

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Minimum Drawing Requirements

The documentation of a printed board assembly consists of several drawing types that are included or referenced in the documentation package.

All drawings are not always supplied to the fabricator or to the assembly company; however, the designer must have a good understanding of the minimum information necessary to convey the design intent.

- ***IPC-D-325 being revised***

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The IPC-D-325 defines three types of documentation packages. These are:

Class A: Minimal Documentation - This is usually used for internal use and consists primarily of a copy of the layout and artwork in hard copy or NC format. The information requires a great deal of coordination between the design and manufacturing disciplines. Notes on the layout convey much of the needed information. Class A documentation requires the use of a manufacturer that can produce a functional product from the information supplied.

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Class B: Moderate Documentation -This includes a complete board description without information as to the manufacturing allowances that are included in the design. The parts list and assembly drawing are also supplied to the assembler. CAD data on conductor routing describes the interconnectivity of the circuit and is used by the manufacturer to derive electrical test data. A schematic, logic diagram, or net list may also be supplied. Class B documentation requires working with a manufacturer and assembly company that has a strong CAD/CAM background and an understanding of what the designer expects.

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Class C: Full Documentation — This includes a complete procurement package that may be sent to multiple suppliers with each producing an identical part. The data, as a minimum, the master drawing, the assembly drawing, bill of material (BOM), schematic or logic diagram, test specs, artwork in hard copy and electronic form, and an electronic description of the design. In addition, a panel layout may also be included, especially if the assembly is to be built in panel format. The tooling features are defined and located and manufacturing allowances included in the design are identified.

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IPC-2610 replacing D-325

- ***IPC-2611*** - Generic Requirements for Electronic Product Documentation
- ***IPC-2612*** - Sectional Requirements for Electronic Diagramming Documentation (Schematic and Logic Descriptions)
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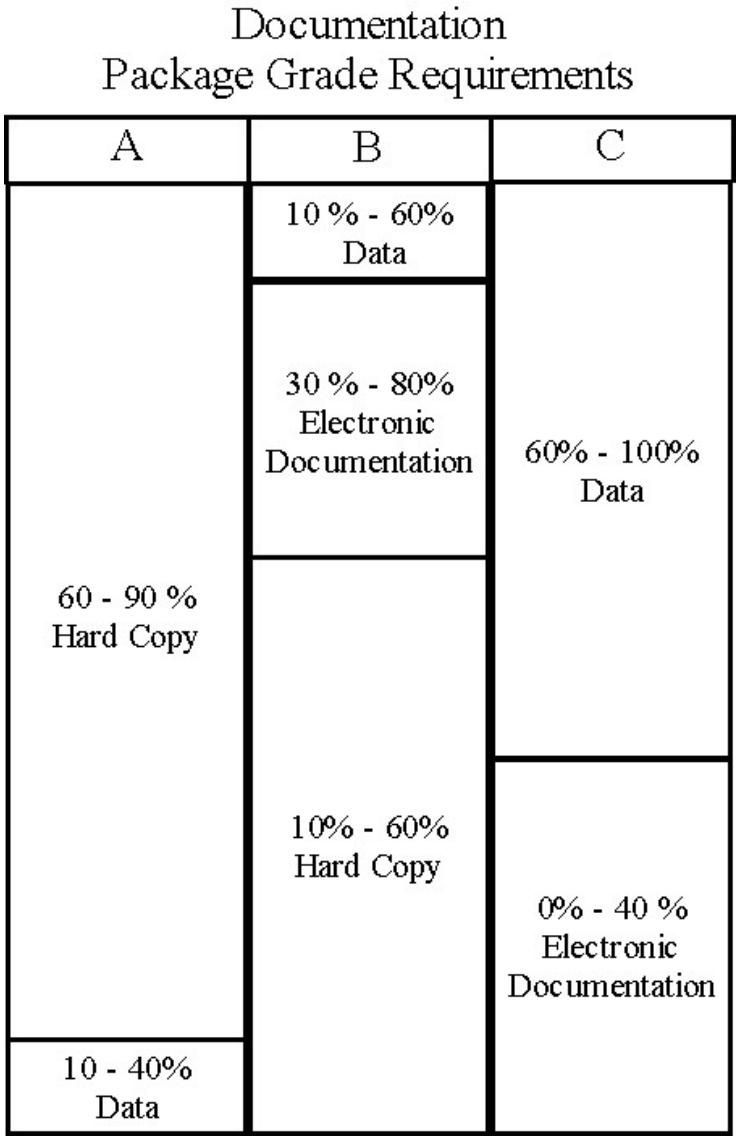
- ***IPC-2618*** -Sectional Requirements for Bill of Material Documentation (Complete Listing of Parts, Materials, and Procurement Documents)

IPC-2610 Classification

- **Grade A**
  - All hard copy; completeness 1,2 and 3
- **Grade B**
  - Mixed hard copy and electronic data, completeness 1, 2 and 3
- **Grade C**
  - All electronic data, completeness 1, 2, and 3



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Completeness Criteria

Name	Full	Design			Fabrication			Assembly			Test		
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AVL (Components and Materials)	Y	N	Y	Y	N	Y	Y	Y	Y	Y	N	N	Y
Component Packages	Y	Y	Y	Y	N	N	Y	Y	Y	Y	N	Y	Y
Land Patterns	Y	N	Y	Y	N	N	Y	N	Y	Y	N	Y	Y
Device Descriptions	Y	Y	Y	Y	N	N	N	N	N	Y	N	N	Y
Component Descriptions	Y	Y	Y	Y	N	N	N	Y	Y	Y	N	Y	Y
Soldermask ; Solder Paste Legend Layers	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Drilling and Routing Layers	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
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Net List	Y	Y	Y	Y	N	Y	Y	N	Y	Y	Y	N	Y
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Inner Layers	Y	N	N	Y	Y	Y	Y	N	Y	Y	N	N	Y
Miscellaneous Image Layers	Y	N	Y	Y	N	Y	Y	N	Y	Y	N	Y	Y
DFX Analysis	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

Drawing Definition

The master drawing (Fabrication Drawing) describes the unpopulated printed board and all the features that become a part of the board. Usually it is for a single board even though the board will be built as a panel by the board manufacturer. The assembly drawing defines the location of all the components that are associated with the assembly.

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Data

- Intelligent information that may be used directly by machine in order to accomplish a particular manufacturing event.

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Drawings

- Hard copy or un-intelligent documentation (example pdf etc.) to which all formatting criteria applies.

Supplier

- The organization or company responsible for providing the goods and/or services required to produce an electronic product which includes physical items as well as intellectual/software characteristics and is documented as either user procurement, supplier data or contractual agreements.

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*User

- The individual, organization, company or agency responsible for the procurement of electrical/electronic hardware, and having the authority to define the class of equipment and any variation or restrictions (i.e., the originator/custodian of the contract detailing these requirements).

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Jisso

- Interface and Solution technology between user and suppliers for Interconnecting, assembling, packaging, mounting and integrating system design. Jisso concepts contain both functional and physical technology.

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Jisso Level 0 – Intellectual Property

- The intellectual property of an item pertains to the idea or intelligence imported or described in a formal document, design entity or patent disclosure. The information may be in hard or soft copy and can include computer code or data format as a part of the descriptive analysis. The characteristics are described as to their physical, chemical, electrical, mechanical, electromechanical, environmental, and/or hazardous properties.

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Jisso Level 1 – Electronic Element

- Bare die or discrete components (resistor, capacitor, diode, transistor, laser), with metallization or termination ready to be mounted
  This can be an IC, or discrete electrical, optical or MEMS element.
  Individual elements cannot be further reduced without destroying their stated function.

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Jisso Level 2 – Electronic Package

- A container for an Individual Electronic Element or Elements which protects the contents and provides terminals for making connections to the rest of the circuit. The Component Package outline is generally standardized. The Component Package may function as electronic, optoelectronic, or Micro-Electro-Mechanical- Systems, and may in the future include Bio-electronic sensors.

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Jisso Level 3 – Electronic Module

- A sub-assembly with functional blocks which consist of Individual Electronic Elements and /or Component Packages. An individual module having an application specific purpose including Electronic, Optoelectronic or Mechanical (MEMS). The module generally provides protection of its elements and packages, depending on the application.

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Jisso Level 4 – Electronic Unit

- A group of functional blocks that have been designed to provide a single or complex function needed by a system in order for the system to serve a specific purpose. The Electrotechnical Assembly may consists of Electronic Elements, Component Packages and/or Application Specific Modules. The function of the Electrotechnical Assembly may be electronic, optoelectronic, electromechanical, or mechanical or any combination thereof. The function may in the future include bio-electronic applications.

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Jisso Level 5 – Electronic System

- A completed, market ready, unit dedicated to combining and interconnecting functional block(s). The functional block(s) generally consist of Electrotechnical Assemblies, but may also include Application Specific Modules, Component Packages or Electronic Elements . The System Product may include the cabinetry, the backplane into which the Assemblies, Modules, Packages or Elements are inserted and the cabling (electrical, optical, or mechanical) needed to interconnect the total functional block(s) into a configured system.

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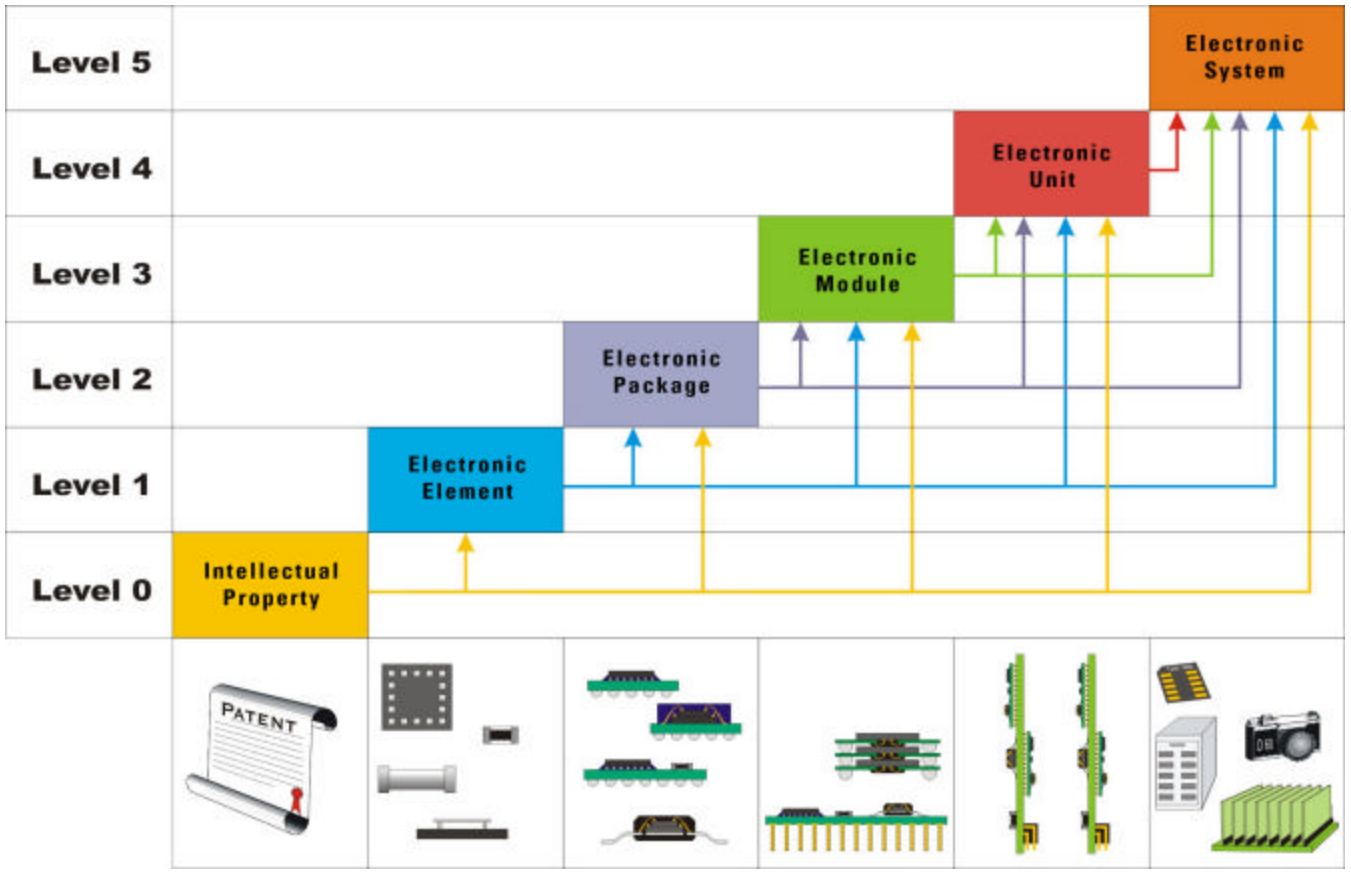
Jisso level hierarchy



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Electronic Diagrams and BOMs

A reference designator is used to coordinate the part identification and location to the electronic diagrams (logic or schematic), and the parts list (BOM). The BOM may be supplied as a computer listing (excel spread sheet)since the electronic forms are often used to tie in to the material issuing system of the assembler.

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Minimum Drawing Requirements

In the United States, drawing size formats are governed by ANSI Y14.1 and come in multiple sizes identified by the letters A, B, C, and D. The A size drawing format is 8 ½" x 11". The next letter is B (i.e., 11" x 17").

Size C is 17" x 22", and D size is 22" x 34". There are also E and F sizes, which may be used when appropriate. Generally, multiple sheets of the D size drawing sizes are preferred over going to the larger sizes.

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Minimum Drawing Requirements (cont.)

Automated data is encouraged wherever possible. The preferred method is to provide data in a neutral standard format.

IPC-D-325, IPC-2511(GenCam), IPC-2581 (Offspring of ODB++ and GenCAM) can describe the board, assembly and electrical test in complete form. Other forms of electronic data are also useful provided the receiver can read the file. i.e., Gerber plot data or Excellon NC data.

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Minimum Requirements for Master Drawing

The master drawing is used to describe the bare (or unpopulated) printed board. It shows the dimensional limits or grid locations that are applicable to any and all parts of a product to be fabricated. This includes the arrangement of conductors and nonconductive patterns or elements, the size, type, and location of all holes, and any other necessary information

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Minimum Requirements for Master Drawing (cont.)

The master drawing identifies the locations of the datum reference planes and the coordinate dimensioning system for the board. This includes the relationships of the three datum planes (primary, secondary and tertiary) and the X, Y, and Z coordinate axes.

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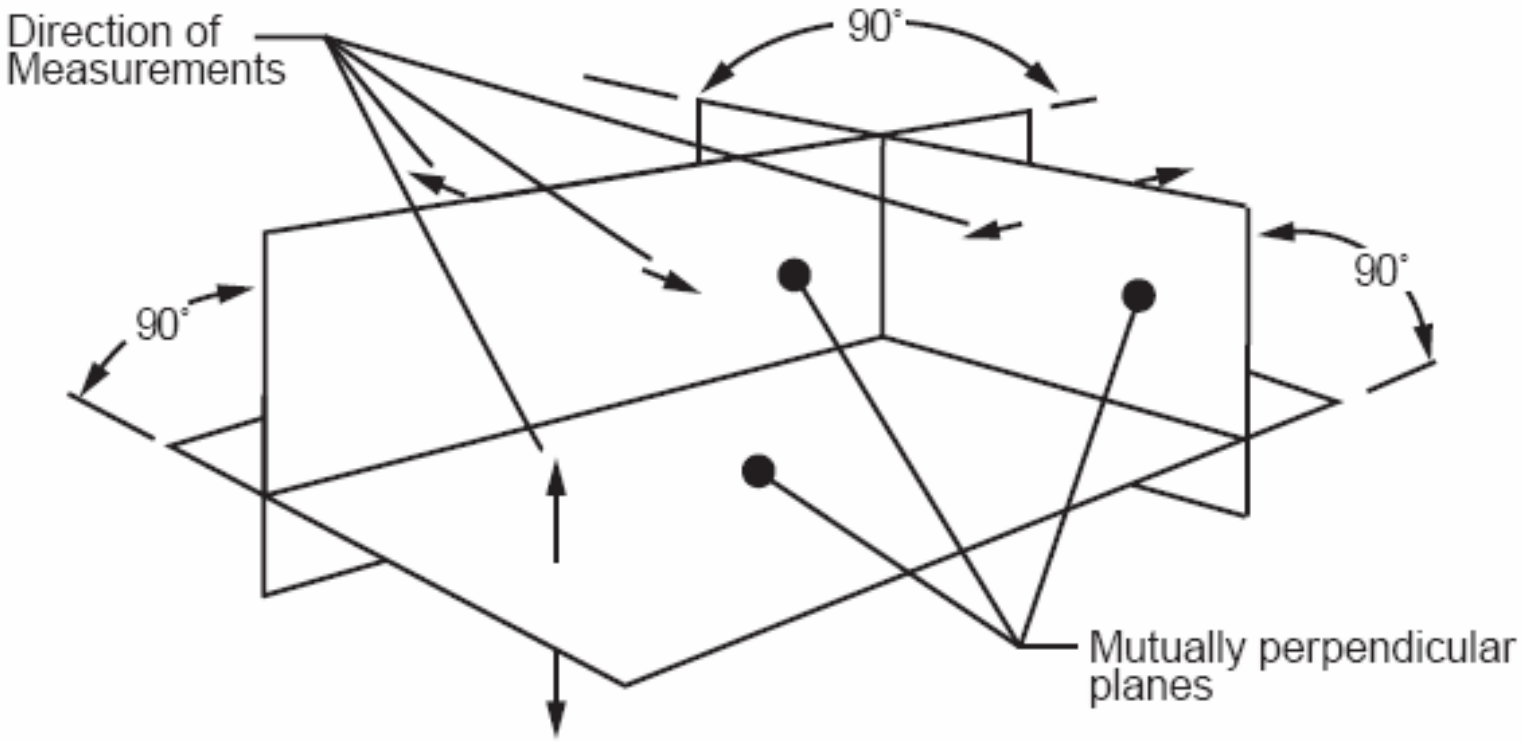
Datum Reference Frame



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Minimum Requirements for Master Drawing (cont.)

These conditions are usually established with the printed board oriented such that the side of the board on which the components are mounted is facing up. Since boards now have components on both sides the designer determines which side is facing up, and that side becomes the primary side. The backside of the board is therefore the reference for the primary datum plane.

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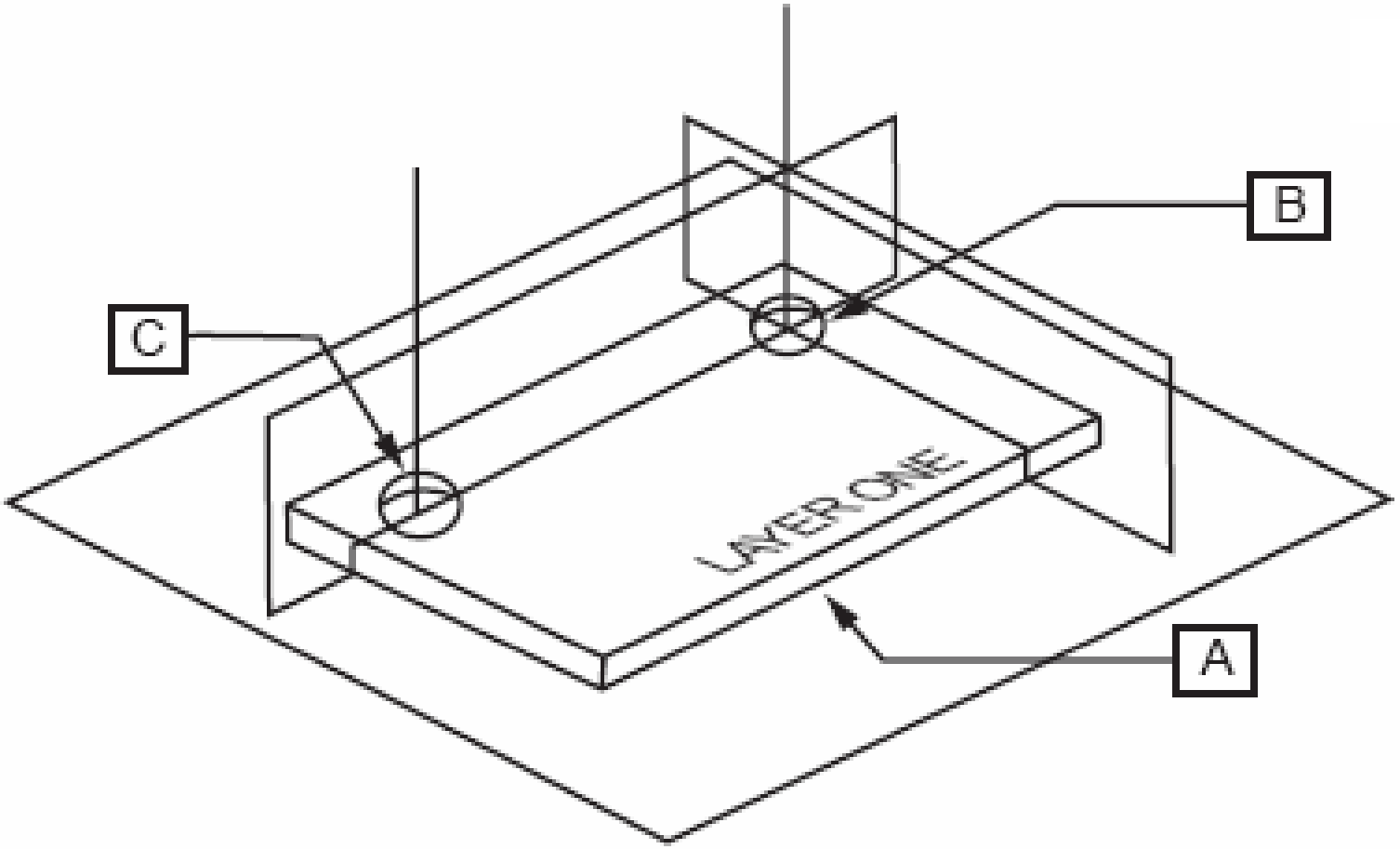
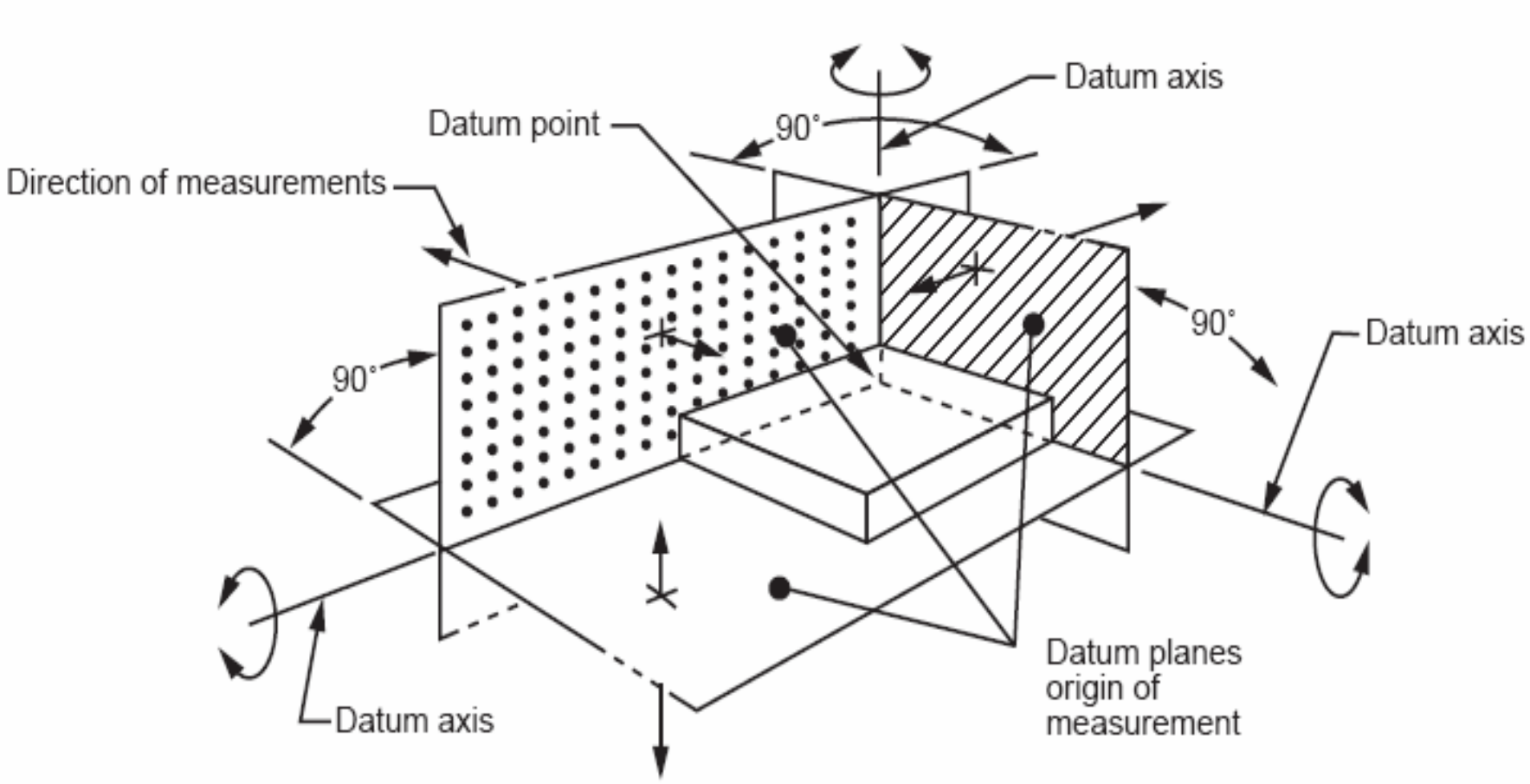
Datum Reference Frame to Printed Board Relationship



IPC-2615

Datum Reference Frame to Printed Board Relationship



Minimum Requirements for Master Drawing (cont.)

Features of the board are used to locate the datum planes. The backside of the board is the feature that establishes the primary plane. Secondary and tertiary planes can established using holes, symbols, or fiducials or board edges. It is preferred to use the features critical to mounting the board in its final package to establish datum planes.

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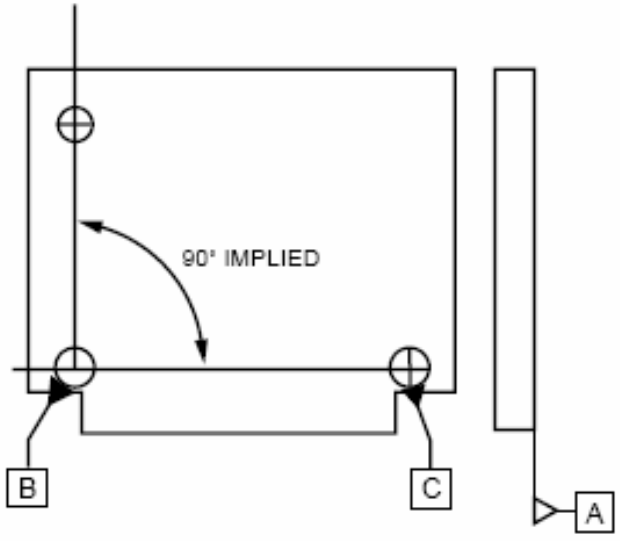
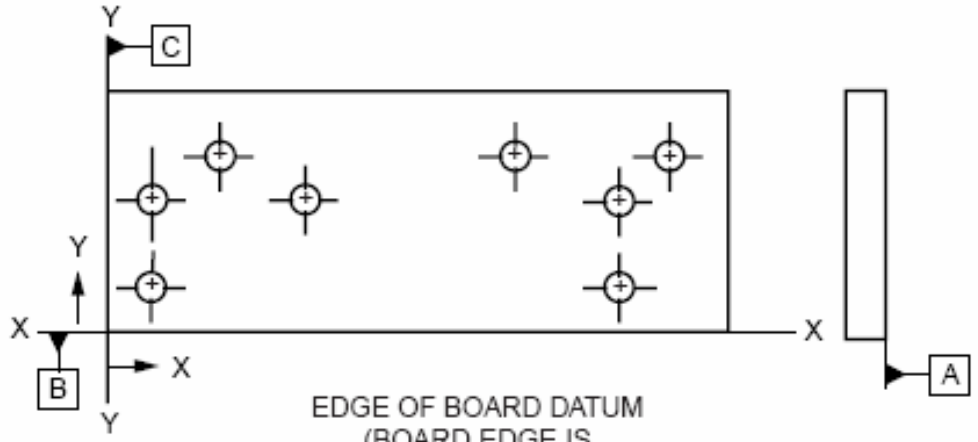
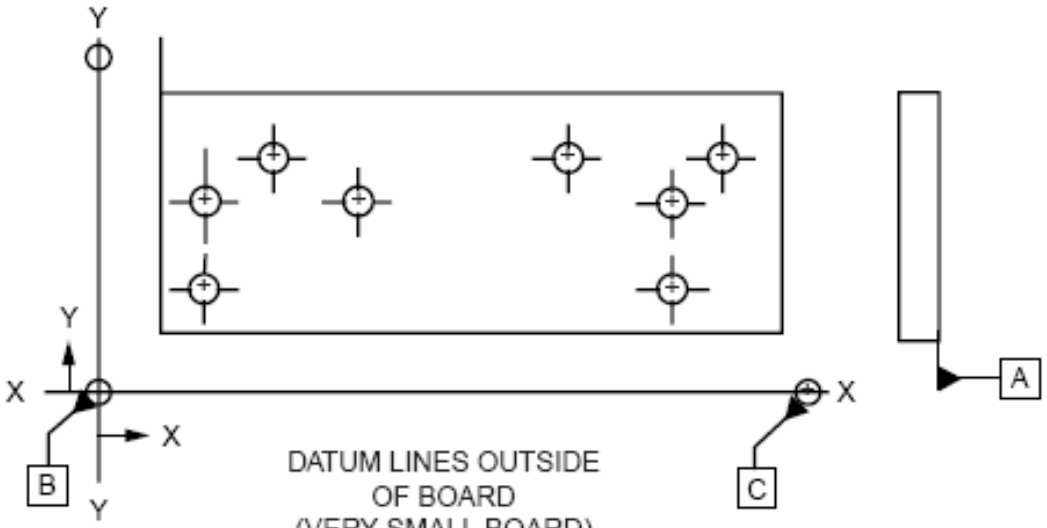
Datum Identification Examples



DATUM LINES WITHIN BOARD
(MOUNTING HOLES MAY BE USED)



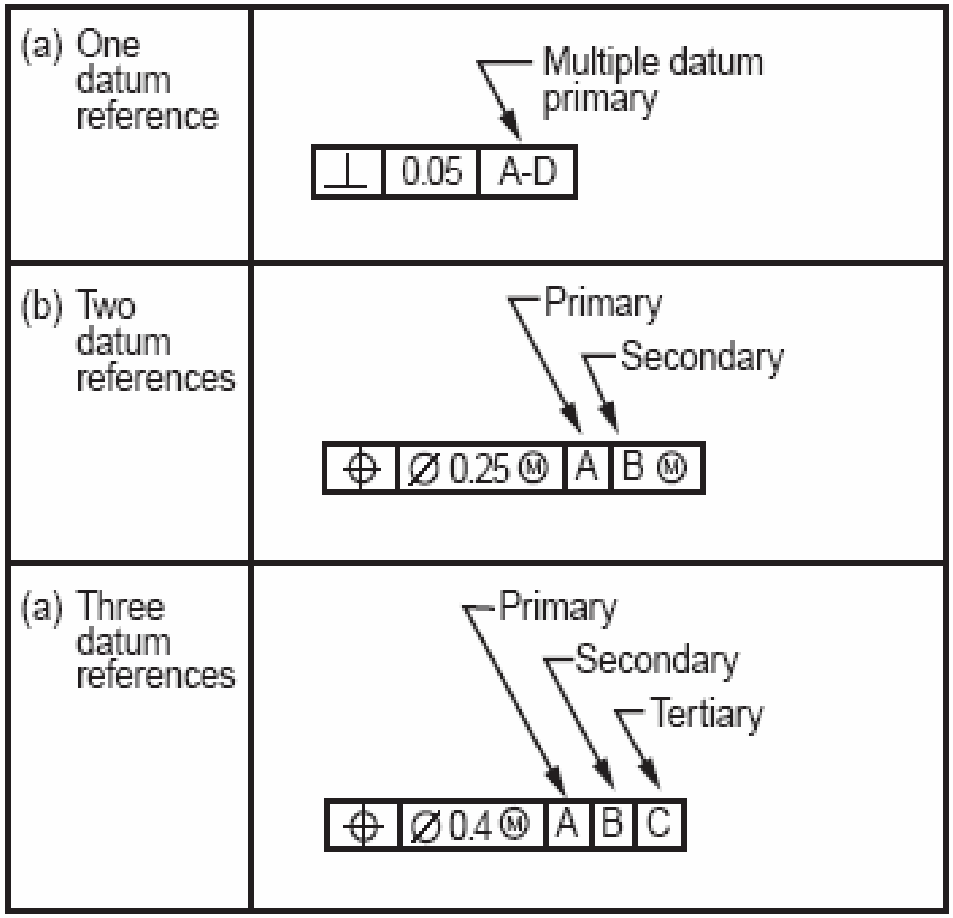
EDGE OF BOARD DATUM
(BOARD EDGE IS
CRITICAL TO MOUNTING)



DATUM LINES OUTSIDE
OF BOARD
(VERY SMALL BOARD)

Minimum Requirements for Master Drawing

When a feature, or pattern of features, is controlled by a geometric tolerance and the feature is also intended to serve as a datum feature, the feature control frame and the datum feature symbol are combined.



Minimum Requirements for Master Drawing

There are classes of master drawing completeness just as there are documentation completeness requirements. A complete disclosure master drawing provides information on all the board details including, dielectric separation, overall thickness and tolerances, and allowable bow and twist of the final product. The requirements are defined in the IPC-2611 and flow down to the IPC-2614.

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Minimum Requirements for Master Drawing

Material descriptions include the base material, conductive and non-conductive properties as well as the plating, coating, and marking ink requirements. Conductors and hole requirements are documented. This includes shape, arrangement, and acceptance criteria.

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Minimum Requirements for Master Drawing

Identification and traceability requirements are defined and all process allowances that were used in the design are detailed, such that the manufacturer doesn't have to guess that they have the correct precision equipment needed to produce the part.

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Characteristics	Requirements
A. Board Details	1. The type, size and shape of the printed board and all tolerance conditions thereof. 2. Dielectric separation between layers. 3. Bow and twist allowances. 4. Overall board thickness requirements including tolerances.
B. Materials	1. Type class and grade of material, including color if applicable. 2. Plating and coating material(s) type and thickness(es). 3. Marking inks or paint and permanency.
C. Hole Details	1. The size, location and tolerances for all holes. 2. The plating requirements for all holes. 3. The hole cleaning requirements including if etchback is required or permitted.
D. Conductor Definition	1. Shape and arrangement of both conductor and non-conductor patterns on each layer of the printed board. (Paper or film copies of the production master(s) or copies of artwork may be used to define these patterns.) 2. Electronic data may be supplied, in lieu of reproductions (as noted above), refer to Table 4-1, Figure 4−1, and 4.2.3. 3. Conductor width and spacing on the finished printed board. 4. Dimensions and tolerances for critical pattern features which may affect circuit performance. 5. Conductor layer identification starting with the primary side, the next conductive layer **shall** be Layer 2. (For assemblies with components on both sides the most complex or densely populated side **shall** be Layer 1.)
E. Marking	1. Printed board identification marking. 2. Layer identification - revision (optional). 3. Size, shape and location of reference designation and legend marking, if required. 4. Traceability marking and/or date code and serial number (when required). 5. Location and size requirements for fabricator's I.D., UL, ESD marking and cage code.
F. Processing Conditions	1. Processing allowances that were used in the design of the printed board, including but not limited to: a. Conductor width allowance b. Conductor spacing allowance c. Land/hole fabrication allowance d. Solder mask or cover layer registration allowance 2. Applicable processing specifications. 3. Location of quality conformance coupons or circuitry.
G. Design Concepts	1. Maximum rated voltage (maximum voltage between two non-connected adjacent conductors with the greatest potential difference). 2. Identification of testing and test point locations (when applicable). 3. Modular grid system(s) used: a. Metric grid - 2.0, 1.0, 0.5 or multiples of 0.1 mm b. Inch based grid - 0.100, 0.050, 0.025 or multiples of 0.005 inches
H. Documentation	1. Terms used on the master drawing **shall** conform to this standard and IPC-T-50. 2. Notes either included on the first sheet(s) or location of notes specified on the first sheet(s)

Minimum Requirements for Master Drawing

If a lesser master drawing is produced the liaison and understanding between the design and manufacturing disciplines increases dramatically. Nevertheless, a good working relationship can overcome many shortcomings in the documented requirements.

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Master Drawing Hole and Conductor Description

The master drawing defines all the physical characteristics of the printed board. The description starts with the definition of the individual conductive layers that compose the board. Layer 1 is the first layer closest to the primary side and usually has many lands for component mounting. The lands may circumscribe a hole for through-hole components or be without a hole as in the case of surface mount lands.

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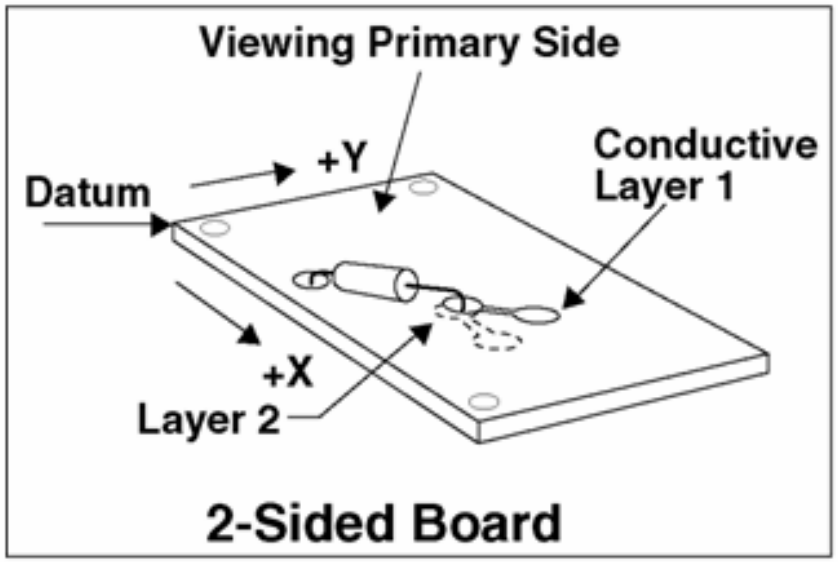
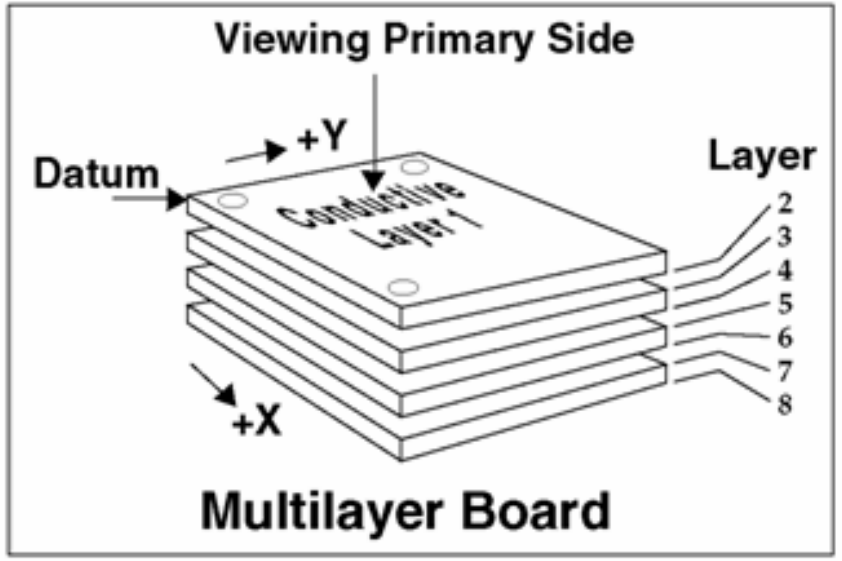
Viewing of Primary Layer and Subsequent Layers





Note: For those printed board assemblies that have components on both sides, any side may be designated as the primary side and used to define **Conductive Layer 1**

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Master Drawing Hole and Conductor Description

Conductors may also be included on layer 1. The conductor definition, arrangement, and relationship to holes that are either part of the circuit or used for physical mounting must also be defined. Thus the shape and arrangement of both conductive and non-conductive patterns must be described for all the layers of the printed board. This may be accomplished using paper or film copies of the production master(s) or copies of the artwork if artwork is supplied with the documentation.

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Master Drawing Hole and Conductor Description

There are separate views of each layer and the conductor width and spacing is indicated. The conductor width and spacing is usually specified through a note, or for critical areas of the circuitry through a specific dimension and tolerance. In many instances finished conductor width and clearance is defined as a least material condition that is acceptable for design performance.

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Master Drawing Hole and Conductor Description

As an example a minimum conductor width might be defined as being 0.25mm [.010”]. Some define the conductor width using a range, i.e. 0.20-0.25mm [.008”-.010”]. In either case the manufacturer selects the target value that he thinks the designer wishes to achieve and tries to come as close to that condition as possible.

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Master Drawing Hole and Conductor Description

Processing allowances should also be defined on the master drawing. This is especially important when providing CAD data which indicates absolute location of the conductor arrangement. If two parallel conductors are routed on a 0.5mm [.020”] grid a good explanation of process allowance would be that there is 0.1mm [.004”] allowance between a minimum conductor 0.2mm [.008”] wide and a minimum spacing of 0.2mm [.008”]. The manufacturer can now adjust his process to meet the required conditions and compensate conductor size for his fabrication allowances.

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Master Drawing Hole and Conductor Description

- One problem exists in that the tolerances are assigned to conductors while the surface mount lands are often neglected. While the manufacturer is concentrating on the minimum conductor, the lands that should be at maximum material condition also come out smaller than required thus reducing the opportunity for a good solder joint.

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Master Drawing Hole and Conductor Description

- Therefore, conductor definition should provide the target values for lands and conductors on each layer. This would usually be least material condition for the conductor (LMC) and maximum for the lands (MMC) to get good solder joints on the surface and no hole breakout on internal layers

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Master Drawing Hole and Conductor Description

- Holes are also defined on the master drawing. This includes the location and whether the hole is unsupported or has plating in the hole. Although there should be an awareness of the drill size that should be used, it is usually best to only specify the range for the hole diameter in terms of LMC and MMC.

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Master Drawing Hole and Conductor Description

The master drawing also describes the minimum plating thickness that must be included in the plated-through hole to meet the reliability expectations of the design. The process allowance that was included in the hole to land calculation is also an important piece of information needed to determine the registration requirements so that holes do not break out of their circumscribing land.

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Printed Board Profile Dimensioning and Tolerances

The master drawing defines the physical outline of the printed board as well as the conductive patterns and holes. This includes the printed board profile, construction in terms of dielectric spacing and thickness, and cutouts and notches included in the periphery of the finished board.

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Printed Board Profile Dimensioning and Tolerances

- All mechanical dimensions are related to the datum reference of the board. Thus the circuit pattern and the board outline originate from the same location; their definition and tolerances describe the allowable variation.

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Printed Board Profile Dimensioning and Tolerances

Dimensions usually start from datum zero-zero. It is important to realize that when using coordinant tolerancing methods an accumulation of tolerances can result. When one feature location is dimensioned from another and a third feature is dimensioned from a second, the chain of dimensions all bring with them the allowable variation that can occur.

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Printed Board Profile Dimensioning and Tolerances

This incremental dimensioning is *not* a preferred method since the distance between the first location and the last location can vary by the total accumulation of all the members of the chain. Therefore most dimensioning techniques start at datum zero and provide information in either X or Y axis to the individual locations and where required make reference to other datum's or datum planes.

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Printed Board Profile Dimensioning and Tolerances

- One popular way to control the board outline is to use the Geometric dimensioning and tolerancing technique of profile dimensioning. The ASME Y14.5M symbol for defining the profile of a surface is a horizontal crescent (a straight line connecting to an arc above the line). This symbol is used in a feature control frame when describing features of the geometric tolerances.

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Printed Board Profile Dimensioning and Tolerances

The use of profile symbols can be further defined by a symbol that indicates that the profile tolerance applies to surfaces all around. This indicator is a circle that is located at the junction of the leader from the feature control frame. The board outline as a feature is controlled in relation to the primary, secondary and tertiary datum planes.

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Printed Board Profile Dimensioning and Tolerances

- There are many ways in which the master drawing can control the position of features and their tolerance. Each technique is predicated on the need to control the dimension and to what degree. It is a good practice to be as liberal as possible in the range of allowable variation.

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Printed Board Profile Dimensioning and Tolerances

Board manufacturers will adjust tooling to accommodate the requirements. These will be checked as the first boards are produced. After initial first article approval, the tooling and tool maintenance control the end results.

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Tooling Hole Location Documentation

The term *tooling feature* is more generically correct to define any physical feature that is used exclusively to position a printed board or panel during the fabrication, assembly, test, or inspection process.

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Tooling Hole Location Documentation

With the increased use of vision systems in the manufacturing discipline, the whole issue of who owns the tooling concepts becomes a bit clouded. Before a design is committed to manufacturing a clear understanding and agreement is required to address all the goals of the various parties involved.

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Tooling Hole Location Documentation

The first step of the process is the design of the single image board. The tooling feature(s) are normally on the board, and may be holes, registration symbols, or fiducials. The reason they are on the board is so that when all processing is complete and the customer is holding the final product in his hand he can identify any location on the board in relation to the zero-zero origin that is established by one of the tooling features.

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Tooling Hole Location Documentation

Inspection, field maintenance, and handbook references find the tooling feature on the board most helpful to orient the operator in the function being performed. When boards are very dense with circuitry or very small there may be no room to have the tooling features located on the board. In these instances the zero-zero origin is off the board and a secondary location identified for visual orientation. Many times marking ink provides this function.

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Tooling Hole Location Documentation

The board manufacturer repeats the single image on the production panel. The number of times that the board can be reproduced is a function of the board to panel size. Original tooling features that are part of the design are maintained, but are not used as a part of the manufacturer's tooling system (which many times is optimized through the panel center to spread the material movement potential over the entire panel evenly instead of just coming from one edge).

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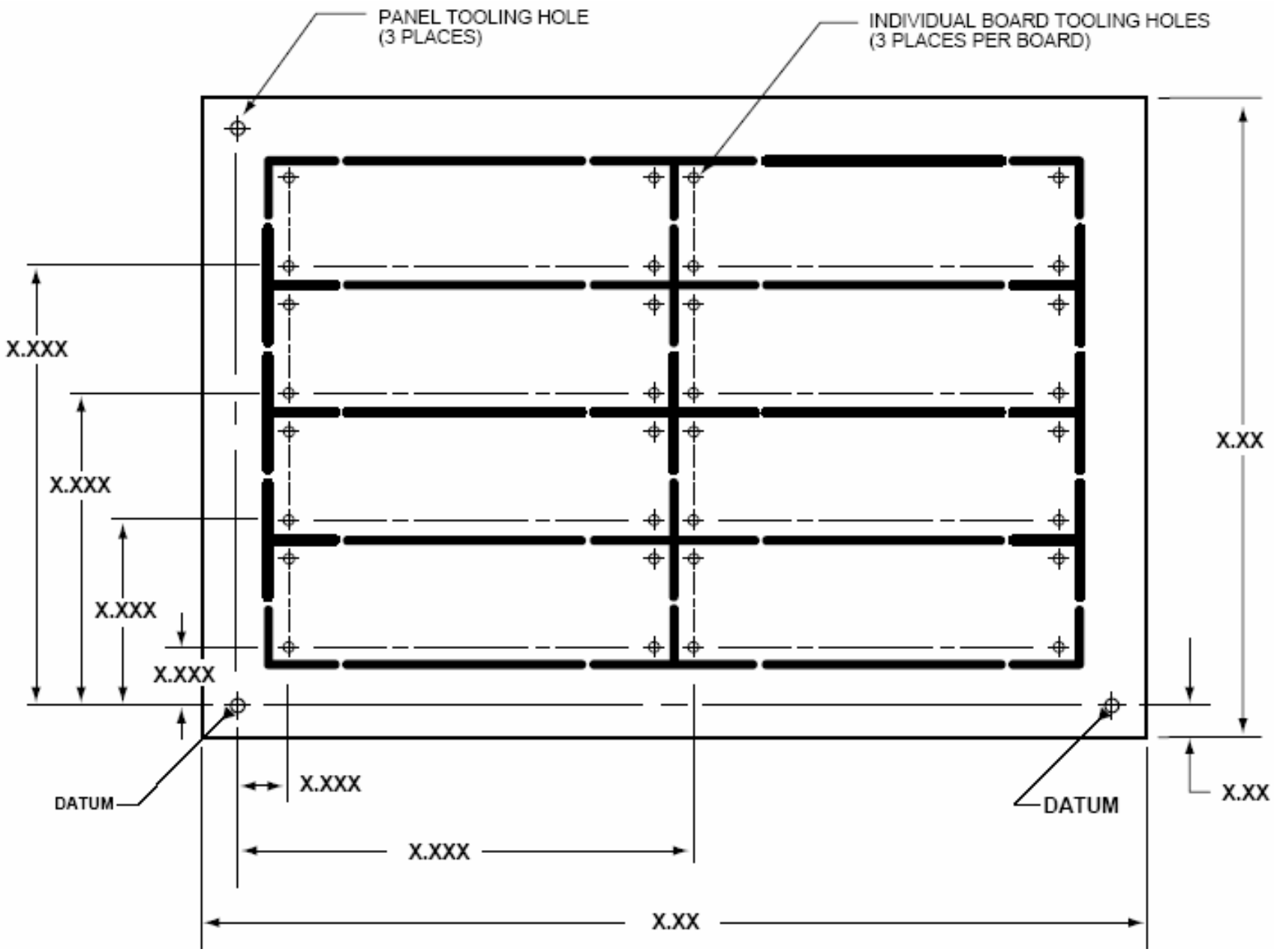
PANEL TOOLING HOLE
(3 PLACES)
INDIVIDUAL BOARD TOOLING HOLES
(3 PLACES PER BOARD)
X.XXX
X.XXX
X.XXX
X.XXX
X.XX
DATUM
DATUM
X.XXX
X.XXX
X.XX
X.XX

Tooling Hole Location Documentation

The board manufacturer adds his own tooling features and only uses the original design tooling features to establish the relationship between and within board images. If the board manufacturer separates the boards to be delivered to the customer from the panel, they might use original tooling features to position the boards during electrical continuity testing of the bare board.

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Tooling Hole Location Documentation

The most significant change in the industry is the automation used to assemble products and the need of the assembler to have well thought out tooling schemes that match the capability of their equipment. Many conveyor systems have positive stops that require holes in the panel or that use the panel edges to obtain the original location of the product.

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Tooling Hole Location Documentation

Vision cameras then look for symbols that help identify more precise locations to correctly mount parts. Additionally, once the assembly is completed tooling holes are usually used to position the assembly in the in-circuit test fixture. All these conditions should be taken into account and fully documented in order to achieve the best coordinated results.

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Need for Panelization

- Boards are built in panel format
- Assemblies are built in panel format
- Issues of responsibility are not clear
- Designers should take charge as the conduit between engineering and manufacturing

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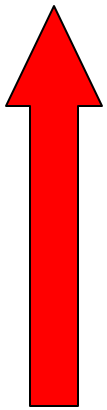
Need For Intelligent Data

Highly Organized, Integrated, Related, clear



IPC-2581

GenCAM, EDIF, AP210, IPC350

EDA DBs, Alg, Men, RR, ...

CAM DBs, GenCAD, PDW, FATF,ODB++

BOMs, CPLs, Netlists

Gerber, drill,

Plots… HPGL, PS, PDF, ...

Phone calls, paper

Flat, dumb, vague, assumptions

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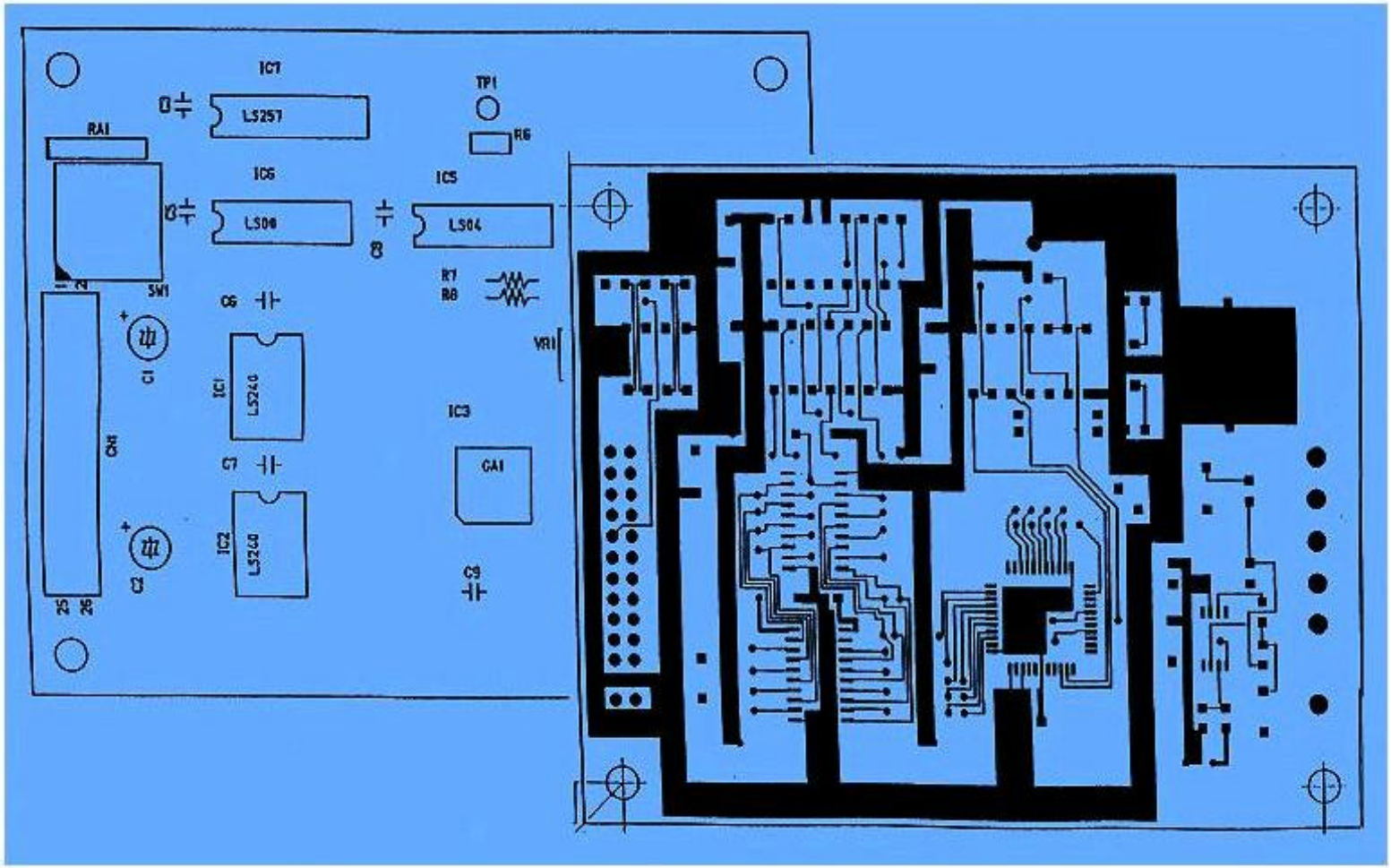
Printed Boards and Assemblies



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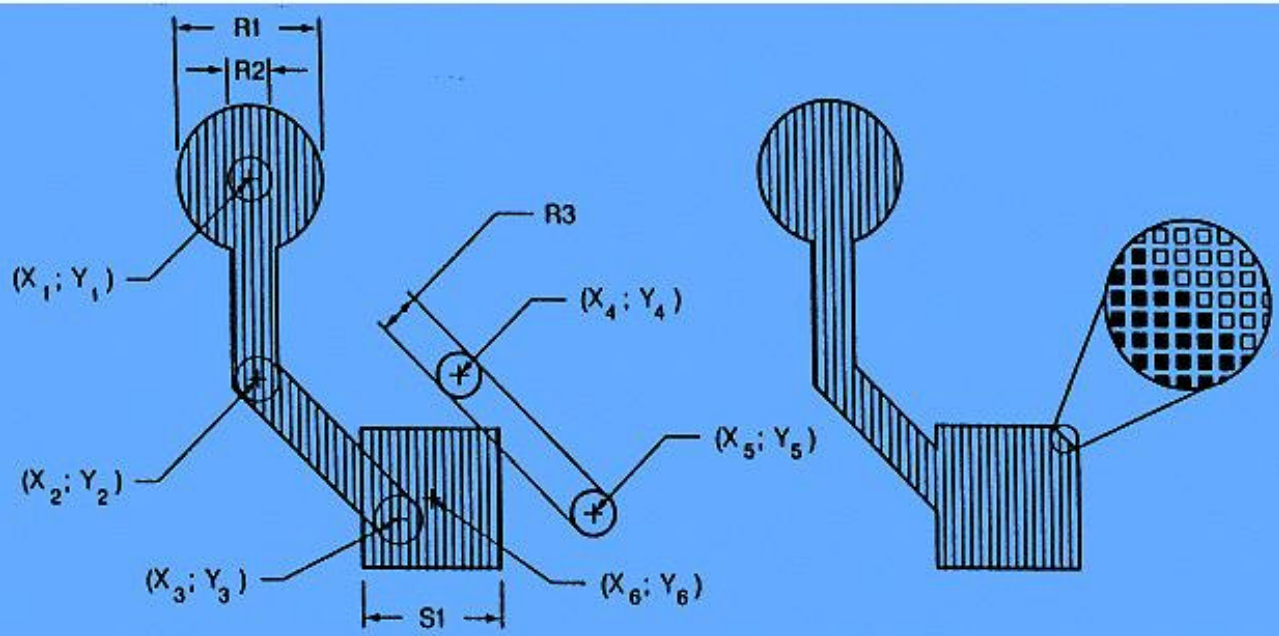
Vector and Raster Representation



FLASH 1 - FLASH POSITIVE, ROUND APERTURE, DIAMETER OF R_1, CENTER COORDINATES $(X_1; Y_1)$

VECTOR 1 - VECTOR, POSITIVE, ROUND APERTURE, DIAMETER OF R_2, START AND END COORDINATES $(X_1; Y_1)$ $(X_2; Y_2)$

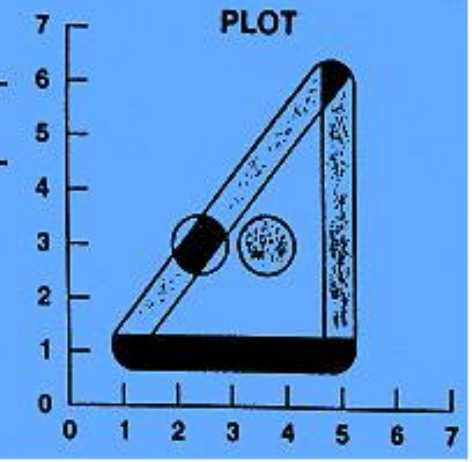
VECTOR 2 - VECTOR, POSITIVE, ROUND APERTURE, DIAMETER OF R_2, START AND END COORDINATES $(X_2; Y_2)$ $(X_3; Y_3)$

FLASH 2 - FLASH, POSITIVE, SQUARE APERTURE SIZE S_1, CENTER COORDINATES $(X_6; Y_6)$

VECTOR 3 - VECTOR, NEGATIVE, ROUND APERTURE, DIAMETER OF R_3, START AND END COORDINATES $(X_4; Y_4)$ $(X_5; Y_5)$

Gerber Format Resultant Plot

EXAMPLE, GERBER FORMAT PROGRAM, 2.4 LEADING ABSOLUTE FORMAT	
* G54D13* D2*	(ALWAYS A GOOD IDEA TO START A PLOT WITH AN ASTERISK) (SELECT APERTURE NUMBER 4) (DON`T DRAW; ALWAYS A GOOD IDEA AFTER AN APERTURE SELECT)
X10000Y10000D2* X50000D1* Y50000*	(GO TO X1.0",Y1.0", NOT DRAWING A LINE) (GO TO X5.0", Y1.0", DRAWING THE BASE OF THE TRIANGLE) (GO TO X5.0", Y5.0", STILL DRAWING)
X10000Y100000* G54D71* D2*	(GO TO X1.0", Y1.0", DRAWING THE HYPOTENUSE) (SELECT APERTURE NUMBER 12) (DON'T DRAW; ALWAYS A GOOD IDEA AFTER AN APERTURE SELECT)
X25000Y30000D3* X35000D3* X0Y0D2*	(GO TO X2.5", Y3.0", AND FLASH A PAD THERE) (GO TO X3.5", Y3.0", FLASH ANOTHER PAD) (GO TO X0.0", Y0.0", NOT DRAWING)
M2*	(END OF PLOT)



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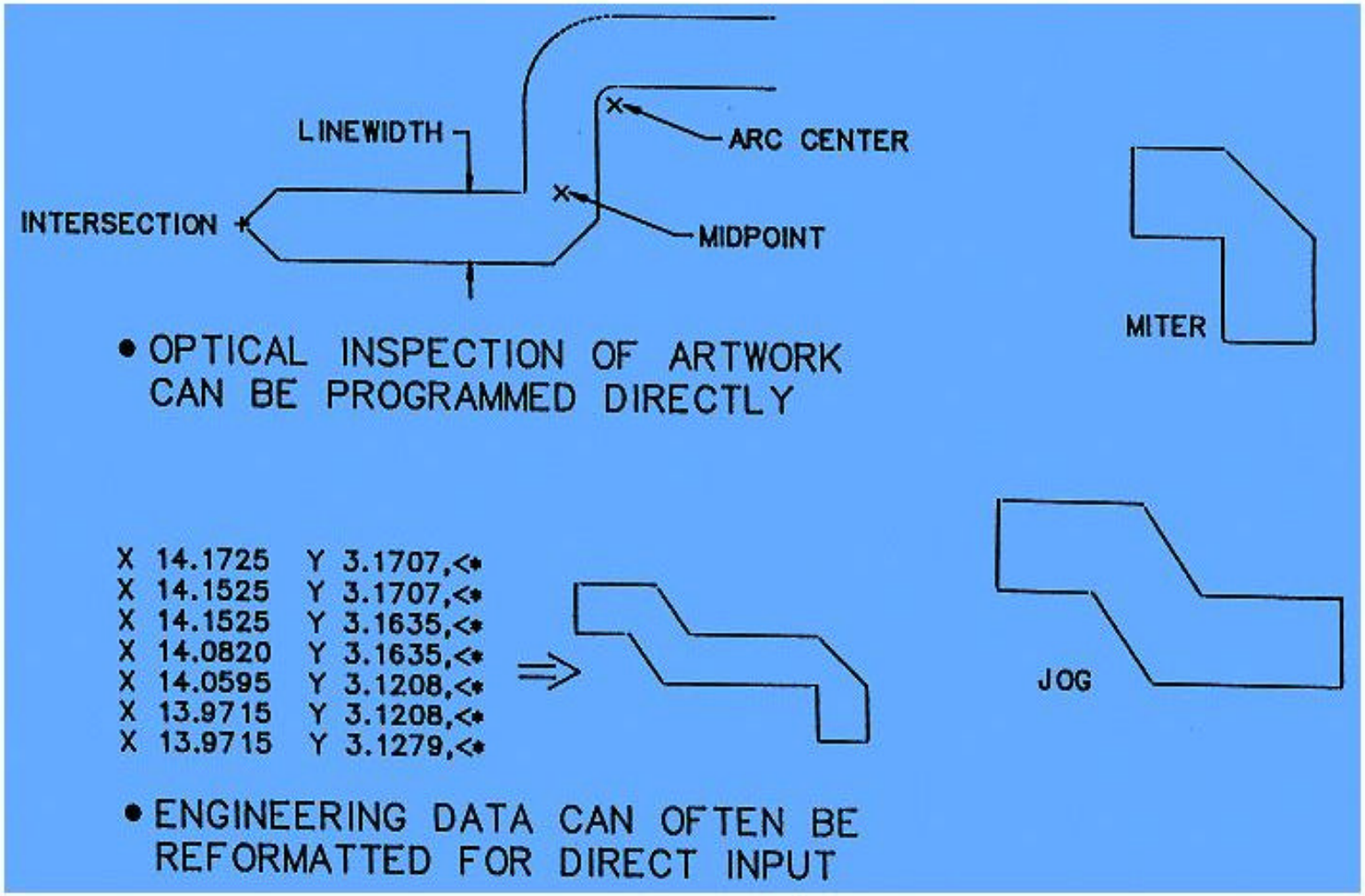
Line Width Accuracy



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Titles and Content

Part #	Description	Purpose
IPC-D-350	Printed Board Description in Digital Form	Artwork and board description records
IPC-D-351	Printed Board Drawings in Digital Form	Schematic drawing, master drawing, assembly drawing, and miscellaneous part drawing records
IPC-D-352	Electronic Design Data for Printed Boards in Digital Form	Electronic description and bill-of-material records
IPC-D-353	Automatic Test Information Description in Digital Form	Electronic assembly testing format records
IPC-D-354	Library Format Description for Printed Boards in Digital Form	External and internal library description records
IPC-D-355	Printed Board Automated Assembly Description in Digital Form	Assembly data description records
IPC-D-356	Bare Board Electrical Test Information in Digital Form	Bare board testing format records
IPC-D-357	Automatic Optical Inspection Information in Digital Form	AOI format records
IPC-D-358	Guide for Use of Digital Descriptions of Printed Boards	IPC-D-350 User's Guide

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History and Status

1972
Released IPC-D-350
"Printed Board Description
in Digital Form

1975
Revision "A" released
(Contracts led by U.S. DoD)

1977
Revision "B" released
(IPC agrees to make no
changes for 5 years
to allow companies
to develop CAD iinterfaces

Approved for use on
U.S. DoD contracts
required by MIL-STD-275

1985
Released IPC-D-351,
"Drawings in Digital Form"

1985
Released IPC-D-352,
"Electronic Design Data
Description for Printed
Boards in Digital Form"

1985
"IPC-D-350B" reaffirmed
without change

Working Group 6 draft
developed after several
meetings suggest circulation
to National Committees
as U.S. proposal

52 (U.S.A) 122 Draft sent
to Geneva for circulation

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History and Status (Continued)

1986
IPC-D-351 and IPC-D-352 approved for use by DoD

1987
IPC-D-354 "Library Format Descriptions for PW Board Digital Databases approved"

1988
Start work on IPC-D-353, "Automatic Test Information Description in Digital Form"

1990
Industry certification to IPC-D-350C

1989
Release Revision "C"

1990
Start work on Users Guide IPC-D-358

1991
Revision "D" Released July, 1992

1987
Start work on Revision "C" of IPC-D-350. approved early 1988

52 (U.S.A.) 122A updated draft to reflect agreements on Revision "C" of IPC-D-350

TC52 agrees to circulate as Secretariat draft under accelerated procedure at May 1988 meeting in Stockholm

1990
Japan suggests improvements new basic format

1992
Release of international document IEC 1182-1 approved

1994
Release of Test Standard IEC 1182-7

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International Strategy

IPC Publication	IEC Publication	Record Description
D-350	1182-1	Artwork records
D-350	1182-1	Board description records
DG-358	1182-2	Guide for digital descriptions
D-351	1182-3	Schematic drawing record
D-351	1182-3	Master drawing records
D-351	1182-3	Assembly drawing records
D-351	1182-3	Miscellaneous part drawing records
D-352	1182-4	Electrical description records
D-352	1182-4	Parts list records
D-354	1182-5	Library description records
D-355	1182-6	Assembly description records
D-356	1182-7	Bare boards electrical test description records
D-353	1182-8	Automatic test information
D-357	1182-9	Automatic optical inspection records

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Hierarchy of Data

JOB	
DIM K	External subroutines
998	End of external subroutine
DIM L	Internal subroutine
997	End of internal subroutine
DIM G	Electrical description
DIM A	Artwork
DIM B	Boards
DIM C	Schematic
DIM D	Master drawing
DIM E	Assembly Drawing
DIM F	Parts
DIM F	Parts
DIM F	Parts
999	End of job

Basic Record Entities

- ***Command Data*** - commands to the program or provides operation codes
- ***Feature Descriptions*** - provides detail information for various features identified by the command data
- ***Location Descriptions*** - describes the positioning of features
- ***A User Area*** - contains any alpha-numeric indicating a sequence or number specified by the user

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Major Record Types

- Parameter Record
- Feature/location Record
  - ***Line***
  - ***Point***
  - ***Annotation***
- Comment Record
- Subroutine Record
- Subroutine Call Record

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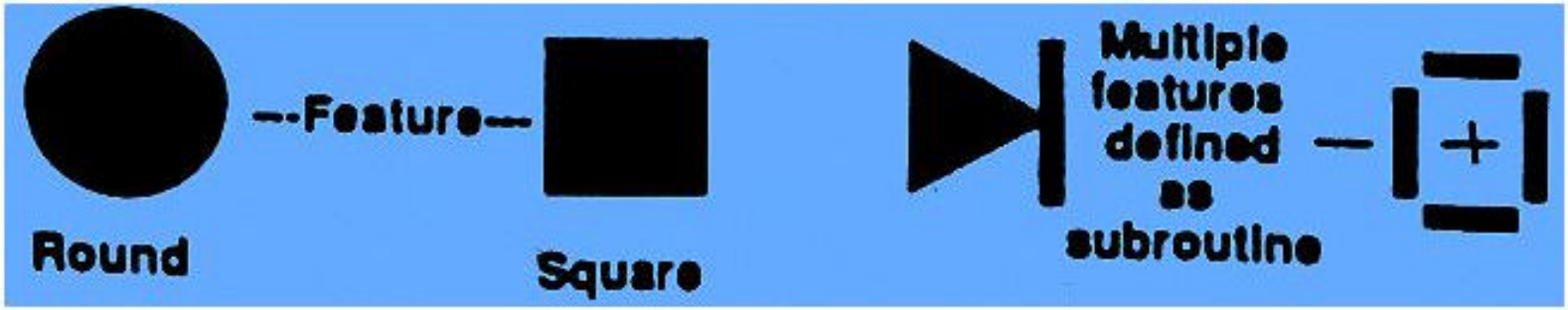
Parameter Records

- Parameter - JOB
- Parameter - DIM (Data Information Module)
- Parameter - UNITS
- Parameter - TITLE
- Parameter - NUMB (Number)
- Parameter - REV (Revision)
- Parameter - TOL (Tolerance)
- Parameter - SCALE
- Parameter - LAYER
- Parameter - FAB (Fabrication)
- Parameter - LANG (Language)
- Parameter - IMAGE

Feature Descriptions

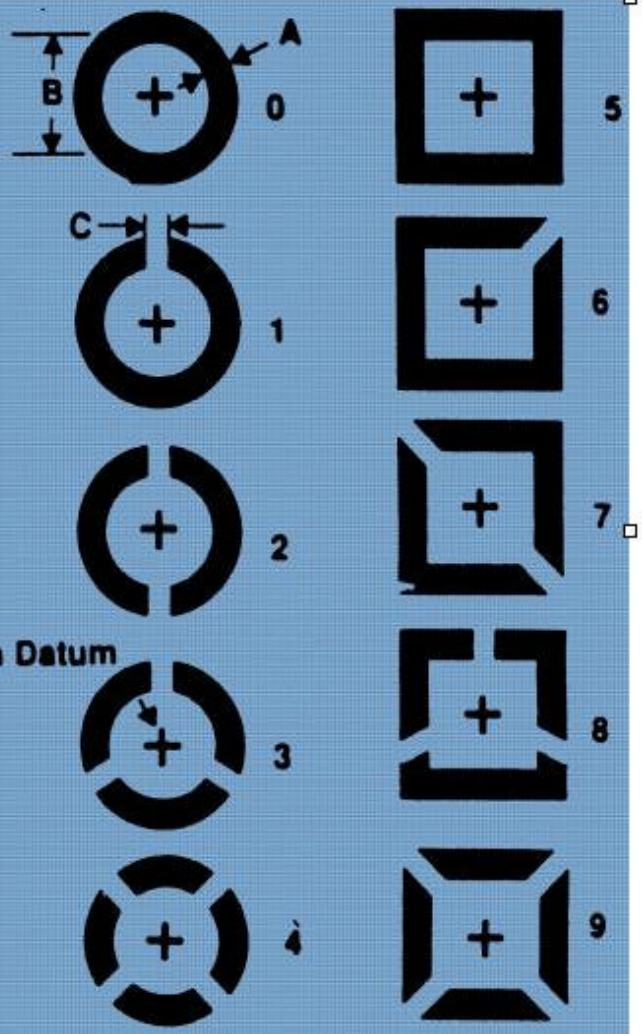
A point record may have:

- Feature and hole concentric at the point
- Feature only at the point
- Hole only at the point
- Tooling feature and hole at the point
- Tooling feature only at the point
- Tooling hole only at the point



Feature Descriptions (Cont.)

A/C	0.40	0.50	0.60	0.70	0.80	1.00 mm
B						
1.00 mm	400	401	402	403	404	405
1.13	406	407	408	409	410	411
1.25	412	413	414	415	416	417
1.38	418	419	420	421	422	423
1.50	424	425	426	427	428	429
1.63	430	431	432	433	434	435
1.75	436	437	438	439	440	441
1.88	442	443	444	445	446	447
2.00	448	449	450	451	452	453
2.25	454	455	456	457	458	459
2.50	460	461	462	463	464	465
2.75	466	467	468	469	470	471
3.00	472	473	474	475	476	477
3.25	478	479	480	481	482	483
3.50	484	485	486	487	488	489
3.75	-	490	491	492	493	494
4.00	-	495	496	497	498	499



Note: For the D4000 Series, the numbers in the matrix represent the first three digits in the "D" Field. The last number in the "D" Field corresponds to one of the shapes on this page. The numbers in the left column of the matrix (dimension "B"), are the choices for the inside diameter of the D4000 Series shapes. The numbers in the top row of the matrix (dimension "A") are the choices for dimension equalling the outside minus the inside diameter of the D4000 shapes. "A" dimensions also specify any slot (or "rib") width ("C").

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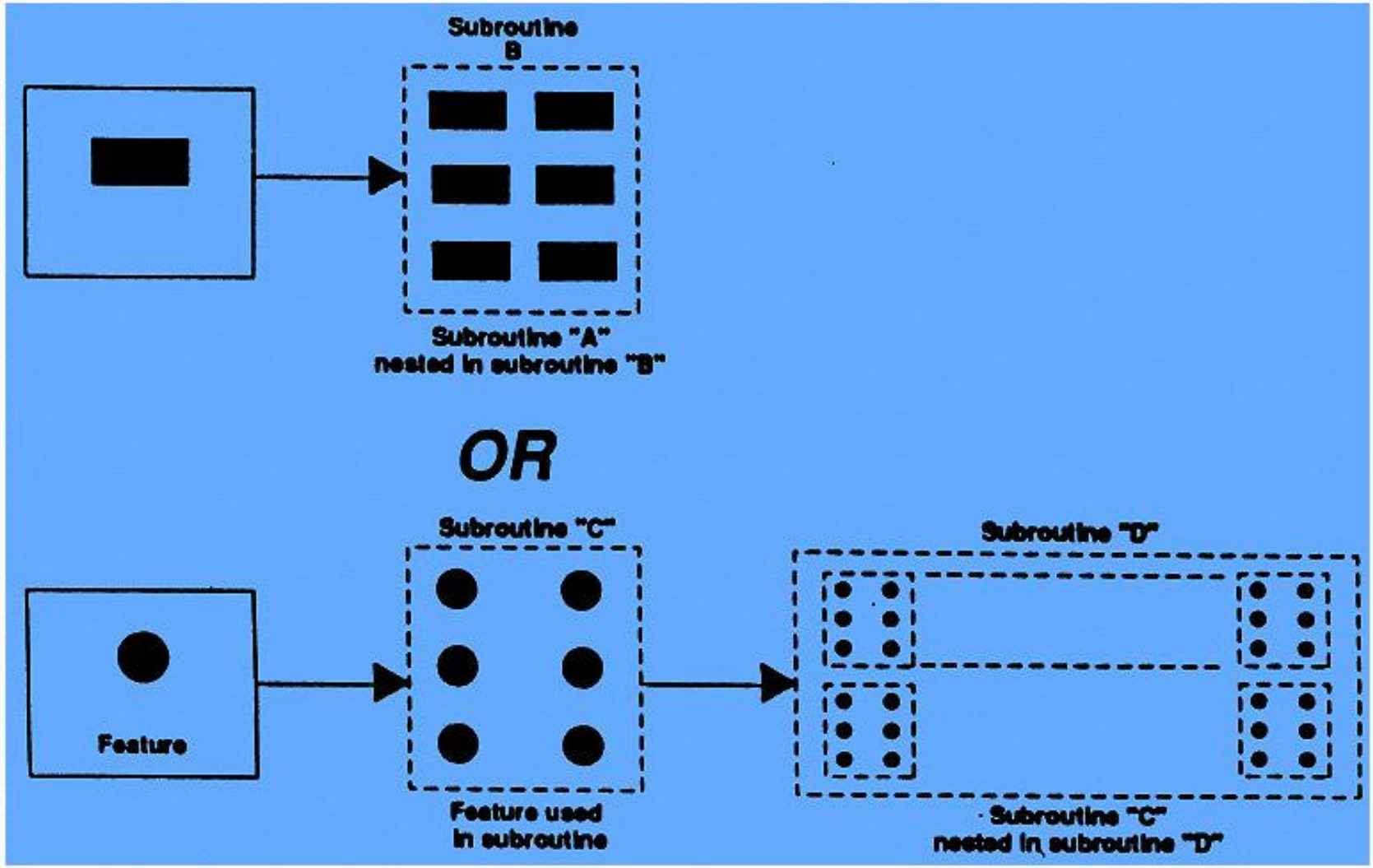
Subroutines



JPCA Initiative (IEC 61182-10)

New Work Item Proposal (NWP) submitted to IEC TC52 by Japan National Committee

(Sponsor is Japan Printed Circuits Association)

. Committee developed to elevate CAD to CAD transfer

- Chairman Mikio Takagi, Institute of Industrial Science

Sony	Hitachi Software	Kyoden
Zuken (REDAC)	Tokyo Inc..	Sharp
Fujitsu	Pentax	Unitech
Dai Nippon Screen	Mentor Graphics Japan	Ohron
NEC	Yokogawa Digital Co..	Sowa
CAD Japan	Uchida - Yoko	SUD
Toshiba	Cadence Design Sys.	Cadix
Izumia IC	Recal Redac-Japan	Hitachi

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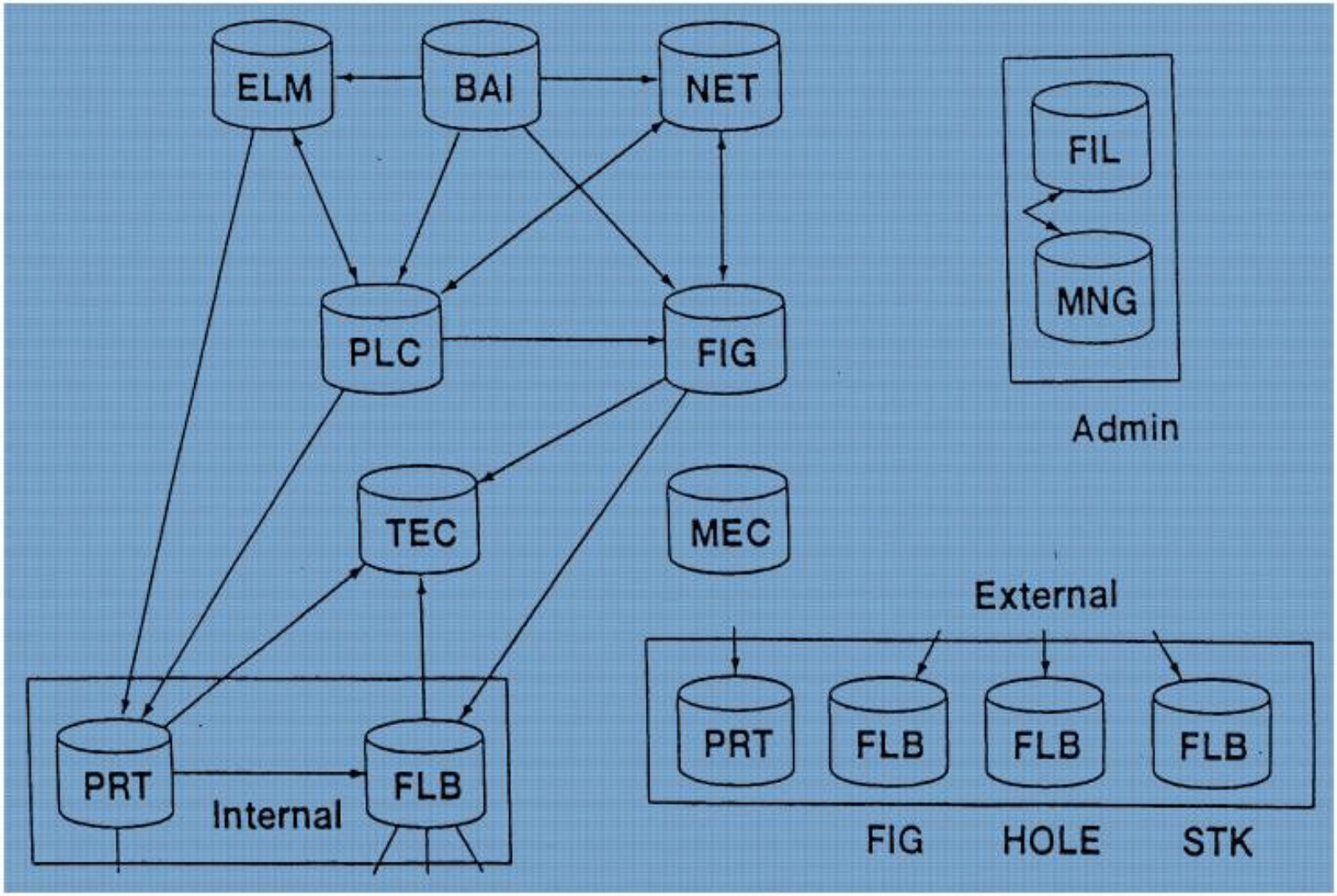
IEC 61182-10 File Structure

Category Name (Filename Extension)	Content
File Control Information (FIL)	•Interface control info (format name, version, output category list, date)
Management Information (MNG)	•Information for CAD data management (board name, name of drawing, Identification number)
Technology Information (TEC)	•Board characteristics (board size, number of layers) •Design spec. (clearance, line width)
Net Information (NET)	•Net information •Signal attributes (routing limitations)
Component Information (ELM)	•Component description (component identification number, component type, assembly process, catalog number)

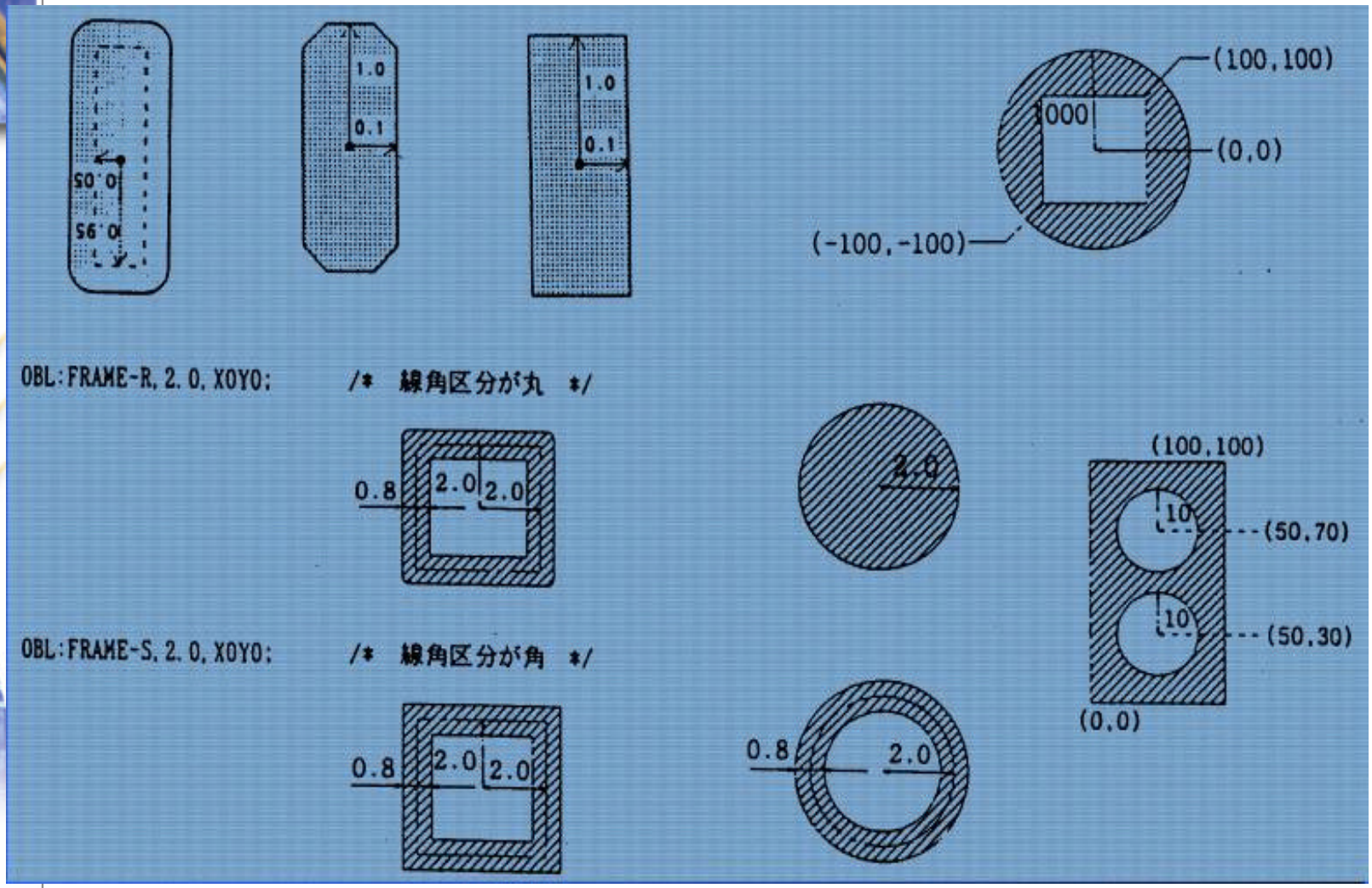
IEC 61182-10 File Structure

Category Name (Filename Extension)	Content
Primitive Figures Library (FLB)	•Figure-shape library (definitions of pads) •Hole library (definitions of holes) •Stack library (registration of pins and vias)
Part-shape Library (PRT)	•Part shapes (outlines, pins location, symbol patterns, inhibited areas, character strings)
Component Placement Information (PLC)	•Included components (identification number, registered part-shape name) •Component locations (coordinates, rotation angles, placement layers)
Figure Information (FIG)	•Description of patterns, vias, characters and other figure information) •Description of figure attributes (line types, line widths, logical layers, paint-ins)
Back-annotation Information (BAI)	•Description of addition/change/deletion information of components •Description of addition/change/deletion information of component-pins

IEC 61182-10 File Structure



Specified Primitives



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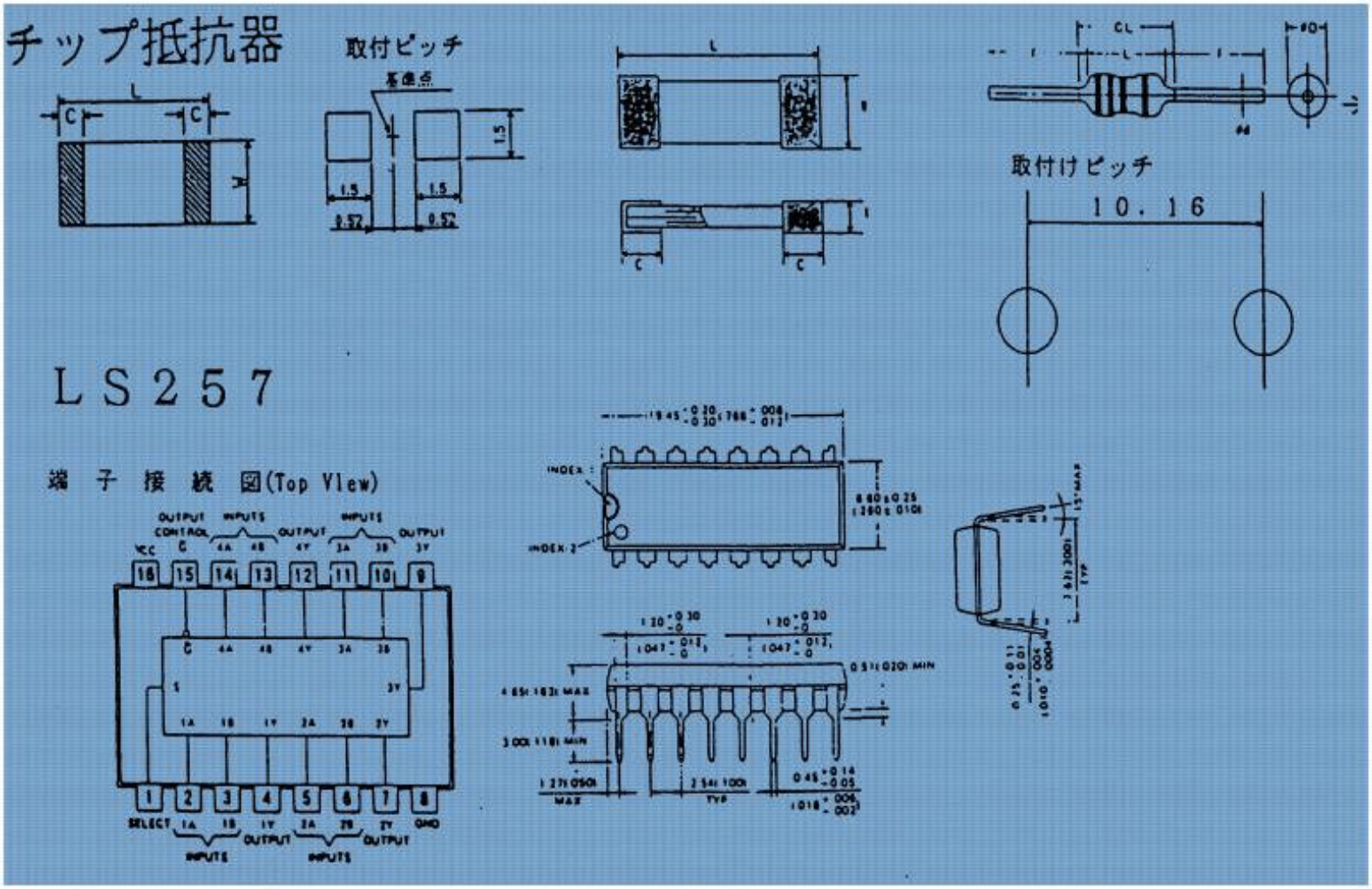
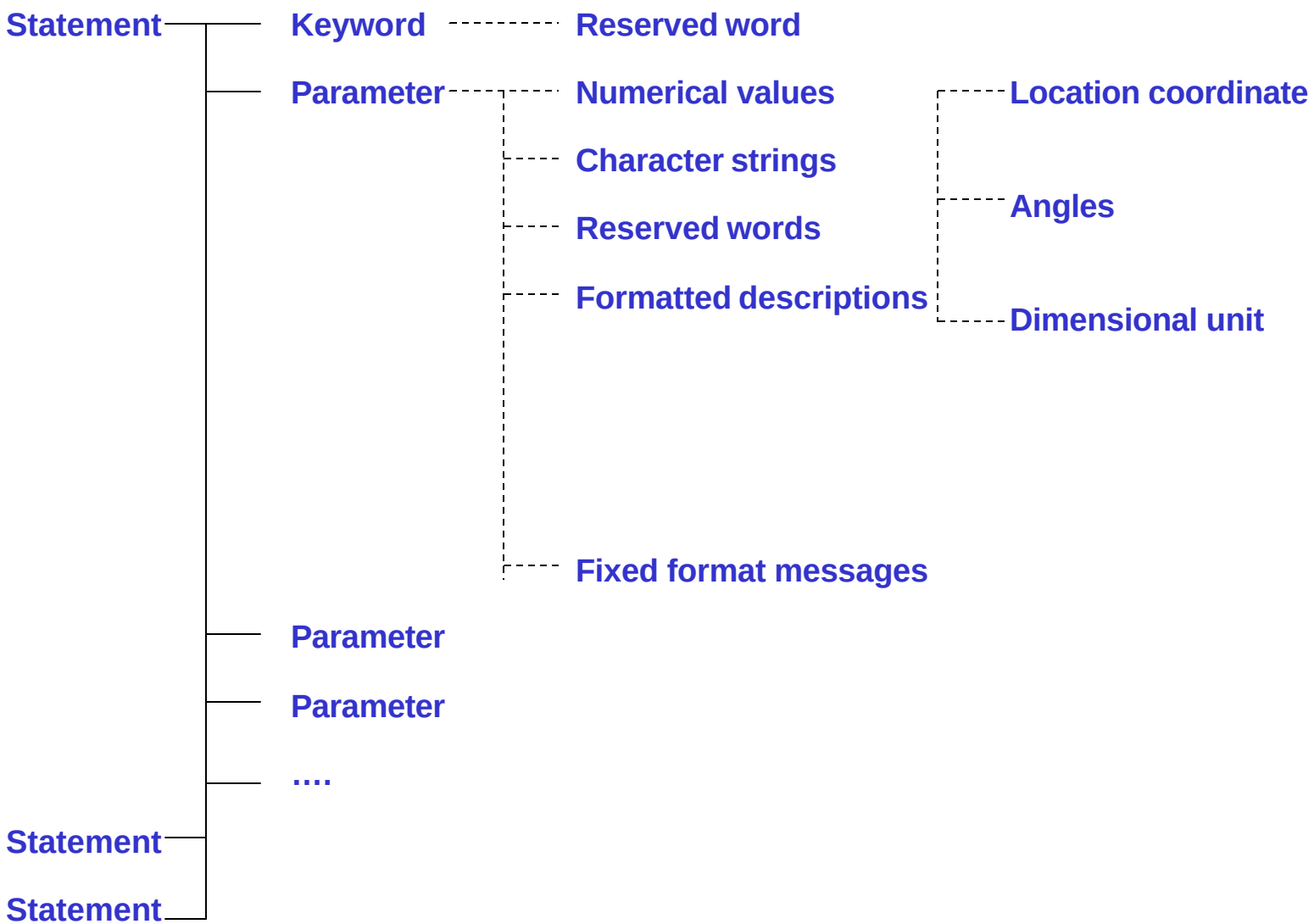
Component Description



Format Structure



ANSI Harmonization

- American National Standards Institute
- The Standard Developers
  - EIA - IPC - CFI
  - NIST - IEEE - ASMI - Others
- The Standards
  - IGES - CFI DR - Others
  - EDIF - VHDL
  - STEP AP210 - VERILOG
  - STEP AP211 - IPC-D-35X

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The Harmonization Process

Gather | Federate | Test | Harmonize | Submit | Integrate | Insertion

Develop Data Model Repository

Define Classification Scheme

Collect Test Vehicles

Provide Support Infrastructure

Develop Data Models

Construct Database from Federated Model

Run Test Cases

Report Progress to HPS

Educate

Establish MOUs

Develop Application Protocols

Identify Data Voids

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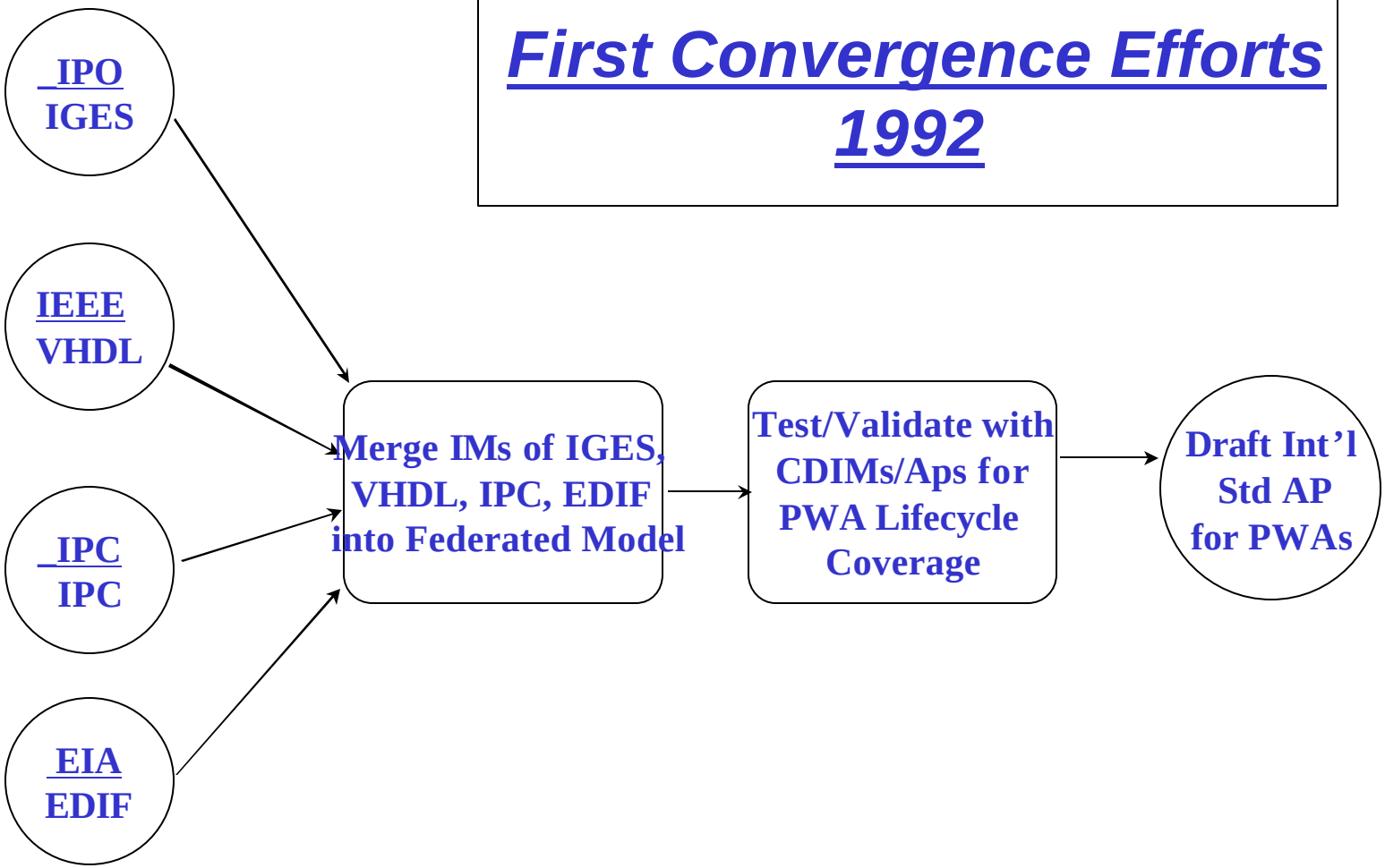
Federated Model Harmonization



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International Electrotechnical Commission Committees

- TC3 Symbology
- TC52 Printed Circuit
- TC93 Design Automation
  - WG1 - Electrotechnical Data Harmonization
  - WG2 - Component, Circuit and System Description Languages
  - WG3 - Electrotechnical Product Design Interchange Formats
  - JWG11 - Printed Board Electronic Data Description and Transfer
  - WG5 - Testing and Data Conformance

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Data Transfer Techniques

- Gerber Machine Language the start
- Gerber Data Still the Norm
- Data not Consistent from Different CAD Systems
- Many Problems With Large Files
- Many Problems with Line Drawn Features
- Test Information Tools not always correct

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Current Realities

- Better Design Tools - CAD & CAM
- Better Manufacturing Tools - CAM
- Better Electronic Communication
  - Internet-WWW-High Speed Modems
- Better Understanding Capabilities (SPC)
- Greater Expectations
- Old-Fashioned Data Transfer
- Quick-Turn Environment - 10 day turns
- *New formats address the above issues*

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Industry Complacency

- Competitive stature - No Complaints
- Extra costs - Hidden or built-on
- CAD Vendors have had no incentive
- The Printed Board and Assembly Companies made it work
- CAE and Engineering has the spotlight
- Slower speeds, less dense, Designs weren’t as critical

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Industry Complacency

- CAM tools were able to “Reverse Engineer” from artwork
- Manufacturing wasn’t as sophisticated
- Large OEMs have their own point solutions
  - Dollars Invested
  - Changing OEM/contract manufacturing environment

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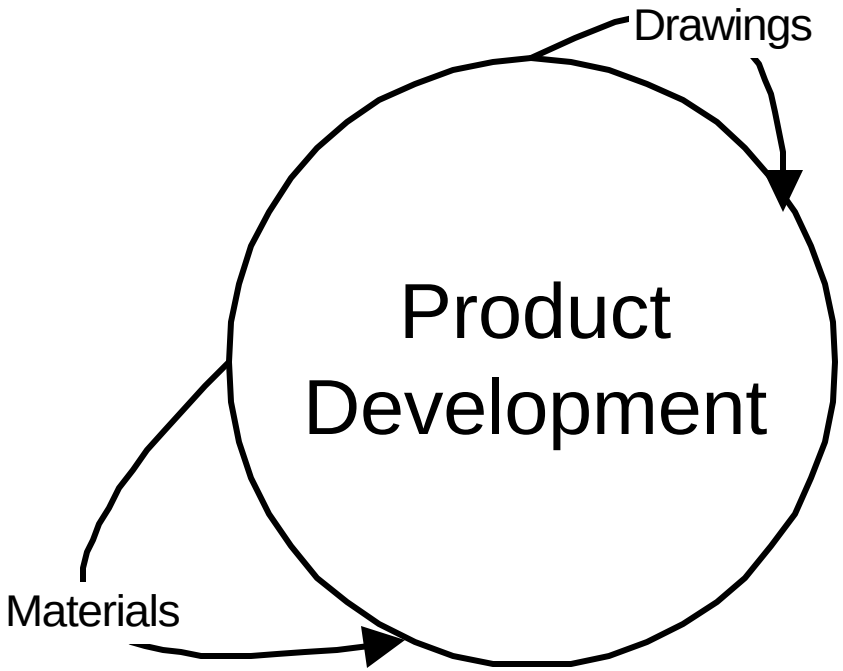
In-House Development- Past

Design
Fabricate
Assemble
Mock-Up
Test
Burn-in
Retest
Ship



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Partnered Development

Design

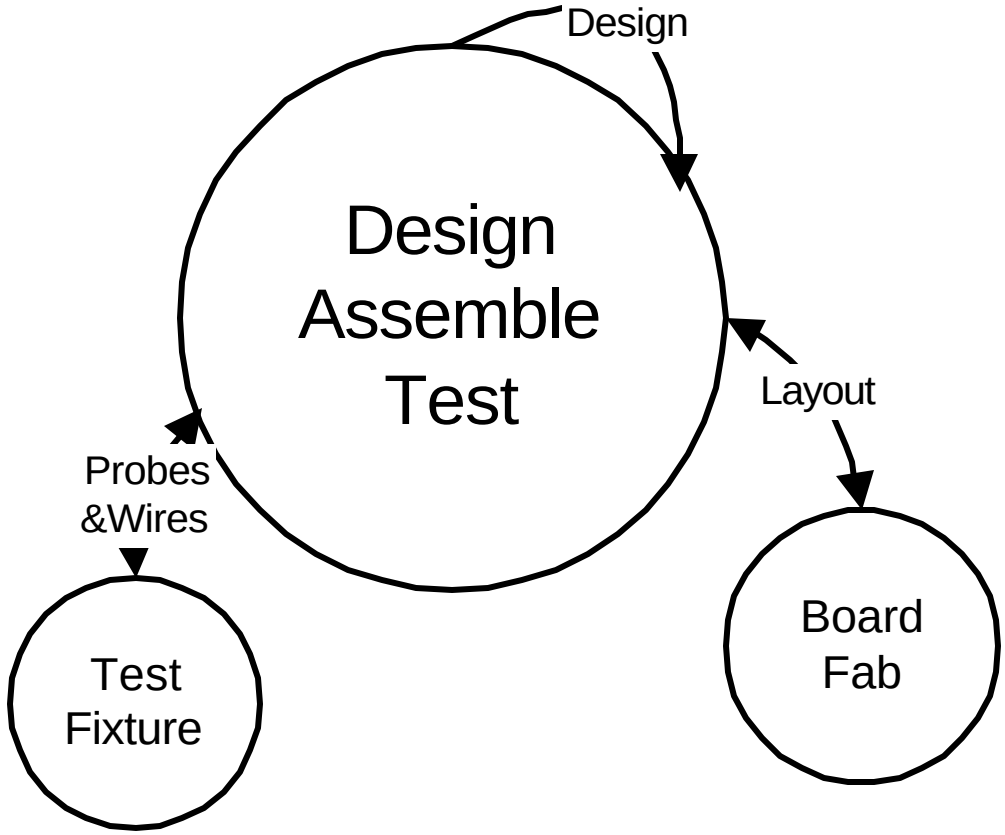
Assemble

- Outsource
- Fabrication

In-Circuit Test & Rework

- In-house Test Development
- Outsource Fixture Build

Final Assembly & Test



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Distributed Development- Present

Design

Outsource

Board Fabrication

Prototype Test

Test Development

Outsource

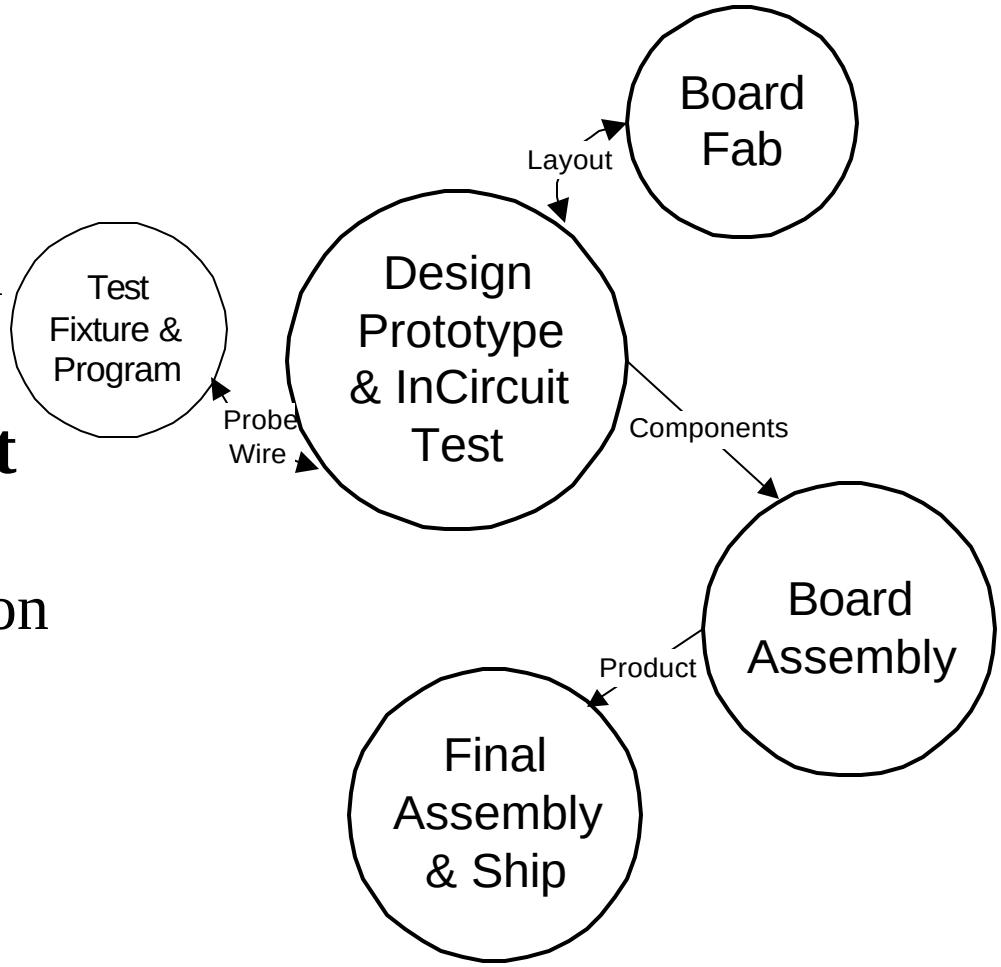
Fixture Fabrication

Outsource

Board Assembly

Outsource

Final Assembly



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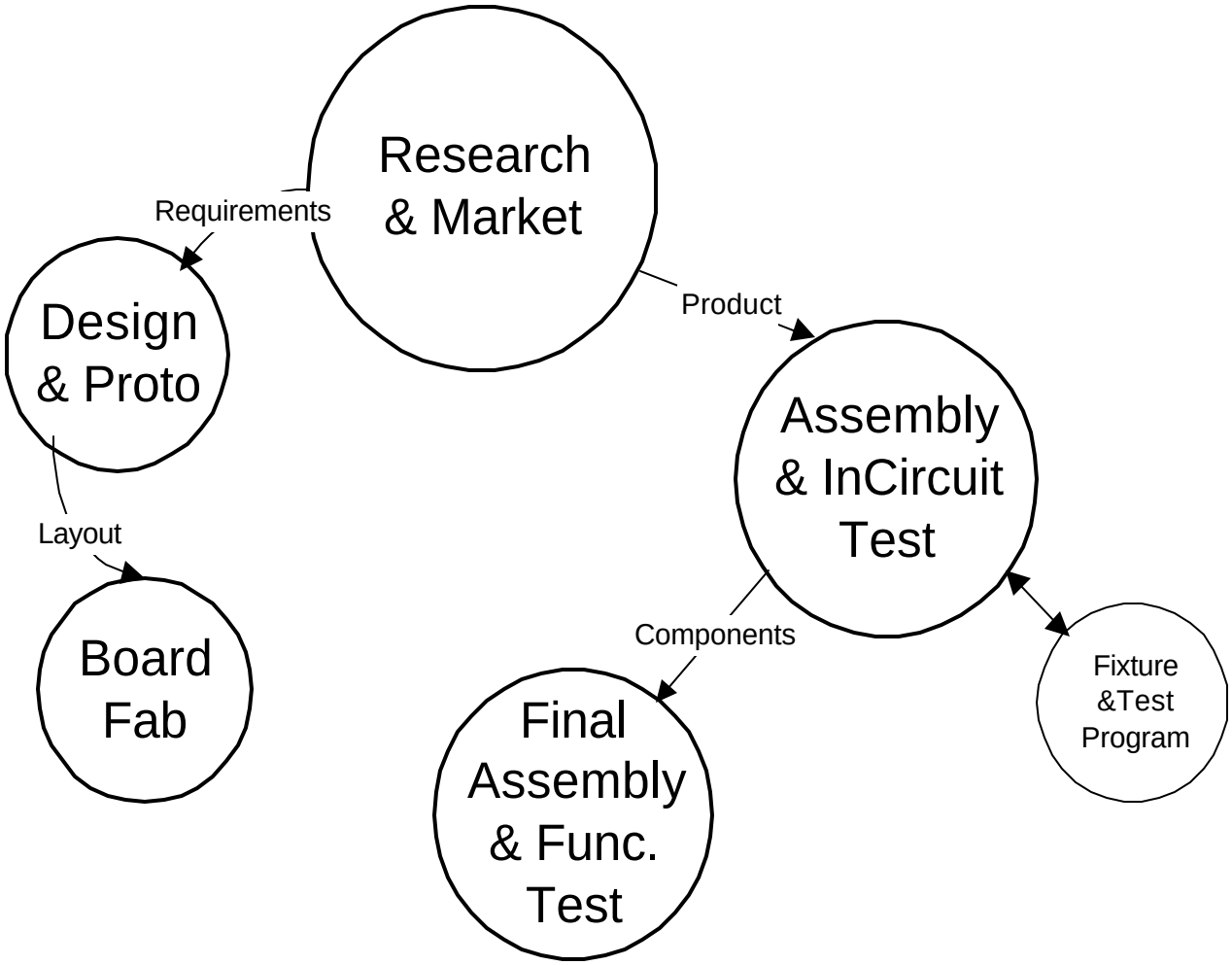
Sarah Lee Development-Future

Outsource
Design
Outsource
Fabrication
Outsource
Test Development
Outsource
Assembly & Test



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Data Transfer Solution

A continuous program to serve the data transfer needs of the Electronics Interconnection Industry and its' customers

- Parses large data files into Process Oriented Segments
- Promotes user oriented ASCII formatting
- Establishes Compliance Test Modules for data verification
- Encourages International participation through the IEC

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The GenCAM Initiative

- Start a program to address the Data Transfer Solutions (DTS) such as DTS '97, DTS '98, DTS '99, DTS '00, DTS '01, DTS '02…..
- Closely coupled to the IEC 61182-10 format developed by the JPCA
- Builds on the capabilities of Mitron/IGI, two CAM providers who would help provide input
- An IPC committee and subcommittes open to users, manufacturers, assemblers, testing experts and CAD/CAM tool developers.

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Benefits of IPC-2511

- Saves Time decreases time to market
- Better quality - less misinterpretation
- Improves communication among members of the supply chain
- Easy to use - less time to train
  - ☞ less time to implement
- ANSI standard owned by the industry
- Reduces data transfer time & confusion
- Method for improvement feedback
- Establishes capability for a single file

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Partial Summary of IPC's data exchange efforts

- IPC has a long history of focusing on the data exchange problem
  - Educating the industry about advantages of replacing Gerber for more than 30 years
  - IPC D350 standard released in the '70's
  - IPC D356 BBT released in late '80's
  - IPC-2511 (GenCAM) development started by DTS'97 committee in 1997

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Partial Summary of Valor's Data Exchange Efforts

- Valor has been developing ODB++ format, tools, and educating customers for the past 8 years
  - ODB format and Genesis 2000 CAM software for bare board fabrication in 1995
  - ODB++ format and Enterprise 3000 DFM software released in 1997, adding component descriptions
  - ODB++ format extended again with BOM/AVL information for Trilogy 5000 CAM for Assembly in 1999
  - ODB++(X) XML-based format released in 2000
  - All major EDA tools have ODB++ interfaces today as well as over 20 third party software vendors

Where is the Industry now with Data Standards?

- In spite of Valor and IPC efforts, the majority of the Industry is still using Gerber-based data exchange and treating the subject with indifference despite the costs they incur
- Industry press has created an image of competition between the IPC and Valor, dubbing it the “Data Format Wars”
- Some parties remain on the sidelines seeing who will “WIN” the war
- Meanwhile, inadequacies of current methods continue to hurt the PCB industry

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Vision Statement

- The IPC and Valor agree to best serve the needs of the PCB industry, both parties will submit their data exchange formats, GenCAMX and ODB++(X), to the NEMI VFIIP committee for the purpose of convergence into a single XML-based industry standard

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Goals and Objectives

- Eliminate the use of Gerber and related old, non-intelligent formats for data exchange
- Unite IPC/NEMI/Valor behind a single Industry standard for data exchange
- Make the new standard XML compliant
- Combine the best of both ODB++(X) from Valor and GenCAMX from IPC
- Focus on providing solutions as well as standards
- Formalize the converged standard using ANSI procedures

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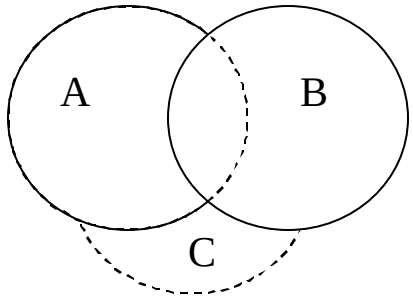
Information Model Comparison

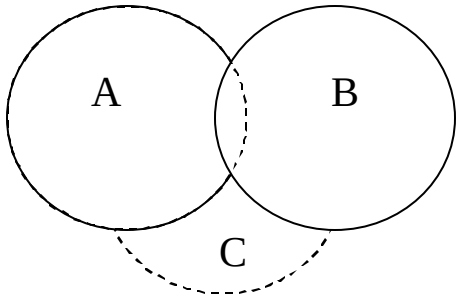
A ODB++ Info Model

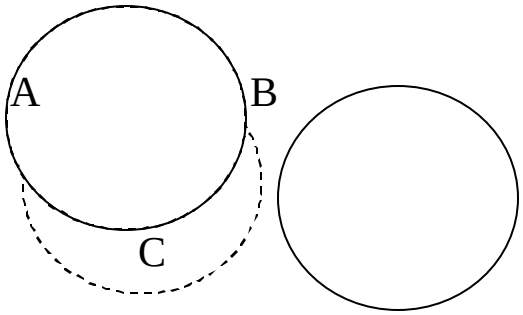
B GenCAM Info Model

C "New Stuff"

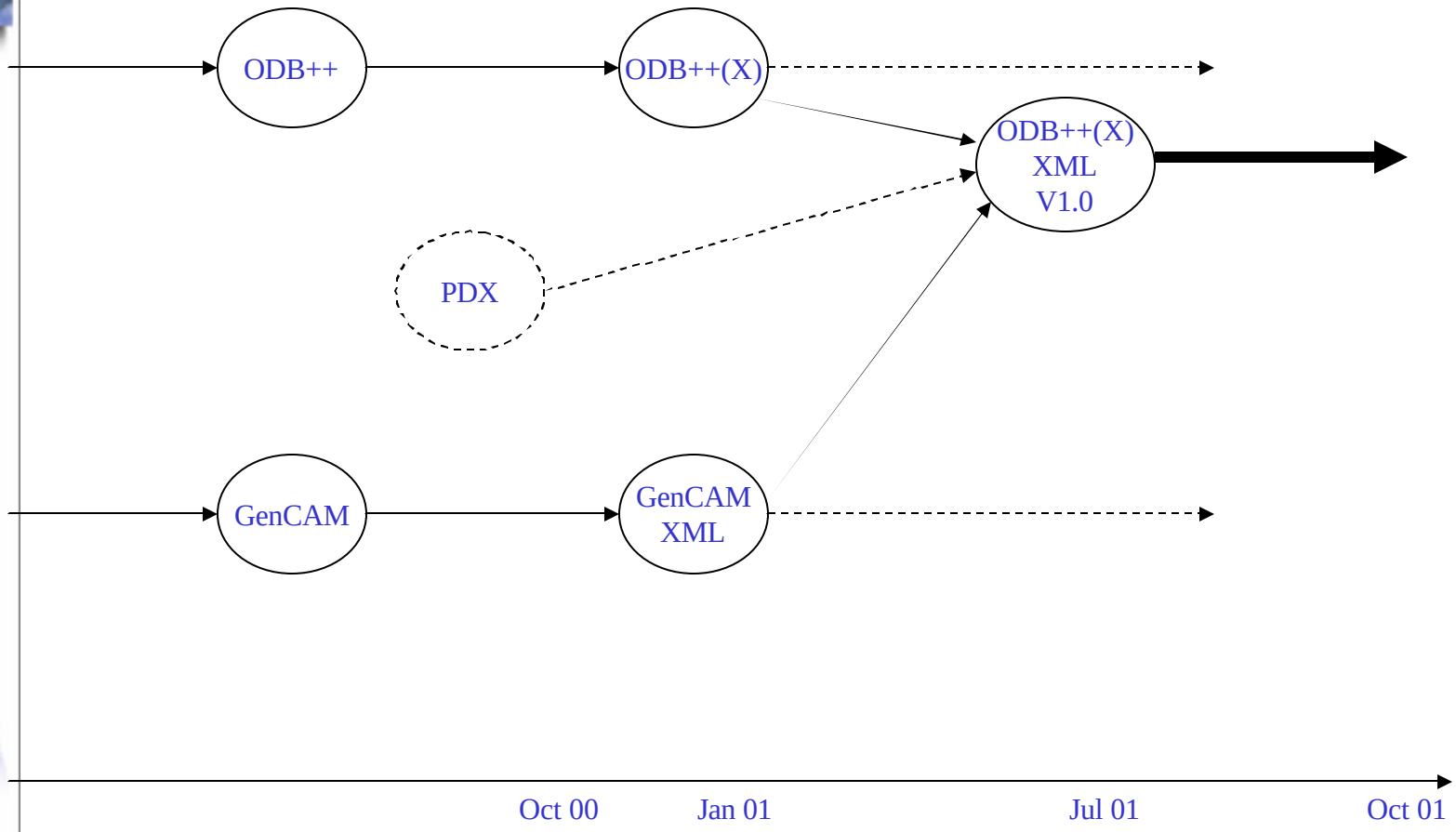
- Select base model
- Add what's missing
- Resolve overlaps
  - Where, how much
  - Names
  - Structure
  - Relationships
  - References







GenCAM-ODB++ Convergence
Valor Starting Point



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Convergence Project Objectives

- Develop Technical Recommendation for CAD/CAM data exchange format geared towards:
  - Wide adoption
  - Timely deployment
- Build on strengths of current solutions:
  - GenCAM
  - ODB++
- Encourage early adoption & implementation thru tool development, demonstrations, and partnerships with other consortia/industry groups.

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Organization/Approach

- **Convergence Technical Team (CTT)**
  - Responsible for creating technical recommendations
  - Subgroups of Technical Team will work in Parallel to Evaluate Major sections of existing formats to determine most efficient starting point.
  - Open to All Parties with a stake in the outcome.
  - Work is Internally Focused.
- **Convergence Management Team (CMT)**
  - Responsible that Project focus is on needs of Industry.
  - Responsible for scope, timeframe, and goals of project.
  - Structured membership criteria with Emphasis on the Customer.
  - Responsible for Accepting Technical Recommendation and providing all External communications (to press, other organizations, etc.).

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Convergence Success

- The best of both worlds
- Version 1.0 released February 2004
- Available for free download
- XML schema is included
- Takes advantage of the latest XML
- webstds.ipc.org web site being rebuilt
- Includes all web-based standards
- The format of choice for today and tomorrow

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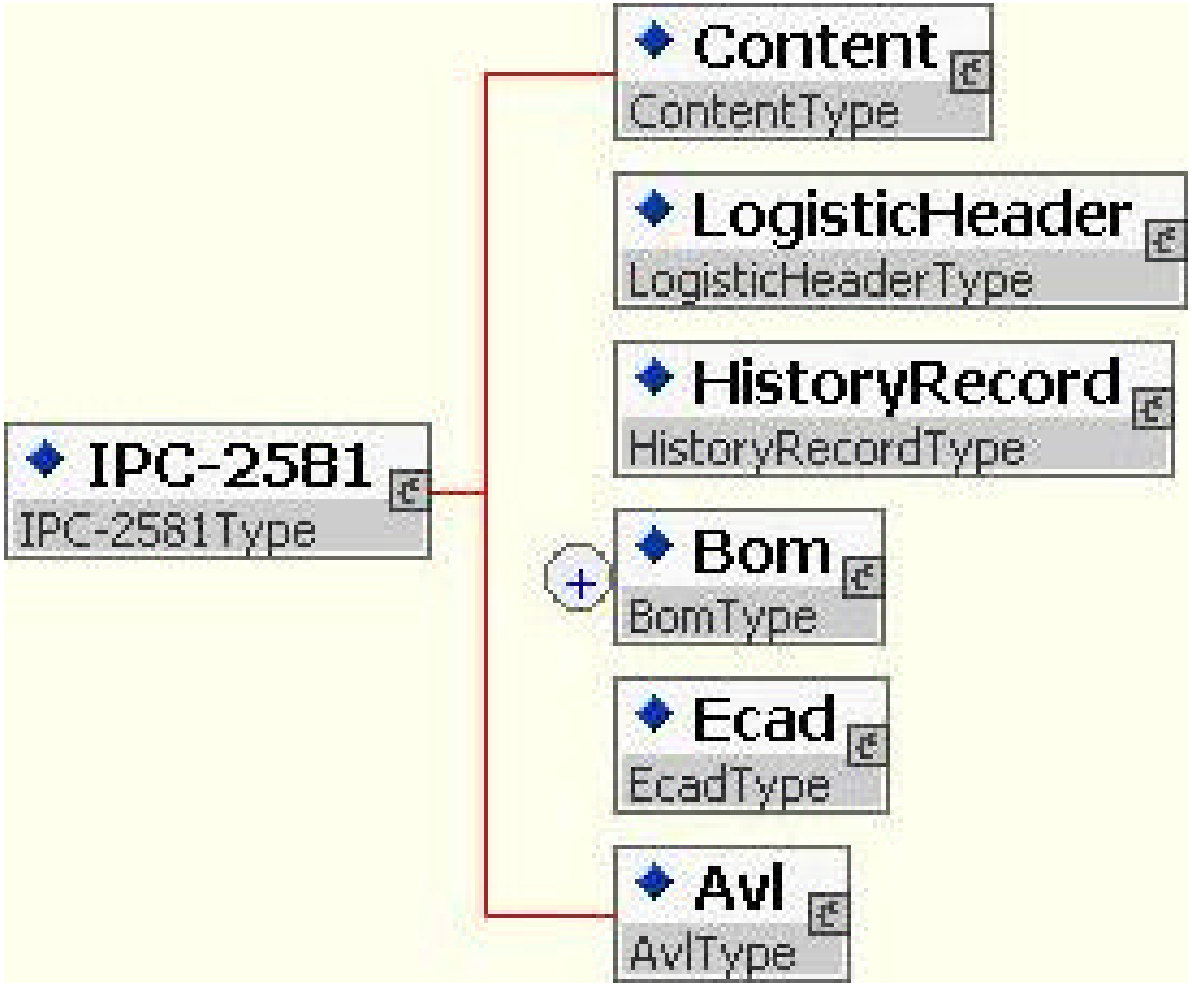
IPC Number/ Function	-XXX1 Generic	-XXX2 Admin	-XXX3 Docmnt	-XXX4 Board Fabric.	-XXX5 Bare Bd.Test	-XXX6 Assemb Manuf	-XXX7 Assembl Test	-XXX8 Comp. & Mat'l	-XXX9 Informat Modeling
IPC-2500 Message Broker	IPC-2501 Published		IPC-2503 Working						
IPC-2510 Product Data GenCAM	IPC-2511 Published	IPC-2512 Publish	IPC-2513 Publish	IPC-2514 Publish	IPC-2515 Publish	IPC-2516 Publish	IPC-2517 Publish	IPC-2518 Publish	
IPC-2520 Quality Product Data				IPC-2524 Publish					
IPC-2530 SRFF Process Data Recipe File	IPC-2531 Published								
IPC-2540 Shop Floor Communication	IPC-2541 Published					IPC-2546 Publish	IPC-2547 Publish		
IPC-2550 Execution Systems	IPC-2551 Working								
IPC-2560 Enterprise Communication									
IPC-2570 Supply Chain Communication	IPC-2571 Published					IPC-2576 Publish	IPC-2577	IPC-2578 Publish	
IPC-2580 Application Product Data	IPC-2581 Published								

IPC-2581 Basic Structure



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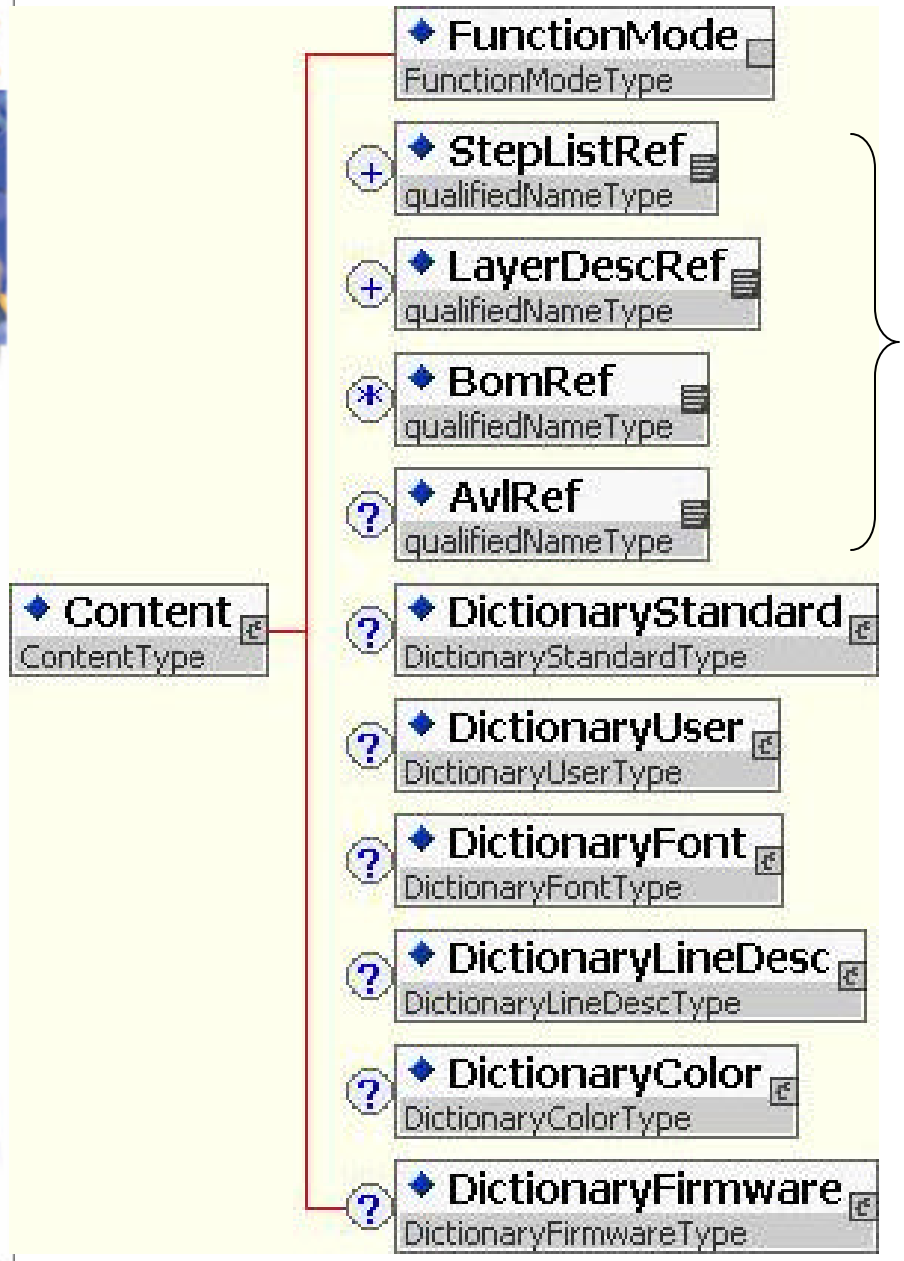

References to sections contained in the file

Dictionary Sections for predefined shapes, fonts, line descriptions, color, and firmware

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Function Mode

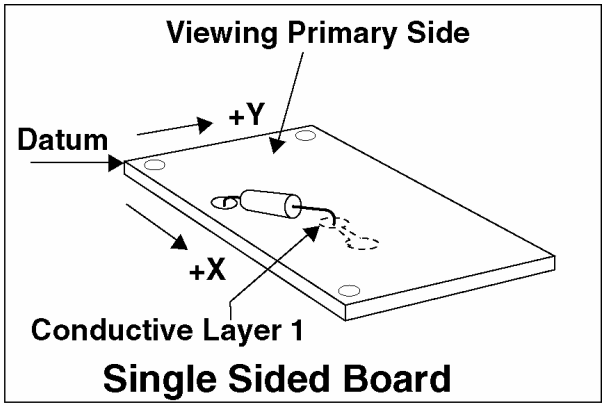
Name	Full	Design			Fabrication			Assembly			Test		
		1	2	3	1	2	3	1	2	3	1	2	3
Hierarchical layer/stack instance files	Y	N	Y	N	N	N	N	N	N	N	N	N	N
Hierarchical conductor routing files	Y	N	Y	N	N	N	N	N	N	N	N	N	N
BOM (Components and Materials)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	N	Y	Y
AVL (Components and Materials)	Y	N	Y	Y	N	Y	Y	Y	Y	Y	N	N	Y
Component Packages	Y	Y	Y	Y	N	N	Y	Y	Y	Y	N	Y	Y
Land Patterns	Y	N	Y	Y	N	N	Y	N	Y	Y	N	Y	Y
Device Descriptions	Y	Y	Y	Y	N	N	N	N	N	Y	N	N	Y
Component Descriptions	Y	Y	Y	Y	N	N	N	Y	Y	Y	N	Y	Y
Soldermask; Solder Paste Legend Layers	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Drilling and Routing Layers	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Documentation Layers	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Net List	Y	Y	Y	Y	N	Y	Y	N	Y	Y	Y	N	Y
Outer Copper Layers	Y	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Inner Layers	Y	N	N	Y	Y	Y	Y	N	Y	Y	N	N	Y
Miscellaneous Image Layers	Y	N	Y	Y	N	Y	Y	N	Y	Y	N	Y	Y
DFX Analysis	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

Printed Board Viewing

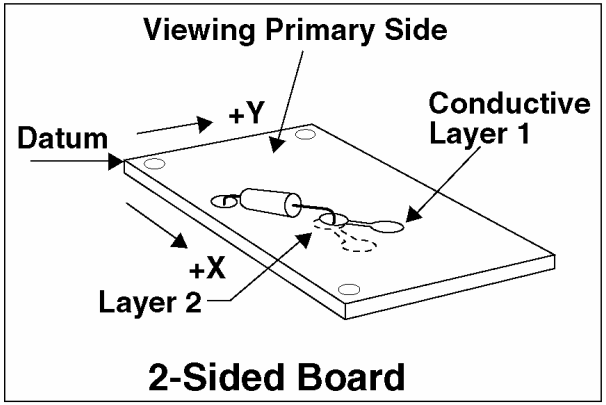
All layers are defined from the “primary side” of the HDI structure.

The designer dictates which side is the primary side.

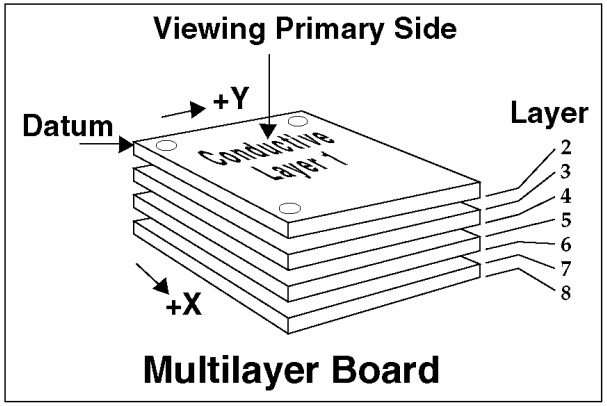
The first conductive layer is layer 1, closest to the primary side.



Single Sided Board



2-Sided Board



Multilayer Board

Note: For those printed board assemblies that have components on both sides, any side may be designated as the primary side and used to define **Conductive Layer 1**.

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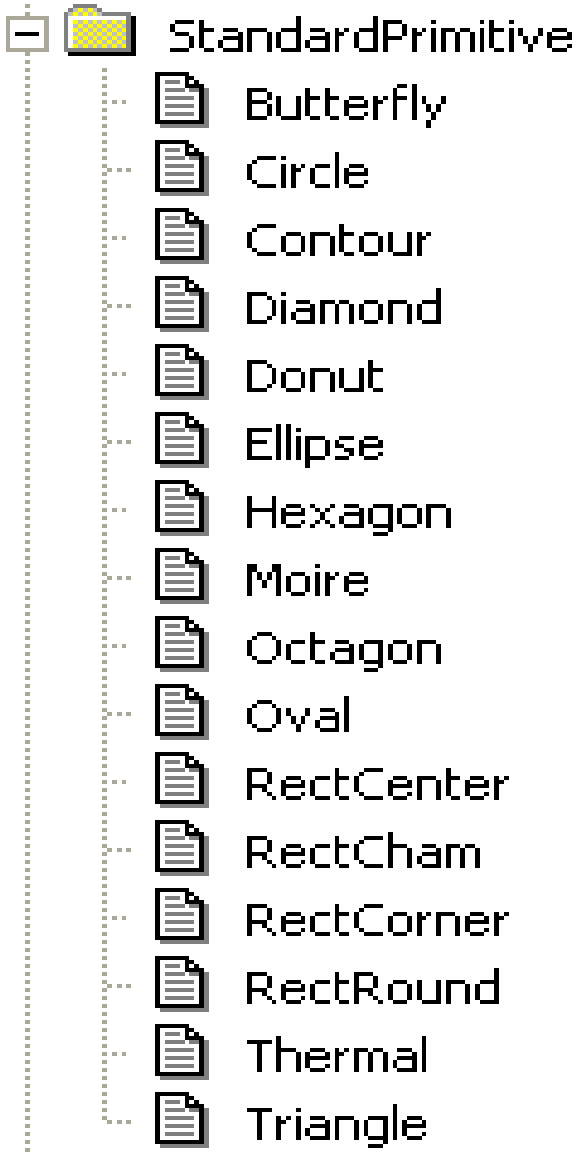
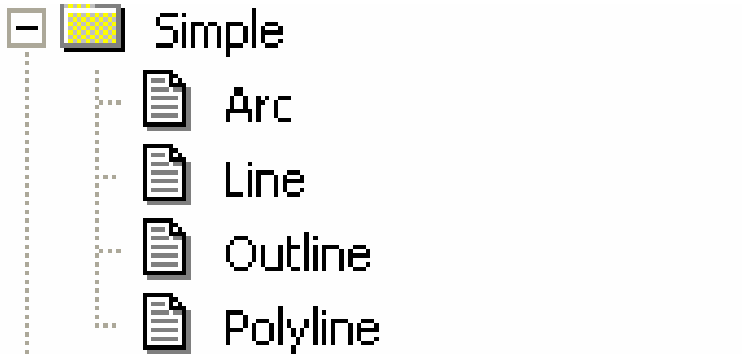
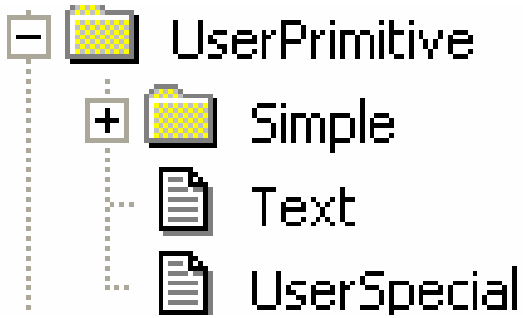
Standard and User Dictionaries







All Dictionary elements are Substitution Groups

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XML is Human Readable

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<EntryStandard id = "Diamond1">
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</EntryStandard>

<EntryStandard id = "Diamond2">
      <Diamond width = "6.00" height = "8.60"/>
</EntryStandard>

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</EntryStandard>

<EntryStandard id = "Donut2">
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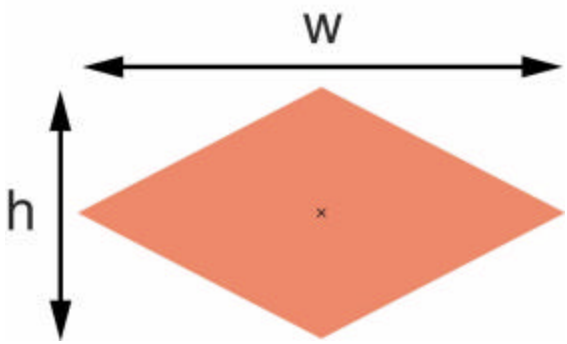

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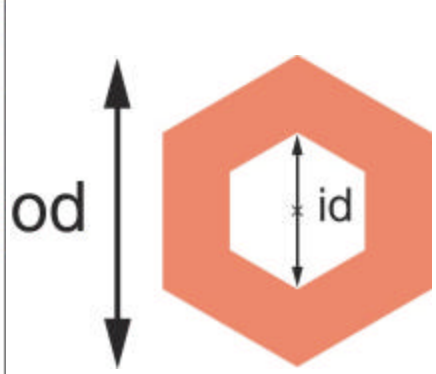
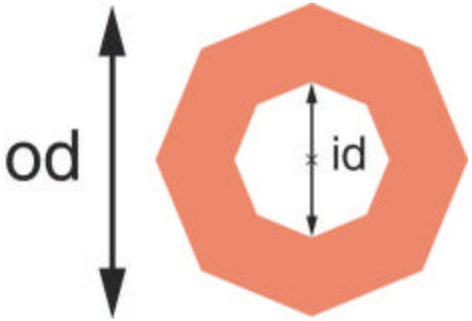
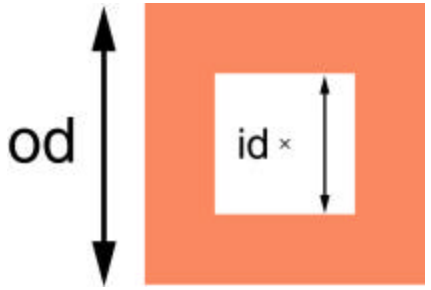
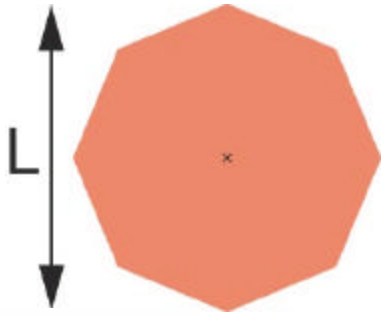
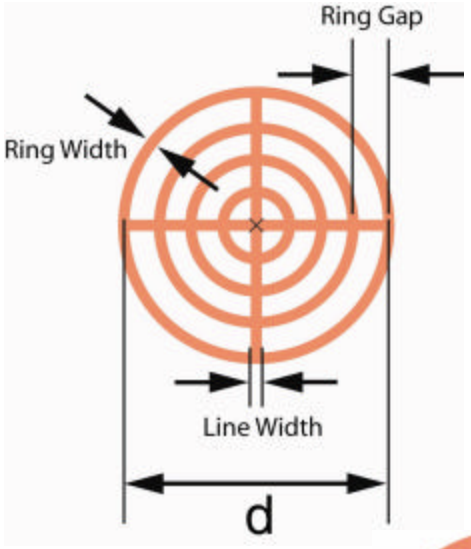
Other Standard Primitives

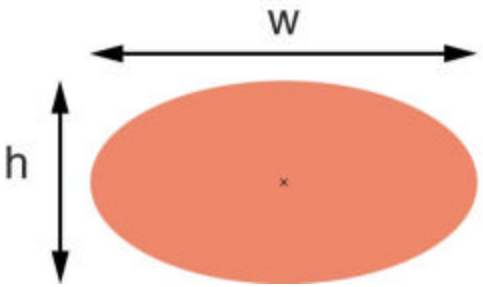


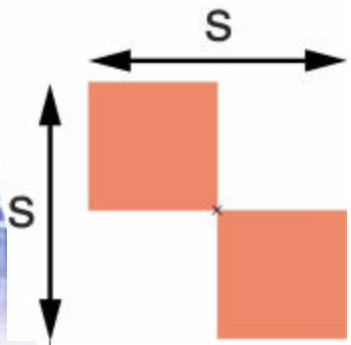


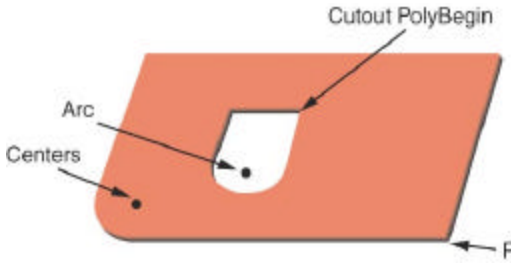


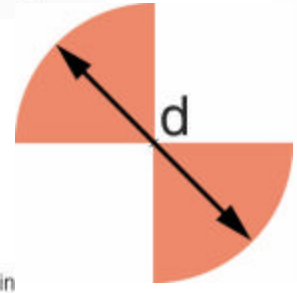


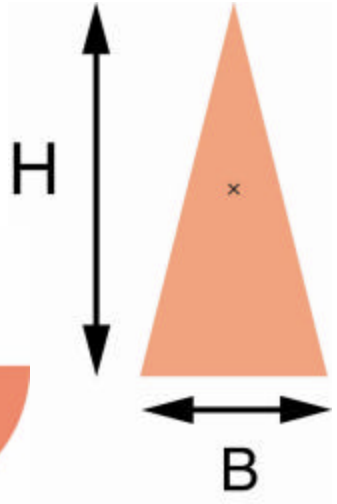












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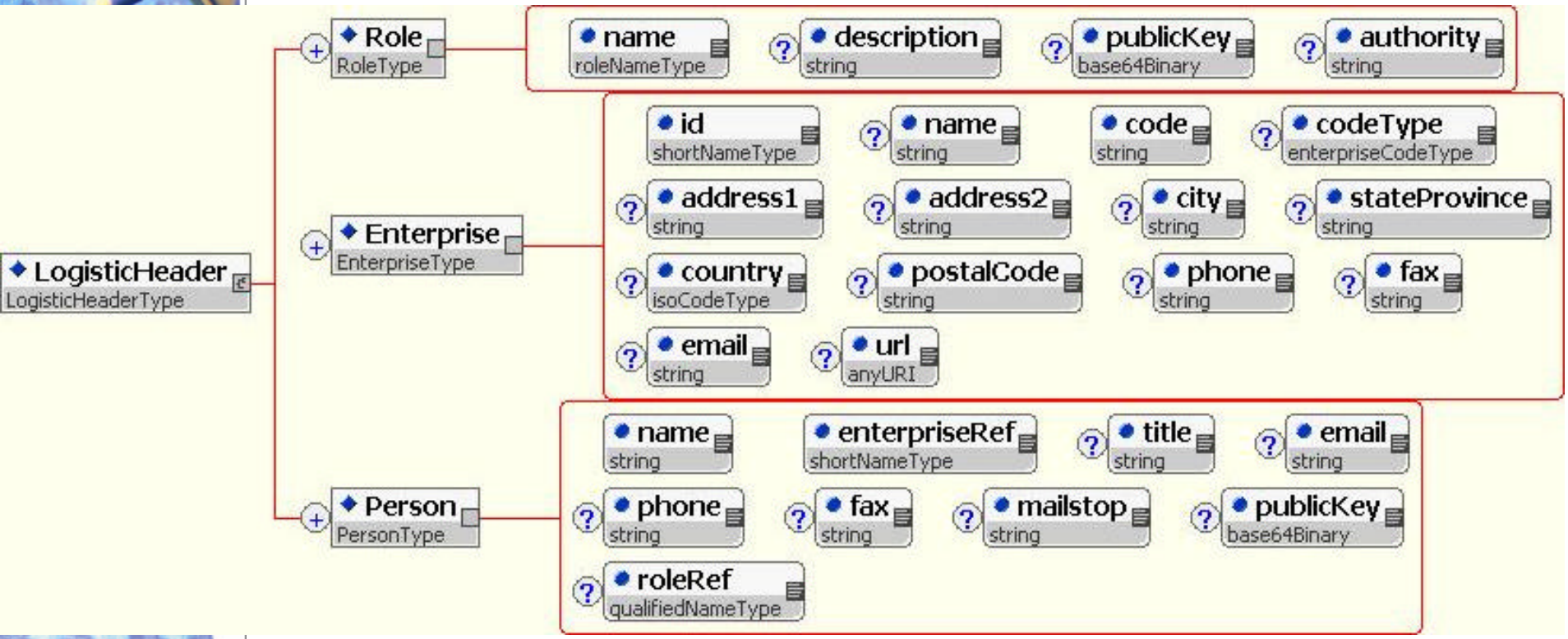
Logistic Header



Indicates file owner as well as Approved Vendors

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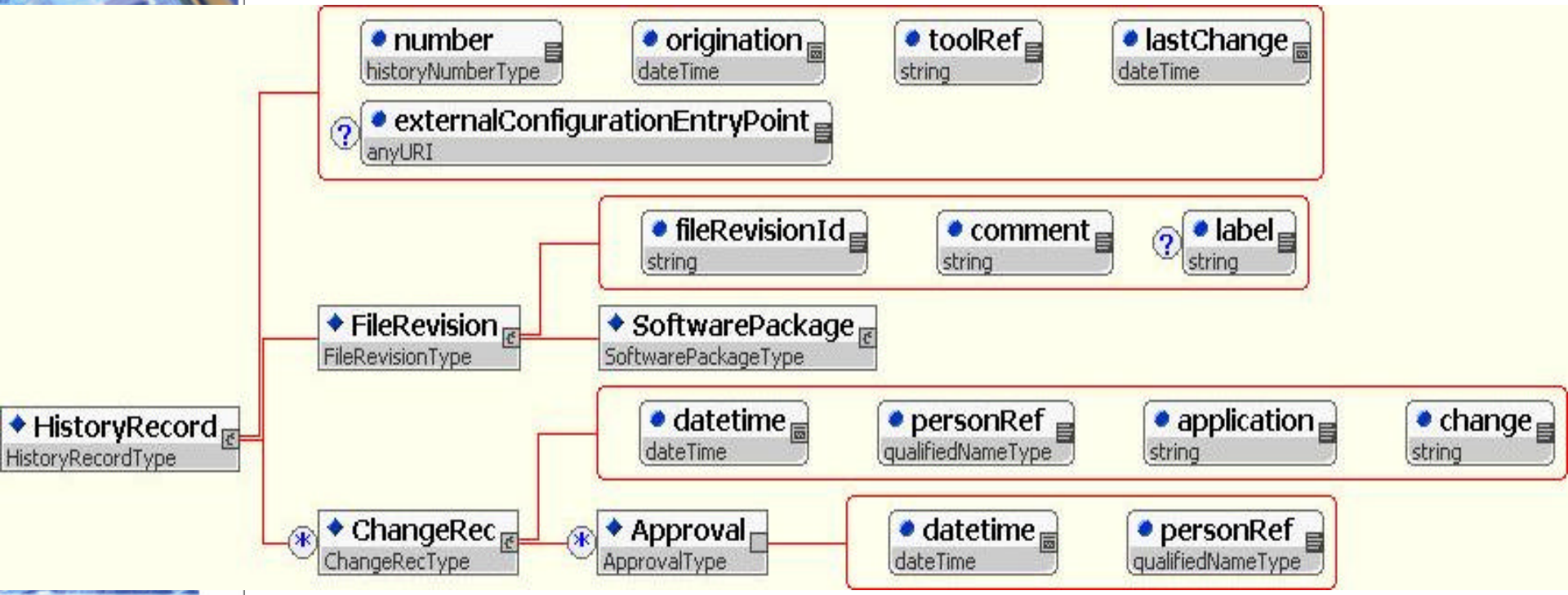
History Record



Configuration Management Section

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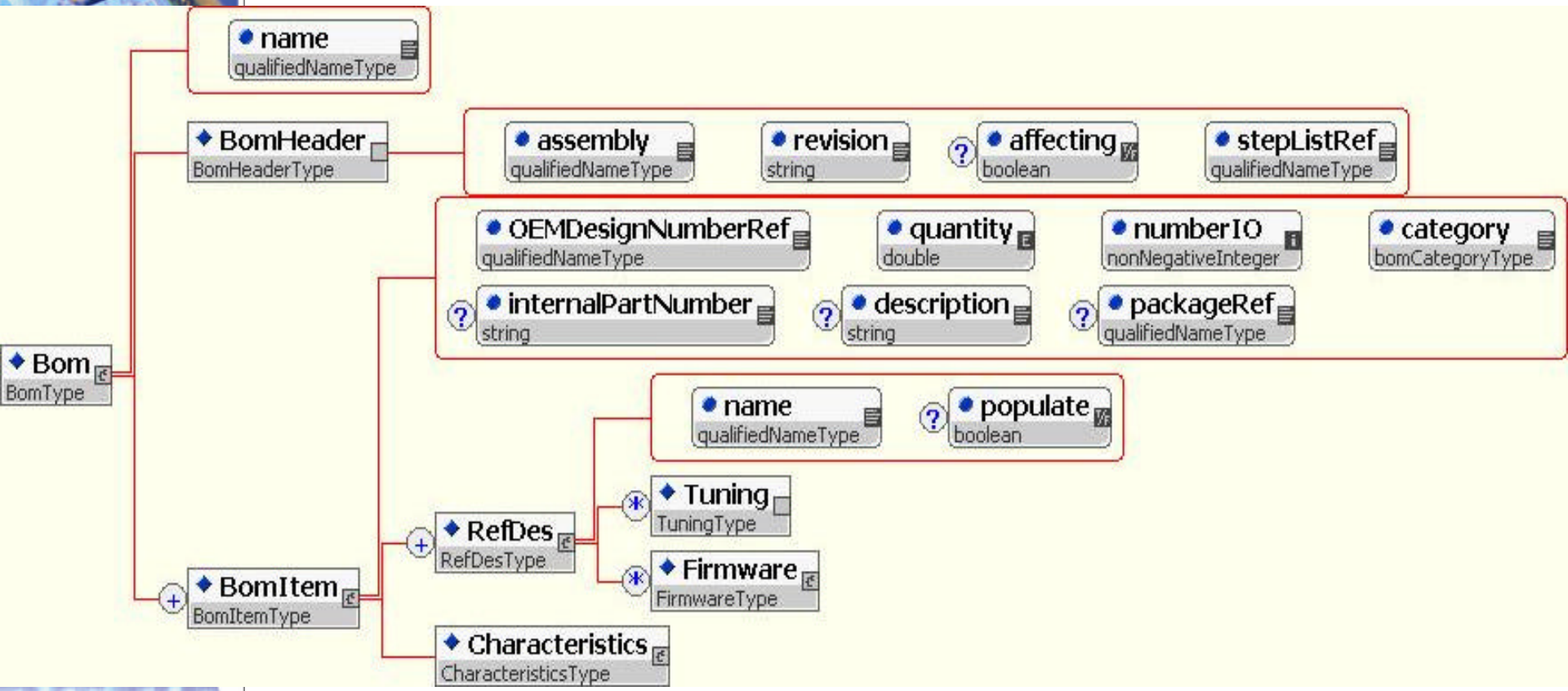
Bill of Materials



One to many BOMs including one for Board Material

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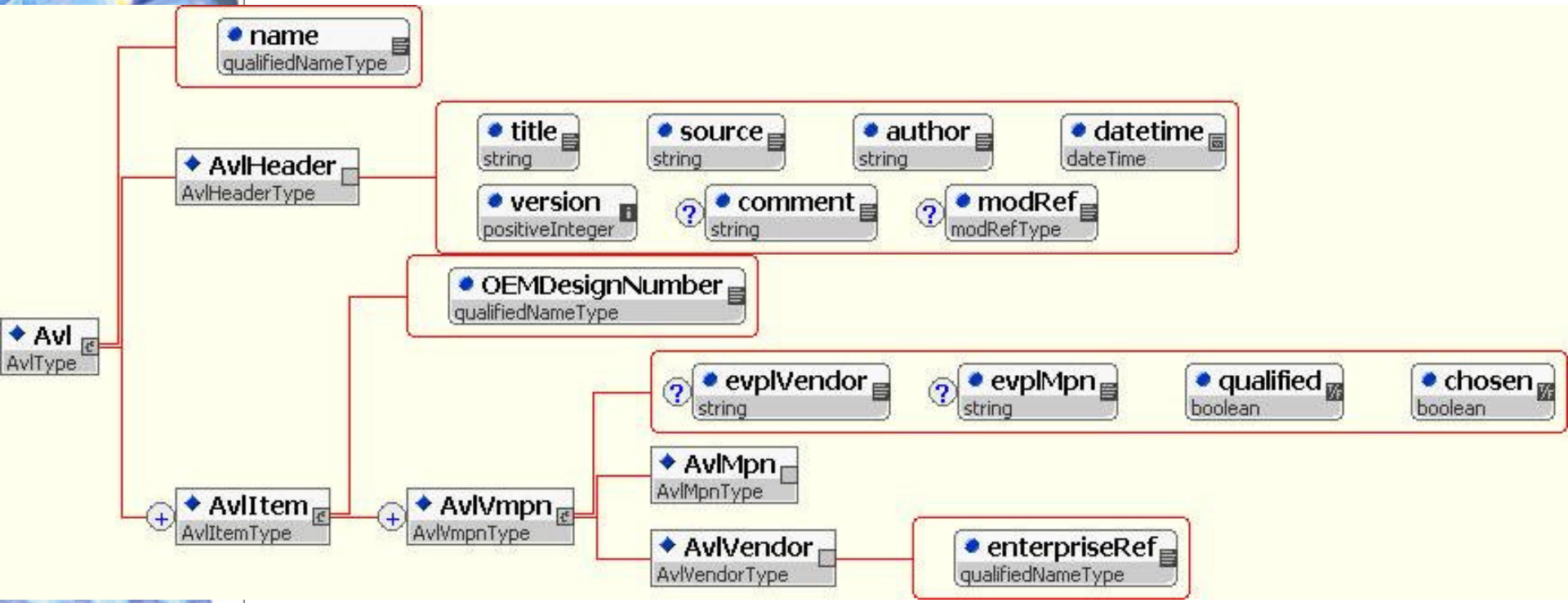
Approve Vendor List



One master list referenced to BOM item & enterprise

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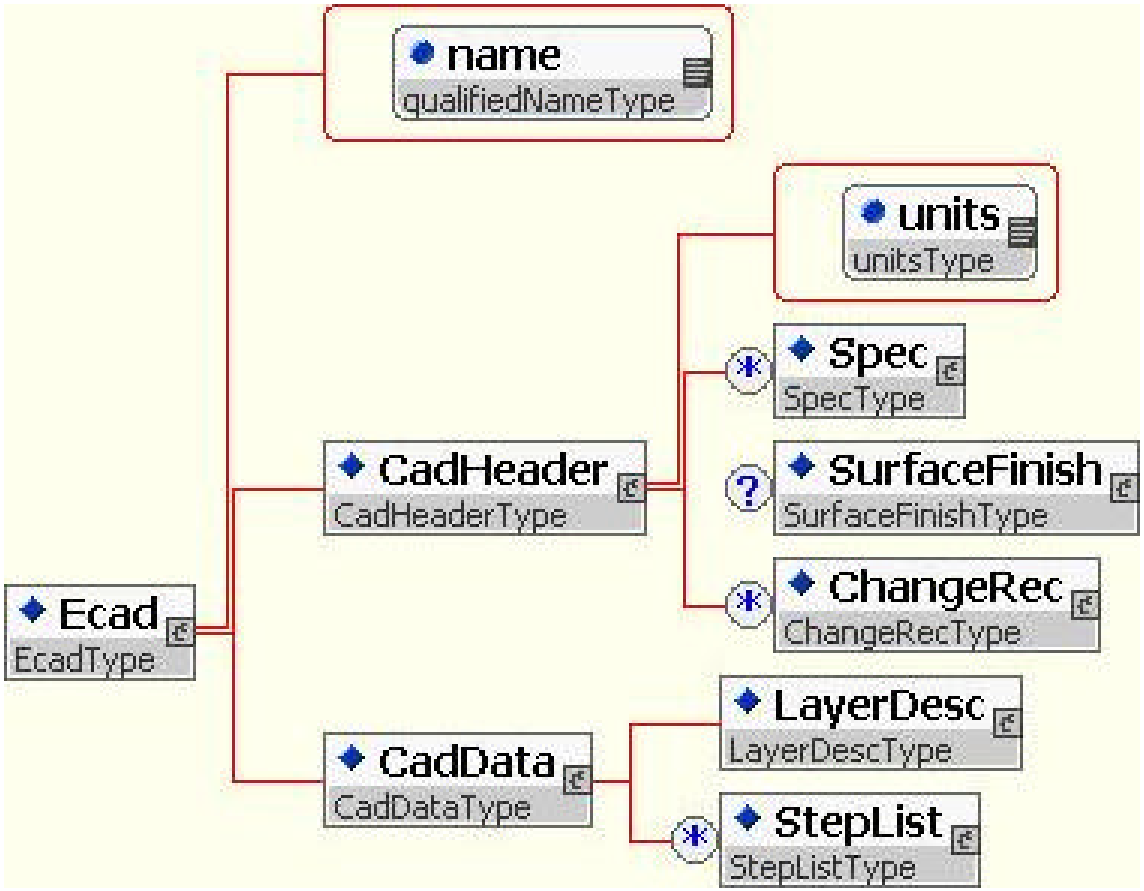
The Heart and Stamina



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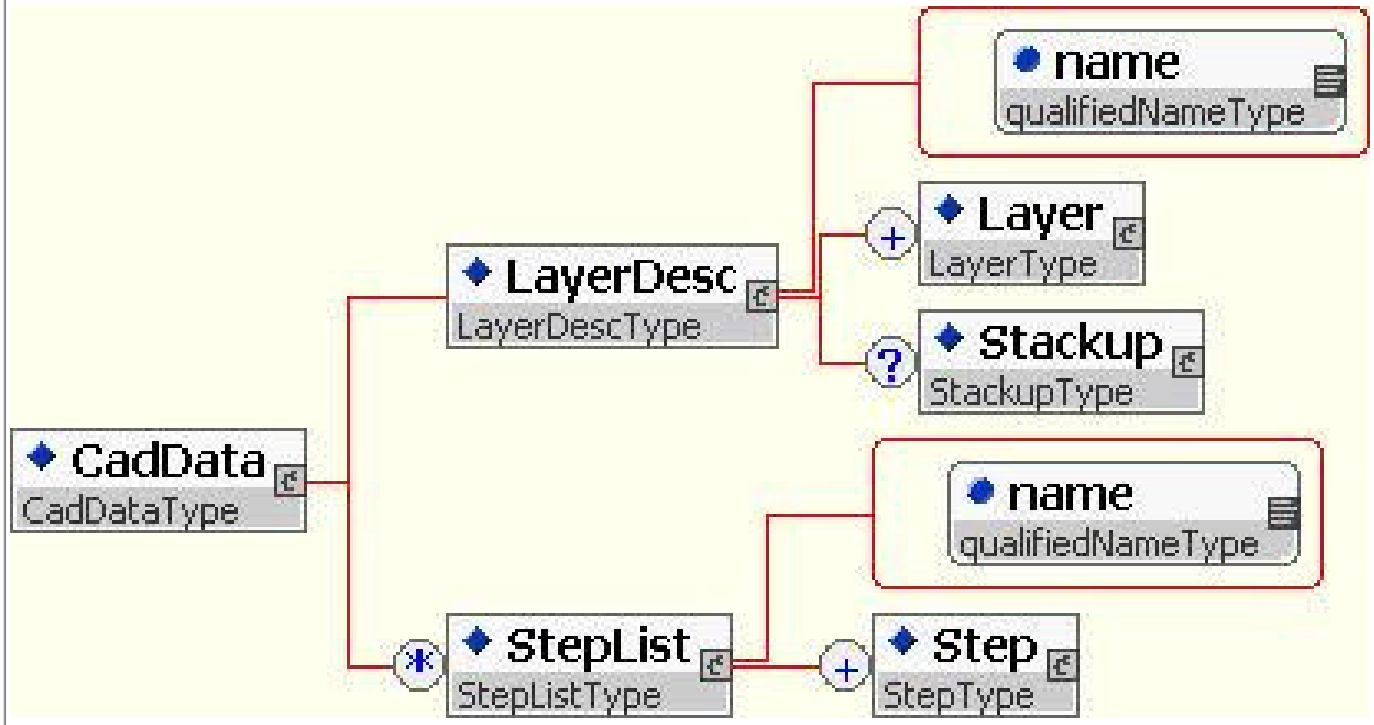
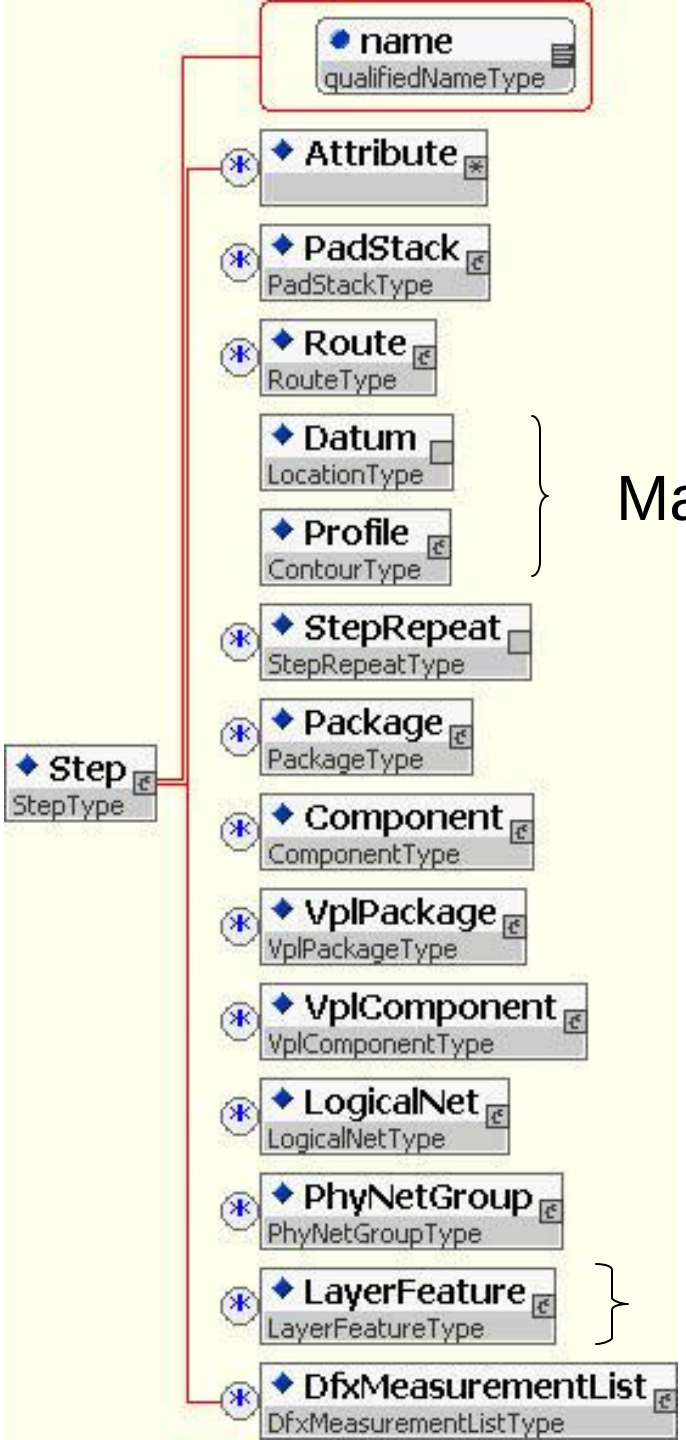
The Information Vessels



Step Description



Mandatory Requirements

The step functions define the details of the electronic assembly. This includes the parts, conductors, net list, and DFX analysis.

The individual features

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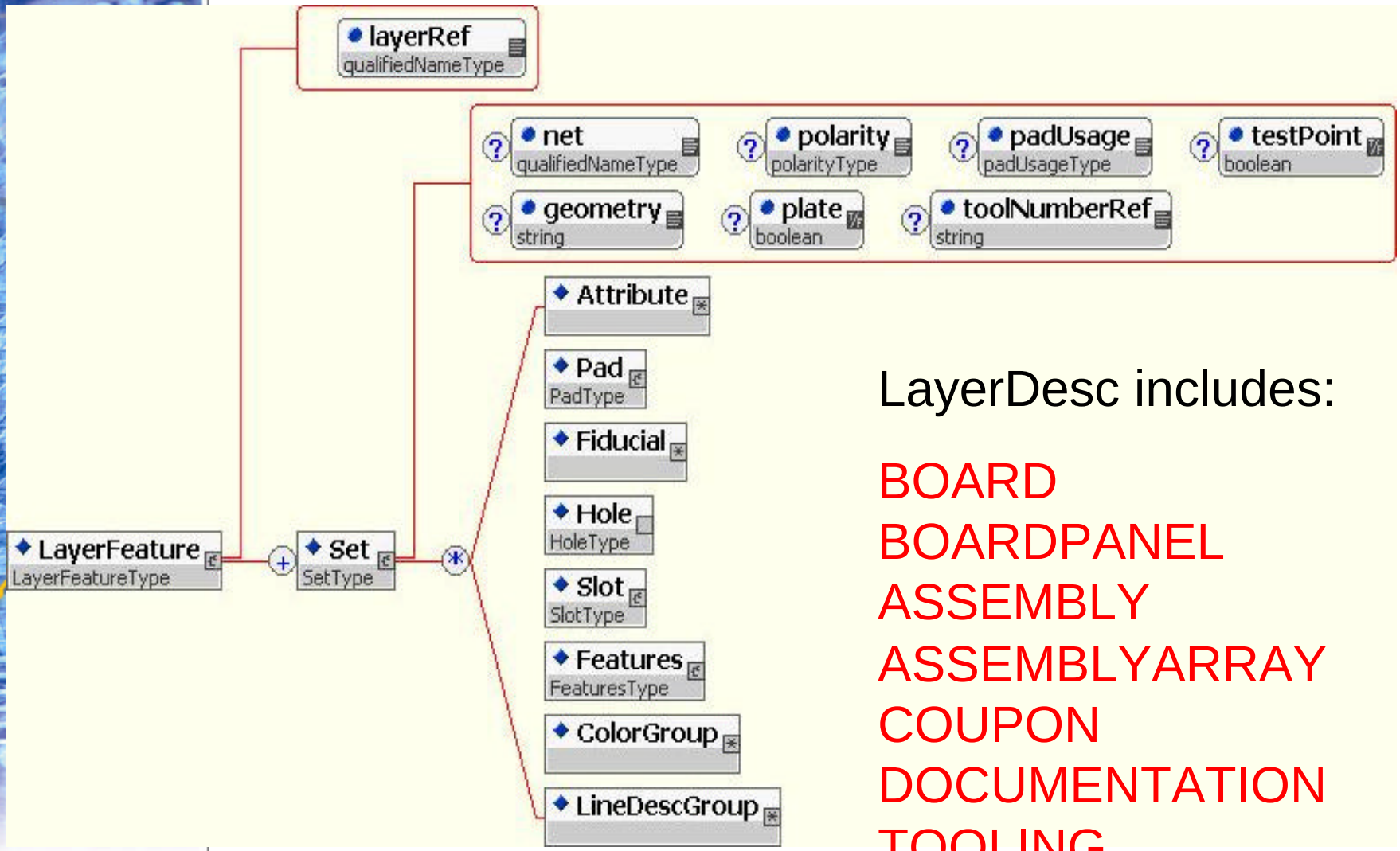
Detail Descriptions



LayerDesc includes:

BOARD
BOARDPANEL
ASSEMBLY
ASSEMBLYARRAY
COUPON
DOCUMENTATION
TOOLING
MISCELLANEOUS

What's Next?

- Major support by CAD tool providers
- NIST viewer can be used to check data files
- NIST Gerber to IPC-2581 conversion
- New tools becoming available daily
- Golden boards in development
- Beta testing to start in fourth quarter
- Certification of tools and read write capability for IPC-25XX standards

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