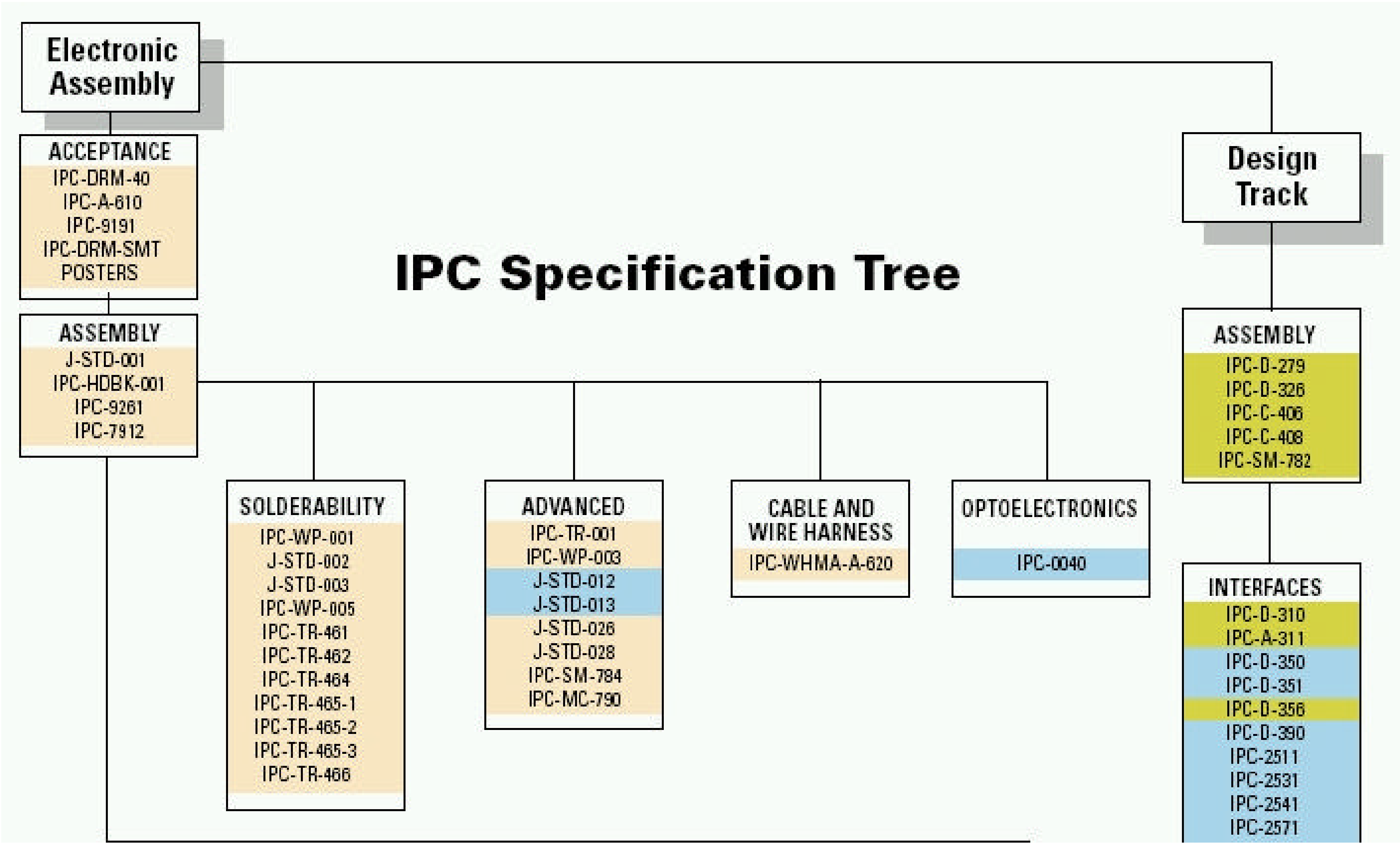
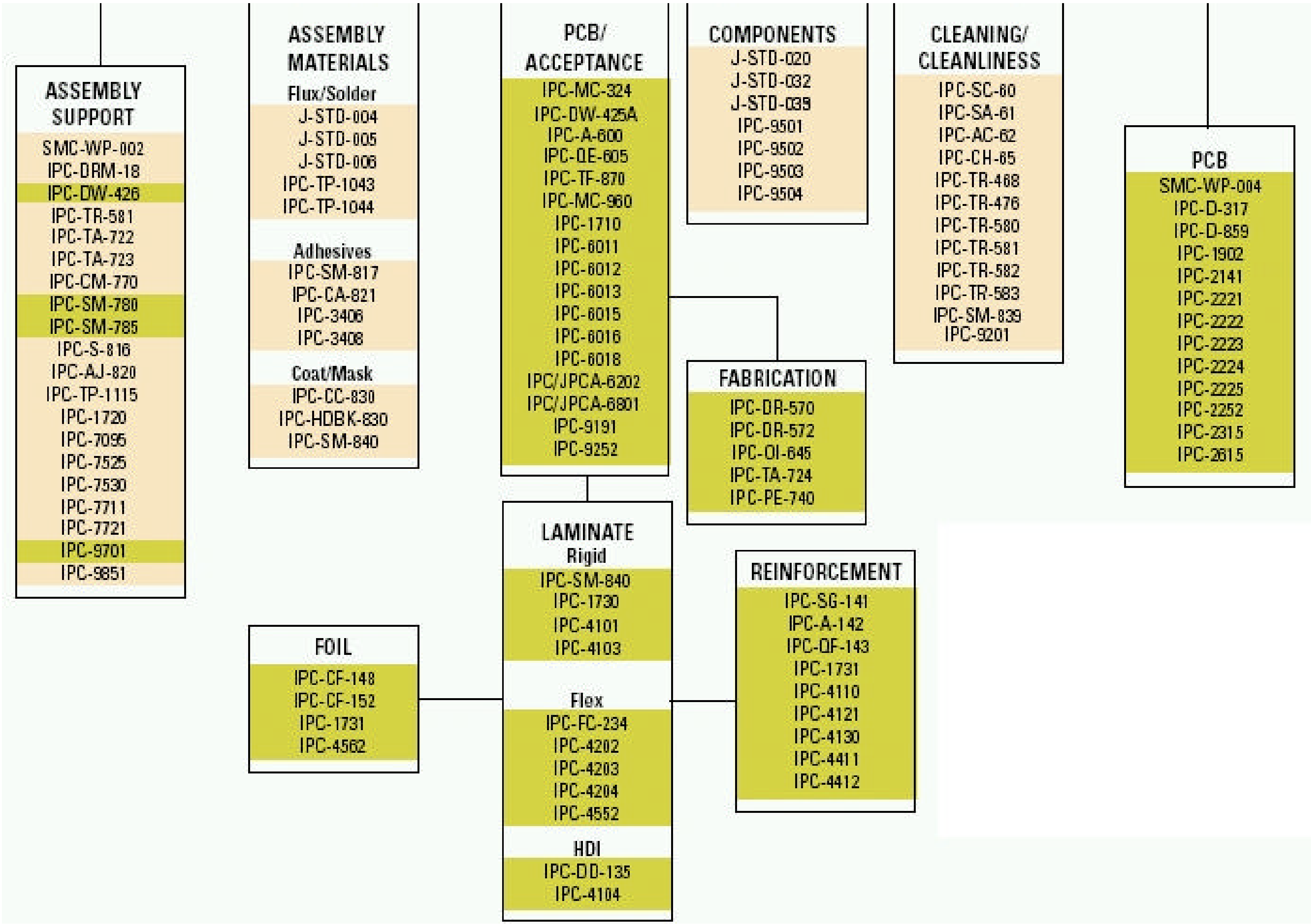
Design Technology What Does the Roadmap Say?

IPC STANDARDS MAP



IPC STANDARDS MAP (cont.)



How Does the Standards Process Work?

- Task groups develop drafts of new standards and resolve comments at IPC meetings
- Participants represent their company
- Four stages to get comments from industry
    - ❶ Project Submission - TAEC approves form
    - ❷ Working Draft - gets project started
    - ❸ Proposal -solicits comments from industry
    - ❹ Interim Final - resolves comments for balloting

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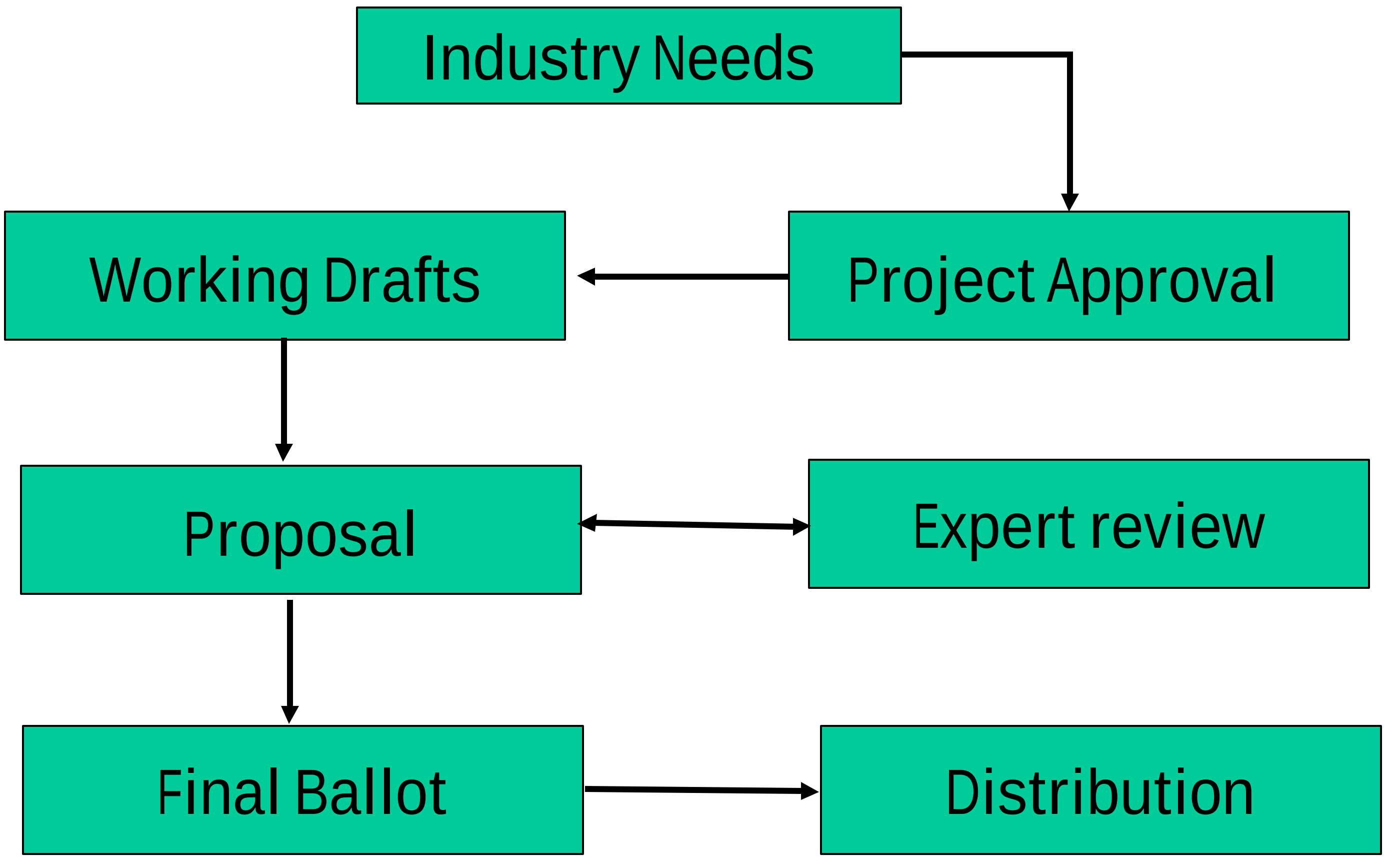
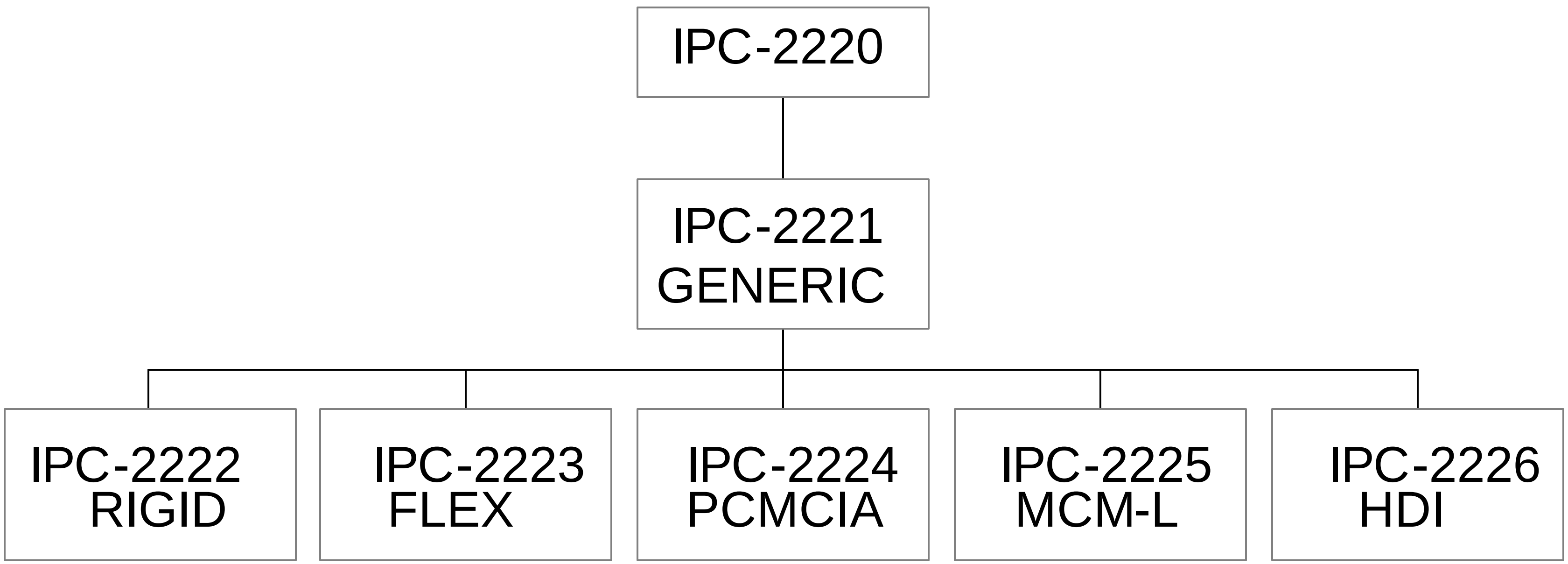
Standard Development Cycle



Hierarchy of IPC Design Standards (2220 Series)



IPC-2227 In Progress for Embedded Components

Applicable IPC Standards

- -SM-782; Land Pattern Considerations
- -7095; BGA Process Implementation
- -2315; HDI & Microvia Design Guide
- -SM-785; SMT Reliability Testing
- -D-279; Design for SMT Reliability
- J-STD-001; Soldering Requirements
- -A-610; Assembly Acceptability
- -6010; Printed Board Series
- J-STD-004/005; Solder Flux/Paste
- -2316; Embedded Component Design Guide

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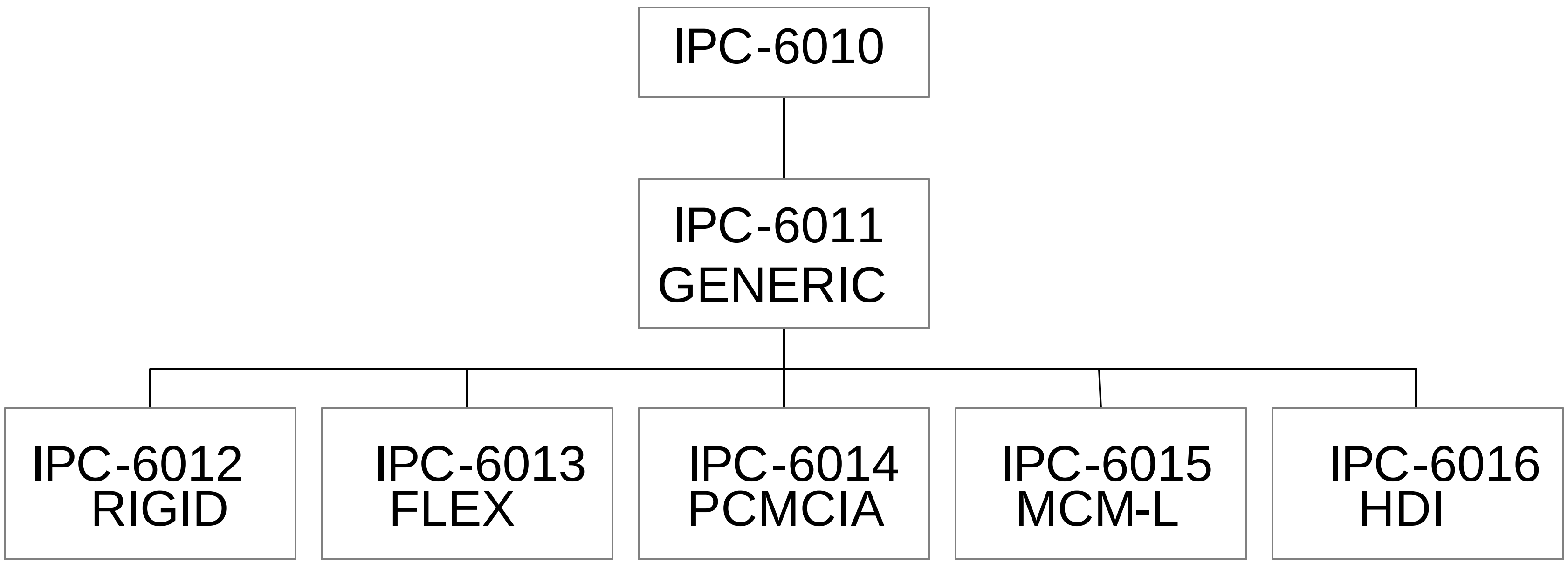
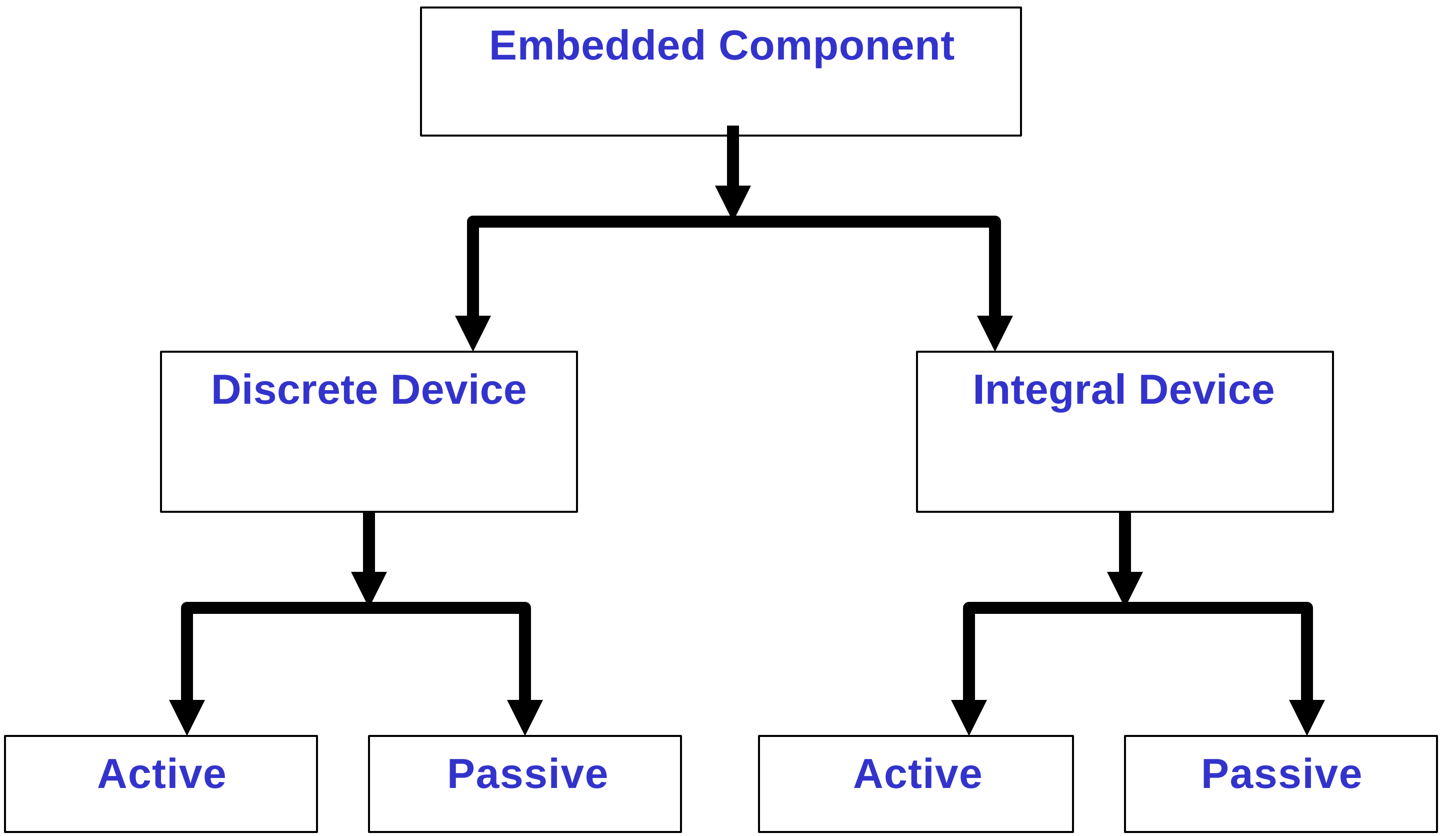
Hierarchy of Printed Board Performance Standards (6010 Series)



IPC-6017 Planned for Embedded Components

Embedded Component Hierarchy



Definition

- **Discrete Passive Component**

This is a single passive element in its own leaded or surface mount technology (SMT) package. An example would be a single resistor, capacitor, or inductor.

- **Embedded Passive Component(Device)**

A passive component that is formed or otherwise inserted inside the primary interconnect substrate as opposed to being on the surface.

CONFORM TO NEMI

Definition

- **Integrated Passive Component**

This is a general term for multiple passive components that share a substrate and packaging. They may be housed inside the layers of the primary interconnect substrate, which would give them the sub-designation of an "embedded passive component", or they may be on the surface of a separate substrate that is then placed in an enclosure and surface mounted on the primary interconnect substrate, in which case they would be called "passive arrays" or "passive networks".

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Definitions

■Passive Array

Multiple passive components of like function are formed on the surface of a separate substrate and packaged in a single SMT case. This case is then mounted on the primary interconnect substrate of the system.

Examples include an array of capacitors or an array of resistors

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■Passive Networks

Multiple passive components of more than one function are formed on the surface of a separate substrate and packaged in a single SMT case. This case is then mounted on the primary interconnect substrate of the system.

New Definition Proposal

- Inserted type Embedded Component

A component that is inserted between the layers of the primary interconnect substrate as opposed to being on the surface. Before inserted in the substrate, it can work as an independent component. Furthermore it should have terminals which can connect with the layers of the substrate.

- Formed type Embedded Component

A component that is formed inside the primary interconnect substrate as opposed to being on the surface. It is made of some low materials at the same time of the substrate manufacturing.

New Definition Proposal

■Embedded Active Component(Device)

An active device that is inserted between the layers of the primary interconnect substrate. It should have terminals which can connect with the layers of the substrate. It does not include a bare die in the current plastic IC package, that is housed inside the encapsulant.

■[__] with Embedded Components

This is a term for the entire body of product that has the embedded passive and/or active components. The head word, [__], requires the word that shows the type of products, e.g. substrate, module, package, or PWB.

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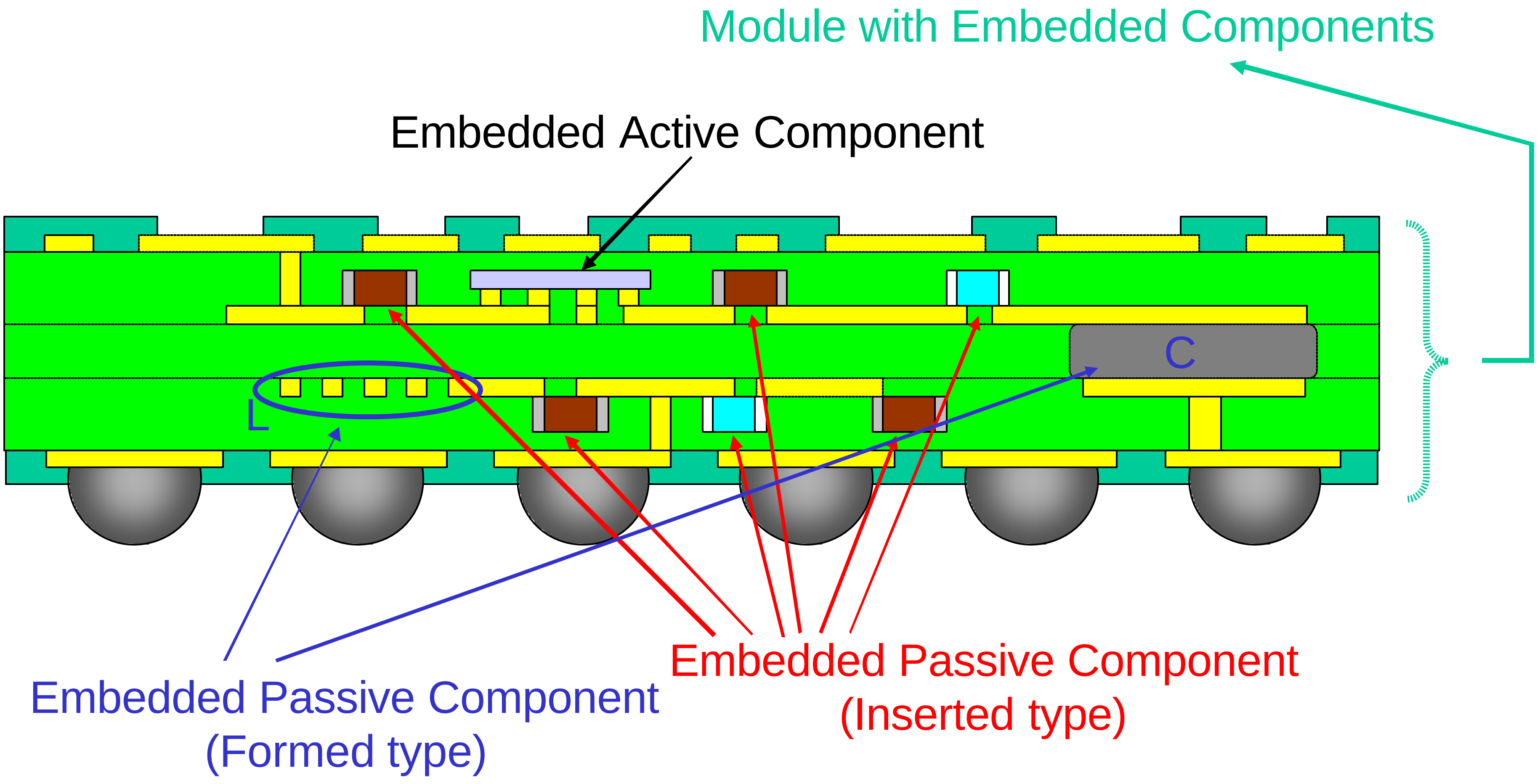
Typical Example of Module with Embedded Components



Minimum IPC Standards Tool Kit

Minimum Tool Kit

Design
2221 Generic
2222 Rigid
2223 Flex
2224 PCMCIA
2225 MCM-L
2226 HDI
2227 Discrete wiring

Performance
6011 Generic
6012 Rigid
6013 Flex
6014 PCMCIA
6015 MCM-L
6016 HDI
6017 Discrete wiring

Component Mounting
7071 Generic
7072 Through-hole
7073 Standard SMT
7074 Fine pitch
7075 Array product
7076 Chip scale
7077 Chip wire bonding
7078 Flip chip

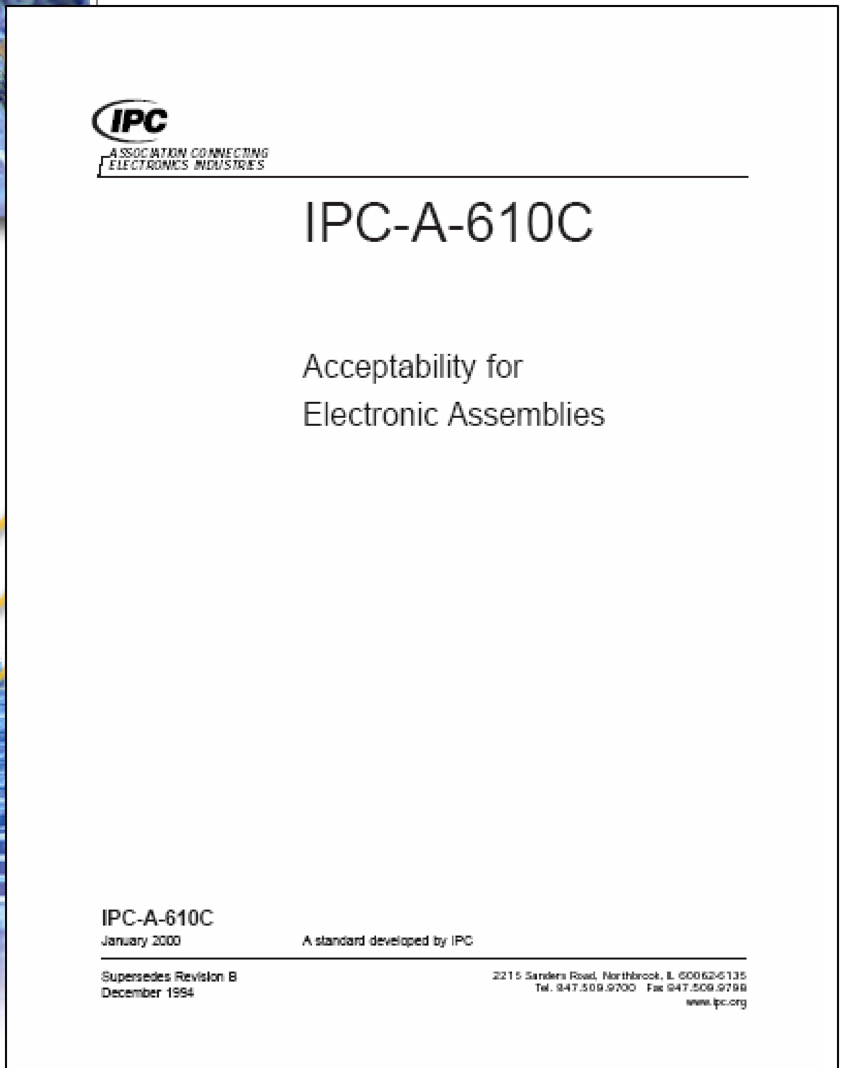
Attachment
J-STD-001 Soldering requirements
J-STD-002 Solderability testing of parts
J-STD-003 Solderability of boards
J-STD-004 Solder Flux
J-STD-005 Solder paste
J-STD-006 Solid solder

Materials
SM-840 Solder mask
FD-2231 Flex material
FD-2232 Coated material
MF-150 Copper foil
CF-148 Coated copper foil
CC-830 Conformal coating
SM-817 Adhesive
4101 Rigid materials
4104 HDI materials

Workmanship
A-600 Printed board
A-610 Printed board assembly
R-700 Modification and repair

Quality Assessment
TM-650 Test methods
SPC 9190
9191 Generic
9192 Base materials
9193Board
9194 Assembly

Global Workmanship Standards



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IPC-A-610C

Acceptability for
Electronic Assemblies

IPC-A-610C
January 2000

A standard developed by IPC

Supersedes Revision B
December 1994

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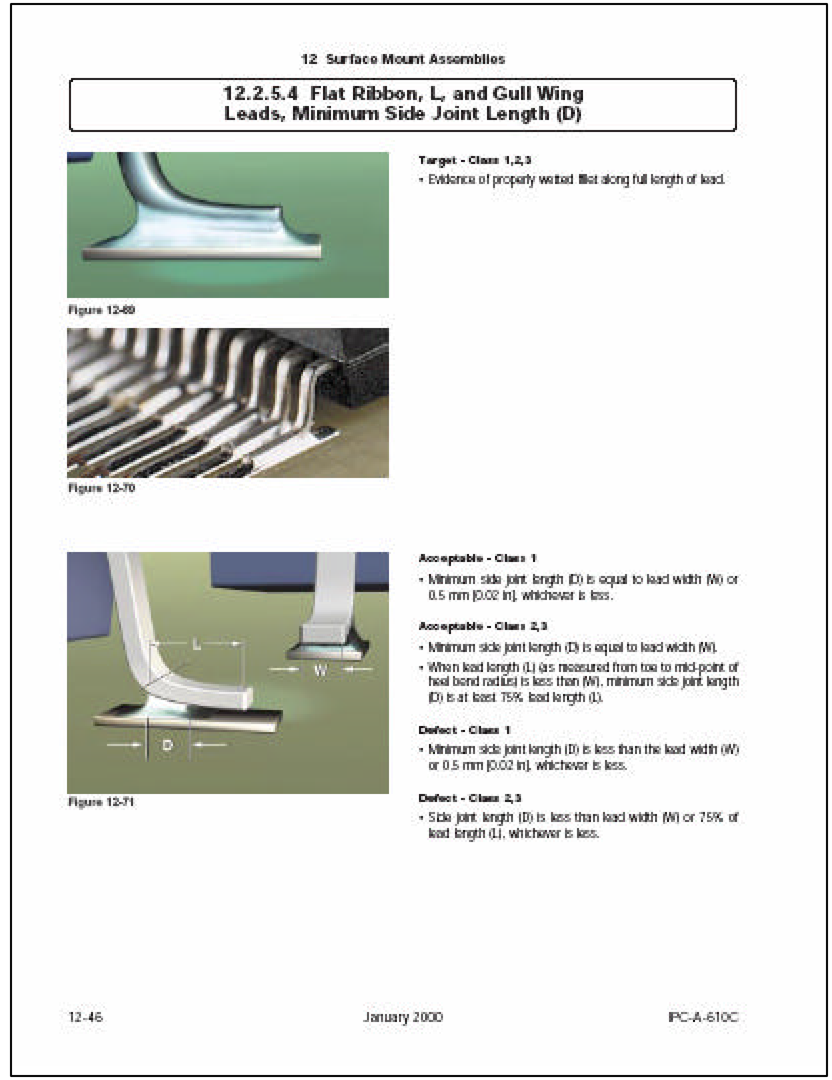
Tel. 847.509.9700 Fax 847.509.9799
www.ipc.org



12 Surface Mount Assemblies

12.2.5.4 Flat Ribbon, L, and Gull Wing Leads, Minimum Side Joint Length (D)

Figure 12-69

Figure 12-70

Target - Class 1,2,3

- Evidence of properly wetted fillet along full length of lead.

Figure 12-71

Acceptable - Class 1

- Minimum side joint length (D) is equal to lead width (W) or 0.5 mm [0.02 in], whichever is less.

Acceptable - Class 2,3

- Minimum side joint length (D) is equal to lead width (W).
- When lead length (L) (as measured from toe to mid-point of heel bend radius) is less than (W), minimum side joint length (D) is at least 75% lead length (L).

Defect - Class 1

- Minimum side joint length (D) is less than the lead width (W) or 0.5 mm [0.02 in], whichever is less.

Defect - Class 2,3

- Side joint length (D) is less than lead width (W) or 75% of lead length (L), whichever is less.

12-46 January 2000 IPC-A-610C

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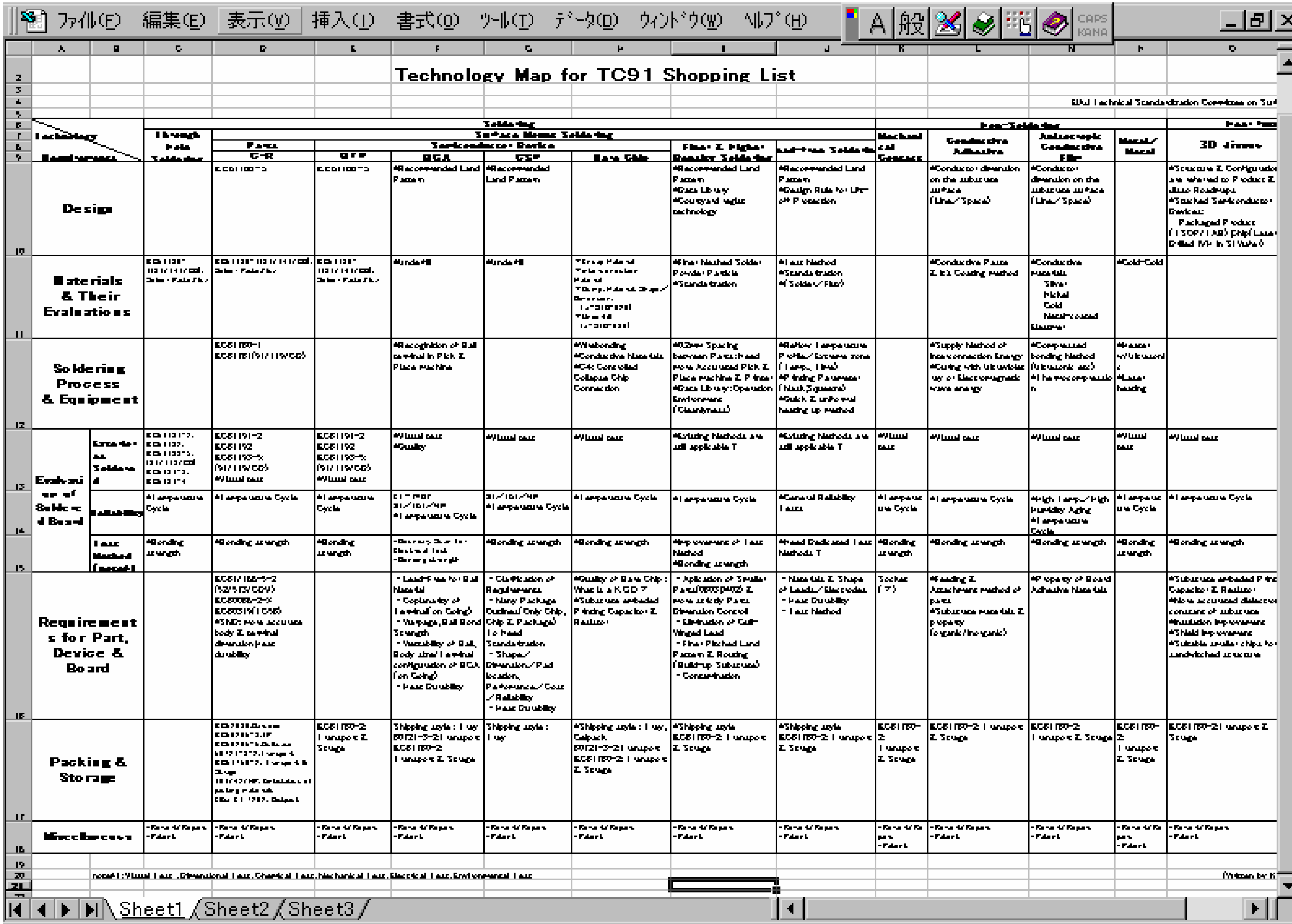
Technology Map



(Source:Japan National Committee proposal at IEC TC91 Kyoto meeting in October 1999)

Zoom-Up of Map

ファイル(F) 編集(E) 表示(V) 挿入(I) 書式(O) ツール(T) データ(D) ウィンドウ(W) ヘルプ(H)

Technology / Requirements		Soldering					
		Through Hole Soldering	Surface Mount Soldering				
			Parts	Semiconductor Device			
			C·R	QFP	BGA	CSP	Ba
Design			IEC61188−5	IEC61188−5	*Recommended Land Pattern	*Recommended Land Pattern	
Materials & Their Evaluations		IEC61190−1(91/141/CD): Solder Paste,Flux	IEC61190−1(91/141/CD): Solder Paste,Flux	IEC61190−1(91/141/CD): Solder Paste,Flux	*Underfill	*Underfill	* Encap M *interco * Bump: M /Dimensi (J-STD- * Underfil (J-STD-
Soldering Process & Equipment			IEC61760-1 IEC61761(91/119/CD)		*Recoginition of Ball terminal in Pick & Place machine		*Wirebon *Conduct *C4: Cor Collapse Connecti
Evaluation of Soldered	Exterior as Soldered	IEC61191-2: IEC61192: IEC61193-5: (91/119/CD) IEC6191-3: IEC6191-4	IEC61191-2 IEC61192 IEC61193-5: (91/119/CD) *Visual test	IEC61191-2 IEC61192 IEC61193-5: (91/119/CD) *Visual test	*Visual test *Quality	*Visual test	*Visual t
		*Temperature Cycle	*Temperature Cycle	*Temperature Cycle	ET−7407 91/161/NP	91/161/NP *Temperature Cycle	*Tempera

Sheet1 / Sheet2 / Sheet3

(Source:Japan National Committee proposal at IEC TC91 Kyoto meeting in October 1999)

National Technology Roadmap for Electronic Interconnection

The mission of the roadmap is to:

- Guide manufacturing, process, material, equipment, and product research and development in order to establish and maintain leadership in electronic interconnection technology
- Integrate the development in the electronic industry with partners in academia and government
- Excel in the global market by implementing these developments and continuously improving customer satisfaction.

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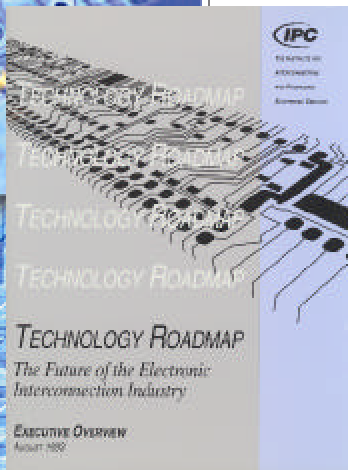
Focus of the IPC Roadmap

- Electronic interconnections include the processes for fabrication of the interconnection structure and materials plus the attachment mounting the assembly of electronic components.

- This National Technology Roadmap is intended to provide the vision, and direction for product development, process development and services required to satisfy the short term, near term and long term requirements for electronic interconnections

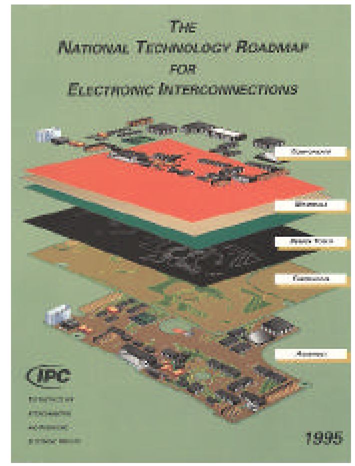
History of IPC Roadmapping



1993

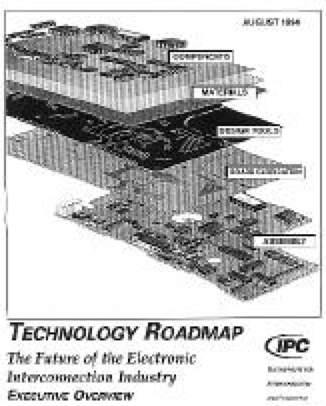
Base Element First National Technology Roadmap Survey
Established IPC as a National Roadmapping entity
9 Business Segments
151 R&D Tasks
Identified Potential Showstoppers
- Lack of coordinated technology integration into manufacturing
- No single common set of needs between industry, government and academia
- Lack of process controls
- Poor customer/supplier relationships

4 year outlook
Led to the creation of ITRI



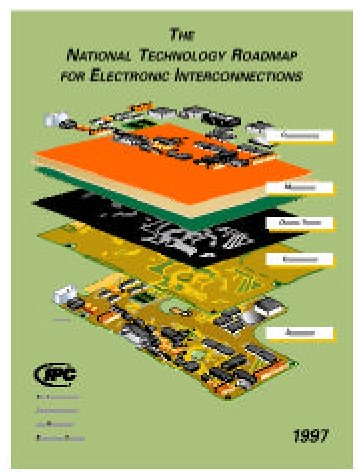
1995

Base Element - OEM Input - 8 Emulators
Nationally Integrated, NEMI, SIA, MCC, SIA
Presented to U.S. Congress - June 1995
15 Year Outlook
Focus on Revenue Center of Gravity
Conventional
Leading Edge
Initiated the 1996 Worldwide Benchmark



1994

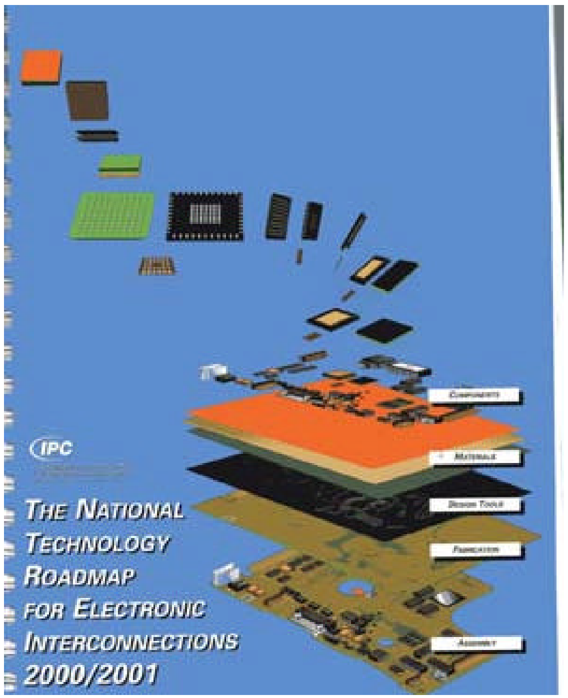
Base Element - Survey
10 Business Segments (EH&S)
162 R&D Tasks
4 Year Outlook
Established ITRI Priorities



1997

Base Element - OEM Input - 20 Emulators
Nationally Integrated
Added Chapters
Ceramic Interconnections
Backplanes
Connectors
Added State of the Art focus

History of IPC Roadmapping



2000 - 2001

Base Element - OEM Input -

Nationally Integrated

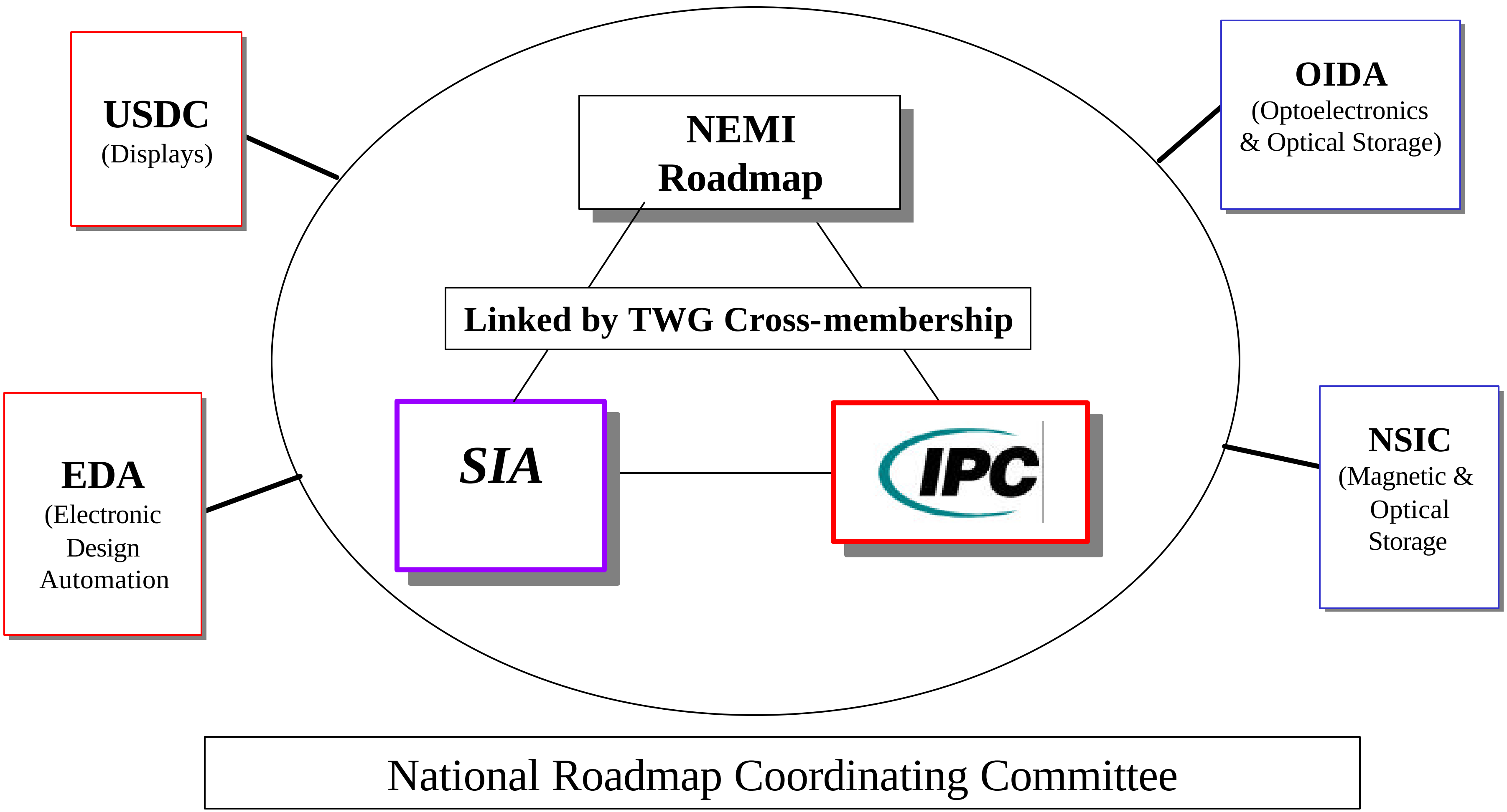
11 Product Sectors

Added Chapters

- **Component Manufacturing**
- **Packaging**
- **Optoelectronic**
- **Reliability**

2002 - 2003

National Roadmapping Linkages



IPC's Multi-dimensional Approach

MARKET SECTORS

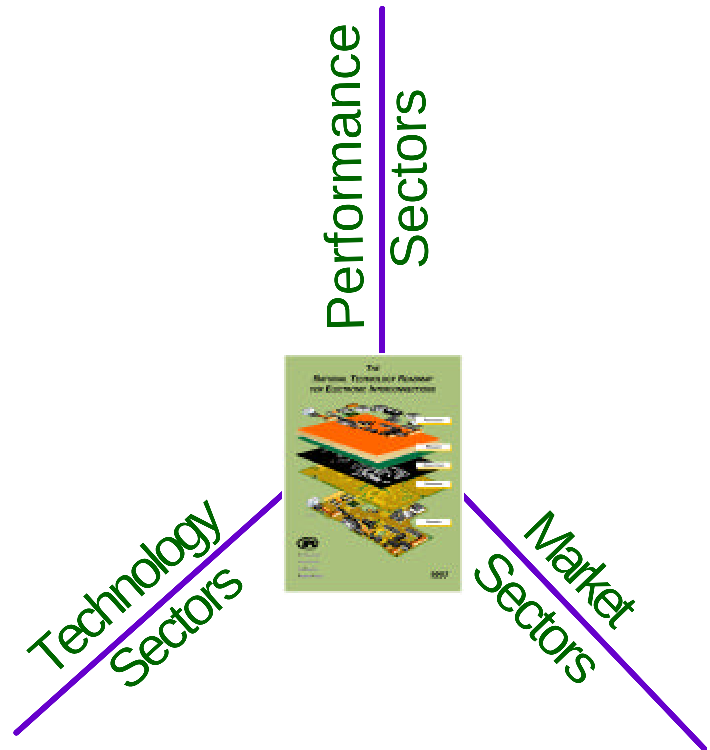
Auto
Computer
Military
Telecommunications
Education/Retail
Consumer
Industrial
Instrumentation

PERFORMANCE SECTORS

Harsh Environment
Portables
High Performance
Low Cost, High Volume
Cost & Performance Sensitive

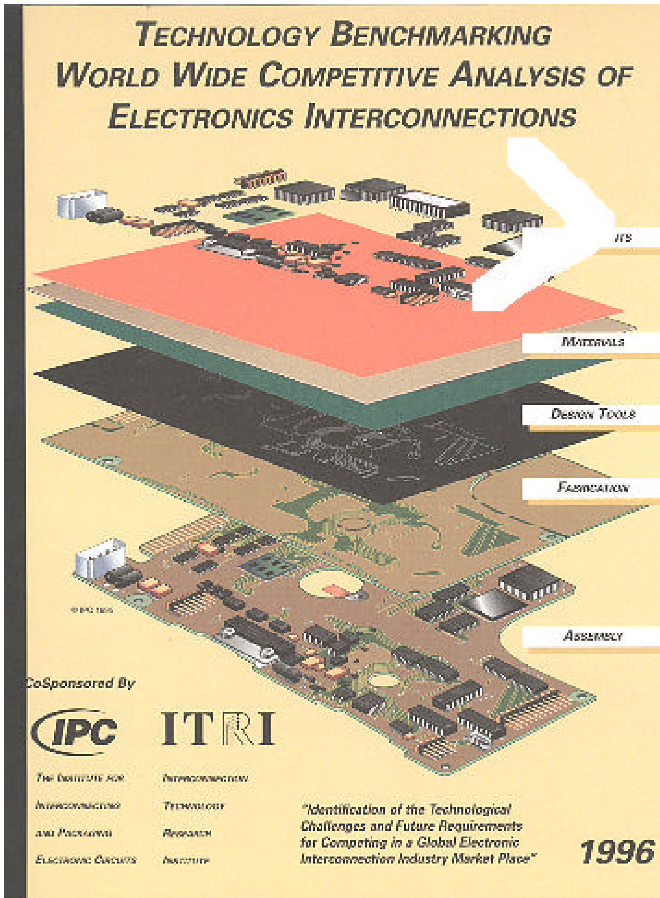
TECHNOLOGY SECTORS

Commodity
Leading Edge
State of the Art



Technology Planning is Multidimensional

World Wide Benchmark



Roadmap for U.S. turns out to be the Benchmark for the World.

International acceptance represented by Asia and Europe.

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Paradigm Shifts for 2003-2004 Roadmaps

- Technology Drivers
  - **Packaging   High Frequency   Optoelectronics**
- Array Components
- Vias
  - **Through hole and microvias**
- Solder Connect Density(Joints/area)
- One layer of HDI, two layers max
- Discrete Component Technology
  - **Buried Integrals (Embedded Passives)**
- Roadmap Validation (PCQR^2)
- Backplanes

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Changes Necessary for Industry to Prosper

- Shared Vision -- A common view of technology needs and priorities
- Strength in industry linkages -- Cooperation between all levels of technology. Chip to Package to Board to Box
- Improved Cooperation - Focus on National Technology Needs
- Sustained Support - Research, Development & Manufacturing

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Organization of the 2002/2003 Roadmap

Purpose & Overview

- Introduction
- Situation Analysis
- Executive Summary
- OEM Requirements
- Roadmap Technology Verification

Related Technologies

- Design Technology
- Data Requirements and Transfer
- Supply Chain Management
- Cost Relationships

Technology Trends

- Package Style/Physical Attributes
- Ground and Voltage Distribution
- Component Assurance Testing
- Optoelectronics
- Build-up Sequential Interconnections
- Connector Technology
- Packaging and Handling
- Reliability Expectations

Component Packaging

- Organic Rigid Interconnections
- Organic Flexible Interconnections
- Ceramic Interconnecting Structures
- Optoelectronic Interconnections
- Assembly of Die and Passives

Product Board Characteristics

- Organic Rigid Printed Boards
- Flexible Printed Boards
- Optoelctronics Structures
- Assembly of Product Boards

Additional Considerations

- Environmental Health and Safety
- Back Planes
- Box Build Requirements
- System Reliability
- System Architecture

Product Emulators – 2002/2003

The TECHNOLOGY

#	Product
E-1	Electronic Games (portable)
E-2	Consumer Products (Low Cost Under $500)
E-3	Hand-held/Wireless Electronics
E-4	Mid Range Performance Electronics (Office Systems)
E-5	High Performance Systems (Mainframe/Mass Storage)
E-6	RF and Microwave Electronics (10 MHz)
E-7	Harsh Environments/Aerospace
E-8	Harsh Environments/Auto Electronics

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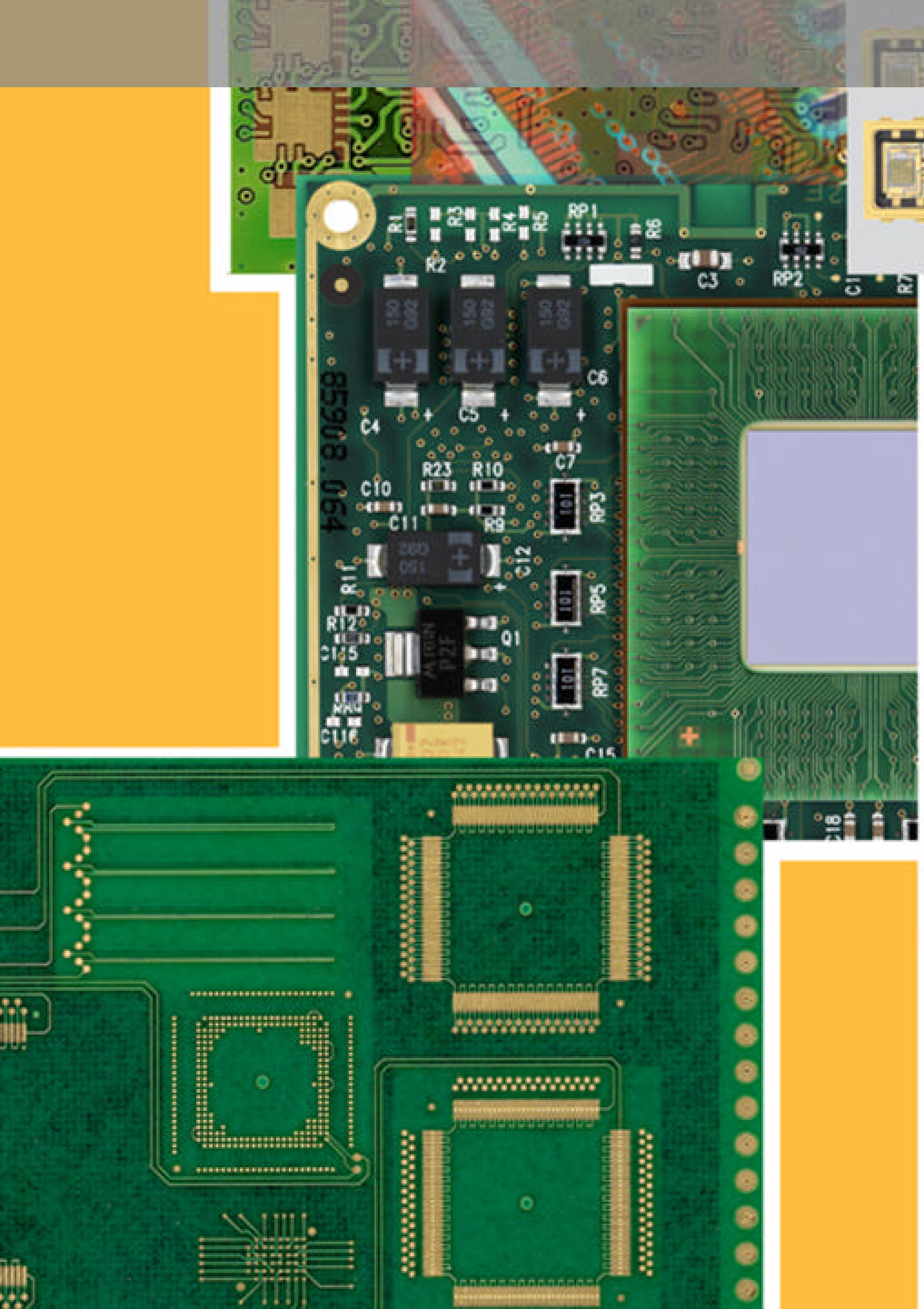

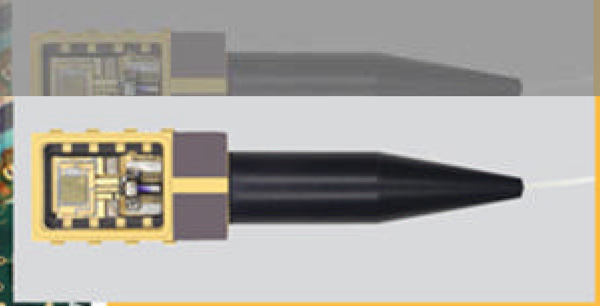

IPC International Technology Roadmap

2004 / 2005

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Roadmap Globalization

ITRS – A truly global roadmap. TWGS in US, Asia, & Europe. Roadmap working meetings are held at international locations

JISSO – Japanese only

NEMI – Plan is to internationalize the emulators in next roadmap

IPC – European and Japanese input since 1995, plan is to include additional input from China in 2004/2005.

WebEx conferencing will be used as a communications tool for some committee meetings.

Product Emulators – 2004/2005

The TECHNOLOGY

#	Product
E-1	Electronic Games (portable)
E-2	Consumer Products (Low Cost Under $500)
E-3	Hand-held/Wireless Electronics
E-4	Mid Range Performance Electronics (Office Systems)
E-5	High Performance Systems (Mainframe/Mass Storage)
E-6	RF and Microwave Electronics (10 MHz)
E-7	Harsh Environments/Aerospace
E-8	Harsh Environments/Auto Electronics

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Design Issues

Technical Driver	Metric Measure	CURRENT 2002-2003		NEAR TERM 2004 - 2005		MID TERM 2006 - 2007		LONG TERM 2008 - 2012	
Design Issues		RCG	SoA	RCG	SoA	RCG	SoA	RCG	SoA
On Chip Rise Time	Nanoseconds	1.8	0.8	1.4	0.6	1.2	0.5	1.0	0.4
On Chip Frequency	MHz	450	700	500	800	600	1000	1000	2000
Min. Device Voltage	Volts	3.0	2.0	2.5	1.8	1.8	1.5	1.0	1.0
Voltage Levels	Avg levels	5	3	4	2	4	2	2	2
Frequency (Chip to Bd)	MHz	150	350	180	450	200	500	500	750
Thermal Dissipation	Watts avg/max	8/75	5/35	8/100	5/80	10/120	6/80	10/150	10/100
EMC Susceptibility	mV/M	60	90	70	100	80	120	90	130
MTBF	Hrs of operation	4000	20000	8000	30000	12000	40000	40000	40000
Operating Range	Min / Max °C	-10/40	-10/60	-10/40	-10/70	-10/40	-10/80	-10/80	-10/80
Max. Board Temp	°C	25	45	30	50	30	60	30	70
Interconnect factor	Max. / cm^2	8.88	4.50	9.32	5.51	9.18	5.09	9.03	5.06
Attachment factor	Max. / cm^2	25.20	42.00	35.73	59.72	56.00	84.00	62.00	91.00

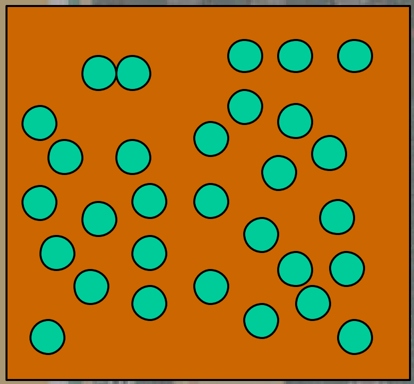
Printed Board Technology Issues

Technical Driver	Metric Measure	CURRENT 2002-2003		NEAR TERM 2004 - 2005		MID TERM 2006 - 2007		LONG TERM 2008 - 2012	
Printed Board Technology Issues		RCG	SoA	RCG	SoA	RCG	SoA	RCG	SoA
Materials	Mat'l type code	FR4	BT Epoxy	FR4	BT Epoxy	CEM	Mod. FR4	CEM	MOD FR4
Board Size-Area	sq cm	600	500	550	450	500	400	525	400
Thickness- Cond. Area	Mm	2.0	1.5	1.75	1.2	1.5	1.0	1.5	0.8
Layer count	Avg. layers	12	6	10	4	8	4	6	4
Line width/ space	Min. internal μm	200/200	100/100	175/175	100/100	150/150	75/75	100/100	50/50
Min. hole Dia.-thru Via	μm	350	300	300	250	250	200	200	175
Min. hole Dia.-buried/ blind	μm	200	125	200	100	175	100	150	85
Min. microvia-buried/ blind	μm	125	100	125	100	100	75	90	70
Land diameter value (area cm sq.)	Add to Hole μm	400	250	350	250	300	200	275	185
Hole Qty - Mechanical	Avg./ board	8000 (10.)	5000	10000	6000	12000	8000	14000	10000
Hole Qty - Microvia	Avg./ board	3000	6000	4000	8000	6000	10000	8000	12000

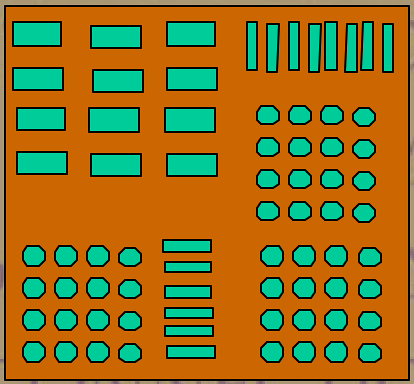
Board Assembly Issues

Technical Driver	Metric Measure	CURRENT 2002-2003		NEAR TERM 2004 - 2005		MID TERM 2006 - 2007		LONG TERM 2008 - 2012	
Board Assy Technology Issues		RCG	SoA	RCG	SoA	RCG	SoA	RCG	SoA
Leads/component	Avg. leads	12	20	15	25	20	30	25	40
Max. # leads/component	I/O count	308	480	480	520	520	640	800	1200
Solder joints primary side	# joints	9072	12600	11790	16125	16800	20160	16900	20240
Solder joints secondary side	# joints	6048	8400	7860	10750	11200	13440	11400	13560
# discretes	Total parts	1084	861	1087	839	1120	829	1140	852
Max. array components	Total parts	50	95	118	151	196	202	203	210
Max. peripheral components	Total parts	126	95	105	86	112	90	113	92
Electrical assembly	Type	2X	2Y	2Y	2Y	2Y	2Z	2Y	2Z

Board & Assembly Purchasing Issues



Cost per square centimeter is based on density of holes and solder joints



Holes per square centimeter

Solder joints per square centimeter

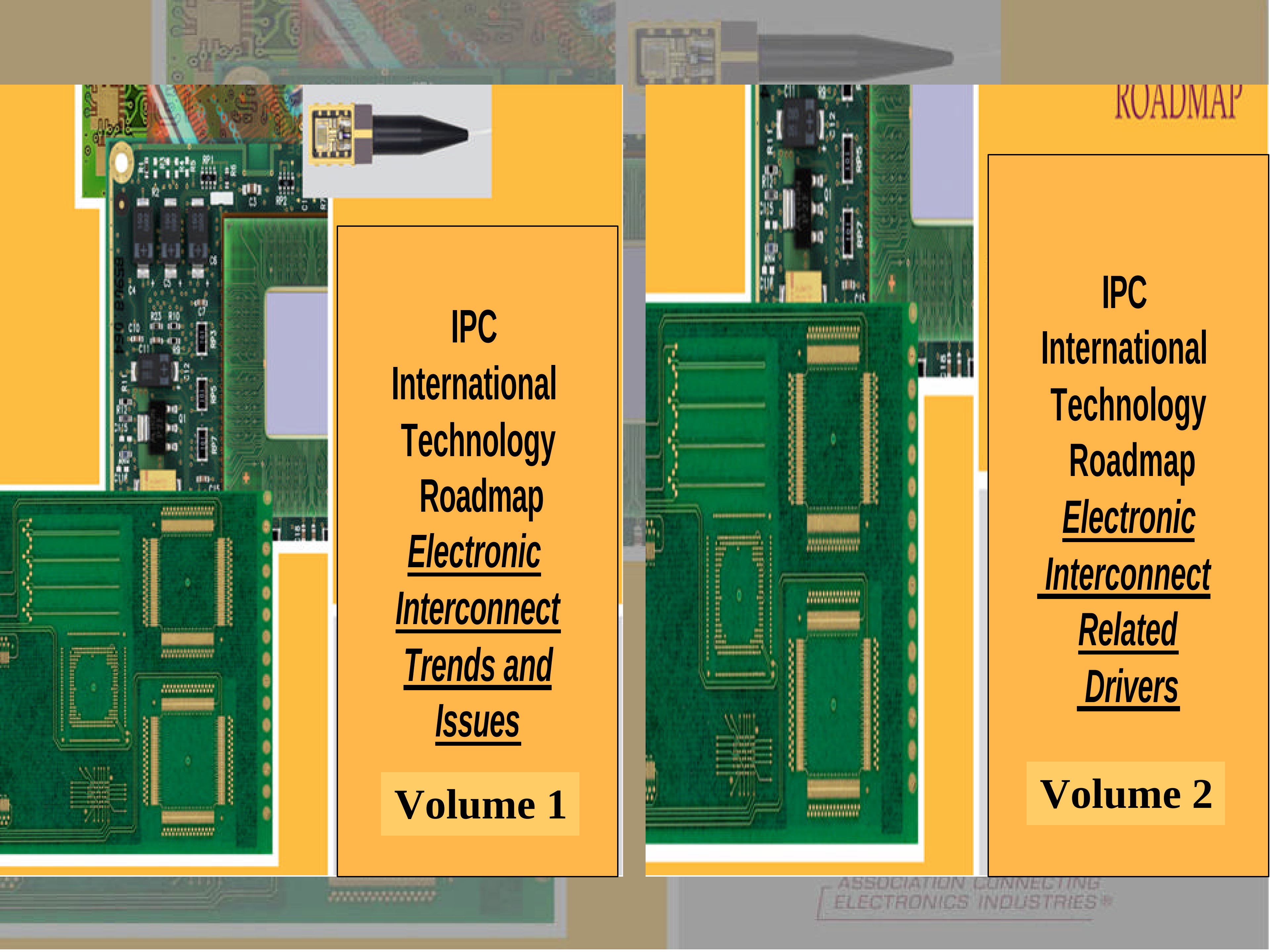
Technical Driver	Metric Measure	CURRENT 2002-2003		NEAR TERM 2004 - 2005		MID TERM 2006 - 2007		LONG TERM 2008 - 2012	
PWB Purchasing Issues		RCG	SoA	RCG	SoA	RCG	SoA	RCG	SoA
Cost/ interconnect	$ /cm^2	0.03	0.05	0.04	0.06	0.04	0.07	0.04	0.06
Cost/ attachment	$ /cm^2	0.003	0.004	0.004	0.004	0.004	0.005	0.004	0.005
Recyclable	Percent	20	15	30	25	30	25	100	100

New Emulator Dialog

Narrative section

Types of product(s) and product selected in emulator
System Impacts, Architecture, and Reliability
Human interface description
Wireless considerations
MEMs considerations
Opto considerations
SIP considerations
Multi media status
Green Manufacturing
Substrate description
Special environment needs if appropriate
Processor type and description if applicable
Energy source and description
Sockets and connector description

Other special considerations



IPC
International
Technology
Roadmap
Electronic
Interconnect
Trends and
Issues
Volume 1
ROADMAP
IPC
International
Technology
Roadmap
Electronic
Interconnect
Related
Drivers
Volume 2
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ELECTRONICS INDUSTRIES

Roadmap Organizational Structure

Volume 1

Part A Purpose and Overview

Part B Technology Trends

Part C Component Packaging

Part D Product Board Substrates

Part E Product Board Assembly

Index

Roadmap Organizational Structure

Volume 2

Part A Purpose and Overview

Part B Related Technologies

Part C Appendix
- Definitions and Acronyms
- Emulator analysis
- Index

Roadmap Organizational Structure

Volume 1

Roadmap Organizational Structure

Volume 2

Part A Purpose and Overview

Part B Related Technologies

- B1 Design Stds. Tools & Technologies
- B2 Documentation and Electronic Data Transfer
- B3 Supply Chain and Box Build Management
- B4 Cost Relationships
- B5 Environmental Health and Safety

Part C Appendix

- C1 Definitions and Acronyms
- C2 Emulator analysis
- C3 Index

Roadmap Verification

- Compare the current RCG and SoA rigid board manufacturing data presented in **Section D** to the **IPC PCQR^2 Database**
- Validate the technology roadmap data, comment on inconsistencies, and expand on the roadmap information to include additional attributes

IPC PCQR^2 Database

- Capabilities demonstrated by PCB manufacturers based on industry standard test vehicles
- Applications
  - Statistically **benchmark** board suppliers' capabilities
  - Perform **intelligent sourcing**
  - Select **new suppliers**
  - Ensure **design for manufacturability**
  - Establish realistic **design rules**

Database Components

- Process Capability Data
  - Detailed data comparing each supplier’s capability, quality, and reliability
- Industry Statistics
  - Statistical data on the industry's capability
- Analysis Reports
  - Detailed data on each supplier’s process

PCQR^2 Design Library

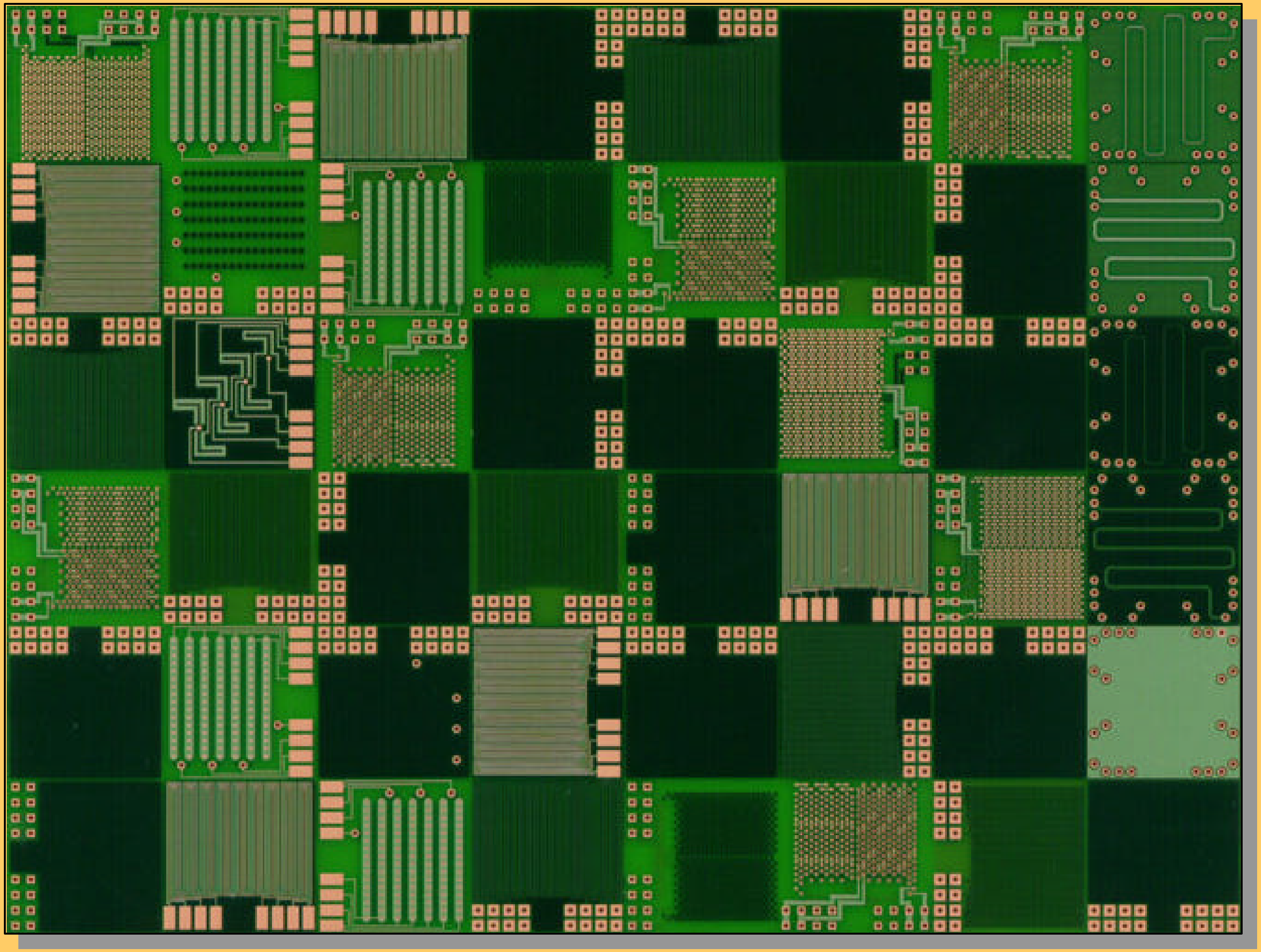
Layer Count	Thickness	Technology	Design File
2	0.062	Medium	IPC-2-062-MB
2	0.062	High	IPC-2-062-HB
6	0.018	Medium	IPC-6-018-MB
6	0.018	High	IPC-6-018-HB
6	0.031	Medium	IPC-6-031-MB
6	0.031	High	IPC-6-031-HB
6	0.062	Medium	IPC-6-062-MB
6	0.062	High	IPC-6-062-HB
12	0.062	Medium	IPC-12-062-MB
12	0.062	High	IPC-12-062-HB
18	0.093	Medium	IPC-18-093-MB
18	0.093	High	IPC-18-093-HB
24	0.125	Medium	IPC-24-125-MB
24	0.125	High	IPC-24-125-HB
24	0.250	Medium	IPC-24-250-MB
24	0.250	High	IPC-24-250-HB

Via Structures

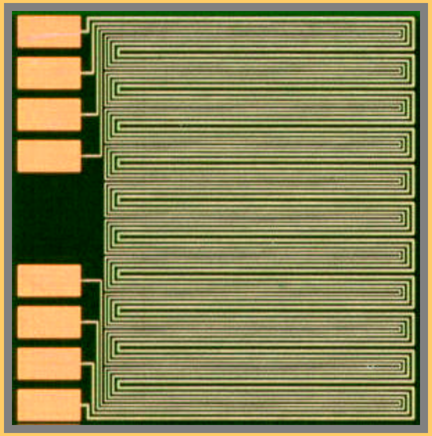
Layer Count	Through	1-Deep Blind	2-Deep Blind	3-Deep CDD	Via Core
2	X				
6	X	X	X		
12	X	X	X		X
18	X	X	X	X	X
24 (0.125)	X	X	X	X	X
24 (0.250)	X				X

Note: Only through vias are required to test and analyze panels.

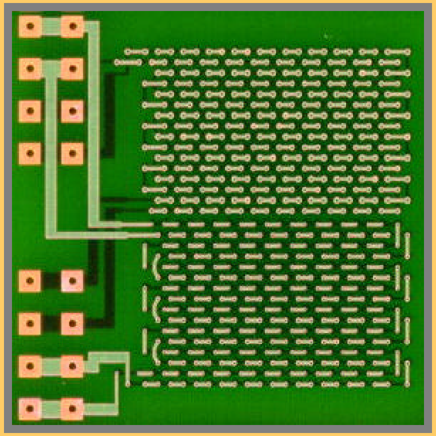
Process Capability Panel



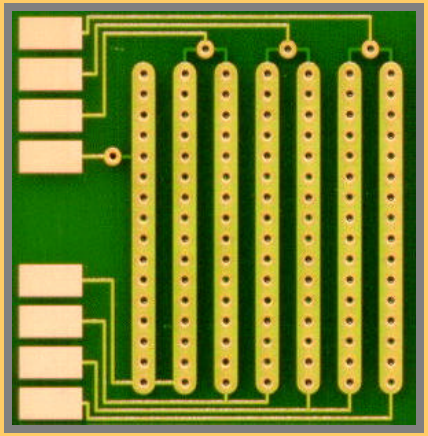
Test Modules



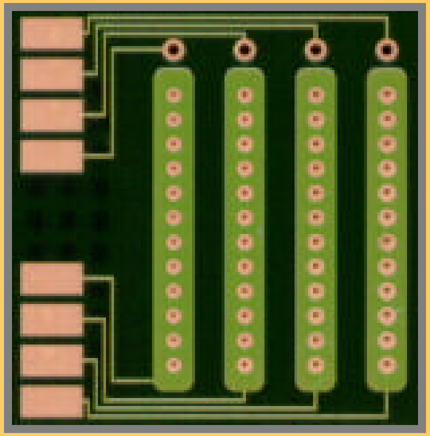
Conductor/Space



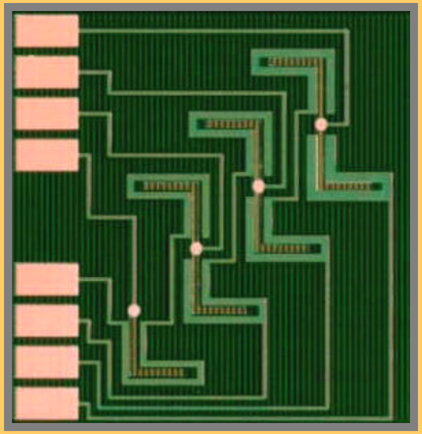
Via



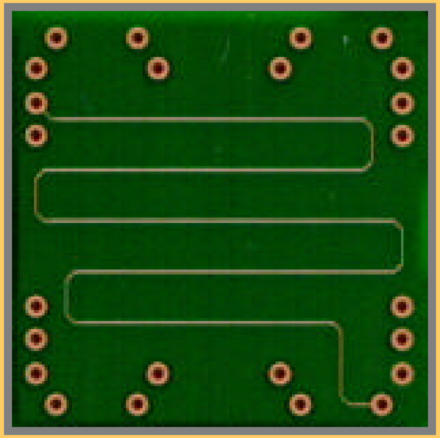
Via Registration



Drill Overshoot



Soldermask Registration



Controlled Impedance

Database Elements

Test Module	Design Type	Capability Information	Quality Information
Conductor/Space	Outerlayer, 0.5-oz innerlayer, 1-oz innerlayer, and buried core	Conductor and space defect density	Conductor width and height uniformity
Via	Through, 1-deep blind, 2-deep blind, buried core, and controlled depth drill	Via defect density	Via net resistance coefficient of variation
Via (Reliability)	Through, 1-deep blind, 2-deep blind, buried core, and controlled depth drill	Yield loss	Percent change in resistance
Via Registration	Through, 1-deep blind, 2-deep blind, and controlled depth drill	Via probability of breakout	
Drill Overshoot	Controlled depth drill	Probability of overshoot	
Soldermask Registration	Outerlayer	Clearance yield	
Controlled Impedance	Single-ended and differential	Impedance uniformity	

Outerlayer Conductor and Space

Table A5-1. Outerlayer Conductor and Space Formation (1.5mm Board Thickness)

ATTRIBUTE	**CURRENT 2002-2003**		**PCQR^2 DATABASE**	
	RCG	SoA	RCG	SoA
Conductor Size (μm)	150	60	150	75
Space Size (μm)	150	60	150	75
Conductor Width Tolerance (μm)	40	15	46	24

Table A5-2. Outerlayer Conductor and Space Formation (3.0mm Board Thickness)

ATTRIBUTE	**CURRENT 2002-2003**		**PCQR^2 DATABASE**	
	RCG	SoA	RCG	SoA
Conductor Size (μm)	-	-	100	75
Space Size (μm)	-	-	175	150
Conductor Width Tolerance (μm)	-	-	50	30

Innerlayer Conductor and Space

Table A5-3. Innerlayer Conductor and Space Formation

ATTRIBUTE	**CURRENT 2002-2003**		**PCQR^2 DATABASE**	
	RCG	SoA	RCG	SoA
Conductor Size (µm)	125	50	75	50
Space Size (µm)	125	50	100	75
0.5-oz. Width Tolerance (µm)	35	10	36	16
1.0-oz. Width Tolerance (µm)	-	-	48	24

Through Via

Table A5-4. Through Via Formation (1.5mm Board Thickness)

ATTRIBUTE	CURRENT 2002-2003		PCQR^2 DATABASE	
	RCG	SoA	RCG	SoA
Minimum Via Size (µm)	300	200	300	200
Annular Ring (µm)	-	-	200	100

Table A5-5. Through Via Formation (3.0mm Board Thickness)

ATTRIBUTE	CURRENT 2002-2003		PCQR^2 DATABASE	
	RCG	SoA	RCG	SoA
Minimum Via Size (µm)	-	-	300	250
Annular Ring (µm)	-	-	300	200

Blind Via

Table A5-6. PCQR^2 Database Blind Via Structures

Description	**Formation Method**	**Interconnect**
1-Deep Blind	Laser (typical)	1 to 2 and n to n-1
2-Deep Blind	Laser (typical)	1 to 3 and n to n-2
3-Deep Controlled Depth Drill	Mechanical	1 to 4

Table A5-7. 1-Deep Blind Via Formation (75mm Dielectric Thickness)

ATTRIBUTE	**CURRENT 2002-2003**		**PCQR^2 DATABASE**	
	RCG	SoA	RCG	SoA
Minimum Via Size (µm)	-	75	150	75
Annular Ring (µm)	-	-	125	75

Blind Via Cont.

Table A5-8. 2-Deep Blind Via Formation (175μm Dielectric Thickness)

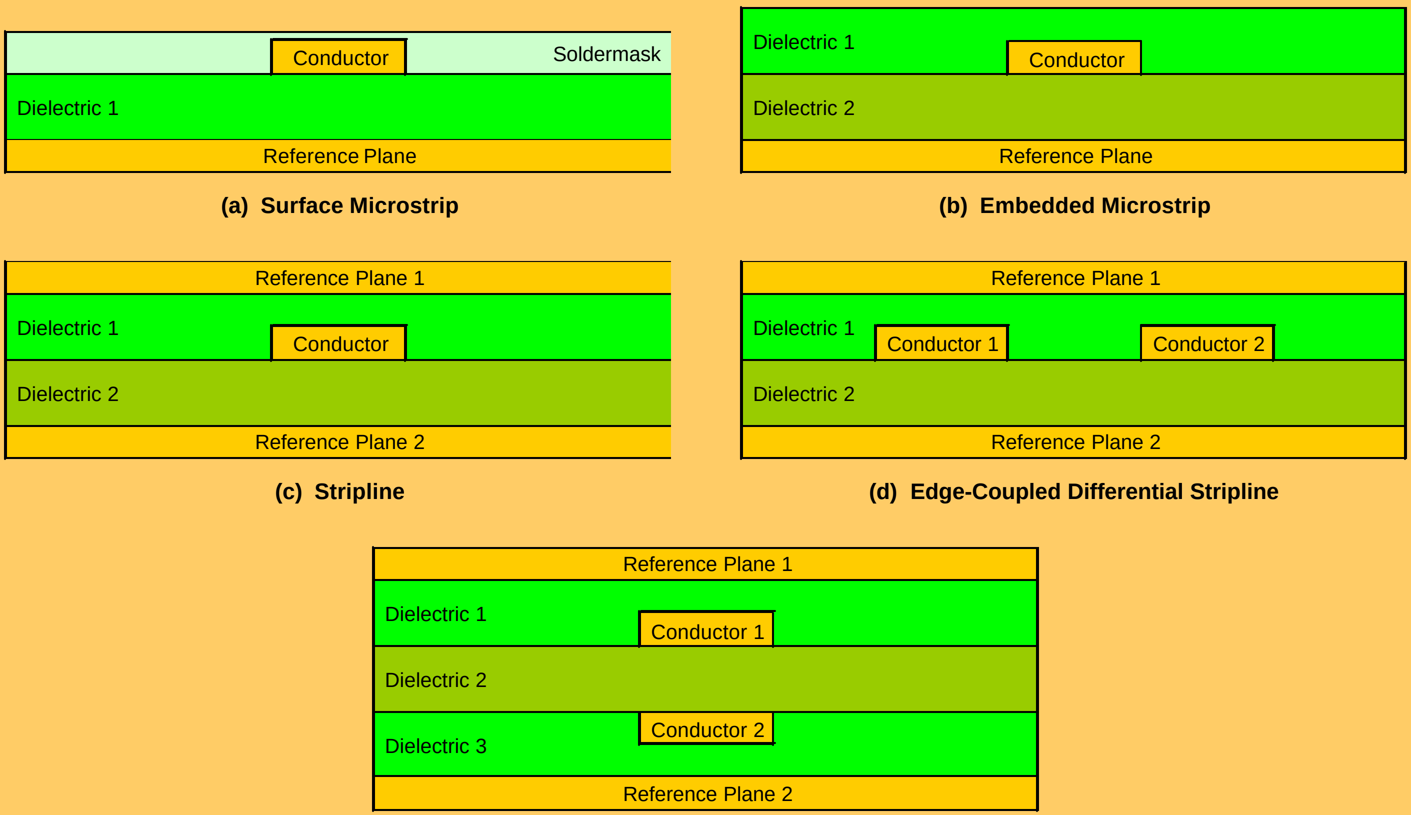
ATTRIBUTE	CURRENT 2002-2003		PCQR^2 DATABASE	
	RCG	SoA	RCG	SoA
Minimum Via Size (μm)	-	-	250	175
Annular Ring (μm)	-	-	125	75

Table A5-9. 3-Deep Controlled Depth Drill Via Formation (300μm Dielectric Thickness)

ATTRIBUTE	CURRENT 2002-2003		PCQR^2 DATABASE	
	RCG	SoA	RCG	SoA
Minimum Via Size (μm)	-	-	450	350
Annular Ring (μm)	-	-	200	100

Controlled Impedance Structures

Figure A5-2. PCQR^2 Controlled Impedance Structures



(a) Surface Microstrip

(b) Embedded Microstrip

(c) Stripline

(d) Edge-Coupled Differential Stripline

(e) Broadside-Coupled Differential Stripline

Controlled Impedance

Table A5-11. Controlled Impedance Formation (125m Conductor)

ATTRIBUTE	**CURRENT 2002-2003**		**PCQR^2 DATABASE**	
	RCG	SoA	RCG	SoA
Surface Microstrip C_p	-	-	0.8	1.4
Embedded Microstrip C_p	-	-	1.3	2.4
Stripline C_p	-	-	1.3	1.8
Edge-Coupled Differential Stripline C_p	-	-	1.3	2.0
Broadside-Coupled Differential Stripline C_p	-	-	1.1	1.6

Assembly Methodology

Technology Drivers

Packaging High Frequency

Optoelectronics

Array Components

Vias

Through hole and microvias

Solder Connect Density(Joints/area)

Discrete Component Technology

Buried Integrals (Embedded Passives)

Process Challenges

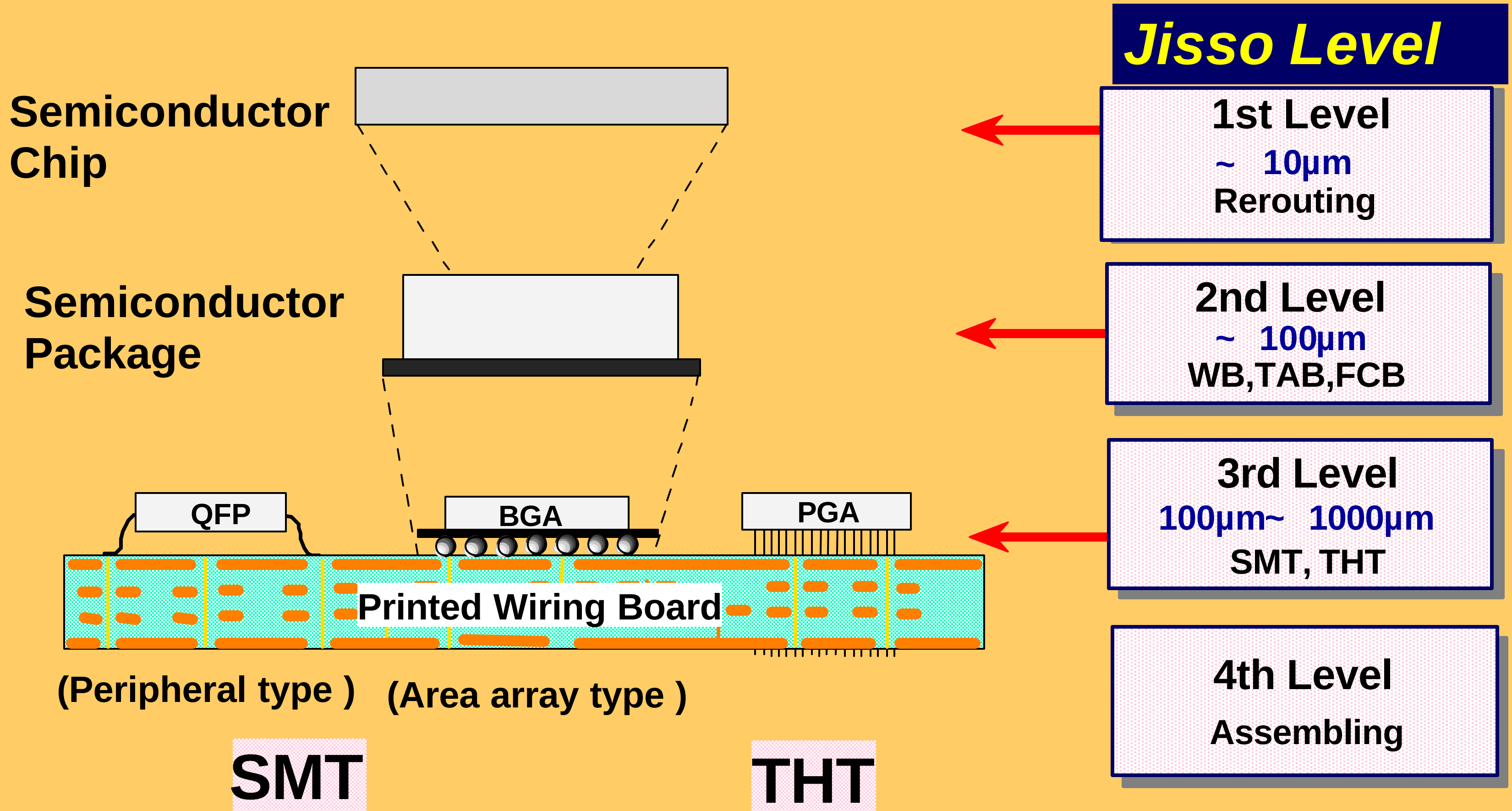
- Nothing ever goes away, e.g. the rumored death of thru hole has been greatly exaggerated. Component Intermix **will** increase!
- Array packages replace high I/O peripherals as the packages of choice: Manufacturability!
- Handheld printed boards decrease in size and thickness, increase in interconnection density. HDI is the alternative to layer count.

Assembly Challenges

- Bare die direct attachment to organic substrates will increase. (Less <2% of the advanced assembly)
- Process windows narrow: harder to inspect, test, and rework
  - Increased I/O counts - peripheral and array packages may compliment each other
  - Process control is becoming embedded in assembly process equipment
- New technologies require new and tighter tolerances
  - “Flatter” boards (low warp) for CSP and DCA component attach
  - Low CTE mismatch between component materials and board materials for CSP and DCA packages, e.g. DCA components that do

The Concept of Jisso ?

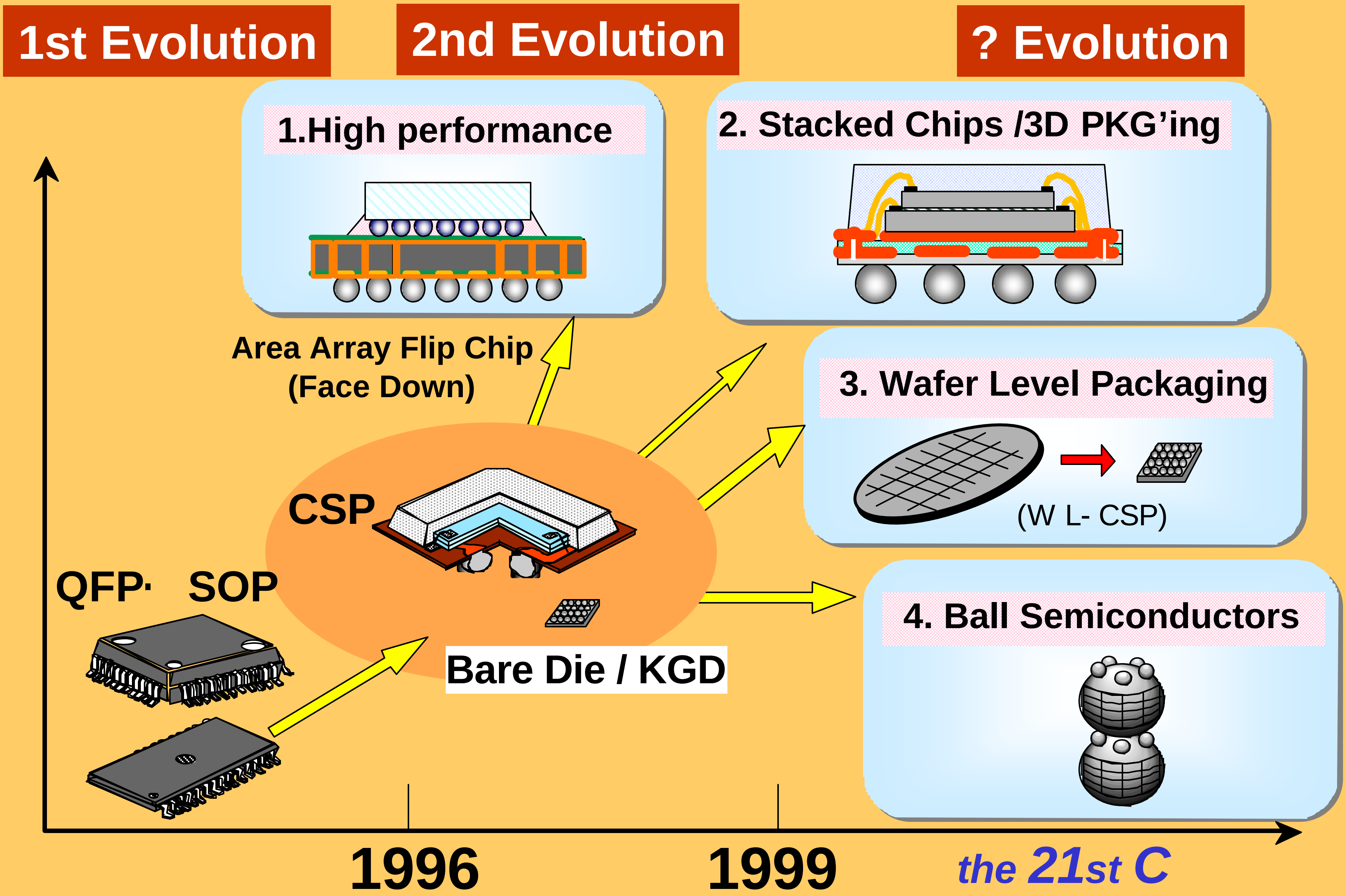
Total solution for Interconnecting, Assembling, Packaging, Mounting and Integrating system design.



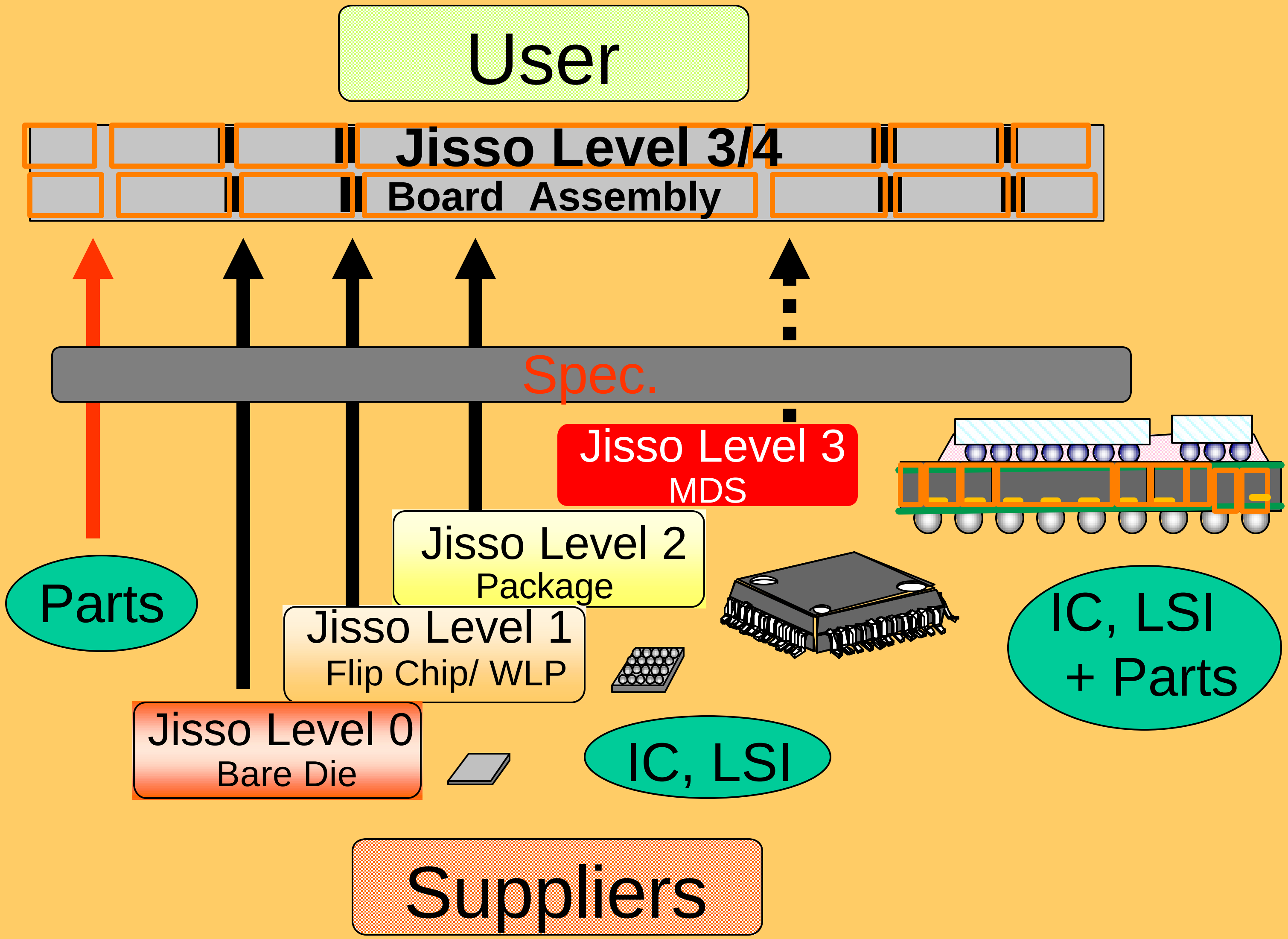
SMT : Surface Mounting Technology

THT : Through Hole Mounting Technology

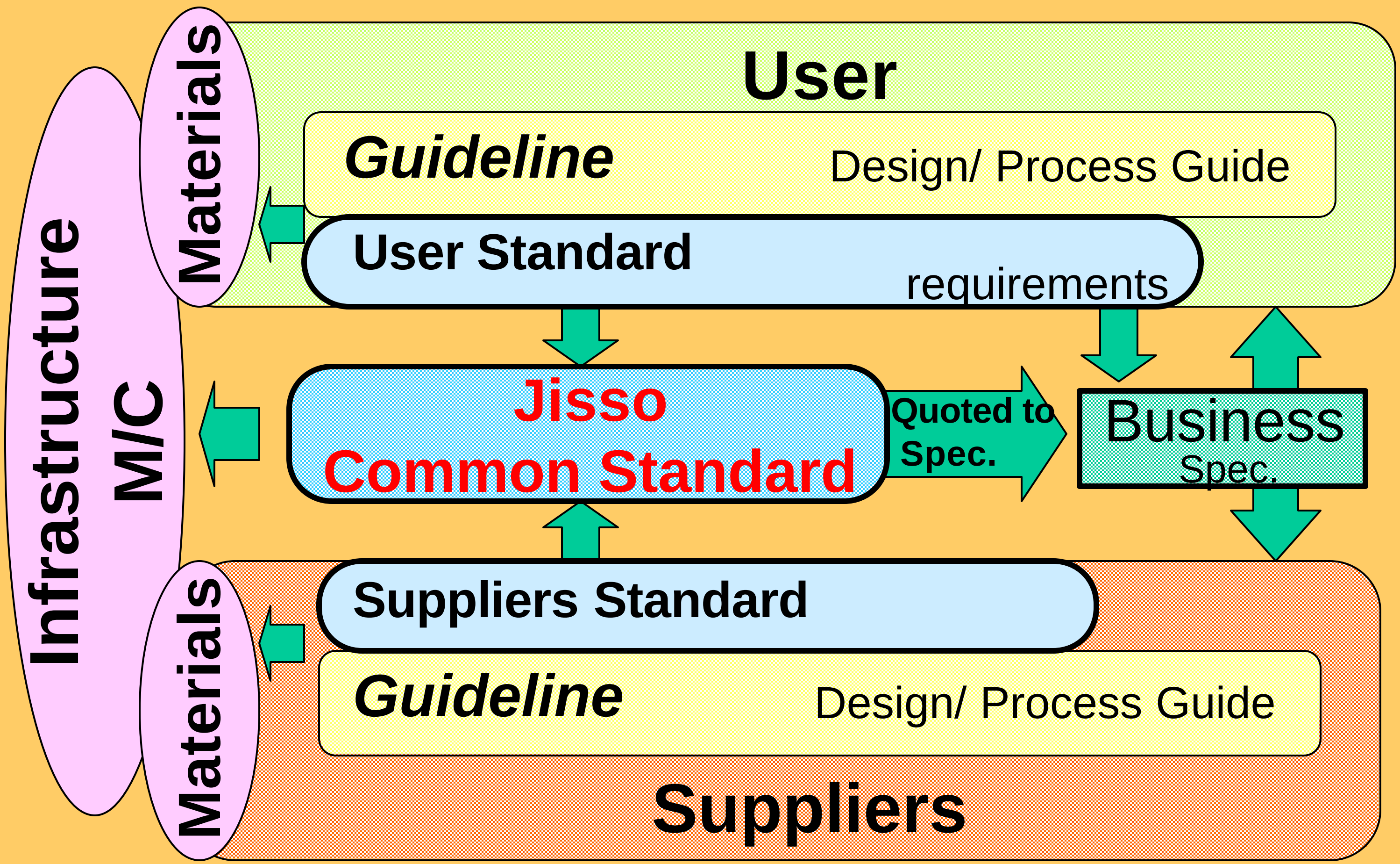
Technology Big-bang into the 21st Century



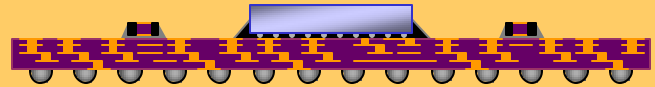
Jisso Single-dimensional View



Jisso Multi-dimensional Standard

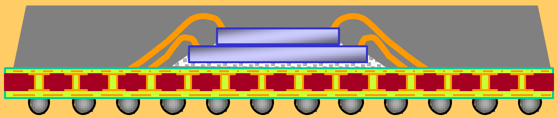


Typical Examples of Jisso Classification



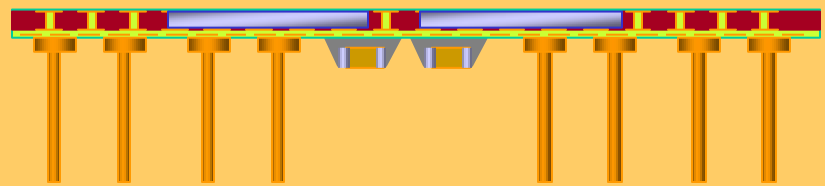
Transmeta Crusoe

"MDS-B1-C-3P-FC"



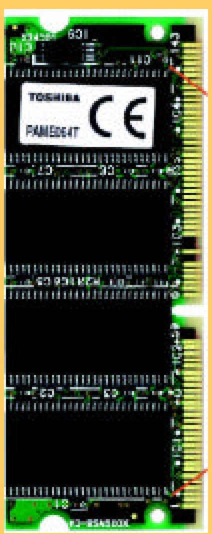
Stacked MCP for Mobile Phones

"MDS-B1-L-2S-W"



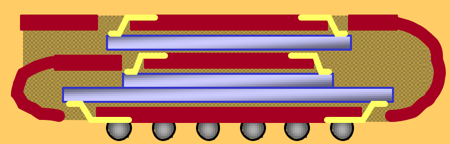
CPU+Chipset in Intel BBUL w/ decap

"MDS-P2-L-2E(3S)-P"



DIMM/SIMM

"MDS-C2-L-1P-Le"



Flash+SRAM in Tessera Folded Stacked

"MDS-B1-L-2F-Le"

The Evolving Process Environment

- Emphasis on process control not process alone.
  - Meet the line production rate
  - Data collection, mining, and analysis processes
  - Standardized data formats and tools
- Line change over time
  - Control and accuracy in component kitting
  - Test and inspection of high mix, high density assemblies
- DFX
  - Land patterns for reliable array attachment
  - Test access for high density designs
  - Materials compatibility and environmental issues up front in design process

The Evolving Process Environment

- Environmental pressures on the assembly processes will continue to increase
  - No scientific consensus
  - No legislative consensus
  - No economic consensus
- Globally implement strategy developments
- Continuous customer satisfaction improvement
- With contract manufacturing increasing:
  - Better DFX needed
  - Concurrent engineering skills at the interface between design and manufacturing needed
- Integrate R&D in the industry with academia and government

Consumables Challenges

- Environmental scrutiny:
  - Halide free material compositions: flame retardant in PWBs?
  - Lead Free: Higher temperature processing
- The use of non-tin/lead coatings will increase, e.g. Au/Ni/Cu, Pd/Cu and/or organic preservatives.
- Compatibility of components/boards with materials and consumables in flux, paste, surface finish, solder mask and cleaning.
- Embedded passives are a technology of interest but a small demand compared to the HDI and “bread and butter” boards.

Materials Challenges

- Environmental scrutiny:
  - Halide free material compositions
  - Lead Free: Higher temperatures
  - Lack of reliability data for lead free joint structure
- Finer features imply:
  - New solder pastes for fine printing
  - Ultra-low residue, no-clean pastes and fluxes and/or new cleaning technologies
  - Understanding of residue impact on high frequency circuits
- Underfill materials for high I/O low standoff arrays:
  - Re-workable
- Cover-coats for harsh environment:

Test Challenges

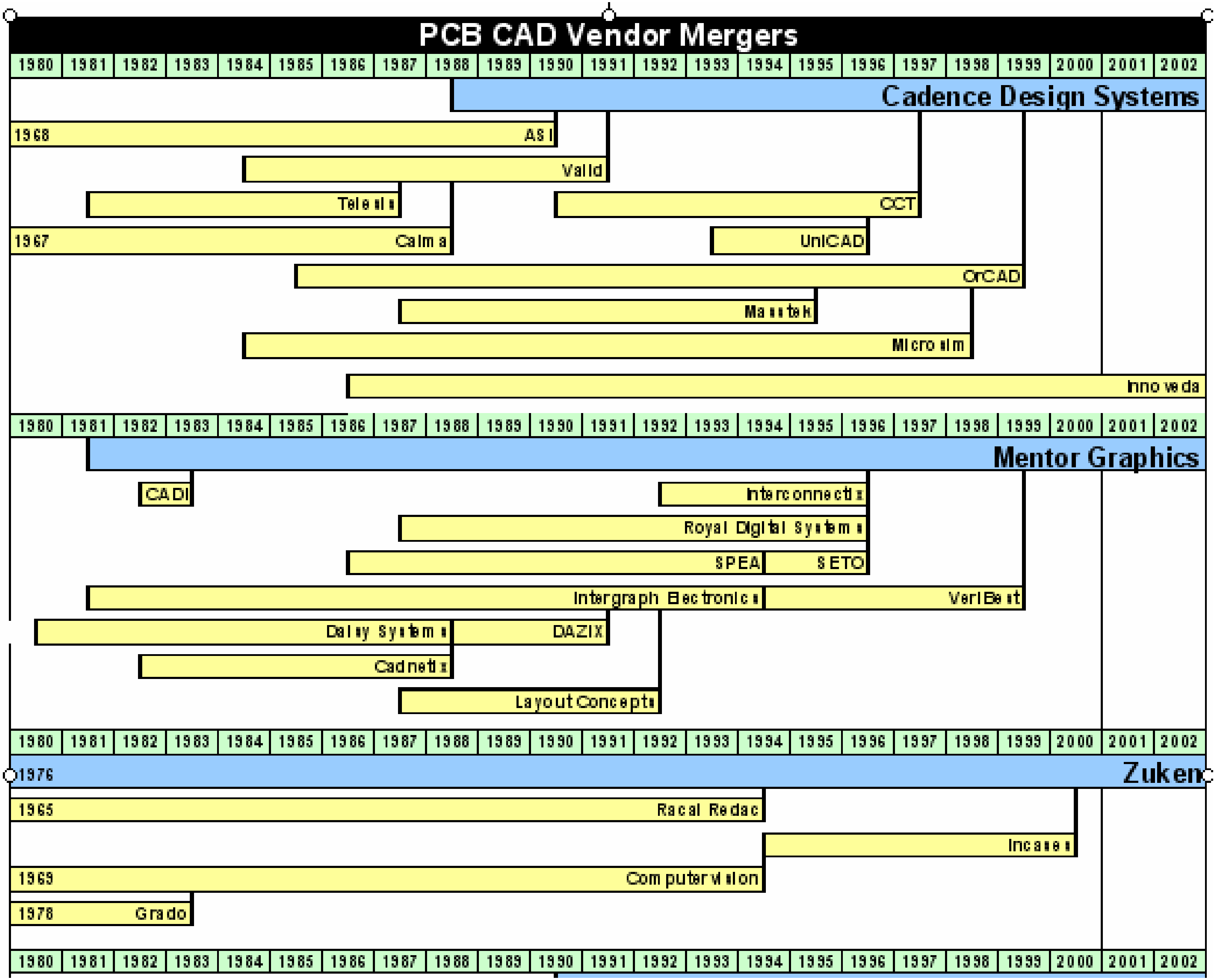
- Density. Density. Density.
- Mixed surface finishes that challenge ICT test probes
- Increased use of no clean with residues that make contact of test probes difficult
- Increased functionality of boards that demands a high level of ICT test access, e.g. 100%
- A multiplicity of products demanding a multiplicity of test fixture types
- Higher speeds of product operation
- Increased use of optical devices that are not testable by traditional electronic methods

Test Challenges (Cont.)

- The need for in depth statistical analysis of data to trouble shoot products
- Advanced test modeling techniques at the design stage, i.e. early development of test vectors and programs for products
  - Determine optimum tradeoffs
  - Boundary scan testing built into the IC
  - Complexity of full nodal access of In-circuit test
- Thin boards
- DFT development for support of contract manufacturing (EMS)

Wither Printed Board Assembly?

- Manufacturing within the U.S. is seeing difficult times
- R&D for manufacturing within OEMs is at an all time low.
- The on-shore operations of EMS providers is experiencing recession difficulties also.
- Manufacturing test and assembly need better support from academia and government to meet the challenges of rapidly changing product technology.
- US industry must position itself without new assembly technology capability
- Design for a specific EMS provider to take full advantage of their equipment and process capability


PCB CAD Vendor Mergers
1980 1981 1982 1983 1984 1985 1986 1987 1988 1989 1990 1991 1992 1993 1994 1995 1996 1997 1998 1999 2000 2001 2002
Cadence Design Systems
1968
ASI
Valid
Telesis
CCT
1967
Calma
UniCAD
OrCAD
Massteck
Microsim
Innoveda
Mentor Graphics
CADI
Interconnectix
Royal Digital Systems
SPEA
ISETO
Intergraph Electronics
VeriBest
Daisy Systems
DAZIX
Cadnetix
Layout Concepts
Zuken
1976
1965
Racal Redac
Incases
1969
Computervision
1978
Grado

CAD Capabilities

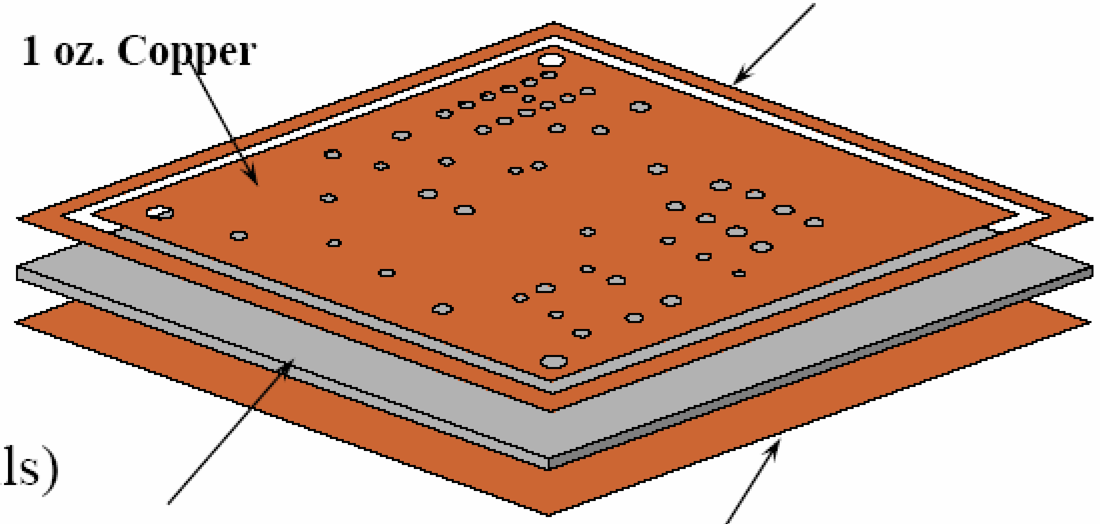
$$C = \frac{.225 A E_r}{t}$$

C= Capacitance (nF)

A=Area of Plates (in^2)

$\mathbf{E_r}$=Dielectric Constant

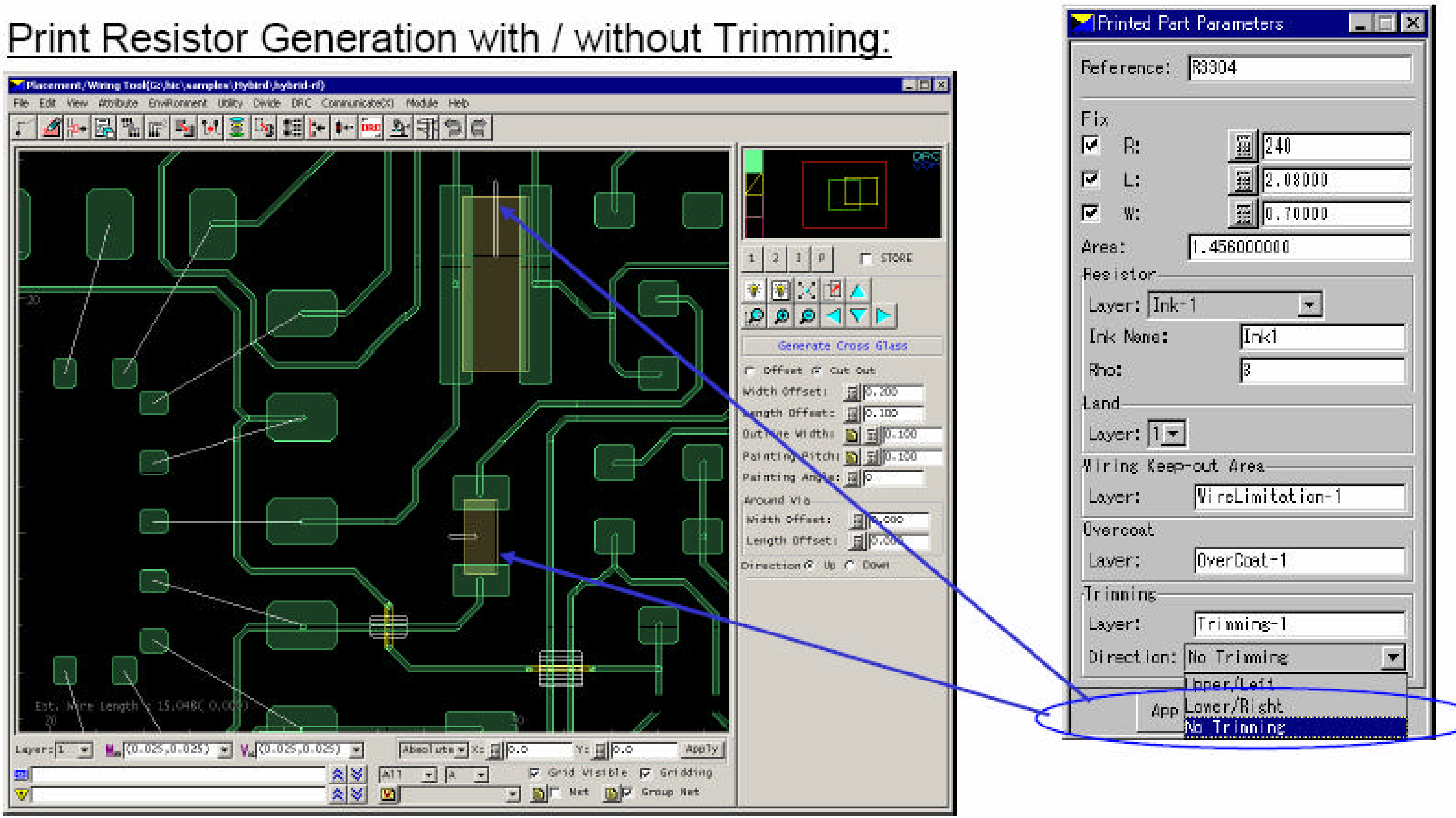
t=Dielectric Thickness (mils)



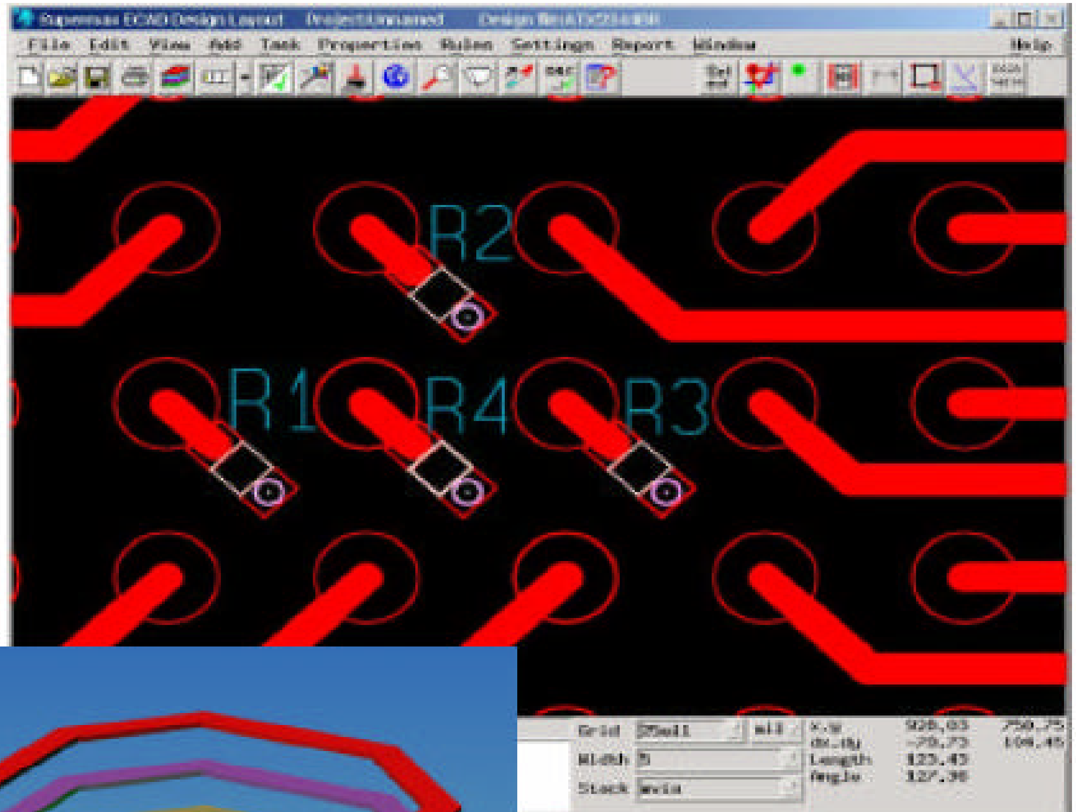
Calculating Capacitance

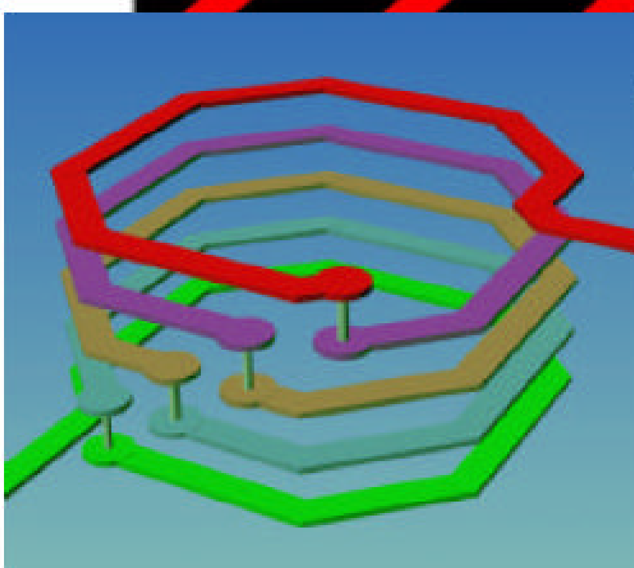
CAD Capabilities (continued)

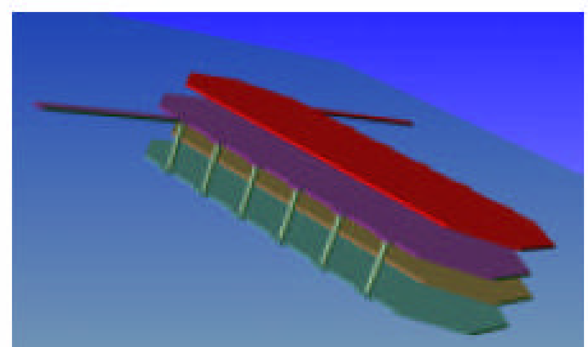
Print Resistor Generation with / without Trimming:



CAD Capabilities (continued)







Conclusions

- Design tools will continually improve
- DFM analysis skills are necessary part of the design responsibility
- Prototype to production will become a greater challenge
- Good designers will become scarce
- Needs for continual education are a must
- Diversification will help the designer to survive the industry changes

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