Low Cost Energy Based TDR Loss Method for PWB Manufacturers

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Abstract
While silicon density doubles approximately every 18 months, following Moore's law, PWB electrical technology advances much more slowly, Up until now trace impedance has been a sufficient high speed electrical specification for PWB traces. PWB manufacturers utilize time domain reflectometry (TDR) to measure trace impedance. The original IPC specification for TDR was written 20 years ago by this author.

Emitter Coupled Logic (ECL) logic drove need for controlled impedance early in the seventies, and considerations of topology and reflections have for some time been the main task for signal integrity engineering. Inevitably, the speed march has pushed gigahertz signaling onto the PWB, which presents new design challenges. At GHz frequencies, for instance, trace loss is actually more important than impedance. New materials and processes for RoHS could affect board loss characteristics.

Traditional loss measurements are done using vector network analyzers (VNA) which are costly and not well suited for a PWB manufacturing operation. A new IPC committee, D24a, has been tasked to develop a low cost TDR/TDT loss measurement method that can utilize pre-existing PWB equipment. The committee's objectives are to develop a low-cost but accurate loss measurement method which empowers PWB manufactures to manage development of low-loss materials and manufacturing methods.

This paper will detail how a single TDR/TDT pulse energy value can be used as a loss specification. It will be shown how this single value method is as serviceable as a VNA measurement, while doing away with the exacting procedures required for the VNA approach.

Chronology – Birth of the digital PWB transmission line
Remember the Corvette Stingray? Well, maybe (or maybe not). This car made its debut at a time when the space race was in its heyday and when computers were in their infancy. Computational circuitry had recently graduated from vacuum tubes, mercury delay lines, and analog servo systems to integration of many transistors on a small silicon monolith. These packaged monoliths were called integrated circuit (IC) chips.

The popular "7400" bipolar logic series operated at frequencies up only to the low megahertz range. But the time required for the signal to change logic states (rise/fall time) implied much faster frequency content. For bipolar logic, this transition time was between 1 and 5 nanoseconds. Managing the faster frequency content would in time prove to be an entirely new problem, leading to the development of a signal integrity discipline. But for now, none of this mattered much.

Circuit interconnects typically used wire wrapping on IC socket posts to achieve high density routing. This was soon replaced with the multi-layer printed wiring board (PWB). With PWB technology, the main problems were electrical opens and shorts. (Interestingly enough, open/shorts are still are a major source of quality issues today).

Waves
Before we get started, let's review the role of waves. How have waves driven PWB requirements? What is a wave on a computer-like board? When do waves become important?

A wave propagates as a digital signal transitions from 1 to 0 (or visa versa). The wave
(i.e. the signal) is transmitted along wires to receivers. In a basic topology we have a transmitter, wire or transmission line, and a receiver. We call the wires on a PWB traces or etches. The wave can be distorted when it encounters an obstruction, defined as any place along the line where the impedance seen by the propagating signal changes.

The wave also occupies physical space. Since the wave is the result of a 0/1 transition, the occupied space is called the transition edge wavelength. It's helpful to visualize this as a series of "freeze frames" as illustrated in Figure 1. Wave disturbance along the line corresponds to a wave disturbance at a respective time.

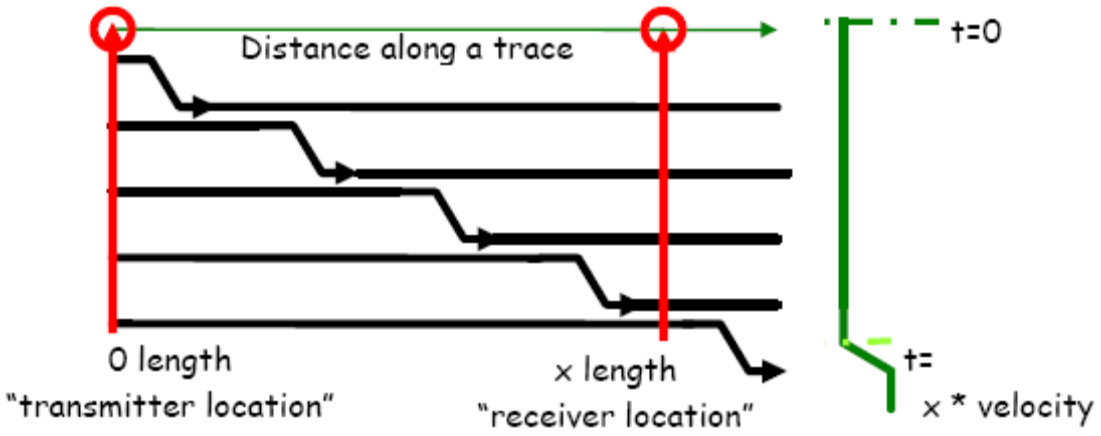

Figure 1 – Relation between Time and Space

When a signal transitions from 0 to 1, the transition time corresponds to the space occupied by the wave propagation. How big is this? How much physical space does this wave occupy? This is only important when we consider the size of electronic circuit paths on which signals are propagating.

For print wiring boards, traces (or channels, to use a term from communications science) range up to a meter in length. The wave front of a 5ns transition time occupies 25 to 30 inches. By contrast, the physical space associated with a data rate of 1MHz is over 600 meters. Hence in the early days of board design, a 7400 logical trace on a PWB was considered a lumped node connection. Most of the signal that was transmitted was received before the next transition, and the question of the time it took a signal to get from the source to a destination (flight time) was irrelevant. In practice, a single source would be connected to any number of receivers.

Even with 5ns edges, it didn't take long to realize that if we put too many loads on a single network the rise time would be degraded. Given a fixed receiver threshold, the limitations to this scheme became apparent, and designers learned to set aside a timing budget item for managing this. The concept became known as "flight time" (not to be confused with the fundamental term associated with propagation constant). Still most of the signal's amplitude was received. Distortion could be determined from simple lumped circuit analysis.

By the 1980's, open-drain CMOS was moving toward 100MHz with 1ns or faster edges (with a spatial wave of six inches). As clock period decreased, less and less time could be tolerated for distortion caused by reflections. Any feature along the trace larger than a quarter wave length (a little over an inch) could contribute to wave distortion. The rapid accumulation of these kinds of problems kindled the field of signal integrity.

A feature change along a transmission line results in an impedance change, causing a portion of the wave to reflect while the remainder is transmitted. This phenomenon follows the law of conservation of energy, much like a mechanical elastic collision. The ratio of transmitted signal to the reflection is called the reflection coefficient (ρ) and is depicted in Figure 2.

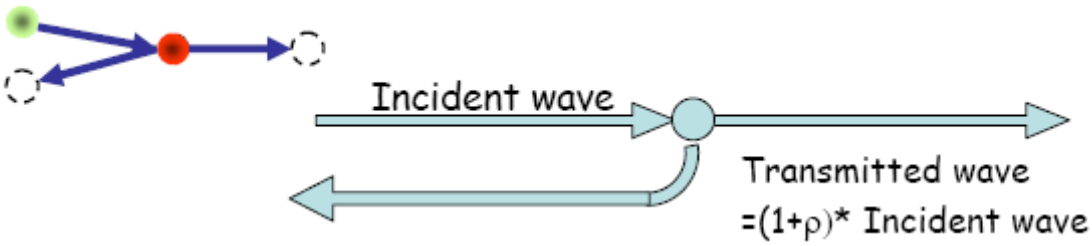

Figure 2 – Incident, Reflected and Transmitted Waves

This reflection may re-reflect at the source or other impedance changes along a line. The net result is that the received wave or signal is distorted. While digital logic is somewhat tolerant of distortion, too much reflection is disastrous. Additive reflections can exaggerate signals so that the resultant voltage wave overshoots or rings back causing damage to chips.

Reflections can also cause edge distortion (also known as ledging or non-monotonicity). This results in flight time changes that can cause loss of data due to set up or hold time violations. These effect are shown in Figure 3

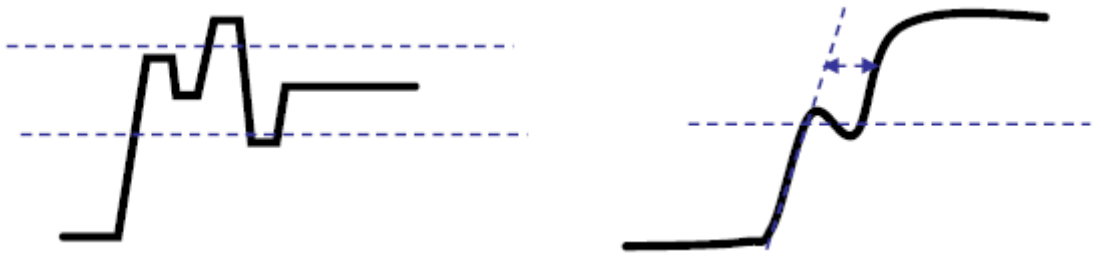

Figure 3 Reflections causing Distorted Signals

Managing Reflections

Reflections can be minimized in several ways. One is to match the transmitter and receiver impedance to the line's characteristic impedance. The other is to control this impedance by design, matching each line segment's impedance. The term "line impedance" or just plain "impedance" may be used when referring the proper term "characteristic impedance". We use either but do acknowledge the distinction.

In the 1980's a call to action in the PWB industry was answered by IPC TM-360 12.5.5.7 which specified time domain reflectometry (TDR) to measure and subsequently to control board impedance.

TDR uses the reflection from a step waveform to determine line impedance and is based on the flowing equation.

$$\rho = \frac{Z_{test\_line} - Z0_{ref}}{Z_{test\_line} + Z0_{ref}} = \frac{V_{reflected}}{V_{incident}}$$

Eq. 1

The TDR waveforms gives us the incident, *Vincident*, and reflected, *Vreflected*, voltages. *Zref* is the reference impedance that corresponds to a "no-reflection" calibration transmission line. This is normally an air dielectric coaxial standard. The impedance of the test line, *Z0test_line*, can be determine from the relations in Equation 1.

TDR has a useful tool for electrical assurance for PWB manufacturing. Typically test coupons are attached to a panel that has representative traces for each layer. The TDR test normally occurs at the end of a PWB manufacturing process. It functions as material and process control gate. Electronic product manufacturers use PWB impedance limits help assure end products will operate reliably by minimizing mismatch on their boards. It is a simple and convenient specification.

"Things are Changing"

Since silicon density is still doubling approximately every 18 months, the corresponding distance signals need to travel between transistors on a silicon chip is decreasing. This in turn results in a data transaction rate increase which is nearly as proportional. (Moore's Law)

We are moving into a new era. Computers before 2000 can be considered "reflections era" designs. Frequencies were tens to hundreds of MHz. As stated before, TDR was used to mange PWB electrical product performance. PWB impedance was the primary electrical performance parameter.

We are entering the era of High Speed Serial Differential (HSSD) gigahertz signaling. Examples include Fibre Channel, XAUI, PCI express, Infiniband, Fully Buffered DIMM, Serial Attached SCSI, and many more. What is really interesting is that the majority of routing on computer boards is trending toward HSSD. Data bits are less than 400ps wide. Some signaling is approaching a 100ps bit width. At these frequencies, the importance of impedance matching is eclipsed by problems of dielectric loss and conductor loss.

With the focus now on loss (attenuation) in differential signaling, let's explore the issues here. Differential signals use 0 volts as the switching threshold. Intuition might suggest that attenuation is centered around 0 volts as shown in the top of Figure 4. This is not actually the case, however. The signal does not just scale down equally with frequency. DC and low frequency signals do not attenuate very much while GHz signal components exhibit extreme attenuation.

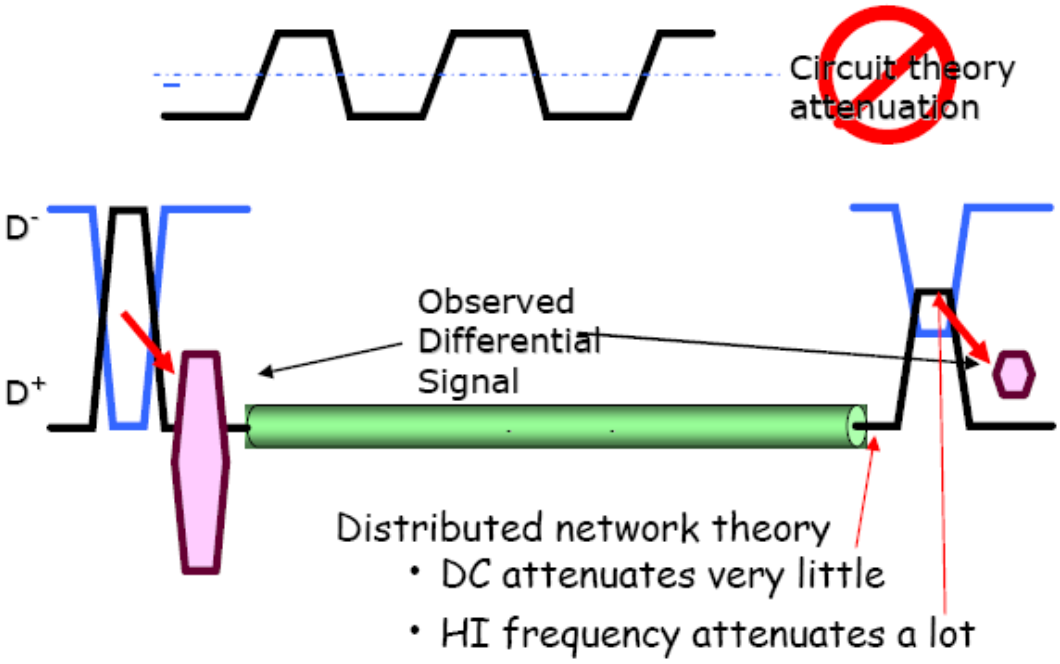

Figure 4 –Frequency Dependent Impacts on GHz Differential Signals

Referring to the bottom of Figure 4, each half of the differential signal attenuates in reference to its own DC (low frequency) voltage. A series of consecutive data bits represents lower frequencies than 101010101 patterns. Each pattern is attenuated differently. If we overlay each of the data bits into a reference unit time interval (UI) or bit time at the receiver, we will notice that that data bits reduce in pulse width and voltage in a manner proportional to the frequency and history of the data. This distortion of data bits is called inter-symbol interference (ISI). Frequency dependent loss results in ISI which can reduce the overall error-free bandwidth of a channel.

We learned how to deal with reflections by controlling impedance with a TDR process. In the "GHz Era", loss becomes the primary problem! Impedance mismatch just represents another form of loss. Board material and construction are prime contributors to loss, and here is where a new PWB test approach is sorely needed.

There are many sources of frequency dependent losses. Examples include loss tangent, dielectric constant, temperature, humidity, chemical absorption, the etch tooth, etch finish, etc. New materials and processes to support initiatives like RoHS and lead free have potential to introduce more frequency dependent loss. Even the stackup and vias can contribute. Above 5 GHz, many vias resonate and can reduce the signal by 70%. It is should be pointed out again that loss has been at best a small nuisance for technologies below 1GHz.

TDR testing empowers board vendors to manage their own process based on direct electrical requirements. We could specify material properties such as loss tangent, specific board raw material vendors, manufacturing process, etc. However, this takes away a degree of empowerment and product differentiation. Since the direct electrical spec is loss, why not empower board manufacturers to manage loss based on the actual requirements? The question is: how?

A vector network analyzer (VNA) has the ability to make very accurate loss measurements. But historically a VNA has not been well suited for the PWB shop floor. The output of a VNA is a complicated list of numbers each with an associated frequency. This list (spectrum) is difficult to write a simple specification around. Our initiative is to use just one number to characterize loss.

The first approach was just to determine the amplitude loss in a pulse. This can be accomplished with existing TDR/TDT equipment. We then asked: "Is this the best way?" So we studied other methods such as peak TDR/TDT pulses, area under TDR/TDT pulses, derivative of TDR/TDT, and root impulse energy (RIE) which was proposed by John Rettig of Tektronix. He suggested that we should be able to come up with a method to assign a single value to represent an impulse response energy loss.

John Abbott of Intel did a sensitivity analysis and determined that RIE fared best, giving the best single-value correlation to s-parameters from a VNA. In the study, a 10% change in loss tangent resulted in 0.095 dB RIE change compared to a VNA

change of 0.110 dB. RIE also was least sensitive to launch noise, least sensitive to edge rate. and had no sensitivity to pulse width. The development of RIE is rooted in the concept of how energy is accounted for in a data transmission system.

Energy

One of Newton's fundamental laws of physics states that "energy needs to be conserved." This is true for systems viewed in the both the time or frequency domain because the frequency domain is nothing but a mathematical manipulation of numbers to allow easier solutions to everyday problems. To satisfy conservation, the energy can be transmitted, reflected, radiated, or absorbed and turned into heat. The energy not delivered to the load is considered lost. The loss can be measured as a ratio of received (Rx) energy to injected (In) energy. That ratio helps determine the signaling transfer characteristics and quality. As stated before, losses can be classified into conductor and dielectric loss. While this may be interesting, only the aggregate loss is important for communication signaling.

Insertion loss is a parameter that is roughly the square root of the ratio of received energy to injected energy and is a function of frequency. Since it is not a single value, it's difficult and complicated to specify in terms of limits. The purpose of this method is to define a single energy loss value as a quality factor. .

Insertion loss, s21, is roughly given by following equation;

$$s21 \approx \sqrt{\frac{V_{rcvd}}{V_{transmit}}} \qquad \text{Eq. 2}$$

,where the received and transmitted voltage as functions of frequency.

Since it is not a single value due to different losses at every frequency point in the spectrum it is difficult and complicated to specify the loss in terms of limits. The purpose of this method is to define and utilize a single energy loss value as a quality factor.

The derivation of RIE loss follows:

$$E = V * I * T \qquad \text{Eq. 3}$$

From an electrical perspective, energy is simply product of voltage current and time

Let's consider that measurement equipment source and load impedance is R. Therefore recombining with ohms law reveals the following:

$$E = \frac{V^2}{R} * T \qquad \text{Eq. 4}$$

We need to integrate over all time to get the total energy as follows:

$$E = \int \frac{V(t)^2}{R} * dt \qquad \text{Eq. 5}$$

The following two equations define injected energy, *Ein*, and received energy, *Erx*, where *Vin* and *Vrx* characteristic voltages measured at the transmitter and receiver respectively**:**

$$E_{In} = \int \frac{V_{In}(t)^2}{R} * dt \qquad \text{Eq. 6}$$

$$E_{Rx} = \int \frac{V_{Rx}(t)^2}{R} * dt \qquad \text{Eq. 7}$$

We now can define the root impulse energy (RIE) loss as a ratio as the follows:

$$RIE_{loss} = \frac{E_{In}}{E_{Tx}} = \frac{\sqrt{\int V_{Rx}(t)^2 * dt}}{\sqrt{\int V_{In}(t)^2 * dt}}$$

Eq. 8

The RIE loss in dB, *RIEloss_dB*, becomes the dB ratio of the RIE of a calibration line and test line.

$$RIE_{loss\_dB} = 10 * \log\left(\frac{\sqrt{\int V_{Rx}(t)^2 * dt}}{\sqrt{\int V_{In}(t)^2 * dt}}\right)$$

Eq. 9

The calibration line is associated with the injected energy and normally contains the RIE associated with the edge, cables, launch, and a small section of transmission line. The test line is identical to the calibration line but only longer and is associated with the received energy. The RIE associated with the received signal also includes cables and launch but has a longer section of line. Thus dividing the *RIEloss_dB* by the length difference between the calibration line and test line results in a *RIEloss_dB* per unit length quantity. This in turn can be associated with a specified channel loss. Optionally an un-normalized *RIEloss_dB* value can be used if the calibration and test line structures are rigorously specified.

An impulse response is required to encompass the widest possible frequency range so that all energy is considered. TDR and TDR utilize a step response, *Vtdr_tdt_in* and *Vtdr_tdt_rx*. The derivative of the TDR or TDT step response is the impulse response. Thus impulse responses can be derived from a TDR or TDT signal by differentiating as follows:

$$V_{rx}(t) = d\frac{V_{tdr\_tdt\_rx}(t)}{dt}$$

Eq. 10

$$V_{In}(t) = d\frac{V_{tdr\_tdt\_in}(t)}{dt}$$

Eq. 11

Substituting in derivatives and converting to dB results in the following *RIEloss_dB* equation:

$$RIE_{loss\_dB} = 10 * \log\left(\frac{\sqrt{\int\left(d\frac{V_{tdr\_tdt\_rx}(t)}{dt}\right)^2 * dt}}{\sqrt{\int\left(d\frac{V_{tdr\_tdt\_in}(t)}{dt}\right)^2 * dt}}\right) = 10 * \log\left(\frac{IE_{test\_line}}{IE_{calibration}}\right)$$

Eq. 12

TDR vs. TDT

There are issues with TDR and TDT methods. Both will be included in IPC TM 360 2.5.5.12. TDT requires 2 probes, however it may be more accurate. TDR is easier for hand-held probes. TDR relies on end reflection which may vary between test specimen manufacturing methods.

Multilayer boards have vias that contribute to loss. Remember we said reflections also result in losses. These effects need to be compensated for as well as the probe and launch. The above methods only partially compensate since reflection many not be calibrated out. D24a is working on measurement data and analysis to quantify if TDT has a distinct advantage over TDR.

Example

RIE test coupons are composed of a short calibration trace and a longer test trace as shown in Figure 5.

As an example we will use TDR to illustrate the process of acquiring an RIE value. The calibration length is ½ inch and the test line is 12.5 inches. The TDR waveforms are on the right in Figure 6 and the TDR derivative squared is on the left. Notice how much larger the ½" trace is than the 12.5 inch test trace in the leftmost graphs, indicating energy loss

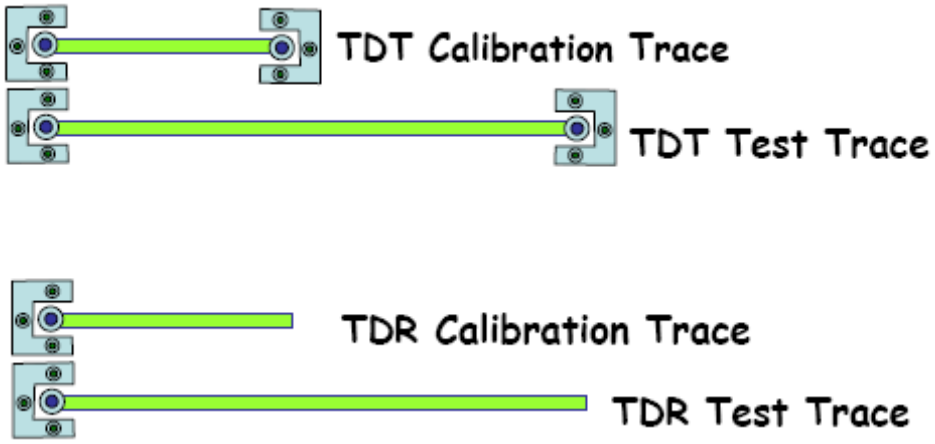

Figure 5 - RIE Test Coupons

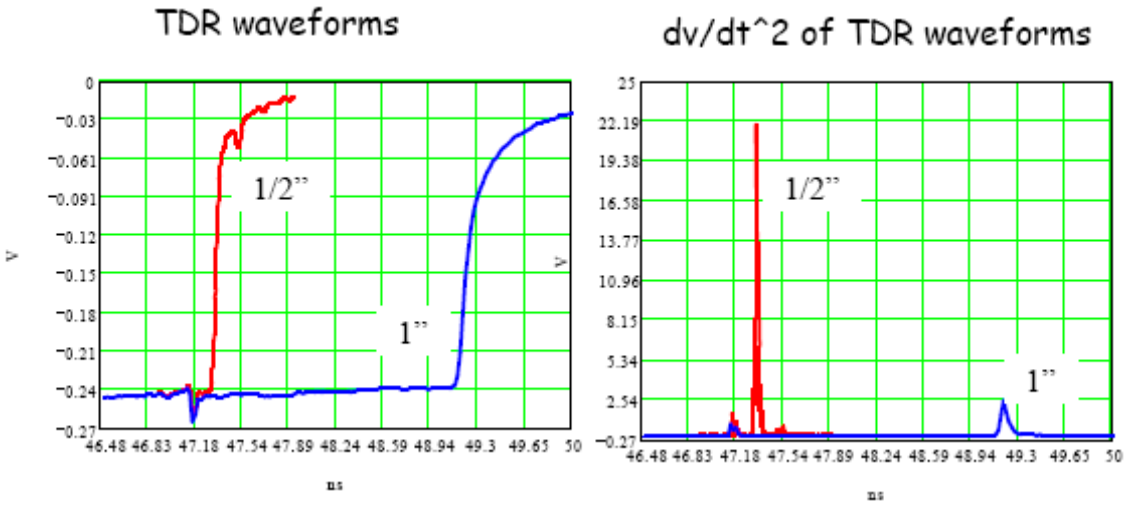

Figure 6 - TDR RIE Waveforms

Processing the waveform in Figure 6 results in the following:

$$RIE_{test\_line} = \sqrt{\int \left(d\frac{V_{tdr\_tdt\_test}(t)}{dt} \right)^2 * dt} = 7.791E3 \frac{\sqrt{J * ohm}}{\sec}$$

Eq. 13

$$RIE_{calibration} = \sqrt{\int \left(d\frac{V_{tdr\_tdt\_cak}(t)}{dt} \right)^2 * dt} = 1.468E4 \frac{\sqrt{J * ohm}}{\sec}$$

Eq. 14

Substituting these values into Equation 12 result in 2.75212 dB RIE loss.

$$RIE_{loss\_dB} = -10 * \log\left(\frac{RIE_{test\_line}}{RIE_{calibration}}\right) = 2.75212dB$$

Eq. 15

Traceable to VNA measurements

The insertion loss measured by a VNA is essentially a system response function. The inverse Fourier transform of the system response in an impulse response. The impulse response is the derivative of the step response which corresponds to a TDR or TDT waveform as shown in Equation 16.

Given:

$$s21(f) = fft(d\frac{V_{step}(t)}{dt})$$

Eq. 16

Then:

Parseval's relation suggests that there is a relationship between RIE derived from a TDR/TDT impulse response and that generated with insertion loss (S21) from a VNA as follows.

$$-10 * \log\left(\frac{\sqrt{\int\left(d\frac{V_{tdr\_tdt\_test}(t)}{dt}\right)^2 * dt}}{\sqrt{\int\left(d\frac{V_{tdr\_tdt\_cal}(t)}{dt}\right)^2 * dt}}\right) = -10 * \log\left(\frac{\sqrt{\frac{1}{2*\pi}\int(s21_{test}(j\omega))^2 * d\omega}}{\sqrt{\frac{1}{2*\pi}\int(s21_{cal}(j\omega))^2 * d\omega}}\right)$$

E1. 17

The TDR/TDT step may not account for all the energy that may be injected into a system, so VNA based value will likely be higher. However TDR/TDT loss specification will correlate to VNA data. The task for D24a is to sufficiently specify test coupons and edge rates to measure energy loss that is reproducible and traceable to refereed VNA data.

Summary

RIE is both evolutionary and revolutionary. It can utilize exiting TDR hardware although additional software may be required. Hence we have a migration path from controlled impedance testing (TDR) which would not require new skill sets employed in a PWB fabrication facility.

RIE enables a single measurement value based on electrical needs of the final product. The single RIE value is electrically usefully to both system designers and PWB suppliers. It enables PWB vendors to manage their own material and process without being locked into a requested single supplier. It also enables PWB vendors to trade off dielectric loss for other trace characteristics. RIE can be used to electrically evaluate and test products which employ new materials and processes that support RoHS.

Low Cost Energy Based TDR Loss Method for PWB Manufacturers

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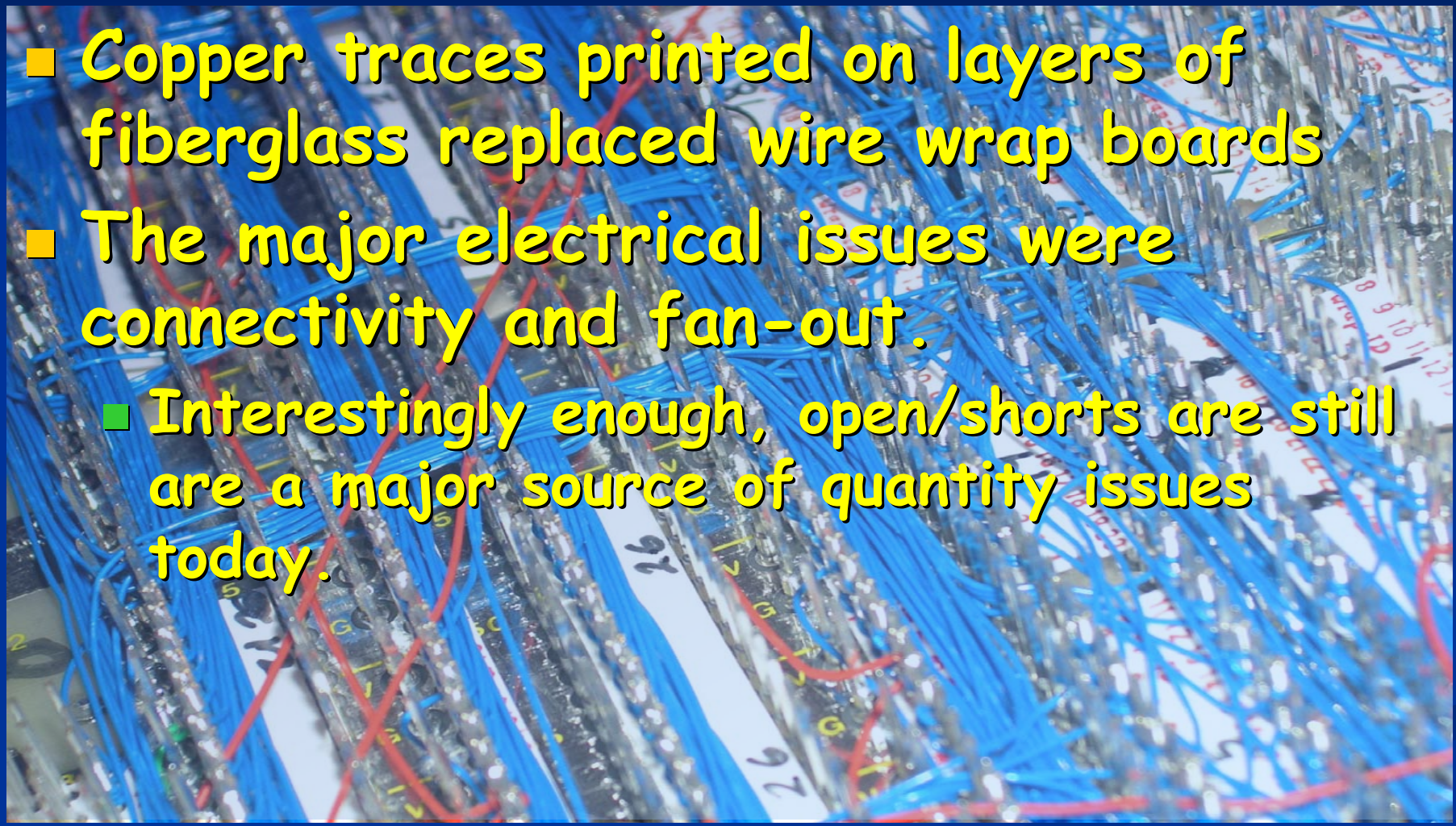
Chronology

- In the 1960's and early 1970's digital logic chips became popular.
  - Remember the Corvette Stingray? ☺
  - Remember when clock rates were megahertz and edges were nanoseconds.
- Computers graduated from vacuum tubes, mercury delay line, and analog servos, to integrated circuit (IC's)
- Remember "7400" bipolar logic

PWBs Enabled Volume Mfg.



- Copper traces printed on layers of fiberglass replaced wire wrap boards
- The major electrical issues were connectivity and fan-out.
  - Interestingly enough, open/shorts are still are a major source of quantity issues today.

Prelude to The History of Signaling

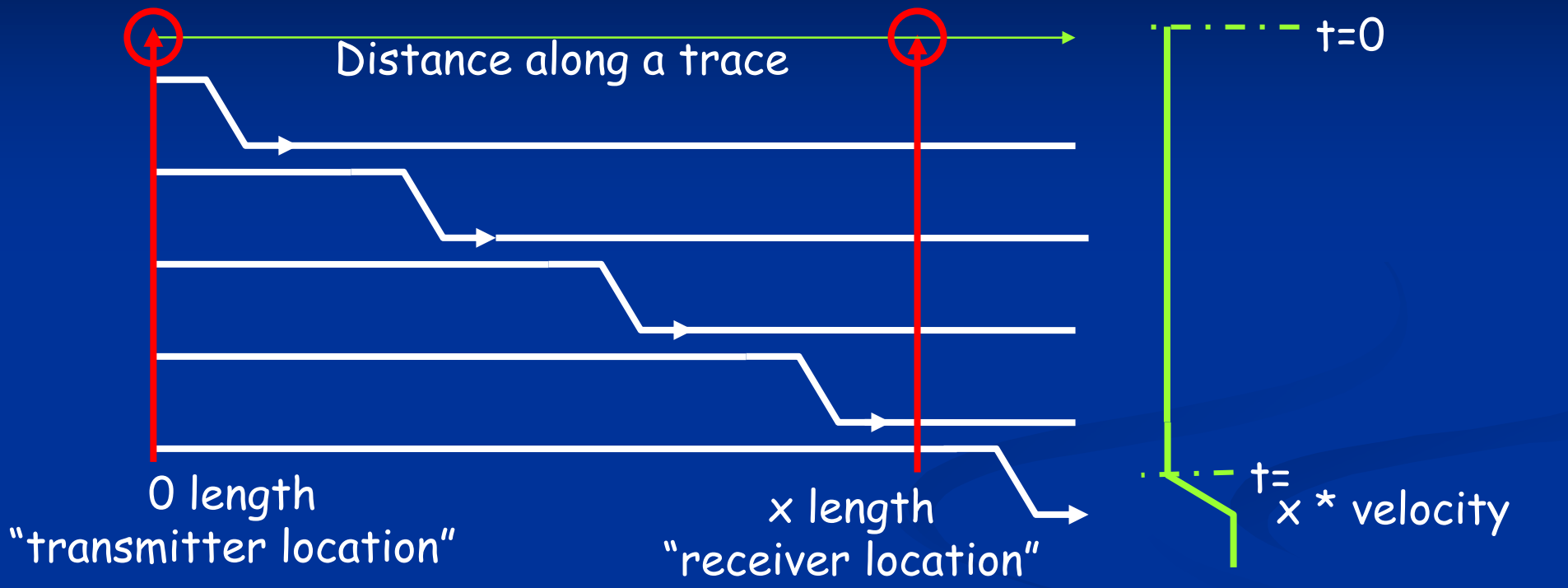
- Before we start, let's review the role of waves:

- How have waves driven PWB requirements?
- What is a wave on a computer-like board?
- When do waves become important?

Edge transition time

- A wave propagates as a digital signal transitions from 1 to 0 (or visa versa).
  - it can be impeded when the wave encounters an obstruction.
- It also occupies physical space.
- The occupied space is called the transition edge wavelength.
  - Lets keep this in mind for latter

The relation between time and space



- Spatial waves and time waves appear inverted with respect to one another.
- Wave disturbance along a line corresponds to a wave disturbance at a respective time.

Why is transition time important?

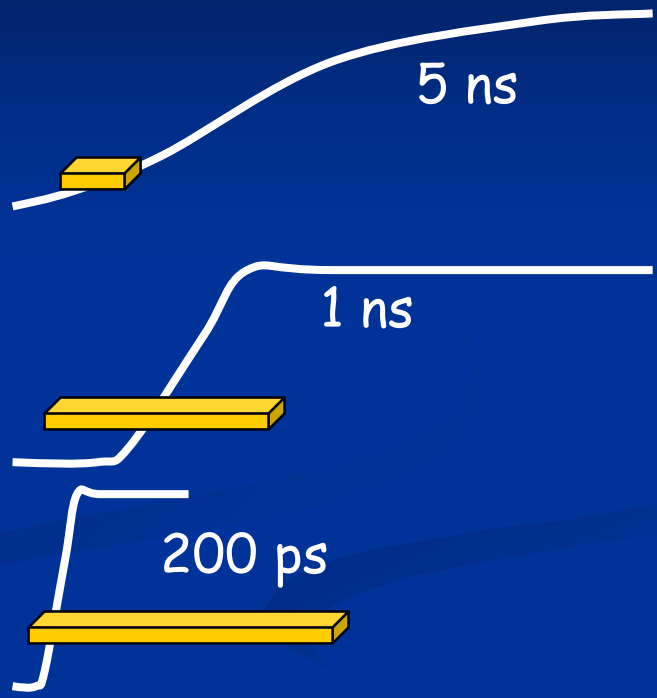
- Transition time determines how much physical space the wavefront occupies.
- PWB traces are about half inch to a few feet.
- A transition of 5 ns occupies 25-30 inches.
- The space associate with a megahertz signal is around 600 meters.
- At few MHz, the uptake is that
  - most of the signal that is transmitted is received
  - the time it takes a signal to get from the source to a destination, call flight time, is negligible.

When are waves important?

Lumped circuit

Increasing relevance of waves

Transmission line

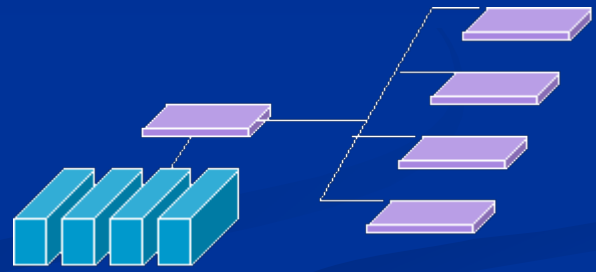


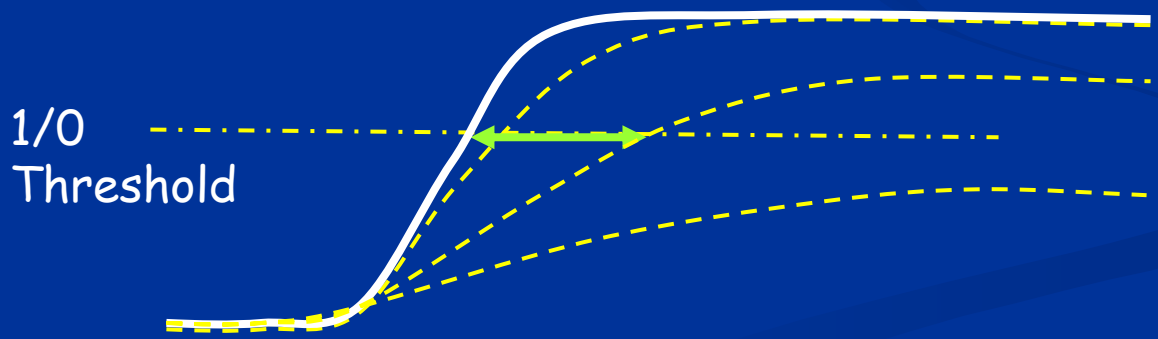
6" of trace vs. rise time

- It all depends on edge rate

Even with 5ns edges, it didn't take long to realize:

- Too many loads on single network degraded rise time and amplitude
- Result:
  - Delayed receipt of signal
  - Data not received





Moving through the 70's

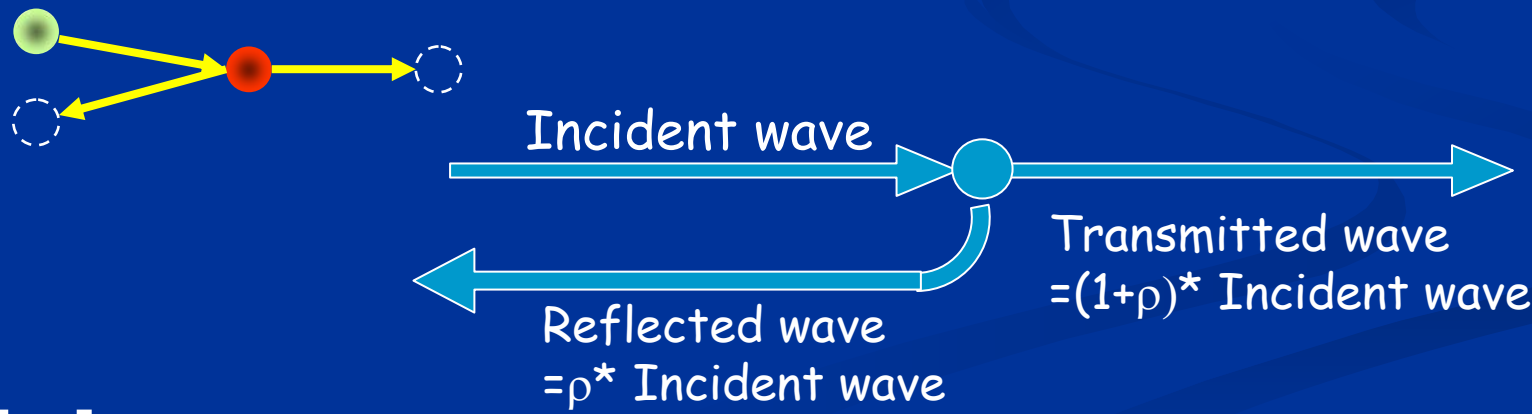
- Some computers started to use emitter coupled logic (ECL) which required termination. Speed was still in the 10's of MHz and while edges pushed toward 1 ns.
  - Around then we started to think about characteristic impedance (Z0) on computer boards
  - Mostly, we were worried about loading and fan-out.
  - Delay on wires was not really a big consideration

The 80's

- … brought on hi speed CMOS and open drain busses
- Computers moved toward 100 MHz operation and had 1ns edges
- As clock period decreases
  - Less and less time can be tolerated for distortion caused by reflections.

Reflections and Characteristic Impedance

- Any impedance change along a transmission lines causes a portion of the wave to reflect and the remainder to be transmitted.
  - The basic reason to is support conservation of energy.
  - It's much like an mechanical elastic collision.



Reflections and Distortion

- The reflection may re-reflect at the source or other impedance changes along a line.
- The net result is that received wave or signal is distorted.
- Digital logic is somewhat tolerant of distortion

Too much distortion is bad

- Additive reflections can exaggerate signals so that resultant voltage wave over shoots or rings back causing damage to chips.
- Reflections can cause edge distortion
  - This results in flight time changes that can cause loss of data due to set up or hold time violations.

Managing Reflection

- Reflection can be minimized
  - Matching transmitter and receiver impedance to line (characteristic) impedance
  - Matching line segment to line segment impedance
- 1980's – call to action in PWB industry
  - Controlled impedance "boards" became part of PWB specifications
  - Time domain reflectometry (TDR)
    - IPC TM-360 12.5.5.7

TDR

- Utilizes a reflection of a step waveform to determine line impedance

$$\rho = \frac{Z_{load} - Z0_{line}}{Z_{load} + Z0_{line}} = \frac{V_{reflected}}{V_{incident}}$$

- The TDR waveforms give us the incident and reflected voltage
- The line can be considered the reference impedance (or an air dielectric coax standard).
- The load is considered the trace under test
- From these relationships, we determine trace's characteristic impedance (Z0)

Electrical Assurance using TDR

- TDR is a useful tool for PWB manufacturing
- Typically test coupons are attached to a panel that has representative traces for each layer.
- The TDR test occurs at the end of the PWB process
  - Functions as material and process control gate.
- Electronic product manufacturers use PWB impedance limits help assure end products will operate reliably
  - It is a simple and convenient specification

The Past Era, Reflections

- Situation: Silicon density doubles approximately every 18 months. Clock speeds follow. (Moore's Law)
- We are moving from this into a new era.
- We were in the "reflections era"
  - Tens to hundreds of MHz
  - TDR was used to mange PWB
  - Impedance was the primary electrical parameter for PWBs.

Things are changing -The GHz Era

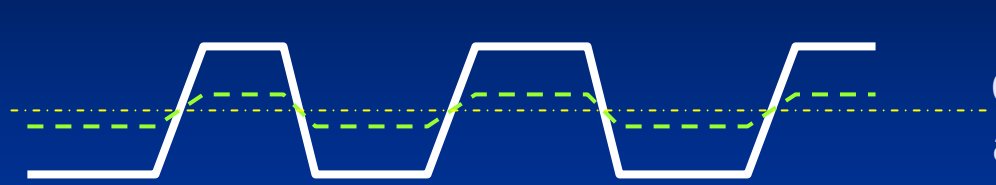
- We are entering the era of High Speed Serial Differential (HSSD) gigahertz signaling
  - Ex: Fibre Channel, XAUI, PCI express, Infiniband, Fully Buffered DIMM, Serial Attached SCSI , and more
  - Majority of routing is trending toward HSSD
- Data bits are less than 400 ps wide
  - Some signaling is approaching a 100 ps bit width

What changed?

- Why is this a new era?
- In last era
  - Most of the amplitude of the transmitted signal was received
  - Albeit, it may have been distorted.
  - Let call this the "reflection era"
- Now
  - Most of the signal may be lost!
  - Hence the GHz era is the "loss era"

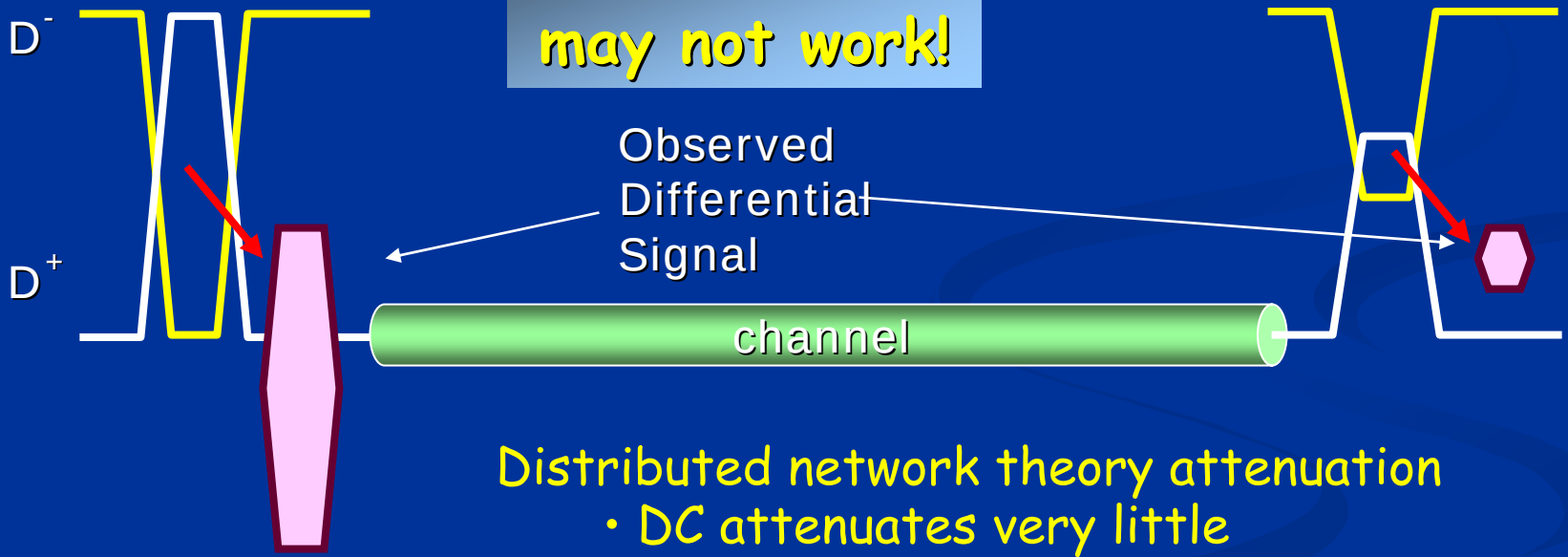
Loss, loss, loss .....

Frequency Dependence Impact



Circuit theory attenuation

Your intuition may not work!



Distributed network theory attenuation

- DC attenuates very little
- HI frequency attenuates a lot

This effect causes ISI and can reduce signals more than expected

Why is this important for PWB's

- We learned how to deal with reflection by controlling impedance with a TDR process
- In the "GHz Era", loss becomes a primary problem!
- Impedance mismatch just results in another form of loss.
- Board material and construction are prime contributors to loss.

What causes PWB loss?

- New materials and processes to support RoHS may impact on PWB loss.
- Dielectric properties.
  - Loss tangent
  - Dielectric constant
- Environmental conditions
  - Temperature & humidity
- Chemical absorption – (during mfg. process)
- Polar molecules have potential for significant frequency dependant loss
- Trace roughness – (new technologies to support RoHS)
  - The "tooth" and the finish
- PWB construction
  - stackup, glass weave, and vias

EMPOWERMENT

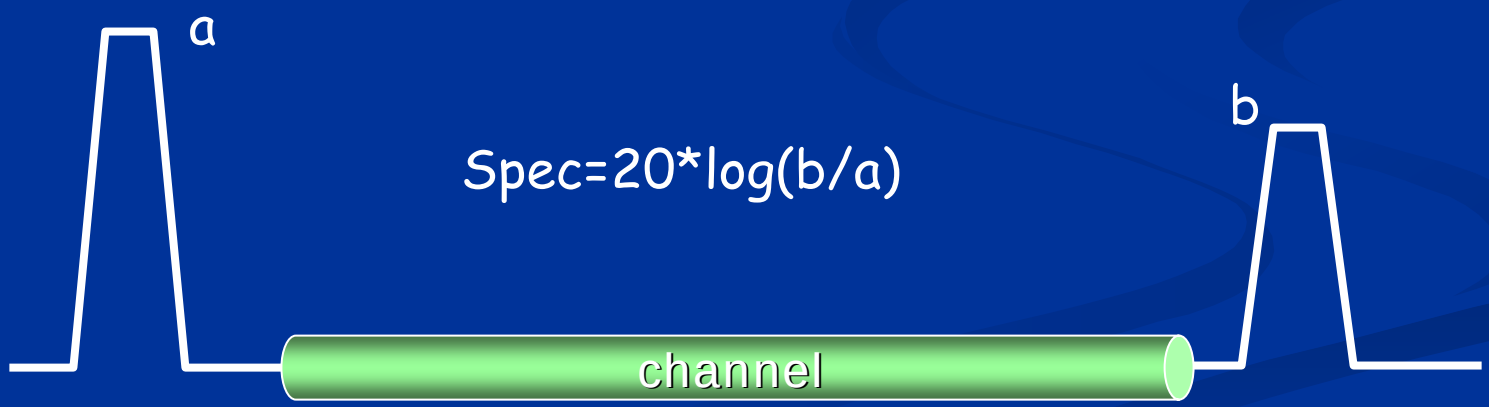
- TDR testing empowers board vendors to manage their own process based on direct electrical requirements
- We could… specify material properties
  - Example: loss tangent, specific board raw material vendors, manufacturing process, etc.
  - This takes away a certain degree of empowerment and product differentiation.
- Since the direct electrical spec is loss;
  - Why not empower board manufacturers to manage loss based on the real electrical requirement
  - The only question is: how?

The Best Way for Accuracy

- Best may not be best.
- A vector network analyzer (VNA) has the ability to make very accurate loss measurements.
- Historically a VNA has not been well suited for the PWB shop floor.
- The output of a VNA is a list of numbers each with an associated frequency
- This list (spectrum) is difficult to write a simple specification around

The Best Way for PWB Process

- Use one number to characterize loss
- The first approach was just to determine the amplitude loss in a pulse.
- This can be accomplished with existing TDR/TDT equipment



Progression methods

- We then asked: "Is this the best way" So we entertained other methods
  - Integrated the square of the pulse and compared areas under the curves.
  - Differentiating the pulse or step
  - In reality, the loss is an energy loss
    - John Rettig of Tektronix suggested that we should be able to come up with method to assign a single value for an impulse response energy loss. (system response)
    - Taking square root of this quantity yields the same units as the VNA
    - We called this root impulse energy (RIE) loss
    - The energy loss would span a wide frequency range.

RIE Chosen

- John Abbott of Intel did a sensitivity analysis for the following methods
  - Peak pulse
  - Area under pulse
  - Derivative of TDR
  - Root Impulse Energy
- RIE faired best
  - Most sensitive
    - 10% change in dielectric constant resulted in 0.095 dB change compared to a VNA change of 0.11 dB
  - Least sensitive to launch noise.
  - Least sensitive to edge rate.
  - No sensitivity to pulse width.

Utilizing the System Response

- Since the TDR/TDR equipment utilized a step waveform
  - This produces a step response.
- If we differentiate the step response we get a impulse response.
- We know from network theory the impulse response can be convolved with any input to get an output.

How do we get to energy loss

- The impulse response has the units volts
- If we square that and divide by the reference impedance.
  - Volts^2/ohms
- Integrating Volts^2/ohms over time results in Volts^2/ohms*sec which is energy.
  - This gives us a single number that is representative of energy

$$E = \frac{V^2}{R} * T$$

- We are looking for the ratio output to input energy. The resistance terms cancels out.
  - For convenience we take the square root which make the units the same as a VNA would produce
  - Next we report the data in power dB, 10*log*(x)

TDR vs TDT

- There are issues with both methods
- Both will be in IPC TM 360 2.5.5.12
- TDT require 2 probes it may be more accurate.
- TDR is easier for hand held probes
- TDR relies on end reflection which may vary between test specimen manufacturing methods.
- Multilayer boards have vias that contribute to loss
  - Remember we said reflections also result in losses.
  - These need to be compensated for as well as the probe and launch.
- D24a is working on measurement data and analysis to quantify if TDT has a distinct advantage over TDR.

Root Impulse Energy

- We will call the energy loss parameter root impulse energy (RIE) loss

$$RIE_{loss\_dB} = -10 * \log\left(\frac{\sqrt{\int\left(d\frac{V_{tdr\_tdt\_test}(t)}{dt}\right)^2 * dt}}{\sqrt{\int\left(d\frac{V_{tdr\_tdt\_cal}(t)}{dt}\right)^2 * dt}}\right) = -10 * \log\left(\frac{RIE_{test\_line}}{RIE_{calibration}}\right)$$

Traceable to VNA Measurements

- Parseval's Relation

Given:

$$s21(f) = fft\left(d\frac{V_{step}(t)}{dt}\right)$$

Then:

$$-10*\log\left(\frac{\sqrt{\int\left(d\frac{V_{tdr\_tdt\_test}(t)}{dt}\right)^2 * dt}}{\sqrt{\int\left(d\frac{V_{tdr\_tdt\_cal}(t)}{dt}\right)^2 * dt}}\right) = -10*\log\left(\frac{\sqrt{\frac{1}{2*\pi}\int\left(s21_{test}(j\omega)\right)^2 * d\omega}}{\sqrt{\frac{1}{2*\pi}\int\left(s21_{cal}(j\omega)\right)^2 * d\omega}}\right)$$

RIE Process

- The process is basically the same for TDR or TDT
- Measure a short trace, this is called the calibration trace
- Measure a long trace. This is called the test specimen
- Find RIE loss with the previous equation

How did we get there?

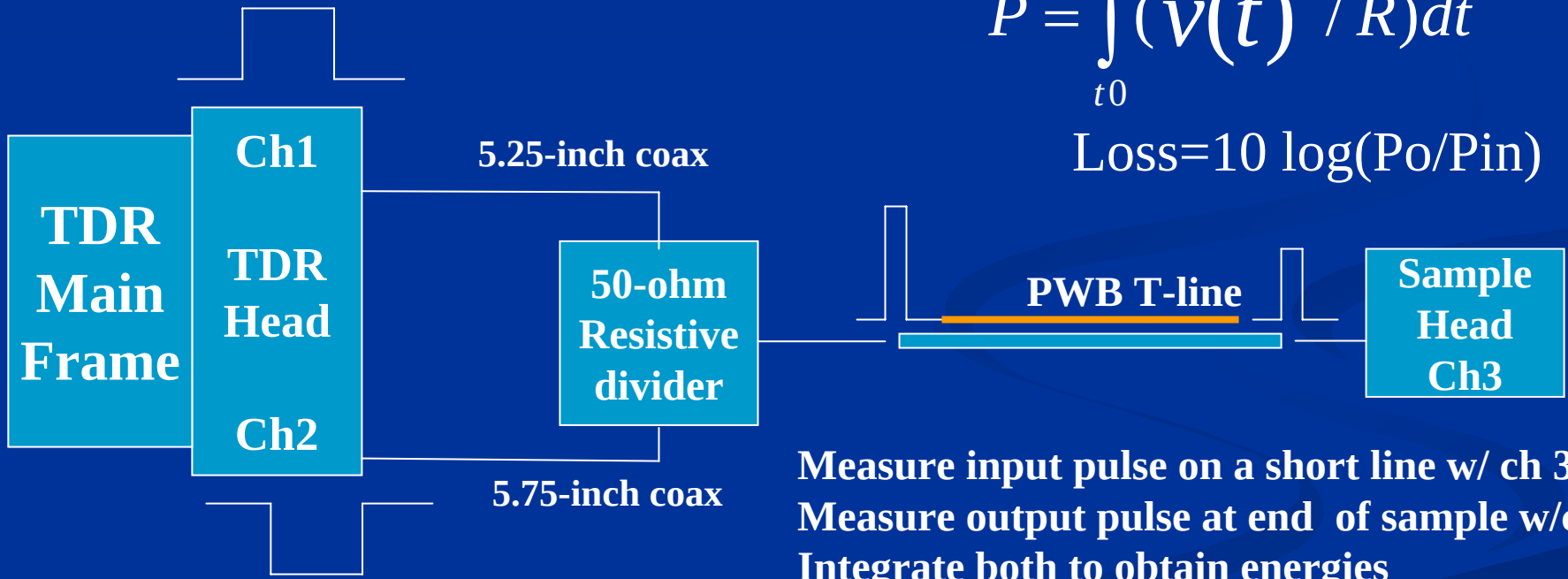
- Borrow from communications science
  - A single pulse response is used to determine channel quality
    - Pulse response is convolved with bit stream
    - Also called pulse analysis
- Observation:
  - Channels with lower loss materials have larger pulses
- Action:
  - Kindled D24a development of loss measurement technique
    - Targeted for IPC TM-360 2.5.5.12

First Investigation: TDT measurement of loss

- Work done by Paul Hamilton, Intel Corporation
- Use the TDR in differential mode to generate a narrow pulse (~100 ps ~ 5GHz)

$$P = \int_{t0}^{tf} (v(t)^2 / R)dt$$

Loss=10 log(Po/Pin)

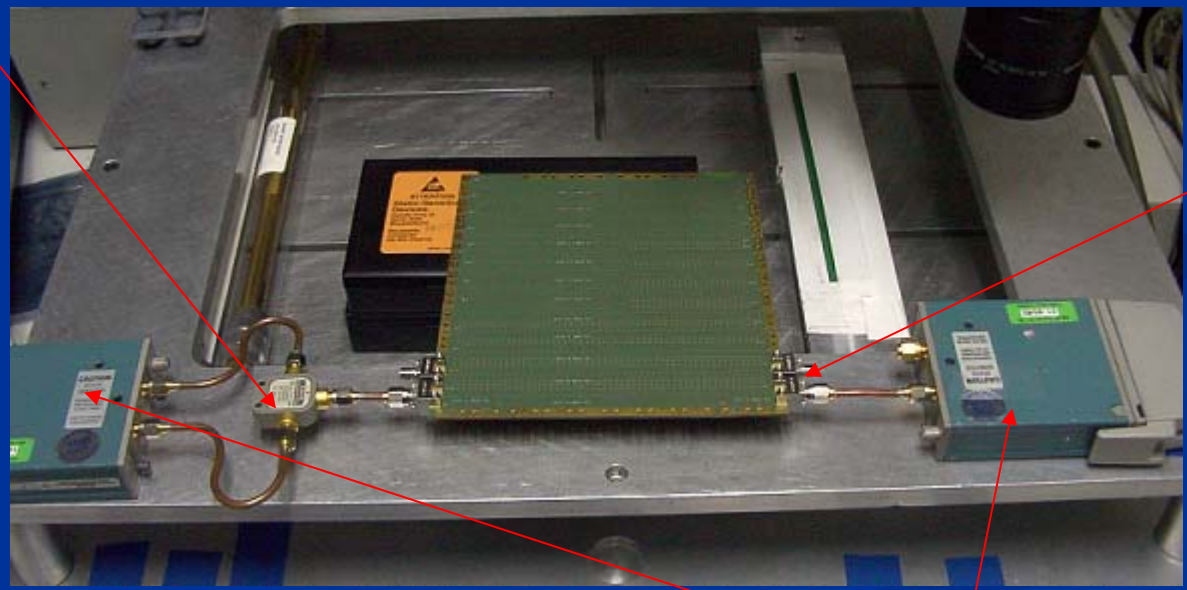


Coax prop rate is 100ps/inch (with teflon di-electric)

Measure input pulse on a short line w/ ch 3
Measure output pulse at end of sample w/ch 3
Integrate both to obtain energies
Difference is loss
Correlate with VNA measurements

First Experiments – Paul Hamilton, Intel Corparation

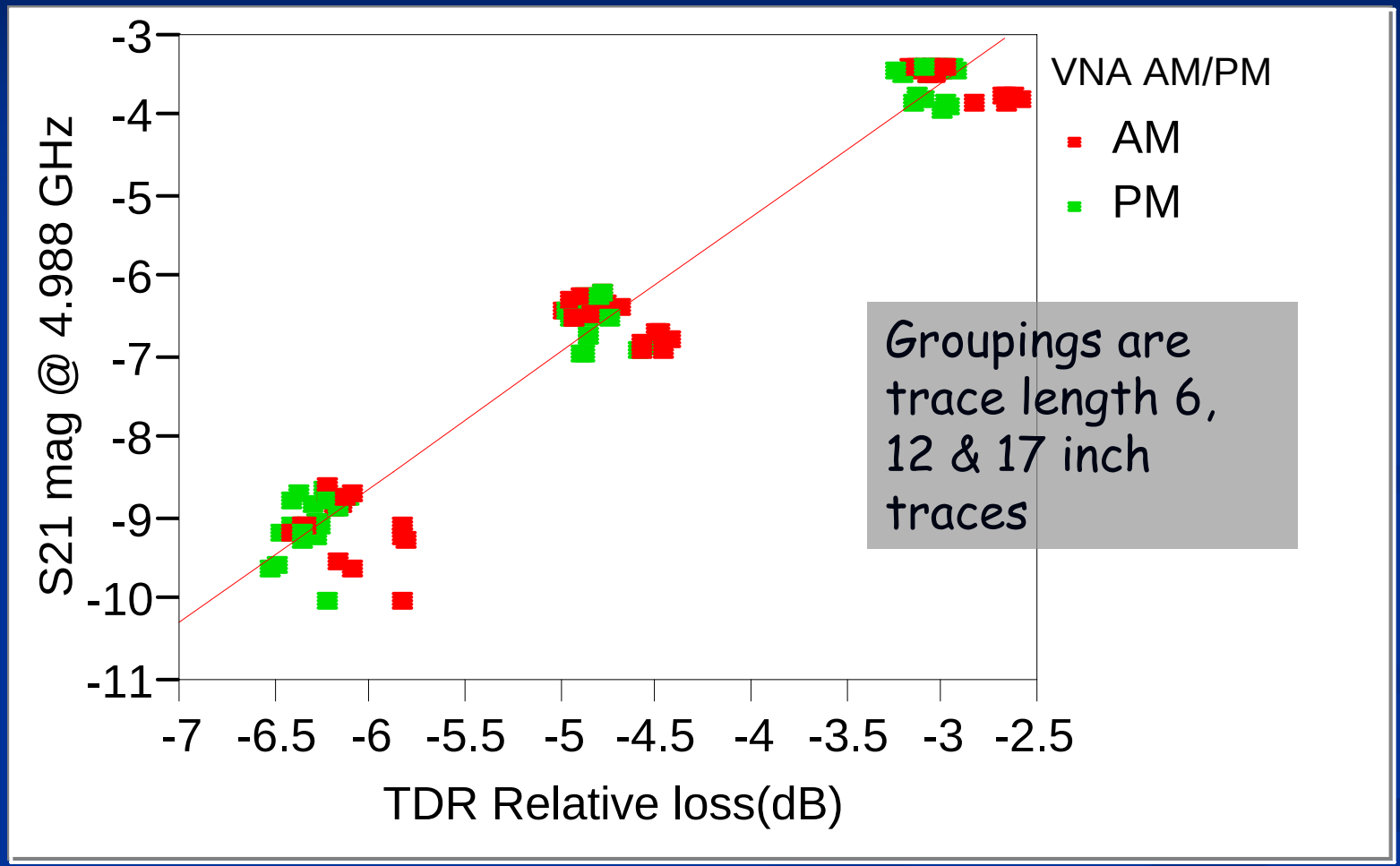
50-ohm resistive splitter/combiner



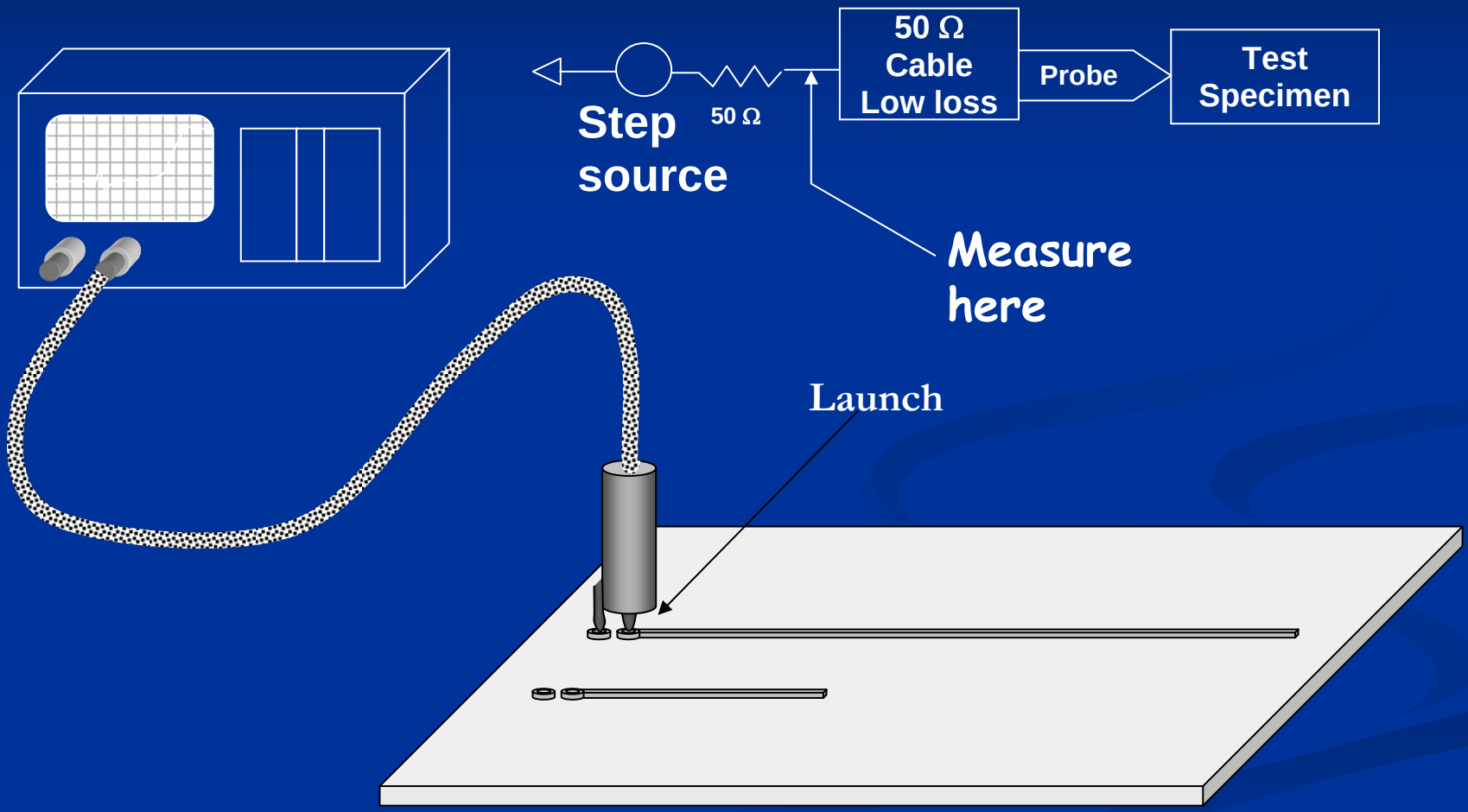
Edge-located connector

TDR heads on extension cables

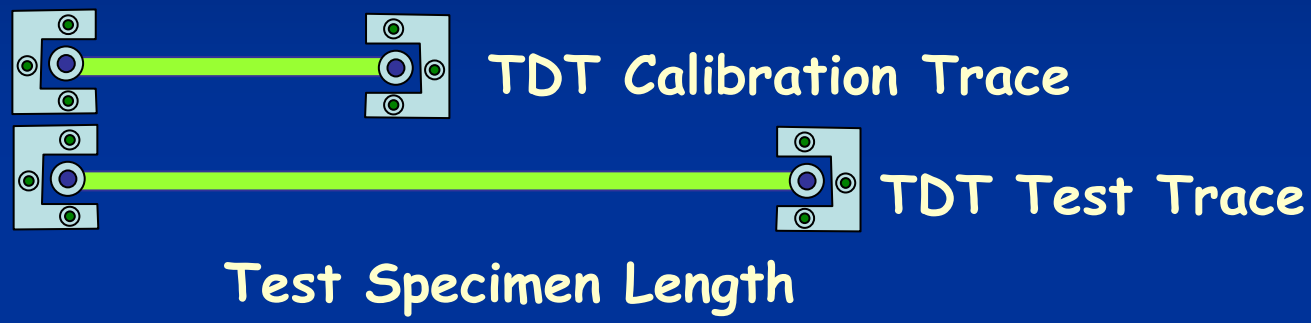
Proof of Concept



The Proposed Process – TDR Setup

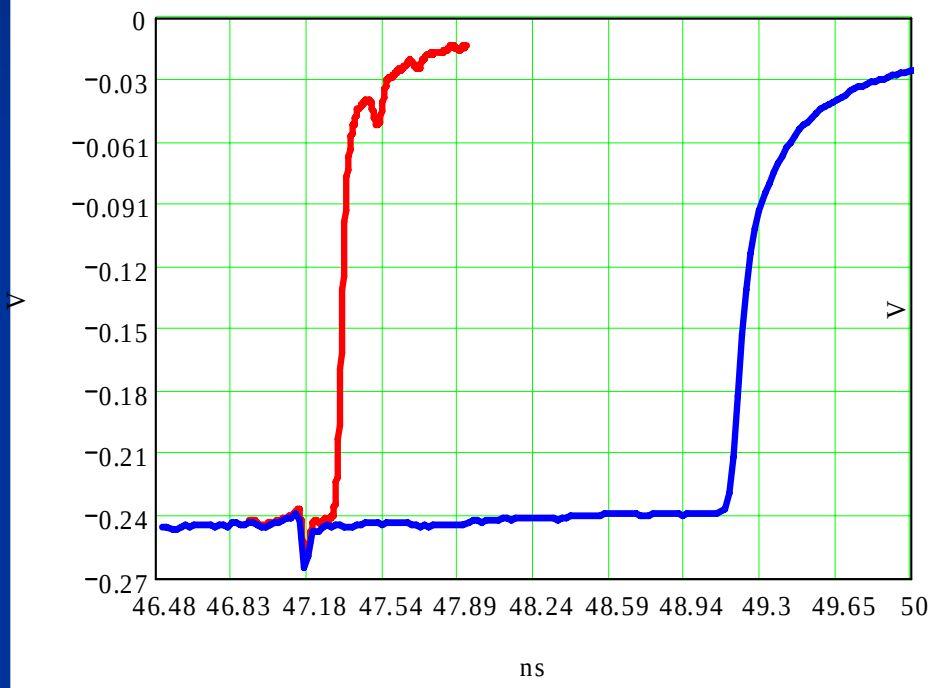


TDT/TDT Test Coupon

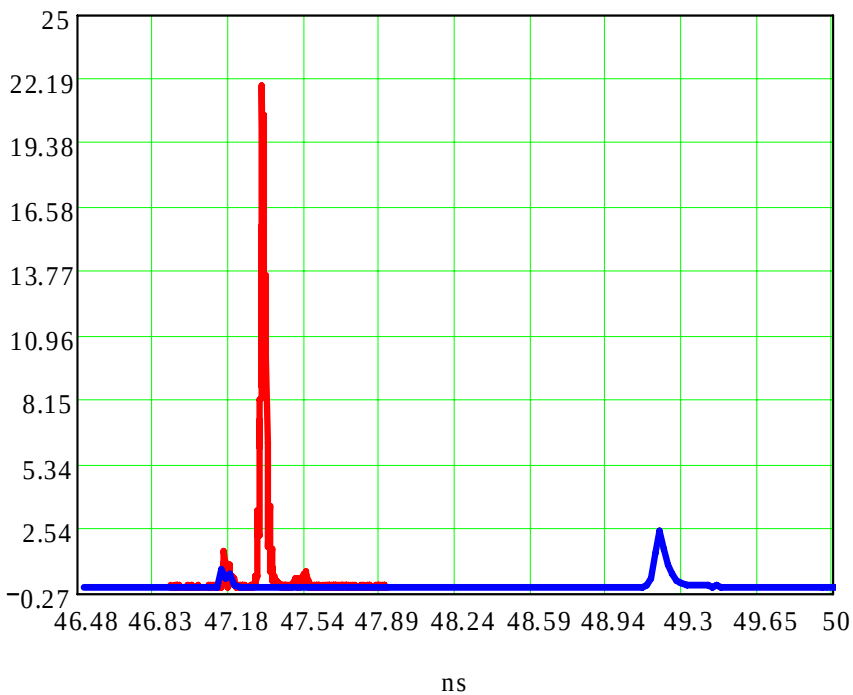


Example Waveform

TDR waveforms



dv/dt^2 of TDR waveforms



Calibration waveforms (1" stripline)

Test line waveforms (12.5" stripline)

Example Calculation

$$RIE_{test\_line} = \sqrt{\int \left(d\frac{V_{tdr\_tdt\_test}(t)}{dt} \right)^2 * dt} = 7.791\text{E}3 \frac{\sqrt{J * ohm}}{\text{sec}}$$

$$RIE_{calibration} = \sqrt{\int \left(d\frac{V_{tdr\_tdt\_cak}(t)}{dt} \right)^2 * dt} = 1.468\text{E}4 \frac{\sqrt{J * ohm}}{\text{sec}}$$

$$RIE_{loss\_dB} = -10 * \log\left(\frac{RIE_{test\_line}}{RIE_{calibration}} \right) = 2.75212 dB$$

Next steps

- Measurements continuing
  - Compare a variety of measurement specimens with VNA results
  - Differential
- Determine impact of vias and launches
- Determine TDR vs TDT impact
- Answer question: Are two measurements really need?
- Draft for review Q4'05

Summary

- RIE is both evolutionary and revolutionary
- RIE can use some existing PWB test equipment
- There is a migration path from controlled impedance testing.
- RIE enables a single value measurement based on electrical needs of the final product… FLEXIBILITY
  - PWB vendors can manage their own material and process without being locked into a requested single supplier
  - PWB vendors can trade off dielectric loss for other trace characteristic's
- RIE can be used to electrically evaluate and test products which employ new materials and processes that supports RoHS.