Benefits and Reliability of a Thin Dielectric in a Power Supply Printed Circuit Board

Valerie A. St. Cyr
Teradyne, Inc.
North Reading, Massachusetts

1.0 Abstract
This paper presents the qualification of a new, very thin, printed circuit board ("PCB") dielectric substrate ("core") to meet Teradyne's performance and reliability design goals for a power supply ("PS") printed circuit board.

The challenges included lower noise margin and higher current carrying capacity. These requirements needed to be met while reducing total product cost and improving system reliability. Newly available copper clad polyimide cores, if they were reliable, could provide a solution to achieving the design goals.

This paper provides details on: A) the design requirements and achievements; B) the core used, a copper-clad 25 micron [0.001"] polyimide film; C) an overview of the performance and reliability testing and results; and D) a quick look ahead at next generation even thinner cores for low inductance and electromagnetic interference ("EMI") reduction.

2.0 Introduction
The application is a power supply board used to distribute power to an instrument board in a large integrated circuit (IC) tester. These are some the design requirements and the resulting achievements:

- Lower supply voltages require lower Power Distribution System ("PDS") impedance. Thinner separations between power and ground reduce impedance and dampen resonances. [1, 2, 6,7]
  - Requirement: DC voltage accuracy < ± 1 mV
    - Achieved: ± .1 mV
  - Requirement: Noise Target < 10 mV point to point
    - Achieved: 0.97 mV
- Higher current requirements: 300 Amps per board, gangable up to 4 boards to power multiple microprocessors running in parallel, each pulling 90 Amps or more, with input voltages of 0.8, 2.0, and 3.0 Volts.
  - Copper foil for planes increased from 1.0 ounce copper/square foot ("oz./sq.ft") to 2.0 oz./sq.ft.
  - More plane layers are required to deliver the power requirements for high current at low voltages and multiple voltage levels; this board was 14 layers while prior PS boards had been 12 layers.
  - The maximum PCB height, surface to surface, is fixed. Reducing the distance between the planes, in the cores, freed up mils of laminate which were reallocated to copper.
- The devices under test have faster clock rates. The PDS must deliver more current faster or there will be voltage droop or fluctuation at the IC.
  - Requirement: Droop < 50 mV at 81A
  - Achieved: 40 mV at up to 486 Amp load
- Mean time to failure requirement ("MTTF", a measure of quality) is increasing.
  - Unreinforced polyimide is not susceptible to Conductive Anodic Filament ("CAF") growth failures, as is the case with glass reinforced epoxy laminates.
  - Polyimide has a higher dielectric breakdown strength, at almost 5 times the voltage/mil; this is an important property for use between closed spaced planes.

3.0 Objective
Our objective was to identify and qualify an alternate, thinner, material, which would in turn provide:

- Lower loop inductance
- Lower impedance to current flow permitting rapid recharging of the planes
- Reduction in EMI (see Figure 1 and Ref. # 2)
- With improved reliability
- At high yields (cost effective)

4.0 Project Overview

The project called for the development of a qualification process and a Test Vehicle; the test plan, including the procedures, the sample sizes, and testing services; the determination of the acceptability requirements; procurement of the Test Vehicles and testing services; compilation and analysis of the data; and pilot introduction of the material into a saleable board.

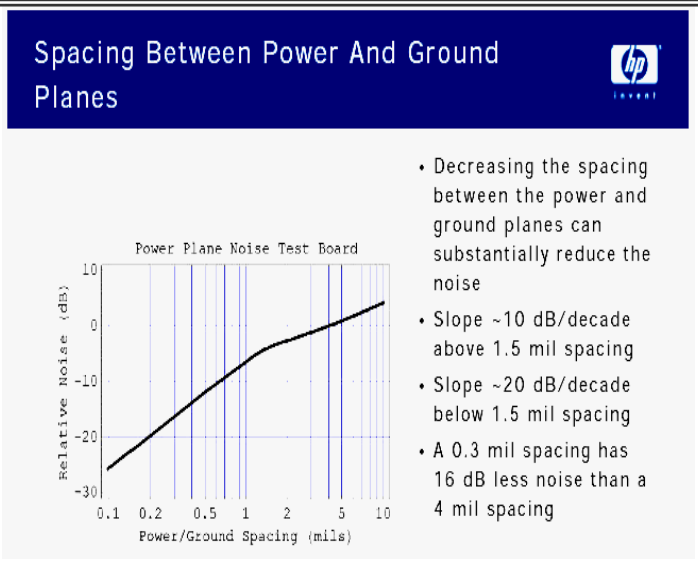


Figure 1 – Noise as a function of spacing – Chart by John Grebenkemper [2]

At the conclusion of testing, the project would be closed after communication to the Teradyne Engineering community; revising the Teradyne "Approved Laminates List" to include the HK 4; and integrating the knowledge gained into Design-for-Manufacturability guidelines and application notes.

4.1 The material

Dupont's "Interra™ HK 4" was selected based on a review of the specifications of the materials available at that time. The HK 4 has 25 micron [0.001"] of polyimide film between the copper foils making it ideal for low impedance at high frequency, power bus decoupling, and electromagnetic interference reduction. [3]

The HK 4 had been released to volume production at DuPont, with their having achieved UL 94V-0 rating. A few of our fabricators had experience with the laminate. It did not require new processes or equipment to implement; it handled easily and yielded as good or better than the core it would replace (a 50 micron [0.002"] fiberglass reinforced epoxy resin).

HK 4 has a high voltage withstanding rating than the glas reinforced epoxy that it would replace, providing better insulation even as the distance between the planes was reduced by half.

DuPont Interra™ HK 4	
Dielectric Thickness	25 micron (0.001")
Capacitance Density	0.8 nF/in^2
Dielectric Constant	3.5 (@ 1 MHz)
Loss Tangent	0.003 (@ 1 MHz)
Dielectric Strength	~6,500 V/mil
Tensile Strength	>50 kpsi
Elastic Modulus	670 kpsi
CTE	25 ppm/°C
Water Absorption	0.8%
Copper Peel Strength	9 pli

Figure 2 – Interra HK 4 Properties

The cost adder per core was moderate. The manufacturing adder varied between $10 to $30 per core (this variability in the fabrication adder is expected to stabilize as more suppliers offer the material).

Figure 2 lists some of the key properties of the HK 4 laminate. Figure 3 is a cross-section showing two of the 25 micron cores.

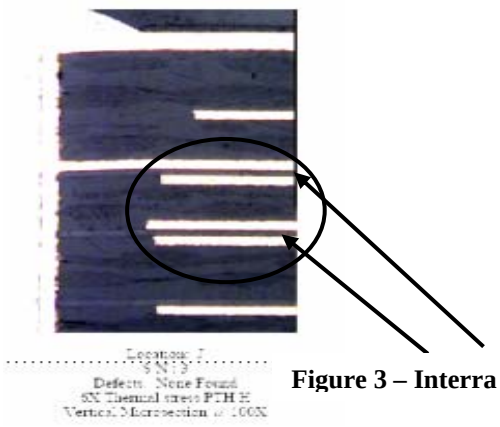


Figure 3 – Interra HK 4

4.2 The Test Vehicles

Two approximately 1.5 mm [0.060"] 14 layer test vehicles were used: a product part number (Figure 4) and a specifically designed evaluation board (Figure 5). The evaluation board emulated the production part's construction and had interconnect stress test coupons, conductive anodic filament testing patterns, dielectric withstanding voltage coupons, and material property coupons for differential scanning calorimetry and thermalmechanical analysis.

The evaluation boards were built 2 ways: one-half with Nelco 4000-13 ZBC for the 4 centermost cores and one-half with Dupont Interra HK 4 cores for the 4 centermost cores. All other elements were identical.

		WITHOUT	WITH	
1	Outer layer	0.0022	0.0022	
	Prepreg	0.003	0.003	
2	Copper	0.0012	0.0012	
	Core	0.004	0.004	
3	Copper	0.0012	0.0012	
	Prepreg	0.0045	0.0045	
4	Copper	0.0012	0.0012	
	Core	0.004	0.001	
5	Copper	0.0012	0.0012	
	Prepreg	0.0045	0.0045	
6	Copper	0.0012	0.0012	
	Core	0.004	0.001	
7	Copper	0.0012	0.0012	
	Prepreg	0.0045	0.0045	
8	Copper	0.0012	0.0012	
	Core	0.004	0.001	
9	Copper	0.0012	0.0012	
	Prepreg	0.0045	0.0045	
10	Copper	0.0012	0.0012	
	Core	0.004	0.001	
11	Copper	0.0012	0.0012	
	Prepreg	0.0045	0.0045	
12	Copper	0.0012	0.0012	
	Core	0.004	0.004	
13	Copper	0.0012	0.0012	
	Prepreg	0.003	0.003	
14	Outer layer	0.0022	0.0022	
		0.0713	**0.0593**	
		Does not fit	Fits	
			-17%	
	Copper	0.0144	0.0144	
	Dielectric	0.0525	0.0405	(- 0.012")

Figure 4 – Product Part Number – 0.001" cores made it possible to add 2 plane layers to stackup and fit in fixed 0.060" height

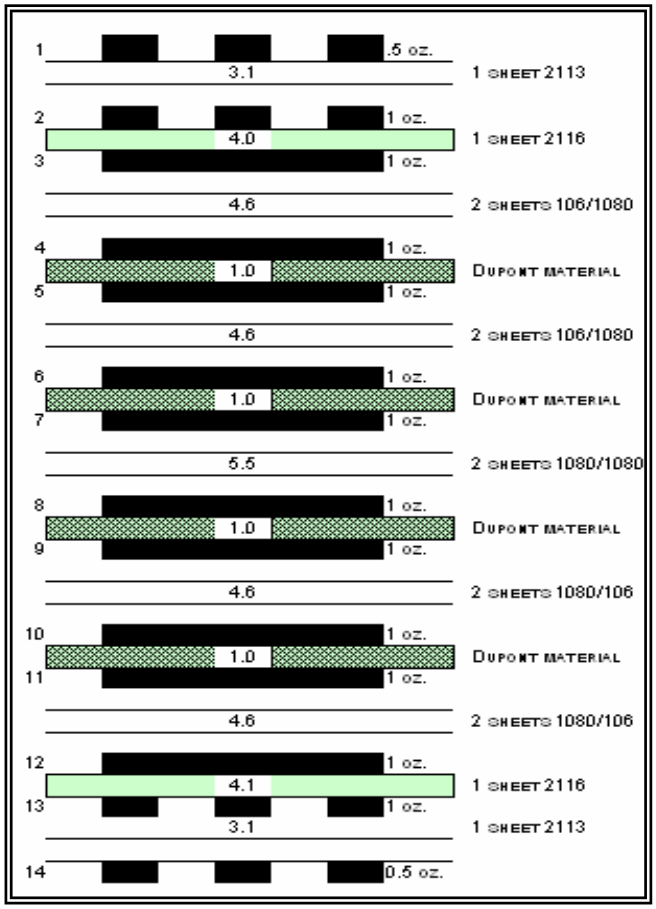


Figure 5 – Evaluation Board – Used for CAF tests and other destructive testing

5.0 The Tests and Results

Figure 6 is a flowchart of the tests used to qualify the Dupont Interra HK 4.

5.1 Conductive Anodic Filament Resistance Test

Conductive Anodic Filament (CAF) formation resistance test, per IPC TM 650 Method 2.6.25, was conducted on the specifically designed evaluation board. CAF is defined by that specification as: "the growth of metallic conductive salt filaments by means of an electrochemical migration process involving the transport of conductive chemistries across a nonmetallic substrate under the influence of an applied electric field, thus producing Conductive Anodic Filaments". The test sets up a voltage bias between isolated elements in the design and then tests for leakage or shorting at 85 ± 2° C [185 ± 3.6° F] Temperature ("T") and 87 +3/-2 % relative humidity ("H"). The test is commonly run to 500 hours under voltage after a 96 hours T & H "soak" and then stopped.

CAF testing was used to determine if Dupont Interra™ HK 4 would show more (or less) propensity to CAF formation than the control group. For this test, half of the evaluation boards had four Dupont Interra cores substituted for four 50 micron [0.002"] Nelco 4000-13 cores, which comprised the control group. Both sets of evaluation coupons were made by the same PCB supplier at the same approximate time (within weeks); the only variable between the sets is the Dupont material.

Eighty coupons were fabricated, 40 of each construction. Fifty-three coupons were sent to Microtek Laboratories in California and 20 were retained by Merix, the fabricator. Each lab (Microtek and Merix) divided the samples testing ½ of each construction at 10V and ½ at 100VDC. At a constant test voltage the Dupont core is subjected to twice the stress per mil of material since The Nelco cores are twice as thick as the Dupont cores. The 7 untested coupons were failed for shorts at electrical test and so not submitted for CAF testing; the shorts were not related to the material but rather to drill deflection.

There were no CAF failures in either the Dupont or the Nelco 4000-13 cores, through the plane, in the z-axis or in-plane, across plane splits. See Appendix, Section 11, for detail on CAF coupons and test results.

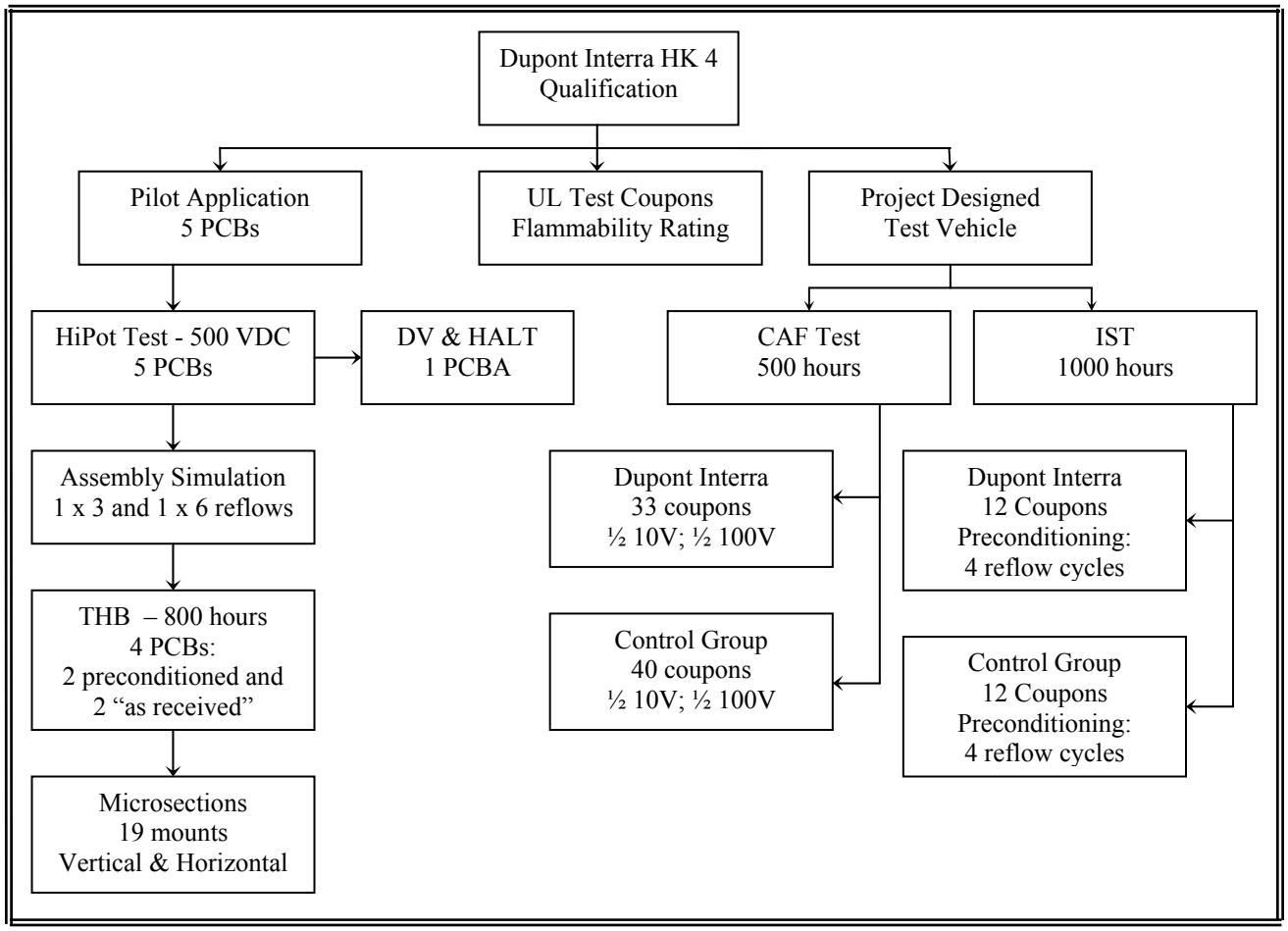


Figure 6 – Qualification Plan

5.2 Underwriters' Laboratories (UL) Certification
Samples as required by UL for flammability, bond strength, and temperature cycle testing were submitted, combining Interra HK 4 with Nelco 4000-13, and also 2 different versions of epoxy FR4 resin. All samples passed UL94 to flame class "V-0", with a 130 °C Maximum Operating Temperature (a common value for this test) and a solder limit temperature of 288 °C.

5.3 Design Verification (DV) and Highly Accelerated Life Testing (HALT)
The DV and HALT testing was performed on the fully assembled product part number. The boards passed all electrical noise testing. In addition, there were no failures to the board portion of the assembly during the thermal and vibration cycling that was performed on an operating and loaded board. [4]

5.4 Temperature, Humidity and Bias (THB)
THB was run for 17 days (> 400 hours), at 85° C / 85 RH / 5VDC. Two boards were tested "as received" from the fabricator; two boards were tested after preconditioning: 1 board saw 3 reflow passes, and 1 board was subjected to 6 reflows, at 215 °C. There was no leakage on any of the boards.

5.5 Dielectric Withstanding Voltage
Five boards were subjected to the Dielectric Withstand Voltage test (IPC TM 650 Method 2.5.7 {a.k.a.: HiPot}) @ 500V for 30 seconds. This test consists of "the application of a voltage higher than the rated voltage for a specific time between mutually isolated portions of a PWB or between isolated portions and ground. This test is used to prove that the PWB can operate safely at its rated voltage and withstand momentary over potentials due to switching, surges and other similar phenomena." There was no shorting between the planes or across plane splits.

5.6 Interconnect Stress Test ("IST")
Two hole diameters were tested by IST: 0.84 mm [0.033"] and 0.30 mm [0.012"]. The IST coupons were preconditioned with 4 passes through IR reflow at a peak temperature of 215 °C. IR was selected for preconditioning because, unlike wave soldering, no solder remains in the holes; past testing had shown that solder in the holes can artificialy extended the cycles to failure masking the true onset of failure.

Maximum Number of IST Cycles	1,000
Maximum Test Temperature	150 °C
Data Capture Every # Cycles	25
% Resistance Increase for Fail, Sense mode	13
% Resistance Increase for Fail, Power mode	13
Precycle Window (seconds)	3
Current Compensation Method	Calculated

Figure 7 – IST Parameters [5]

Initial resistance readings were taken on all of the coupons, confirming that the plated copper thickness in the holes in the different coupons was essentially equivalent, which meant that the results would not be skewed by higher or lower copper wall thickness. The coupons then proceeeded to IST for cycling to 1,000 hours or failure, whichever occurred first. The test conditions are listed in Figure 7.

The control group, which was the all-Nelco 4000-13 construction, passed IST with all coupons achieving 1,000 cycles. The resistance readings for this material (see Appendix, Section 12, for data from IST) showed no preferential weakness for either Post or PTH failures, where Post would indicate an opening developed between the innerplane layer and the barrel of the hole, and PTH would indicate a fractured hole wall. The mean percentance Post resistance increase for the larger holes was 1.5 % while the PTH increase was 1.9 %; for the smaller holes the increases were 0.6 % and 0.7 %, respectively.

The evaluation group, which had the Dupont Interra in the 4 central cores surrounded by Nelco 4000-13 prepregs and sandwiched between two 0.10 mm [0.004"] 4000-13 cores, had some failures before 1,000 cycles. Those failures, on both the larger and smaller diameter holes, followed a typical wearout pattern and were not infant mortality anomalies. [5] Post resistance increase was more prevalent in the larger diameters, while PTH resistance increase was more prevalent in the smaller diameters. These results are consistent with prior testing, and the expectations of failure mode by hole diameter. Where Post resistance was the failure mode, the mean resistance increase was 10 % with a 5.1 % standard deviation. Where PTH resistance was the dominant failure mode, the mean resistance increase was 10.2 % with a 4.1 % standard deviation. [5]

Companies that require 20 year reliability typically specify a minimum of 300 IST cycles after multiple exposures to elevated temperatures above the material glass transition temperature. [5]

Failure anlaysis found that the 0.84 mm holes failed at the innerplane to barrel interconnect due to smear, and the 0.30 mm holes' failures were barrel cracks which originated from the glass fibers and/or the HK 4 material. [5]

5.7 Solder Float Test
Multiple microsections were taken and tested by solder float per IPC TM 650 Method 2.6.8. This test is designed to determine the thermal integrity of laminates using exposure to solder. We thermally stressed the samples from 1 board by floating 3 times in 288 °C [550 °F] solder, and the samples from another board by floating 6 times in 288 °C solder; we then extracted vertical microsections on 70 mm [0.028"], 1.15 mm [0.045"], and 25 mm [0.010"] holes; 6 sections from each board were examined. There were no faults found which were attributable to the HK 4.

5.8 Microsection Analysis
Microsection PTH Quality Evaluation to IPC 6012 B: Qualification and Performance Specification for Rigid Printed Boards was performed. Two boards, one "as received" from the supplier and one preconditioned with 6 reflow passes, were microsectioned in the vertical orientation at 0.25 mm [0.010"], 0.40 mm [0.016"], 0.70 mm [0.028"], 0.85 mm [0.033"], 1.15 mm [0.045"], and 3.10 mm [0.122"] holes; holes at corners were selected; holes in tight groups and isolated holes were selected. In all, 11 vertical sections were taken on each board sampling the smallest to the largest PTHs without any defects found.

A separate board was subjected to 3 IR reflows, then horizontal grinds were done on the 0.40 mm [0.016"] and 3.10 mm [0.122"] PTHs to a signal layer and to a Dupont plane layer without any defects found: no residues; no delamination – there was good adhesion between the HK 4 and the epoxy prepreg.

6.0 DFM Guidelines and Application Notes

HK 4, having passed all the required testing, was placed on Teradyne's Approved Laminates List and the following notes and guidelines were added to Teradyne's DFM Guidelines for PCBs, along with the key properties (Figure 2):

- When to use
  - Need to reduce overall thickness to meet mechanical constraints
  - Need to reduce via inductance
  - Need to reduce plane impedance
- Cores Only
  - Not available as a prepreg
- Plane Cores Only
  - Do not use for signal-over-signal or signal-over-plane
- Copper Cladding
  - 1.0 oz/sq.ft or 2.0 oz/sq.ft both sides
    - Do not use 0.5 oz/sq.ft.
    - Do not use 1.0 oz. on one side and 2.0 oz/sq. foot on the other
- UL 94V-0
  - Verify that the fabricator has 94V-0 rating for a mixed construction of Dupont Interra combined with the other material specified in the construction drawing

These usage guidelines were developed with Teradyne's product in mind, other company's will likely vary somewhat.

7.0 Future Work

There are now more choices in even thinner insulation materials which have the potential to extend the improvements in performance for both high power and high frequency applications. These materials, as they become stable and available for volume use, will be tested to determine if they can contribute to Teradyne's power, speed and density driven requirements. Data gleaned from papers presented in this field show further reductions in impedance to current flow, loop inductance, and EMI with thinner dielectrics (See: Figure 8 and Ref # 6 & 7).

Already under way is an engineering prototype board which was fabricated with 2 cores of Oak-Mitsui Technologies' "FaradFlex BC12" (Figure 9) which is a ½ mil blended epoxy non-reinforced dielectric. The "thickness" of the insulation is less than half that of the copper foils to either side! It is too early to report anything on this experiment.

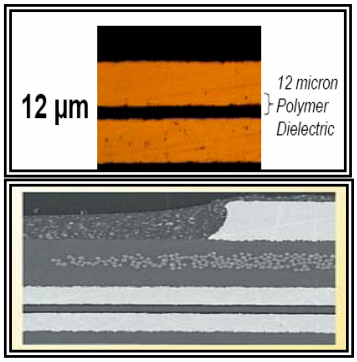


Figure 9 – FaradFlex BC12 with reverse treat foil and 12 mm dielectric thickness
(photos taken from FaradFlex brochure and Ref. # 6)

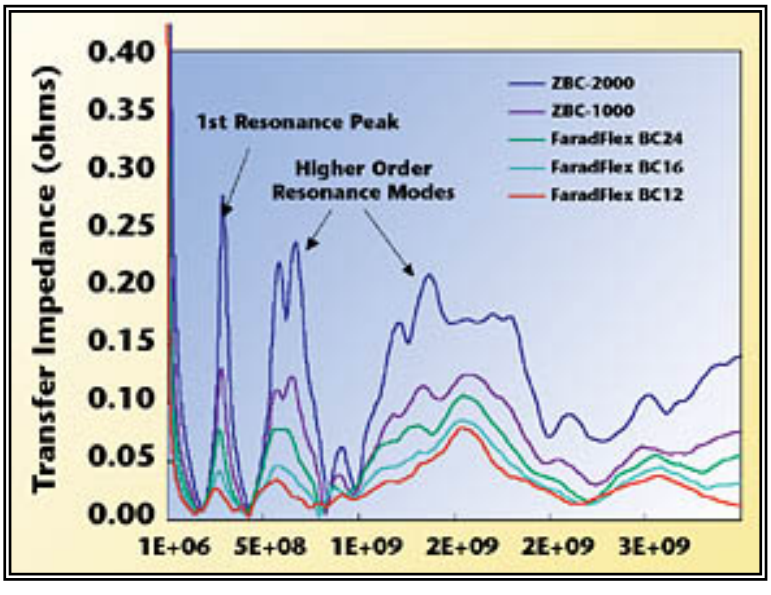


Figure 8 – Reduction in Impedance At Frequency as a Function of Dielectric Thickness [6]

8.0 Conclusions

Testing has confirmed that 0.001" unrienforced , copper-clad, polyimide provides benefits to power supply PCB packaging. "The most positive effect on the design was that the increased dielectric strength allowed me to place supply and return voltages of up to 48V nominal on adjacent layers. The reduced loop areas in the power distribution path helped control noise emitted by the power supply."[4]

Studies to date have shown that thinner separations between power and ground layers do significantly reduce plane resonances, PDS impedance, and loop inductance. "As the spacing between the copper planes decreases (thinner dielectrics) the self and mutual inductance to currents on the planes decreases and an overall reduction of the high frequency impedance is achieved. The overall impedance reduction can be directly converted into a decrease in power distribution voltage noise and reduced EMI in the higher frequency bands from several hundred megahertz up to several gigahertz." [6]

9.0 Acknowledgements

David Seiffert and Tom Emmons of Teradyne, Engineers and designers of the first power supplies in Teradyne to use Dupont Interra HK4, for their collaboration and the knowledge they shared.

Tom Lantzer and Sidney Cox of Dupont Microcircuit Materials, for material samples, their internal testing, and guidance towards the success of this project.

And especially Randy Reed of Merix for design of the CAF coupon and for the IST work. Also Bob Greenlee and the other Merix engineers who took on the task to develop the processes for Dupont Interra within a short time to support this program.

10.0 References

[1] Embedded Devices Subcommittee D-51, "IPC-2316 Design Guide for Embedded Passive Device Printed Boards, Draft"; August 8, 2005

[2] John Grebenkemper, Ph.D., "Thin Laminates and Power Plane Noise", DesignCon 2004, Tech Forum 9: "Thin and Very Thin Laminates for Power Distribution", January 2004

[3] DuPont Electronic Technologies, "Interra HK 4 Series of Embedded Planar Capacitor Laminates, Design Guidelines", November 5, 2003

[4] David Seifert, Teradyne internal memo: "DV and HALT results"; January 28, 2004

[5] Randy Reed, Merix, Report to Teradyne, "IST Results: HK 4 Qualification", 2005

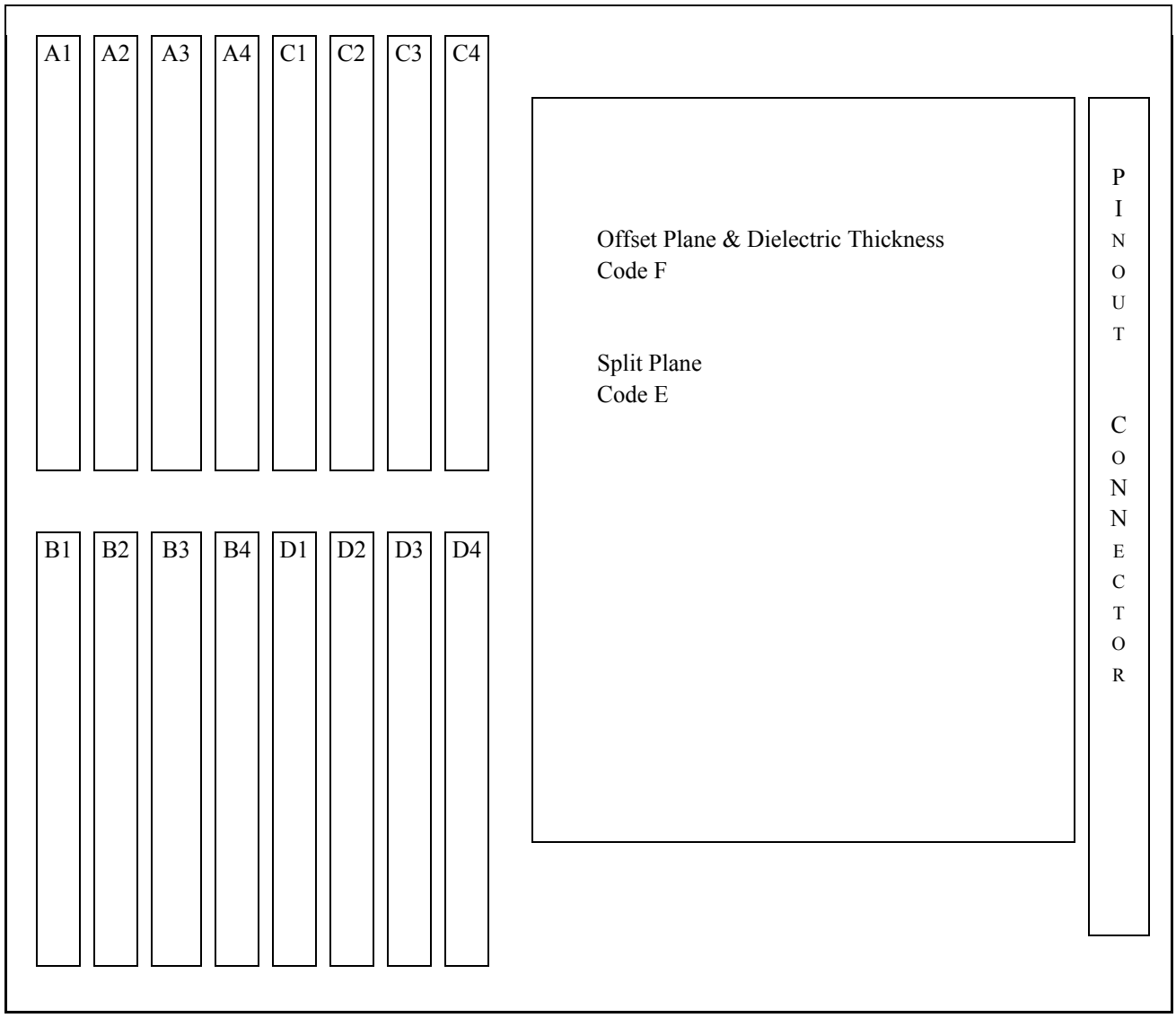
[6] Nicholas Biunno, Ph.D., and Greg Schroeder, "Buried Capacitance™ and Thin Laminates"; CircuiTree, March, 2004

[7] Istvan Novak, Ph.D., "Frequency Dependent Capacitance and Inductance of Thin and Very Thin Laminates", DesignCon 2004, Tech Forum 9: "Thin and Very Thin Laminates for Power Distribution"; January 2004

Appendix

11.0 CAF

11.1 CAF Coupon



— NOT TO SCALE —

11.2 Coupon Design - Mixed construction (Experimental group):
Nelco 4000-13: two .004" cores and prepregs (1080/106 per fill); Dupont Interra HK4: four .001" cores
14 layer .058" nominal thickness

Test feature "A": PTH-to-PTH inline
28 vias (4x7 array) drill .0135" x 4 patterns (112) holes
x 11 coupons (1232 vias) at 10V: spacings via edge to via edge provide 0.7 - 3.3 V/mil gradient conditions
x 12 coupons (1344 vias) at 100V: spacings via edge to via edge provide 5.5 - 33.3 V/mil gradient conditions

Test feature "B": PTH-to-PTH staggered
28 vias (4x7 array) drill .0135" x 4 patterns (112) holes
x 11 coupons (1232 vias) at 10V: spacings via edge to via edge provide 0.5 - 1.7 V/mil gradient conditions
x 12 coupons (1344 vias) at 100V: spacings via edge to via edge provide 5.5 - 16.8 V/mil gradient conditions

Test feature "C": PTH-to-Plane (in plane; x and y axes) with antipads only
14 vias (2x7 array) drill .0135" x 4 patterns (56) holes
x 11 coupons (616 vias) at 10V: spacings via edge to antipad edge provide 0.8 - 1.7 V/mil gradient conditions
x 12 coupons (672 vias) at 100V: spacings via edge to antipad edge provide 8.3 - 16.7 V/mil gradient conditions

Test feature "C": PTH-to-Plane (in plane x and y) with capture pads inside antipads
14 vias (2x7 array) drill .0135" x 4 patterns (56) holes
x 11 coupons (616 vias) at 10V: spacings via edge to antipad edge provide 1.0 - 2.9 V/mil gradient conditions
x 12 coupons (672 vias) at 100V: spacings via edge to antipad edge provide 10.2 - 28.6 V/mil gradient conditions

Test feature "D": NPTH-to-Plane (z axis)
14 vias (4x3.5 array) drill .0135" x 4 patterns (56 holes)
x 11 coupons (616 vias) at 10V: spacings via edge to antipad edge provide 0.4 - 1.0 V/mil gradient conditions
x 12 coupons (672 vias) at 100V: spacings via edge to antipad edge provide 4.0 - 10 V/mil gradient conditions

Test feature "E": Plane splits (in plane x and y)
20 plane segments, 5 segments per quadrant; each quadrant at 90 degrees to the preceding;
4 segments tested to 3" segment of plane at 90 degrees, from 5 to 50 mils of separation
3" x 4 quadrants x 4 "E" planes per coupon (48 linear inches)
x 11 coupons (528 ") at 10V: plane splits provide up to 0.2V/mil gradient condition
x 12 coupons (576 ") at 100V: plane splits provide 2.0 - 20V/mil gradient conditions

Test feature "F": Plane-to-plane dielectric separation (z axis)
Approximately 17 square inches of solid plane-over-plane separation x 1 core
x 11 coupons (187 sq.in.) at 10V: separation plane-to-plane provides 5.0V/mil gradient condition
x 12 coupons (204 sq.in.) at 100V: separation plane-to-plane provides 50V/mil gradient condition

Total test population:

- 7,728 PTH vias
- 1,288 non-PTH vias
- 1,104 linear inches of parallel copper (in-plane)
- 391 square inches of parallel copper (plane-to-plane)

11.2.1 Coupon Design - Uniform construction (Control group):
Nelco 4000-13: two .004" cores; four .002" cores; and prepregs (1080/106 per fill)
14 layer .062" nominal thickness

Test feature "A": PTH-to-PTH inline
28 vias (4x7 array) drill .0135" x 4 patterns (112) holes
x 15 coupons (1680 vias) at 10V: spacings via edge to via edge provide 0.7 - 3.3 V/mil gradient conditions
x 15 coupons (1680 vias) at 100V: spacings via edge to via edge provide 5.5 - 33.3 V/mil gradient conditions

Test feature "B": PTH-to-PTH staggered
28 vias (4x7 array) drill .0135" x 4 patterns (112) holes
x 15 coupons (1680 vias) at 10V: spacings via edge to via edge provide 0.5 - 1.7 V/mil gradient conditions

x 15 coupons (1680 vias) at 100V spacings via edge to via edge provide 5.5 - 16.8 V/mil gradient conditions

Test feature "C": PTH-to-Plane (in plane; x and y axes) with antipads only
14 vias (2x7 array) drill .0135" x 4 patterns (56) holes
x 15 coupons (840 vias) at 10V spacings via edge to antipad edge provide 0.8 - 1.7 V/mil gradient conditions
x 15 coupons (840 vias) at 100V: spacings via edge to antipad edge provide 8.3 - 16.7 V/mil gradient conditions

Test feature "C": PTH-to-Plane (in plane x and y) with capture pads inside antipads
14 vias (2x7 array) drill .0135" x 4 patterns (56) holes
x 15 coupons (840 vias) at 10V: spacings via edge to antipad edge provide 1.0 - 2.9 V/mil gradient conditions
x 15 coupons (840 vias) at 100V spacings via edge to antipad edge provide 10.2 - 28.6 V/mil gradient conditions

Test feature "D": NPTH-to-Plane (z axis)
14 vias (4x3.5 array) drill .0135" x 4 patterns (56 holes)
x 15 coupons (840 vias) at 10V: spacings via edge to antipad edge provide 0.4 - 1.0 V/mil gradient conditions
x 15 coupons (840 vias)at 100V: spacings via edge to antipad edge provide 4.0 - 10 V/mil gradient conditions

Test feature "E": Plane splits (in plane x and y)
20 plane segments, 5 segments per quadrant; each quadrant at 90 degrees to the preceding;
4 segments tested to 3" segment of plane at 90 degrees, from 5 to 50 mils of separation
3" x 4 quadrants x 4 "E" planes per coupon (48 linear inches)
x 15 coupons (720 inches) at 10V: plane splits provide up to 0.2V/mil gradient condition
x 15 coupons (720 inches) at 100V: plane splits provide 2.0 - 20V/mil gradient conditions

Test feature "F": Plane-to-plane dielectric separation (z axis)
Approximately 17 square inches of solid plane-over-plane separation x 1 core
x 15 coupons (255 sq.in.) at 10V: separation plane-to-plane provides 10.0V/mil gradient condition
x 15 coupons (255 sq.in.) at 100V: separation plane-to-plane provides 100V/mil gradient condition

11.3 Total test population

- 10,080 PTH vias
- 1,680 non-PTH vias
- 1,440 linear inches of parallel copper (in-plane)
- 510 square inches of parallel copper (plane-to-plane)

11.4 Results

In the aggregate there was no appreciable difference between the all-Nelco construction and the mixed-Nelco-Dupont construction. All samples passed CAF testing in the vertical axis; there were no failures between planes on in-plane.

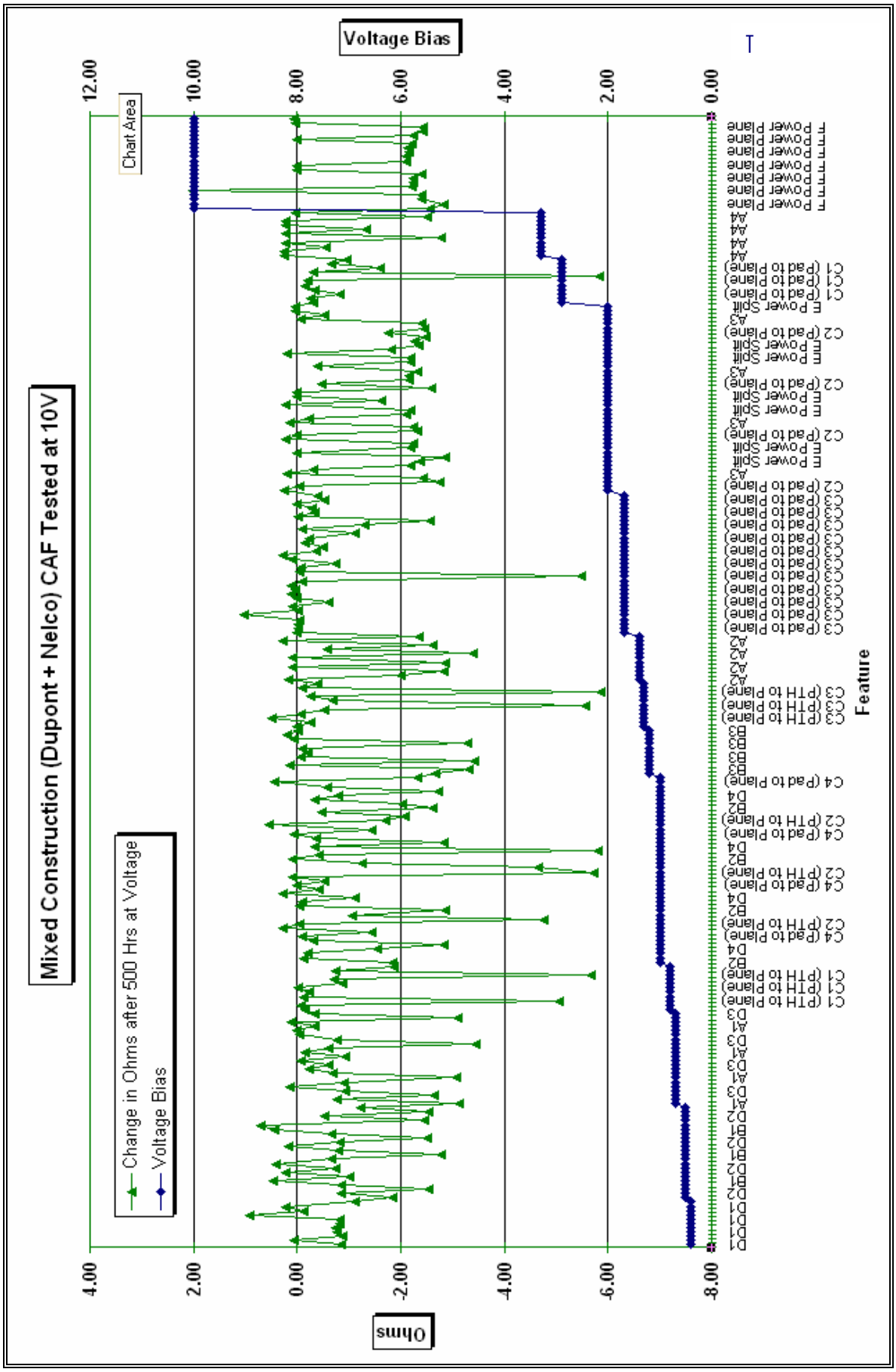
There does seem to be more variation for PTH circuits than planes or plane segments. All the "min" readings reflect failed nets, which bottom out at approximately 6.0 ohms; so any failure in a group of nets, makes the "min" of all nets equal to 6.0, and not a useful number to determine range values.

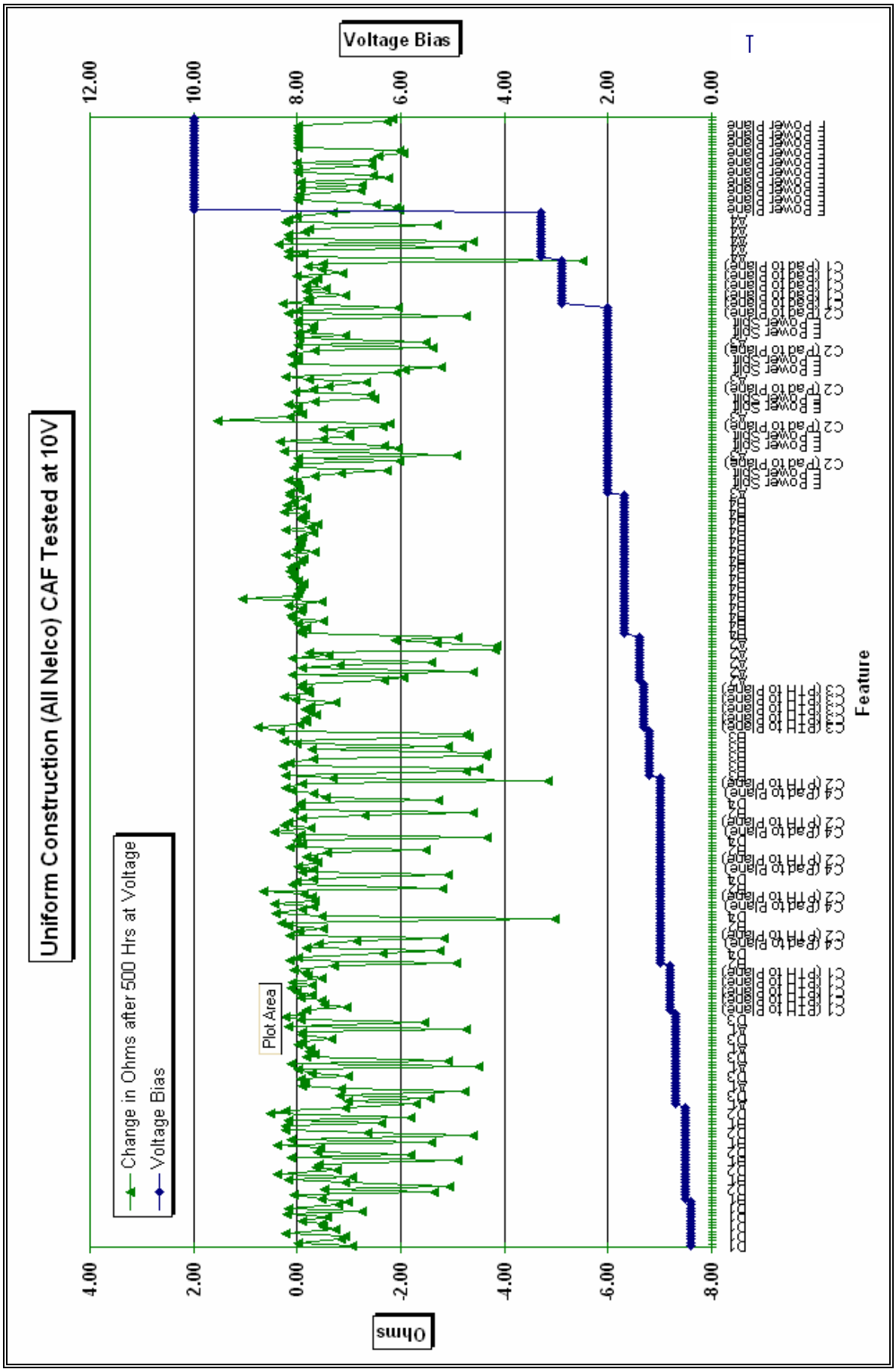
A search of reported CAF tests indicates that our results mimic others' with the PTH circuit at about 13 ohms initially, then dropping by 3 ohms on average.

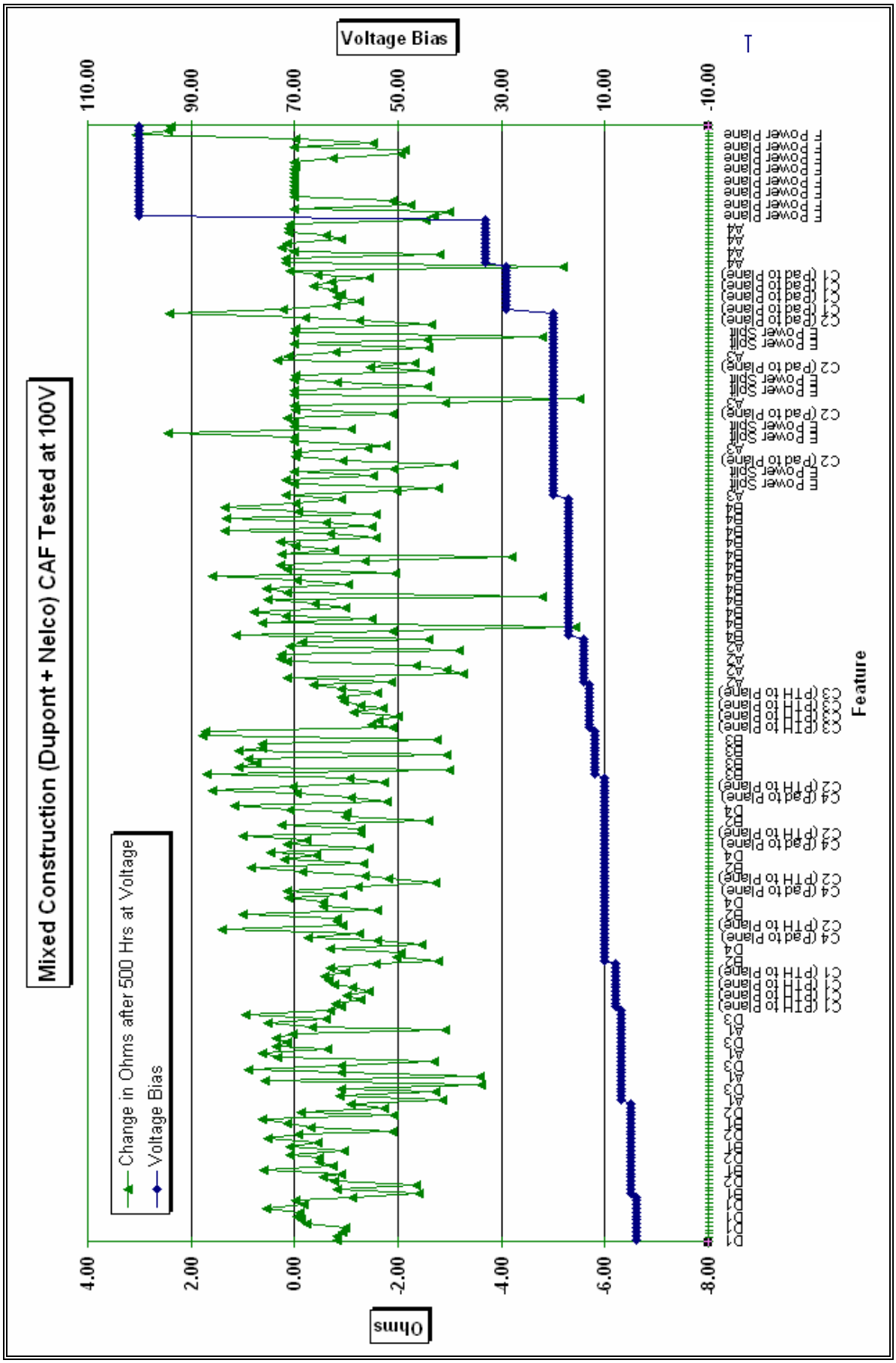
There was no trend discernable between voltage bias and resistance change.

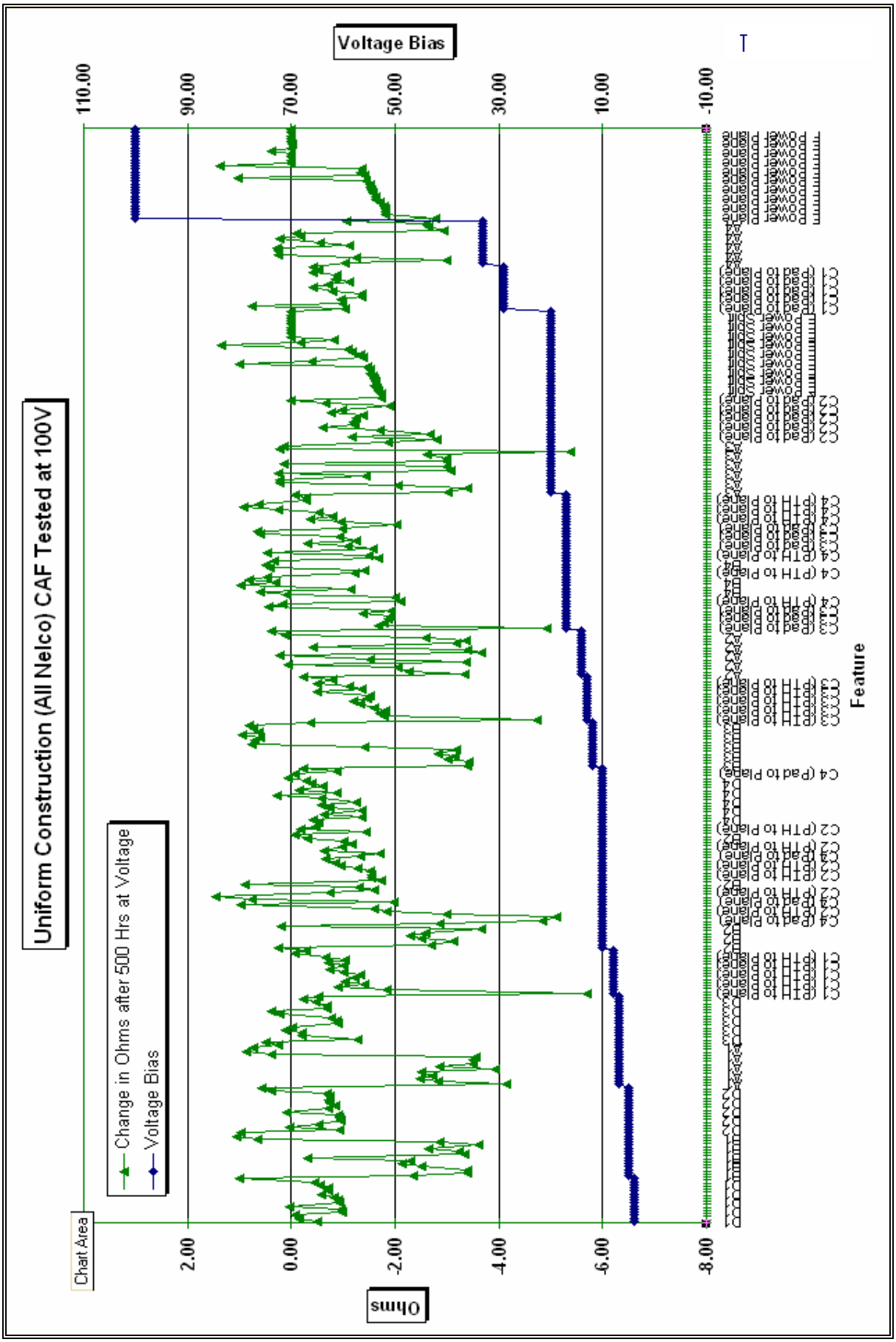
11.5 Plane to Plane and In-Plane (across a split)							Values in Log Ohms	
	Initial Ohms	96 Hours Ohms	168 Hours Ohms	336 Hours Ohms	500 Hours Ohms	596 Hours Ohms	Chg from Initial Ohms to 596 Hrs. Ohms	Chg from 96 Hours Ohms to 596 Hrs Ohms
Mixed Construction (Dupont & Nelco) all Voltages								
Min	10.78	9.03	10.63	10.49	9.71	10.32	-0.46	+1.29
Max	13.30	13.37	13.37	13.37	13.30	13.38	+0.08	+0.01
Avg	11.23	13.00	13.04	11.73	11.83	12.00	+0.77	-1.00
Uniform Construction (all Nelco) at all Voltages								
Min	11.92	10.06	11.04	11.07	10.44	10.49	-1.43	+0.43
Max	13.31	13.38	13.37	13.37	13.37	13.37	+0.06	-0.01
Avg	12.87	13.20	13.08	12.99	12.33	12.36	-0.51	-0.84

11.5.1 PTH Wall to PTH Wall							Values in Log Ohms	
	Initial Ohms	96 Hours Ohms	168 Hours Ohms	336 Hours Ohms	500 Hours Ohms	596 Hours Ohms	Chg from Initial Ohms to 596 Hrs. Ohms	Chg from 96 Hours Ohms to 596 Hrs Ohms
Mixed Construction (Dupont & Nelco) at 10V								
Min	10.81	6.00	6.02	6.02	6.02	6.02	- 4.79	+ 0.02
Max	13.29	13.37	13.37	13.37	13.30	13.32	+ 0.03	- 0.05
Avg	12.72	11.20	10.62	10.26	10.12	10.12	- 2.60	- 1.08
Uniform Construction (all Nelco) at 10V								
Min	10.80	6.00	6.12	6.01	6.15	6.15	- 4.65	+ 0.15
Max	13.35	13.38	13.37	13.37	13.29	13.29	- 0.06	- 0.09
Avg	13.02	11.51	11.13	10.99	10.84	10.84	- 2.18	- 0.67
Mixed Construction (Dupont & Nelco) at 100V								
Min	8.37	5.99	6.20	6.12	6.07	6.07	- 2.03	+ 0.08
Max	13.30	13.37	13.37	13.37	13.30	13.38	+ 0.08	+ 0.01
Avg	12.62	11.13	10.63	10.43	10.29	10.40	- 2.22	- 0.73
Uniform Construction (all Nelco) at 100V								
Min	5.97	5.97	6.15	6.10	6.11	5.99	+ 0.02	+ 0.02
Max	13.31	13.37	13.32	13.37	13.37	13.37	+ 0.06	0
Avg	13.04	11.41	11.08	10.88	10.45	10.35	- 2.69	- 1.06


Mixed Construction (Dupont + Nelco) CAF Tested at 10V
Voltage Bias
Chart Area
Change in Ohms after 500 Hrs at Voltage
Voltage Bias
Ohms
Feature
12.00
10.00
8.00
6.00
4.00
2.00
0.00
4.00
2.00
0.00
-2.00
-4.00
-6.00
-8.00


Uniform Construction (All Nelco) CAF Tested at 10V
Change in Ohms after 500 Hrs at Voltage
Voltage Bias
Plot Area
Voltage Bias
Ohms
Feature
12.00
10.00
8.00
6.00
4.00
2.00
0.00
4.00
2.00
0.00
-2.00
-4.00
-6.00
-8.00


Mixed Construction (Dupont + Nelco) CAF Tested at 100V
Change in Ohms after 500 Hrs at Voltage
Voltage Bias
Voltage Bias
Ohms
Feature
110.00
90.00
70.00
50.00
30.00
10.00
-10.00
4.00
2.00
0.00
-2.00
-4.00
-6.00
-8.00


Uniform Construction (All Nelco) CAF Tested at 100V
Change in Ohms after 500 Hrs at Voltage
Voltage Bias
Chart Area
Voltage Bias
110.00
90.00
70.00
50.00
30.00
10.00
-10.00
2.00
0.00
-2.00
-4.00
-6.00
-8.00
Ohms
Feature

12.0 IST Results
Report by Randy Reed, Merix

Nelco 4000-13 ZBC™ Material Construction (Control Group)
Drilled Hole Diameter: 0.84 mm [0.033"]

Test Condition	Coupon ID	Post Cycles	Post %	PTH Cycles	PTH %	Failure Mode
4X IR Reflow	6337	1000	1.7	1000	1.8	No Failure
4X IR Reflow	8337	1000	1.1	1000	0.2	No Failure
4X IR Reflow	10337	1000	2.2	1000	0.5	No Failure
4X IR Reflow	12337	1000	0.7	1000	2.9	No Failure
4X IR Reflow	14337	1000	0.9	1000	2.5	No Failure
4X IR Reflow	4337	1000	2.3	1000	3.7	No Failure
Mean		**1000**	**1.5**	**1000**	**1.9**	
StDev		---	0.7	---	1.4	
Min		1000	.7	1000	0.2	
Max		1000	2.3	1000	3.7	
Range		0	1.6	0	3.5	

Nelco 4000-13 ZBC™ Material Construction (Control Group)
Drilled Hole Diameter: 0.30 mm [0.012"]

Test Condition	Coupon ID	Post Cycles	Post %	PTH Cycles	PTH %	Failure Mode
4X IR Reflow	21127	1000	NA	1000	NA	No Failure
4X IR Reflow	19127	1000	NA	1000	0.8	No Failure
4X IR Reflow	23127	1000	NA	1000	NA	No Failure
4X IR Reflow	17127	1000	0.6	1000	1.2	No Failure
4X IR Reflow	25127	1000	NA	1000	0.2	No Failure
4X IR Reflow	27127	1000	NA	1000	NA	No Failure
Mean		**1000**	**0.6**	**1000**	**0.7**	
StDev		---	0	---	0.5	
Min		1000	NA	1000	1.2	
Max		1000	0.6	1000	0.2	
Range		0	0.6	0	1.0	

Dupont Interra HK4 Material Construction
Drilled Hole Diameter: 0.84 mm [0.033"]

Test Condition	Coupon ID	Post Cycles	Post %	PTH Cycles	PTH %	Failure Mode
4X IR Reflow	6332	650	13.4	---	7.8	Post / Hot
4X IR Reflow	8332	1000	6.2	1000	4.6	No Failure
4X IR Reflow	10332	1000	5.0	1000	4.0	No Failure
4X IR Reflow	12332	1000	5.1	1000	3.7	No Failure
4X IR Reflow	4332	590	14.6	---	3.9	Post / Hot
4X IR Reflow	14332	431	15.7	---	3.3	Post / Hot
Mean		**778.5**	**10.0**	**1000**	**4.65**	
StDev		253	5.1	0.0	1.6	
Min		431	5.0	1000	3.7	
Max		1000	15.7	1000	7.8	
Range		569	10.7	0	74.3	

Dupont Interra HK4 Material Construction
Drilled Hole Diameter: 0.30 mm [0.012"]

Test Condition	Coupon ID	Post Cycles	Post %	PTH Cycles	PTH %	Failure Mode
4X IR Reflow	19122	---	0.1	775	7.8	Sense / Hot
4X IR Reflow	17122	---	0.3	930	13.0	Sense / Hot
4X IR Reflow	21122	---	NA	801	4.0	Sense / Hot
4X IR Reflow	23122	---	NA	574	13.1	Sense / Hot
4X IR Reflow	27122	---	1.1	996	13.0	Sense / Hot
Mean		**---**	**0.5**	**815.2**	**10.2**	
StDev		---	2.3	162.7	4.1	
Min		---	.1	574	4	
Max		---	1.1	996	13.1	
Range		---	1.0	422	9.1	