# Lessons Learned: Case Studies of Embedded Passives Implementations in Mobile Phones

Robert Croswell, John Savic and Aroon Tungare
Motorola Labs
Schaumburg, IL

**Abstract**
Over the past six years Motorola has shipped over 47 million phones incorporating Embedded Passives (EP) technology. The EP modules shipped in phones have included small modules such as voltage controlled oscillators as well as large modules comprising full phone functionality. Driving the creation of a supply chain—from materials supplier through board fabricator—was also required in order to execute the transformation of embedded passives from R&D curiosity to reality in products. Every implementation of EP has maintained system cost parity or reduced system cost while benefiting from size and routing complexity reduction. This paper briefly reviews the commercialized portfolio of embedded resistor, capacitor, and inductor technologies, and uses several case studies to highlight the lessons learned.

**Introduction**
Since 1999, Motorola has designed, fabricated and shipped in excess of 47 million products incorporating Embedded Passives (EP), which has been recognized as an effective means of providing size and cost reduction for a variety of the company's handheld products. Surface area in a cell phone PWB is at a premium in most designs, therefore moving a part from the surface into the inner-layer by using embedded passives is a distinct advantage. Additionally, removal of solder joints through embedding components is considered to be a distinct reliability and environmentally friendly improvement. Conventional wisdom in the electronics industry has assumed that embedded passives are useful only in limited applications, *e.g.*, power-ground decoupling capacitance planes, pull-up & pull-down resistors in baseband sections, or RF choke inductors in radio sections. However, with proper design choices, EP components can also be effectively used in critical RF applications.

The EP technology portfolio consists of screen printed Polymer Thick Film (PTF) resistors, parallel plate capacitors and simple print and etch multi- & single-layer inductors embedded in the inner-layers of High Density Interconnect (HDI) PWBs . Although the core technology has been extensively utilized over the last 6 years, work continues to build on the leading position in EP by investing in new processes, methods and materials that further enhance the manufacturability and usefulness of the technology. This paper will touch upon some of the latest developments regarding PTF resistors, Embedded Mezzanine Capacitor (EMC) technology and illustrate some of the more advanced products recently manufactured with these technologies. Finally, some of the simple lessons learned through the process or repeated design and fabrication of EP products will be shared.

**Embedded Passive (EP) Technology**
***Embedded Resistor Technology***
Among embedded passives technologies, resistors offer the greatest part count reduction and cost savings for most products. Whereas currently available embedded capacitor and inductor technologies are limited to the lower value ranges (< 300 pF and < 10 nH), embedded PTF resistors can cover the full range of resistor values, from ohms to mega-ohms.

Screen printing of PTF pastes has existed in the PWB industry for a very long time. Screen printing of thick film resistive pastes was enabled by introducing a thin immersion silver layer at the interface between the PTF and the copper termination. This advancement led to improved resistor stability through multiple reflow cycles and extended environmental testing.[1] The carbon-phenolic resin ink is used to create the embedded PTF resistor. This ink is available in sheet resistances from 35 Ω/□ - 1 MΩ/□ and can be blended in order to achieve any value in between. The material and processing cost is a fraction of that of the competitive thin metal film resistor technologies. Moreover, contrast to thin metal film technologies, PTF allows for the printing of multiple inks on the same layer thereby covering resistors with values as low as 10 Ω to as much as 10 MΩ on the same layer. Typical tolerances of screen-printed PTF resistors are between 15-20% for high volume production. Although this may seem high, many resistor applications in portable products do not require tight tolerances—20% tolerance is often acceptable. Furthermore, competitive technologies may claim better tolerance, but no other process has to-date demonstrated better and more consistent tolerance values than PTF in high volume. Laser trimming techniques that dynamically measure resistors while trimming have made it possible to achieve <3% overall resistor tolerance for more critical applications.

Recent innovations have improved the embedded resistor manufacturing process by implementing design changes that enable better predictability of as-printed resistor values.[2] Short and long resistors (with constant width) don't always follow a linear relationship in terms of as-printed resistance. In theory, a 1 square resistor should be exactly 10 times less resistive than a 10 square resistor when printed with the same ink and constant width. In reality, the 10 square resistor exhibits a higher resistance than predicted. This is due to mechanical effects as the print squeegee moves across the resistor terminations. To minimize this mechanical deflection, copper termination "fingers" running parallel to the resistor edge have been introduced to provide topographical uniformity in the resistor print area, preventing squeegee deflection (see Figure 1).

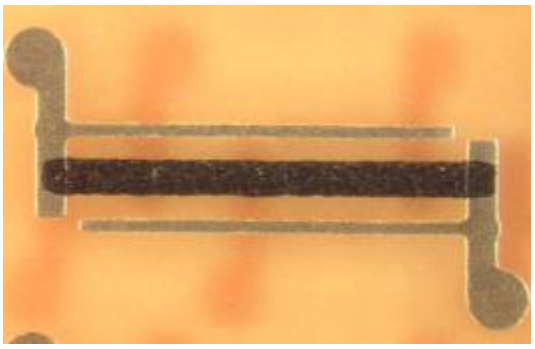

**Figure 1 - PTF Resistor Designed with "Fingers" to Enhance Linearity across Wide Range Aspect Ratios**

The result is excellent linearity of resistance vs. length. Boards can now be designed with multiple resistor values by adopting a standard width (0.25 mm is typical in our designs) and varying length to change resistance. The need for screen modifications and multiple test runs before committing a product run is eliminated for resistors from 0.25 to 2.5 mm long (1 to 10 squares). Although earlier design rules were highly manufacturable, these recent improvements allow our preferred vendors to improve their efficiency by reducing cycle time and scrap and improve overall product yield.

Using preferred design methods, materials and manufacturing processes, resistors as small as 10 mil x 10 mil and ranging from ohms to mega-ohms can be printed with 10-20% untrimmed tolerances, 3% laser trimmed tolerances, and ±5% stability. No other high volume embedded resistor process can make such a claim and substantiate it with consumer products in the field. In the past year, other firms have also started using this technology to reduce product size and cost and achieve superior electrical performance.

**Embedded Capacitor Technology**

Nearly any value of resistor can be formed with the PTF material. Conversely, capacitors have restricted ranges based upon the choice of dielectric material, structure, and area allowed. Typical cell phone PWB designs are based upon HDI constructions, and the first embedded capacitors were parallel plate constructions with HDI resin as the dielectric. Unfortunately, HDI resin has a relatively low dielectric constant (~4), and resin thickness between plates was approximately 50µm, resulting in a capacitance density of 0.8 pF/mm$^2$. Although applicable for a small subset of embeddable capacitor opportunities, a new material with a higher capacitance density was needed.

Embedded Mezzanine Capacitor (EMC) technology utilizes a process whereby a positive acting Ceramic Filled Photodielectric (CFP) is used to produce embedded capacitor structures that typically lay in between main routing layers in a HDI-PWB (*e.g.*, between layers 1 and 2). In effect, a partial layer of dielectric is created within the board—a concept not used before in the PWB industry.

The CFP material is designed to be coated onto a substrate at the board shop using typical board fabrication techniques. Its ceramic loading factor is limited by the need to remain photoimageable, yet the relative dielectric constant of the material is still approximately 21 at 1 MHz. The capacitor structure formed with CFP is intended to be "sandwiched" within a typical HDI construction. It rests on the lower copper layer, but it is completely covered by HDI resin. No space, save a single microvia contact, is required on the upper HDI copper layer. Hence, this construction is called a "mezzanine" capacitor, as it occupies an intermediate layer in the structure of the PWB. The process produces both discrete capacitors and/or shared capacitance layers with a resulting capacitance density of approximately 16.8 pF/mm$^2$. Capacitors ranging in value from 2 pf to 500 pf can be cost- and space-effectively embedded. Radio Frequency (RF) sections of cell phone circuits typically contain large numbers of RF by-pass capacitors that fit within the range that can be easily embedded using this technology.

Using this unique process and the partial dielectric layer has several advantages. First of all, a high-K dielectric layer is avoided throughout the board, which can have detrimental effects to high-speed or high-frequency transmissions. The

embedded capacitors, moreover, can be placed extremely close to (often right underneath) the IC devices requiring fast charge delivery-thus significantly improving the electrical performance of the IC device by eliminating parasitic inductance.

A cross-section of a completed CFP capacitor is shown in Figure 2. For more information on the integration process and the frequency response and reliability properties of CFP, the reader is referred to other literature.[3] Specific implementations are discussed in the sections following.

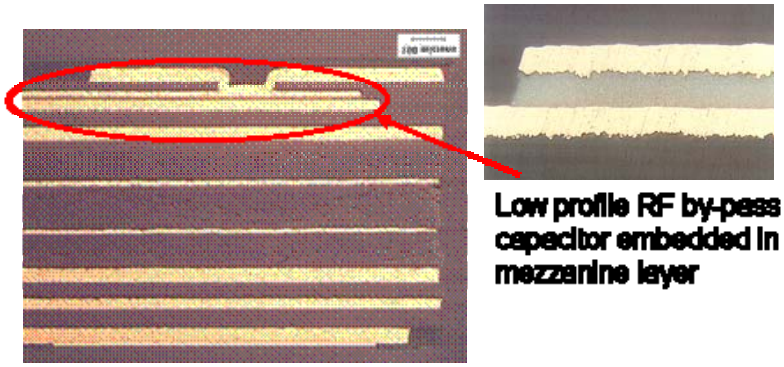


**Figure 2 - Mezzanine Capacitor Cross-Section as shown Buried in a Multi-Layer PWB**

It is important to note that work continues to develop new embedded capacitor technologies to further advance its EP portfolio, including the development of a new High Capacitance Foil (HCF) to augment the existing CFP technology. The HCF will extend the embeddable range for capacitors up to 0.075 µF and will be available to PWB suppliers as a standard foil comprised of a copper-dielectric-copper sandwich. The HCF sandwich will be compatible with conventional lamination and patterning technology and will be applicable to both embedded shared capacitance and embedded discrete capacitor applications. It is envisioned that the combination the CFP technology and the HCF will allow for 95% of all capacitors used in hand-phone applications to be embedded.

**Case Study #1: 800 MHz Local Oscillator**

The first module presented here was the initial commercial deployment of the CFP EMC process. The module is a replacement for a set of motherboard components in a GSM phone product. A set of 18 SMT components that comprise a local oscillator circuit were selected for development into a new module. The estimated area on the motherboard for these parts was 48.1mm$^2$. Both LTCC and organic materials were considered for the replacement module.

The initial bill of materials included 5 resistors, 9 capacitors, 2 inductors, and 2 active parts. Of these parts, all 5 resistors were embedded with PTF ink, using 2 sheet resistivity inks. CFP was used to embed 7 of the 9 capacitors. In addition, a single inductor was embedded into the substrate in a 2.5 turn design. To aid in tuning the mostly embedded circuitry, an additional 0402 SMT capacitor solder pad set was added, increasing the potential SMT part count to 6 for the EP module when the pad set is populated. The resulting module size is 3.8mm X 6.4mm, or 24.3 mm$^2$. A picture of the completed module is shown in Figure 3. In this case, the extra SMT pad set is unused. Layout files of the inner layers showing the embedded resistors and capacitors appear in Figure 4.

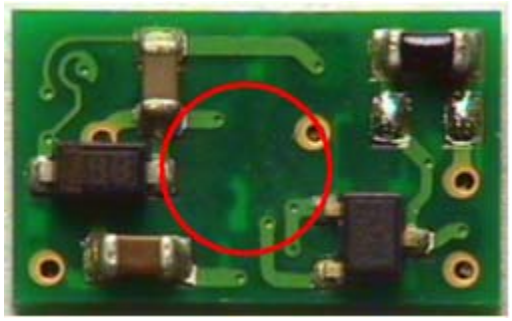

**Figure 3 – Local Oscillator Module – Annotated Circle Indicates Pick and Place Area**

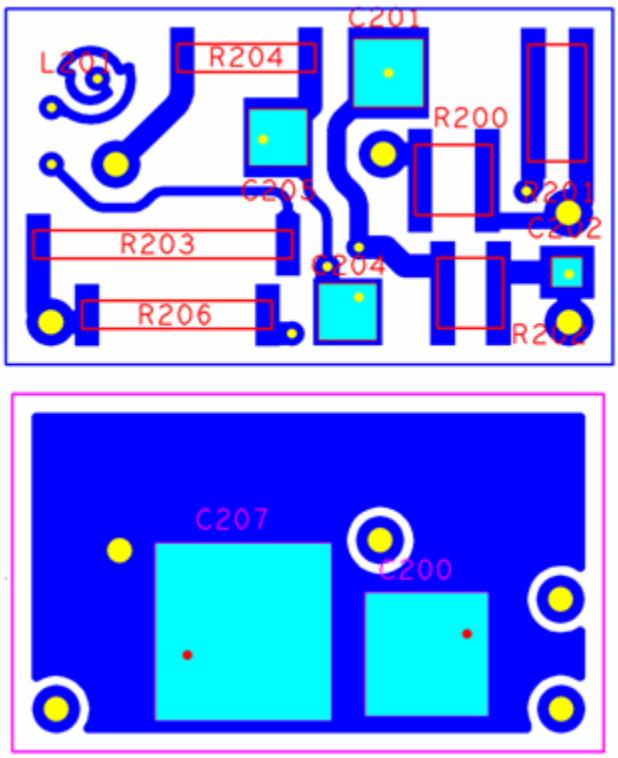


**Figure 4 – Layout Files for EP Module Inner Layers top – Upper core Layer; bottom – Lower core Layer**

The EP module exceeded all of the required electrical specifications. The area consumed by the organic EP module is 24.3mm$^2$, which represents an area savings of 49% compared to the motherboard implementation of the circuit. In addition, there was a cost savings of approximately 25% compared to the motherboard implementation based on the direct materials and conversion costs of the two solutions.

This module requires no metal lid for shielding. For an all-SMT design, something must be done to provide a smooth location for the pick & place vacuum nozzle to grab the module. If no lid is present, the smooth surface is often provided by either encapsulating the module, adding cost, or by affixing a Kapton dot that bridges multiple SMT components. The latter process often has implications at assembly, since the dot does not always adhere smoothly to the module. In the case of the EP version of this module, the remaining SMT parts were shifted to the periphery of the board, leaving a sufficient space in the center for the vacuum nozzle to pick up the module on the board's solder mask. The pick and place area is highlighted by a red circle in Figure 3.

In summary, the use of EP components in this module produced the following advantages:

- Dramatic reduction in solder joints → greater reliability
- Simpler assembly—only 6 SMT components → higher assembly throughput
- Open area for pick & place → no added cost for encapsulation or Kapton dot
- Reduction in overall cost of the circuit by approximately 25%

**Case Study #2: GSM System-on-Module (GSM SOM)**

Early deployments of EP in handheld products focused on small module form factors with very high density of embeddable components. In these cases, the promise of cost savings and size reduction were the motivating factors. In 2004, a new opportunity presented itself that had a focus more on enabling size reduction with only a goal of cost parity. The module in this opportunity was looking at many advanced technologies, arguably the most-proven of which was embedded passives, to create a super-shrink of a broad functional unit. That opportunity was the GSM System-on-Module (GSM SOM).

The GSM SOM is the equivalent of a quad-band GSM/GPRS phone miniaturized to a 3.5cm$^3$ module using advanced packaging and assembly technologies. It incorporates the RF front end, the radio section, the baseband processor, memory, power management and audio functions in that volume. A picture of the GSM SOM along with the major phones it shipped within appears in Figure 5. Along with stacked die packages, stacked and filled vias, fine lines & spaces, and other advanced

board and packaging technologies, the GSM SOM incorporates 27 RF bypass capacitors through the use of CFP EMC technology.


**Figure 5 - GSM SOM (center) incorporating the Embedded Mezzanine Capacitor Technology and the C650 (left) and V220 (right) Phones utilizing the GSM SOM**

The GSM SOM was first introduced in the market in April 2004 in the C650 Quad Band (850, 900, 1800, & 1900 MHz) GSM/GPRS "candy bar" phone. The module was subsequently re-used in May 2004 in the V220 Quad Band GSM/GPRS "clam shell" phone. Approximately 15 million units of the GSM SOM module were shipped in these two phones during 2004 and 2005, which are marketed and sold in North America, Europe, Asia, and South America.

Figure 6 shows a pictorial cross-section of the GSM SOM PWB, and Figure 7 shows the locations of embedded mezzanine capacitors on layers 2 and 7 of the GSM SOM PWB in a layout view of those layers. Figure 8 shows physical cross sections of the board, with an inset that shows an actual EMC capacitor. Notice that the capacitors take up a relatively small area on this large module. Overall, the module saves approximately 40% of footprint space compared to the core GSM/GPRS phone function of the equivalent motherboard

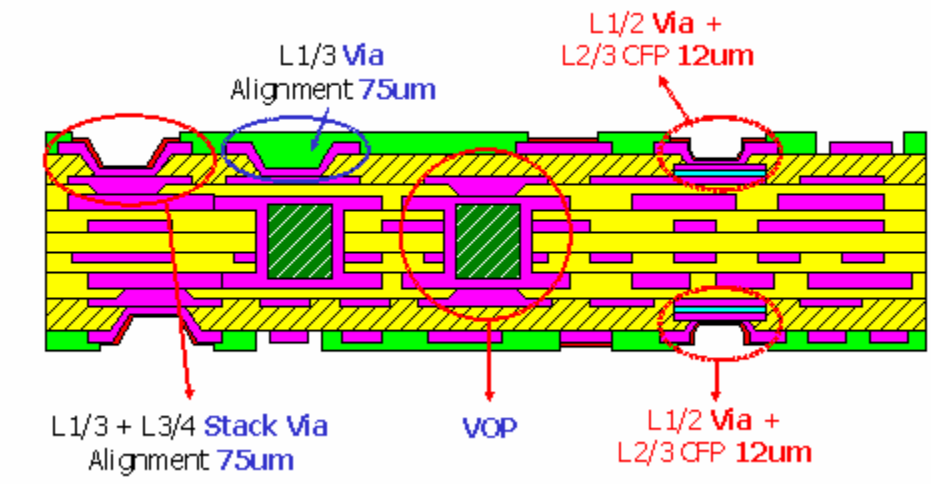


**Figure 6 - Schematic Cross-Section of a GSM SOM PWB**

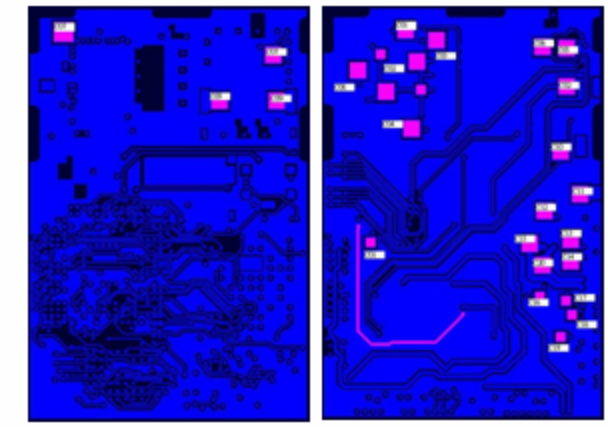

**Figure 7 - Layers 2 and 7 of the GSM SOM PWB showing in Pink the Location of the 27 Embedded Mezzanine Capacitors**

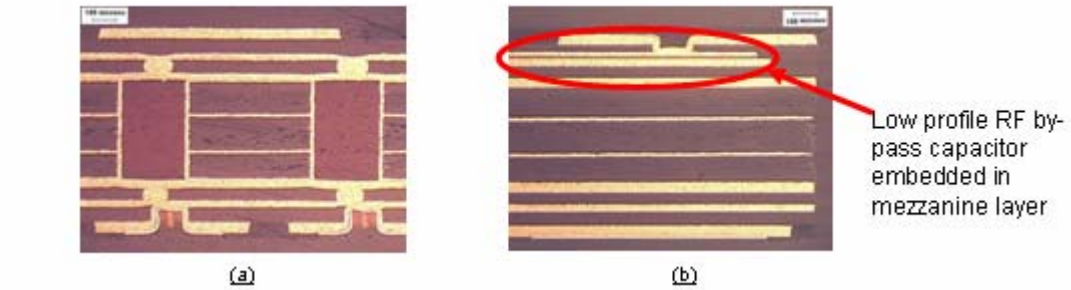


**Figure 8 - GSM SOM Cross-Sectional Views: (a) Layer Structure, (b) CFP Capacitor (Circled In Red)**

Another significance of the GSM SOM milestone in 2004 was the robustness of the CFP mezzanine capacitor technology, both in terms of yield and performance as well as material volumetric scaling, in a very aggressive product ramp-up. For the first time, Motorola's dielectric material supply chain partner had to produce CFP in something other than a lab-based prototype reactor. Up to this point, multi-kilogram batches were sufficient to keep up with production. For instance, little material was needed to produce millions of the 800 MHz LO product, as over 3000 pieces fit on each panel. For the GSM SOM, with equal or greater run rates, only about 50 substrates fit on a panel. In short order, Motorola's partner transitioned the formulation to a production reactor, producing enough CFP for the 15+ million phones using the module—CFP sufficient to coat over 12 football fields with a dielectric layer 11 microns thick.

In the case of the C650 and the V220 phones, the 40% size reduction of the GSM/GPRS phone function, partially as a result of the EP technology, created enough space to be able to add a camera and a joystick module in the phones, along with better design of antennas, resulting in improved reception and enhanced battery life. Functionality improved. In terms of cost, this implementation is difficult to track. Based on materials cost and estimated assembly costs, the CFP functions were displaced at a cost parity compared to an equivalent SMT implementation. The GSM SOM was a successful product launch of embedded passives in a large-scale module with independent functionality.

## Lessons Learned

Motorola has had very good success in commercializing products with embedded passive components, achieving more than $50M in cost savings in just a few implementations. The implementations have been from the simple to the complex, from the extremely small module to the full-functionality phone module. Several lessons have been learned along the way, and the balance of the paper is intended to impart a few of those bits of knowledge to the reader.

### *Lesson #1: Design tool Issues can be Overcome*

A major complaint around trade shows from potential EP users is the lack of proper design tools available that allow proper inclusion of passive, valued components into a board design. Although recent strides have been made by multiple vendors, this statement is still largely fact. However, all of the designs to-date were completed without specialized EDA tools to handle embedded passives. Is it the ideal situation? Absolutely not. Is it possible to complete a design without special tools?

Absolutely! For Motorola, the volume of the business justified the workarounds in error checking and other design steps. It can be done. Find an application where the benefits in cost savings or space savings is worth the extra design verification work.

***Lesson #2: Evaluate Overall System Costs—Not Board Costs***

Nature abhors a vacuum almost as much as a supplier in the electronics chain avoids adding cost to its portion of a product. Almost without exception, the board cost of an embedded passives product will increase. The nature of the electronics supply chain is for each segment of the chain to minimize its costs. If that is the view for EP products, then EP designs will never be realized in any meaningful capacity. Costs must be addressed and marketed at a system level, or in other words, *from the OEM perspective*.

In every case that has been documented by the authors, module cost with embedded passives has been less than or equal to the comparable all-SMT implementation. Typically, the board is reduced in size, yielding more parts per panel. The cost per board is still typically higher. However, simplifications in assembly and direct BOM reductions meet or supersede the increased board costs, yielding a module that is either cheaper or at cost parity than the comparable all-SMT case.

For those seeking to sell material or sell boards into the EP supply chain, the OEM view of system cost must be the prevailing reference point.

***Lesson #3: Make Judicious Implementation Choices***

The key to a good design is the chaining together of several wise design choices. First of all, every opportunity block must be considered, both on the whole of the design and in its major sections. Assess all the BOM parts for replacement with EP in terms of part value first, then restricted by tolerance, TCR/TCC, and other performance limiters. Check the price penalty or benefit for the reduced BOM set. A good module need not embed every "embeddable" part. You must weigh whether or not the benefits merit the risk of your particular design.

***Lesson #4: Challenge EE assumptions***

Nearly all SMT resistors are available in 5% tolerances, if not better. Embeddable resistor technologies, like PTF, are at much higher tolerances in production…more on the order of 20%. Similar disparities are also true with capacitors and inductors. The reactive components also suffer from poor quality factor (an electrical term denoting an energy storage vs. energy dissipated ratio) as compared to many SMT parts. These factors are primarily used to argue against inclusion of embedded passives. Often, the arguments are based upon supposition or simply the fact that better properties are available in SMT parts. No simulation or other work has been completed to see if the tolerances or other property differences are acceptable; the EP parts are disallowed merely because better property SMT parts exist. Challenge the EE (note: the lead author is an EE). The designs presented herein have successfully embedded passive components—including resistors—in sensitive RF circuits such as tri-band voltage controlled oscillators (VCO) operating in the 0.8-1.9GHz range. It can be done. It only takes a little more work in order to make the good choices of parts to embed. (See lesson #3 again.)

***Lesson #5: Density saves the Cost-Conscious Day Start Small***

Doing a first design with embedded passives is not without risk. It is advisable to start with a small design. Even if only a few passives are embeddable, the number of pieces per panel can be high enough to cost-justify the design. This is exactly the case for the 800MHz LO design. This design included a fair number of passives per panel, but the board cost was up significantly because of the inclusion of two technologies. The shear number of embedded parts was very high, though, because of the density of the panelization, allowing approximately 3000 parts per panel. The very large number of passives per panel made the build cost-effective. It was also a more sensible first design for CFP for several reasons: 1) a simpler circuit to debug or tune, 2) a panelization that could accept some reasonable yield loss, and 3) a truly impressive embedding demonstration, embedding more parts than were left on the surface. Similar patterns, at least the first two, should be characteristics of other first designs.

***Lesson #6: Enable the Entire Supply Chain***

EP technology requires a level of effort at materials suppliers, board shops and at the OEM design house. It took significant partnerships to establish new materials or modify existing materials to be appropriate for high-volume, reliable production. Additional partnerships and license agreements were needed to establish a board supply base through world-class board shops. OEMs that are serious about embedded passives must also establish partnerships at each of these levels.

**Summary**

To date Motorola has shipped the Embedded Passives Technology in nearly 50 million portable products. The technology can be found in many of Motorola's most popular GSM phones, namely, L7081 (first shipped in 1999), V60 & V66 (first shipped 2001), T720 (first shipped in 2002), C650, & V220 (first shipped in 2004). In addition to achieving space saving in the cell

phones shipped, a cost savings of over $ 40 million has also been realized through the implementation of EP technology. Others can follow this example if they start small, choose to design despite EDA tool issues, challenge EE assumptions, make judicious choices, and enable their overall EP supply chain.

**References**


1. J. Savic, *et. al*, “Embedded Passives Technology Implementation in RF Applications,” presented at the IPC Printed Circuit Expo 2002, Long Beach, CA, March 24-28, 2002
2. G. Dunn, *et al*, “New Developments in Polymer thick Film Resistor Technology”, presented at the IPC APEX/Expo 2004, Anaheim, CA, February 22-25, 2004.
3. Croswell, *et. al*, “Embedded Mezzanine Capacitor Technology for Printed Wiring Boards,” presented at the IPC Printed Circuit Expo 2002, Long Beach, CA, March 24-28, 2002.
4. A. I. Kingon, T. Kim, P. Vilarinho, J.-P. Maria, and R.T. Croswell, "Thin Film Capacitors Embedded into Printed Wiring Boards," presented at the 2001 IMAPS Conference, Baltimore, MD, October 7-11, 2001.