Decoupling High Speed Digital Electronics with Embedded Capacitance

IPC Works 2005

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Las Vegas, NV

Agenda

- Background on Embedded Capacitance and 3M Material
- Electrical Performance Data
- Capacitor Elimination Metrics
- Cost Considerations
- PCB Fab Compatibility and Reliability
- Commercialization Status

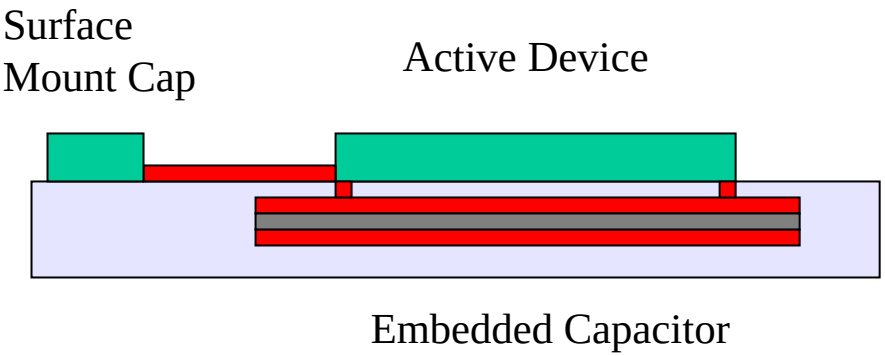
Background on Embedded Capacitance and Materials

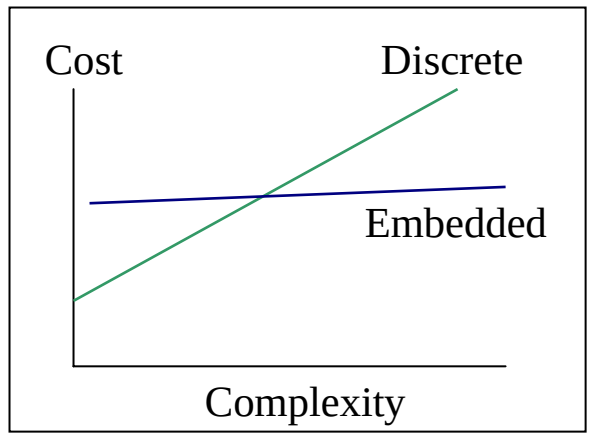
Thin-Film Capacitor Technology

- **Capacitance per unit area (C/A) is proportional to k and inversely proportional to t**
- **Vary C/A by varying thickness (t) or dielectric constant (k)**

Why Embedded Capacitance?

1. Performance
2. Space
3. EMI
4. Cost





Reasons for Embedded Capacitance

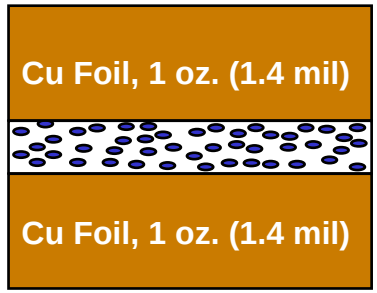
Potential Benefits	Performance	Space	Cost
Faster signaling/Reduce power bus noise	√		
Reduce design time & redesigns	√		√
Eliminate capacitors		√	√
Reduce layer count			√
Enable DS to SS assembly			√
Reduce via count		√	√
Simplify rework			√
Reduce board size, thickness		√	
Reduce assembly time			√
Enable decoupling w/back-side heat sinks	√		
Reduce weight	√		
Reduce opportunities for damaged components	√		√
Improve PWB panel utilization			√
Reduce EMI	√		√

Very Thin, Ceramic Filled Embedded Capacitor Materials

Product Description

Sheets of Cu-clad laminate
Thin, high Dk dielectric

- Ideal for high frequency decoupling
- Eliminates discrete capacitors
- Dampens plane resonances



Use

Power-ground innerlayer for rigid and flex PWBs

Customers/ Markets

High end rigid and flex board fabricators
High speed datacomm/telecomm equipment
Servers/workstations, Military applications

3M Embedded Capacitor Material
Key Properties

Attribute	Value
Capacitance /area	5.7 nF/in^2
Dielectric Constant	16
Dielectric Thickness	16 um (0.6 mil)
Dielectric loss @ 1GHz	0.03
Resin system	Epoxy, ceramic filler
Freq., Voltage, Temperature	Meets X7R
Dielectric Strength	~130V/um (3300 V/mil)
Breakdown Voltage	>100V
Copper Thickness	35 um (1.4 mil)
Flammability Rating	94V-0

*Thinner dielectric thickness and higher voltage breakdown in development

Electrical Performance Data

Driving Trends in Silicon

SIA Roadmap	'01	'02	'03	'04	'05	'06	'07	'10	'13	'16
Power Supply Voltage (V) Vdd (High Performance)	1.1	1.0	1.0	1.0	0.9	0.9	0.7	0.6	0.5	0.4
Allowable Max Power (W) High Performance with Heatsink	130	140	150	160	170	180	190	218	251	288
NEMI Roadmap	**'01**	**'02**	**'03**	**'04**	**'05**	**'06**	**'07**	**'10**	**'13**	**'16**
Max Power/Device (W) Large Business Machine Products			200		225		225	240	280	300
Max Current/Device (A) Large Business Machine Products			200		250		280	300	350	375

- **Lower voltage**
- **Higher power/current**
- **Higher frequency**

$$\frac{V\downarrow}{I\uparrow} = \downarrow Z$$

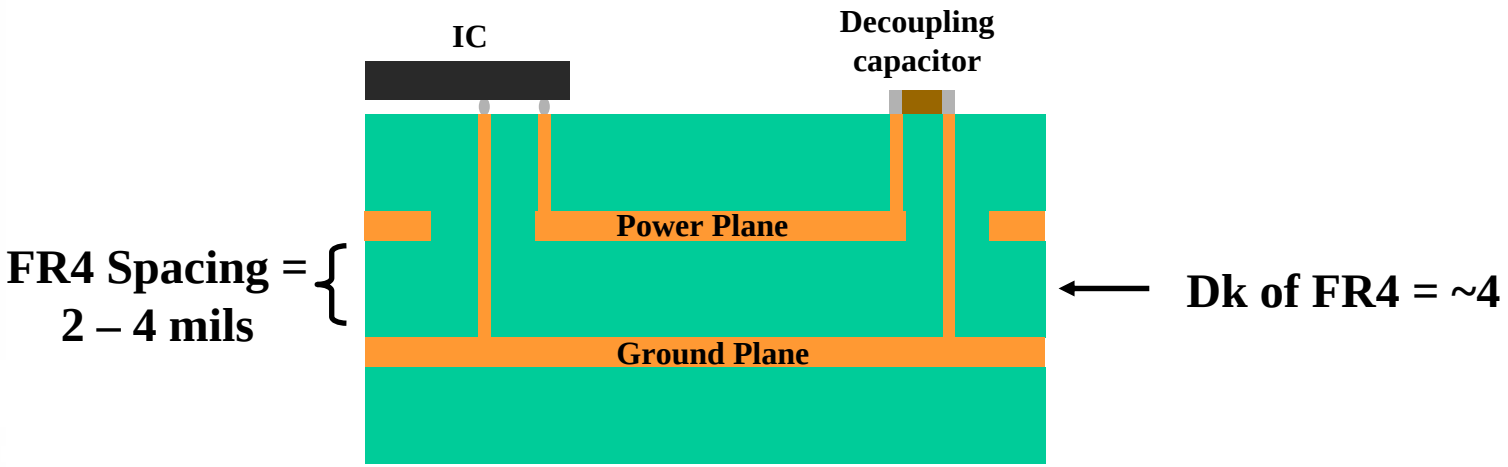
The Need for Electrical Performance

- High speed digital electronics require **low impedance power distribution**, driven by trends in silicon
  - Lower voltages
  - Higher currents
  - Higher frequencies

  } $\frac{\downarrow \text{Voltage}}{\uparrow \text{Current}} = \downarrow \text{Impedance}$

- If the impedance of the power distribution system is too high, the impact will be signal bit errors (e.g. a “0” read as a “1”)
- 3M™ Embedded Capacitor Material is a very simple and effective way to lower the impedance of the power distribution system
  - Lowers voltage ripple and dampens board resonance
  - Reduces EMI
  - Eliminates decoupling capacitors

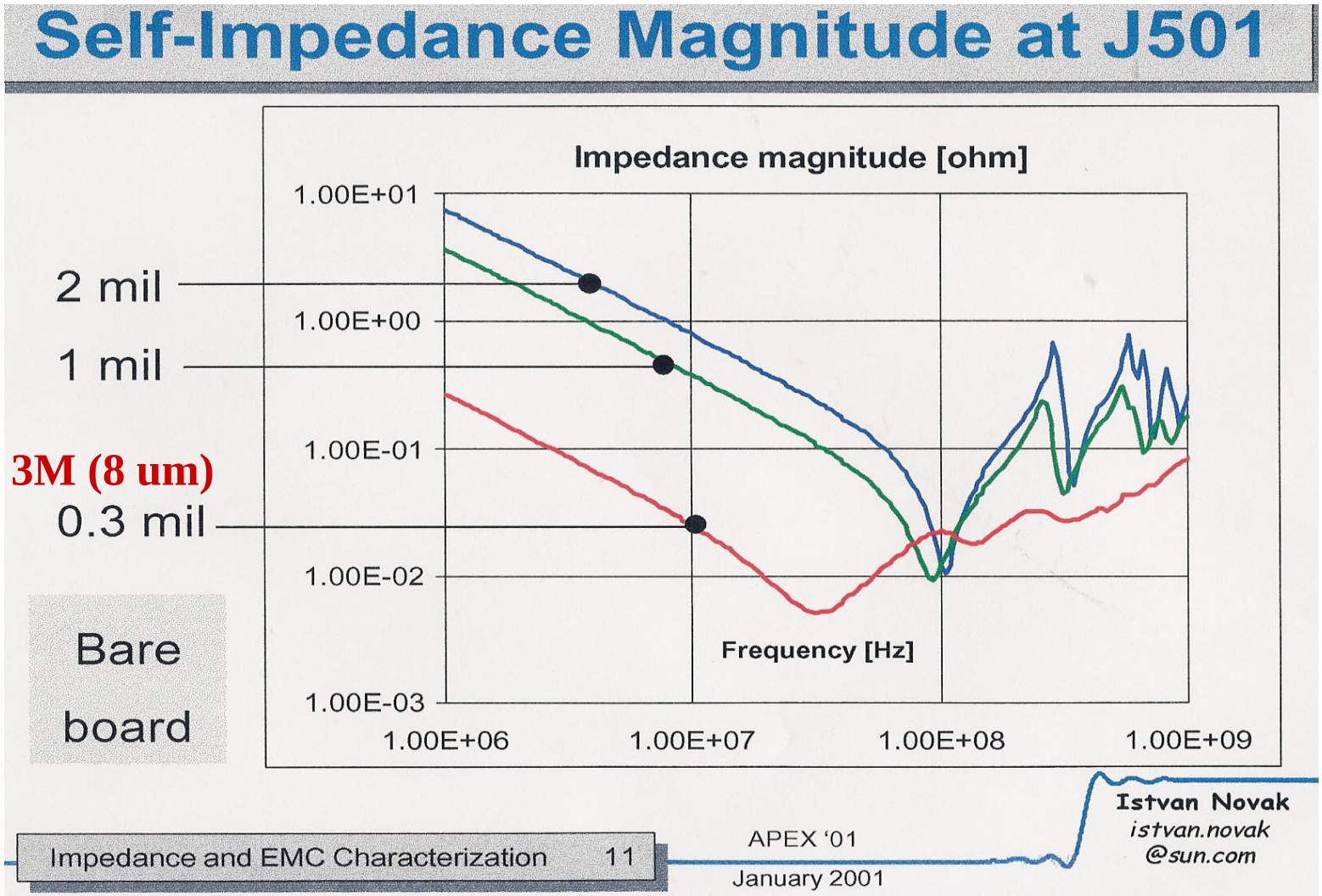
Power Distribution Impedance



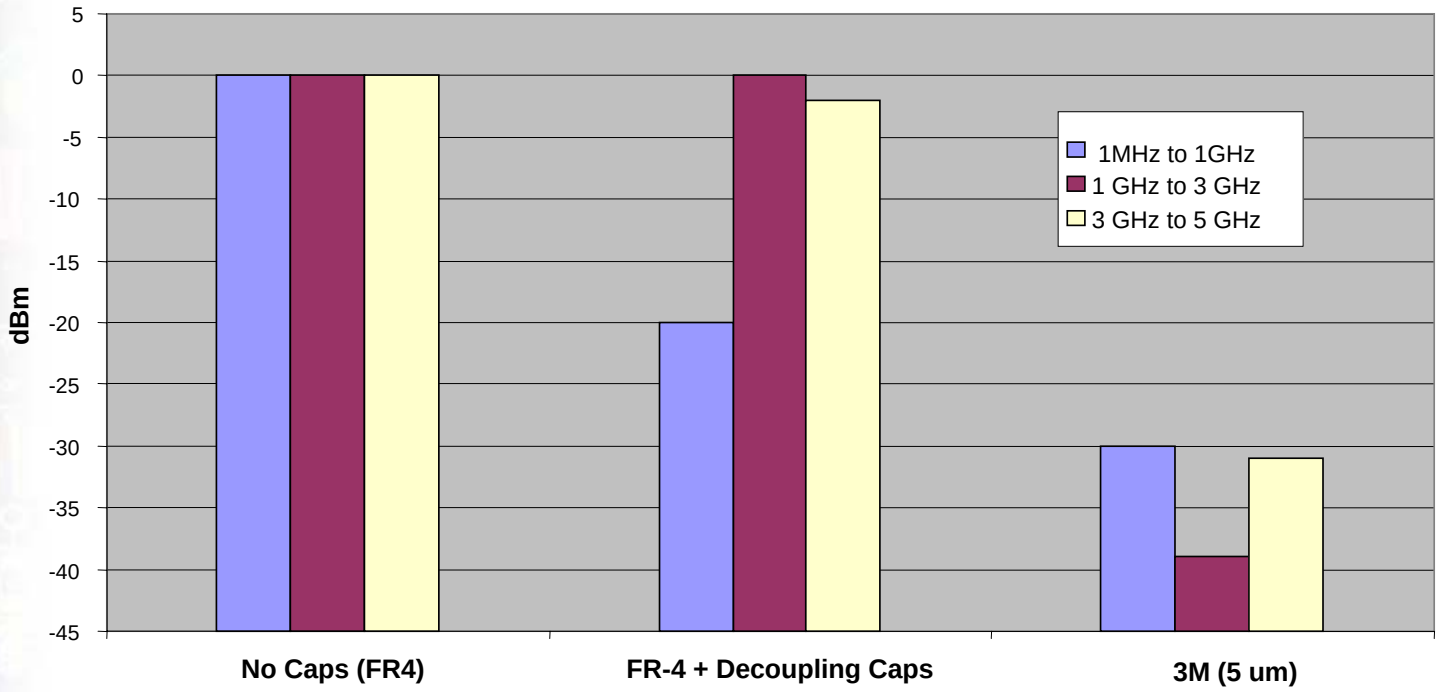
Ways to lower power distribution impedance:

- Reduce power-ground plane spacing
- Increase Dk of material separating power-ground planes

Impedance Comparison



Power Bus Noise on Test Vehicle



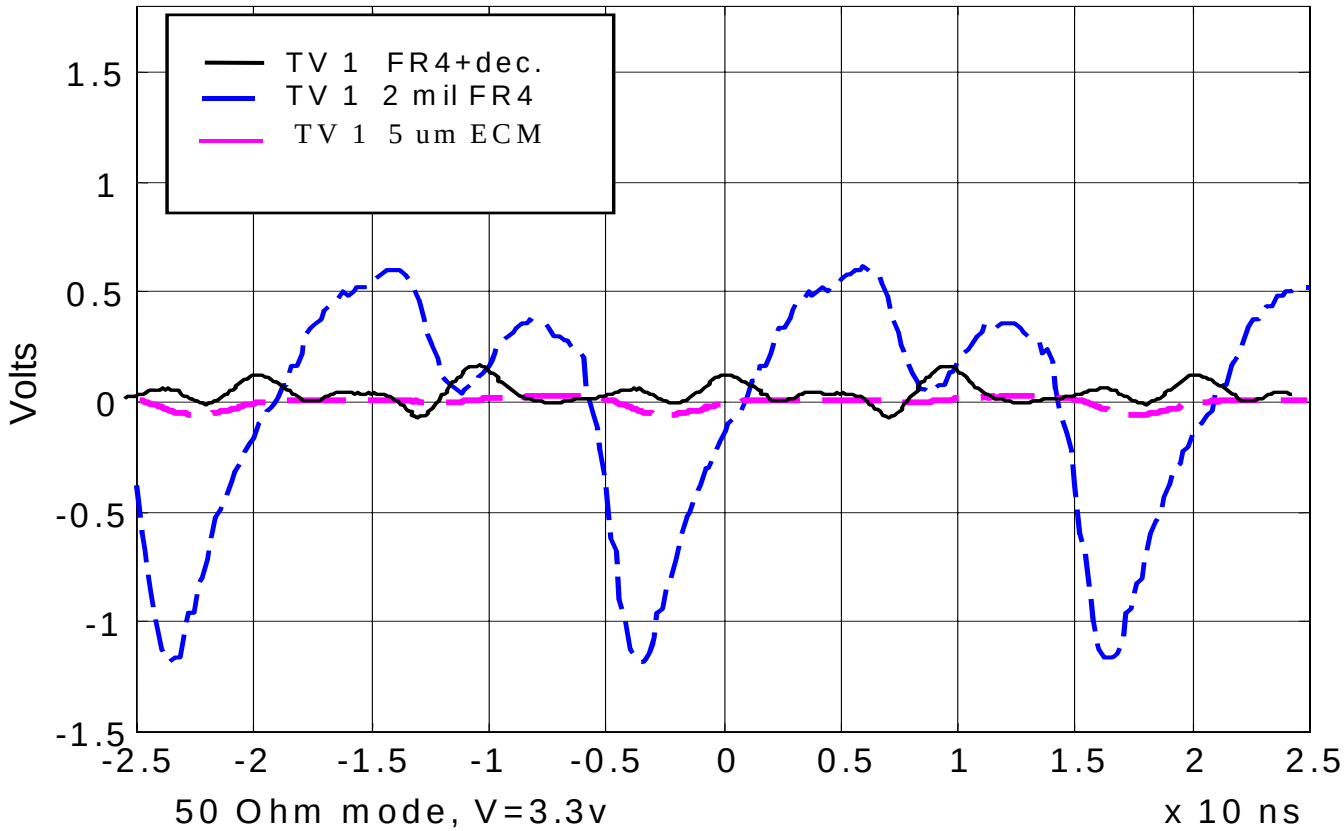
Less Noise

- **Traditional decoupling capacitors are not effective at frequencies above 1 GHz**
- **Very thin, ceramic filled material has excellent performance to 5 GHz**

Data from NCMS Embedded Decoupling Capacitance Project Report - 12/00

Power Bus Noise

(Time Domain - 50 MHz)



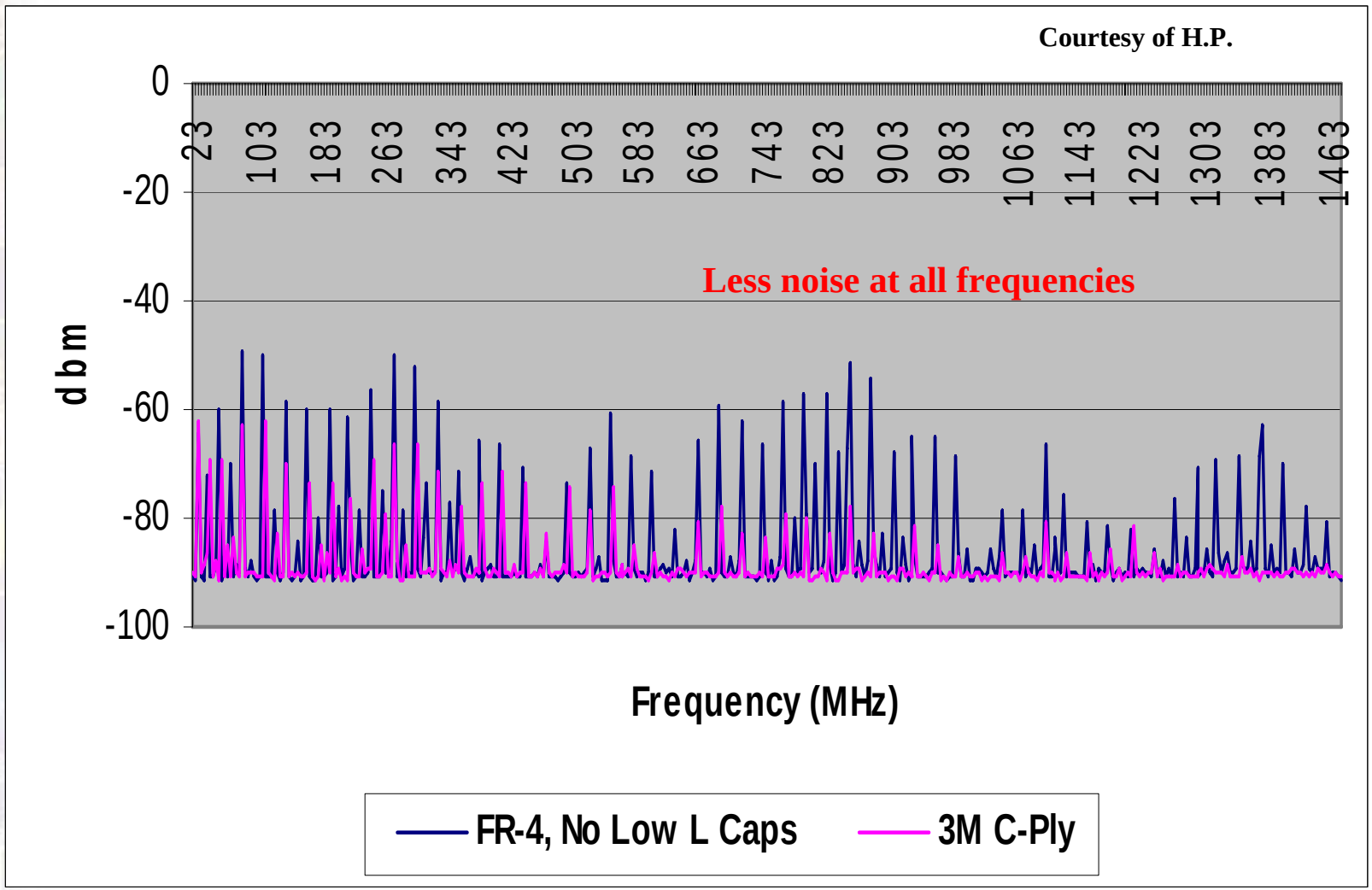
Data from NCMS Embedded Decoupling Capacitance Project Report - 12/00

Embedded Capacitor Test Board

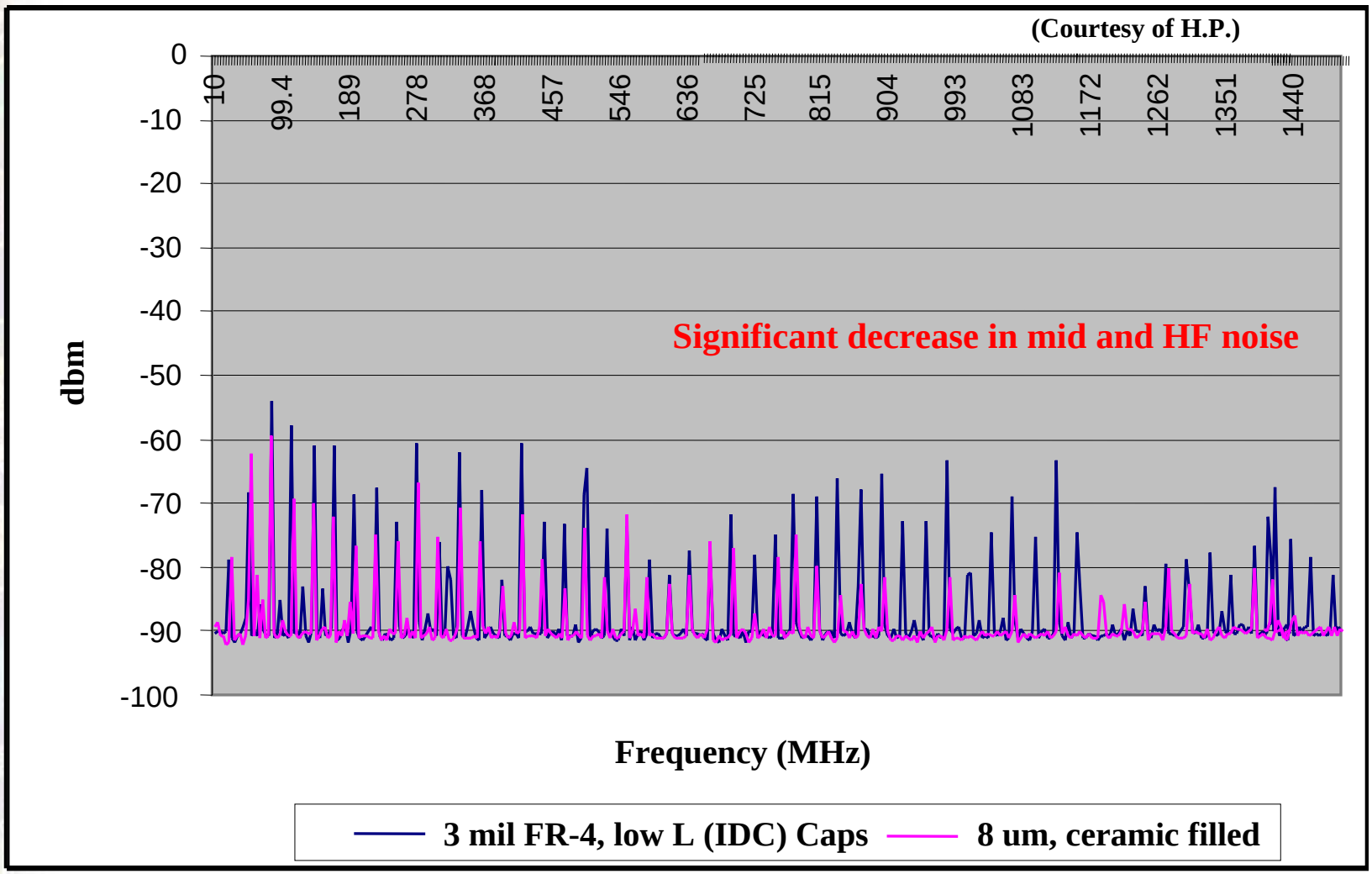
(Courtesy of Hewlett Packard)

- **Processor daughtercard**
  - MIPS R14K processor @ 550 MHz
  - 9 Secondary cache SRAM's @ 275 MHz
- **Laminate thickness between power and ground modified**
  - 3 mil FR-4
  - 3M Embedded Capacitor Material, 0.3 mil thickness (8 um)
- **Measurements made on 1.5 volt I/O power distribution**

Power Bus Noise vs. Frequency



Power Bus Noise vs. Frequency

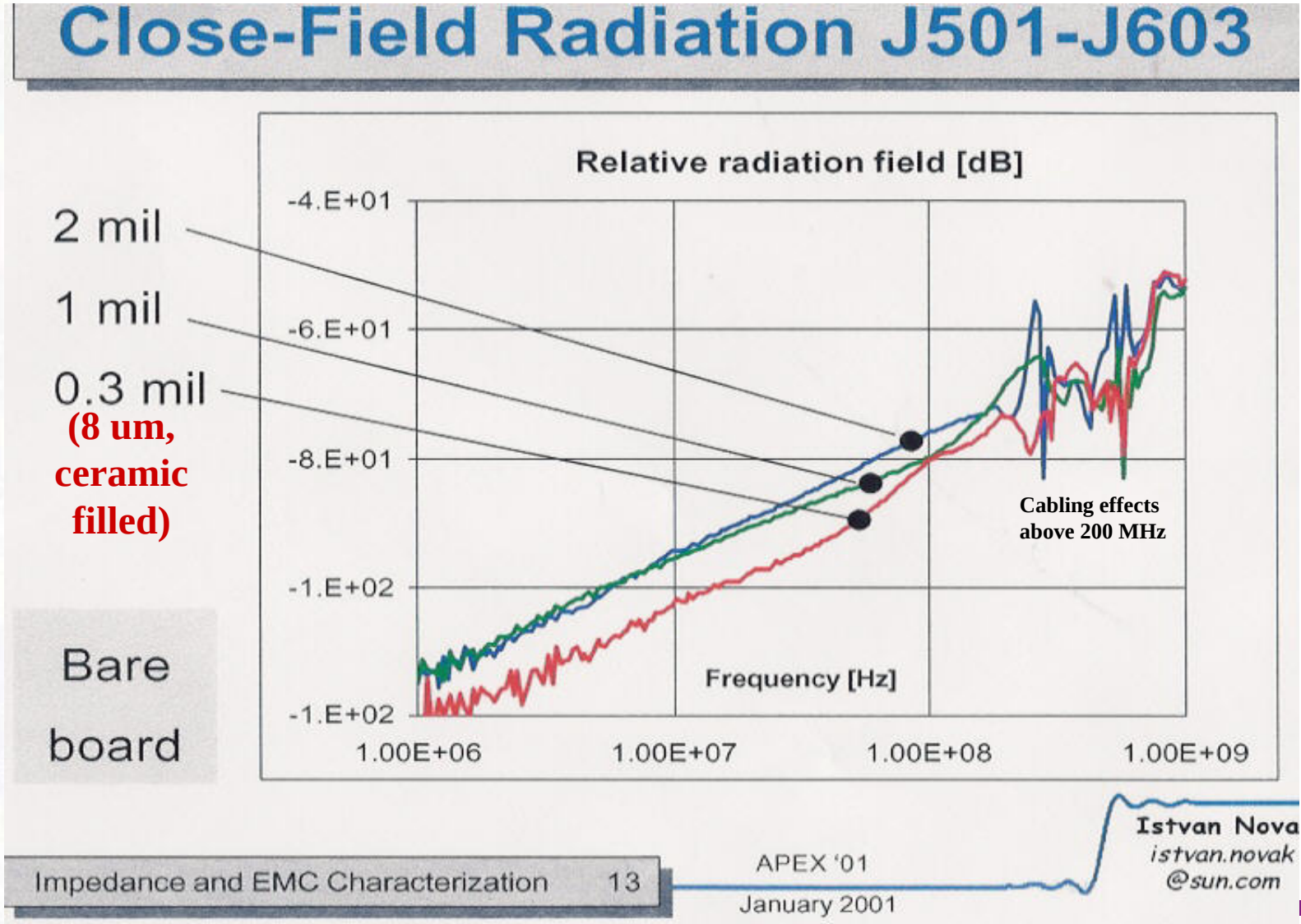


H.P. Test Board Noise Levels

3 mil FR-4 without Low L Bypass Caps	0.0 dB
3 mil FR-4 with Low L Bypass Caps	-6.8 dB
Ceramic Filled ECM (8 um) without Low L Bypass Caps	-13.3 dB
Ceramic Filled ECM (8 um) with Low L Bypass Caps	-13.9 dB

Reduction of ~13 dB with the use of ultra-thin power-ground core

Radiated Emissions Comparison



Electrical Benefits of Embedded Capacitance for Power-Ground Decoupling

- Lowers impedance of power distribution system
- Dampens board resonances
- Reduces noise on power plane
- Reduces radiated emissions

Capacitor Elimination Metrics

Examples of Very Thin, Ceramic Filled Embedded Distributive Capacitance Replacing Discretes

Design	Discrete Capacitance Removed (nF)	Embedded Capacitance (nF)	Ratio of Removed to Embedded	% of Total Discrete Capacitance Removed
EDC TV1	330 *33 x 0.01 uF*	105	3.1	100%
OEM A	12,600 *126 x 0.1 uF*	300	42.0	>75%
OEM B	6,310 *62 x 0.1 uF* *11 x 0.01 uF*	210	30.0	>60%
OEM C	3,180 *29 x 0.1 uF* *28 x 0.01 uF*	305	10.4	>75%
OEM D	52,900 *529 x 0.1 uF*	1970	26.9	>75%
OEM E TV	9,900 *99 X 0.1 **uF***	660	15.0	100%

Examples of How Many Discrete Caps Can be Replaced per Board Area

Design	Board Layers	No. of ECM Power-Ground Cores	Approx. Board Area (in^2)	Total No. of Caps Removed	Caps Removed per sq in
EDC TV1	6	1	6	33	5.5*
OEM A	12	1	35	126	3.6
OEM B	10	2	17	73	4.3
OEM C	8	2	12	57	4.6
OEM D	14	2	121	529	4.4
OEM E TV	4	1	120	99	0.8*

*100% of decoupling caps removed

How Many Caps Can be Replaced per Given Amount of Embedded Capacitance

Design	Discrete Capacitance Removed (nF)	Embedded Capacitance (nF)	No. of Discrete Caps Removed	No. of Caps Removed per 100 nF of ECM
EDC TV1	330 *33 x 0.01 uF*	105	33	31*
OEM A	12,600 *126 x 0.1 uF*	300	126	42
OEM B	6,310 *62 x 0.1 uF* *11 x 0.01 uF*	210	73	35
OEM C	3,180 *29 x 0.1 uF* *28 x 0.01 uF*	305	57	19
OEM D	52,900 *529 x 0.1 uF*	1970	529	27
OEM E TV	9,900 *99 X 0.1 **u**F*	660	99	15*

***100% of decoupling caps removed**

Functionality/Power Bus Noise/EMI Test Results

Design	Discrete Cap. Removed (nF)	Functionality Testing	Power Bus Noise	EMI
EDC TV1*	**330** *33 x 0.01 uF*	**Fully Functional**	**Much Improved** **(90 vs. 230 mV)**	**Somewhat Better**
OEM A	**12,600** *126 x 0.1 uF*	**Fully Functional**	**Not Tested**	**Not Tested**
OEM B	**6,310** *62 x 0.1 uF; 11 x 0.01 uF*	**Fully Functional**	**Not Tested**	**Similar**
OEM C	**3,180** *29 x 0.1 uF; 28 x 0.01 uF*	**Fully Functional (>2 yrs at 24/7)**	**Not Tested**	**Not Tested**
OEM D **OEM D TV***	**52,900** *529 x 0.1 uF* **1,600** *16 X 0.1 uF*	**Fully Functional** **Fully Functional**	**Not Tested** **Much Improved** **(20 vs. 120 mV)**	**Much Better** **(10-15 dB)** **Not Tested**
OEM E TV*	**9,900** *99 X 0.1 **u**F*	**Fully Functional**	**Much Improved** **(30 dB+)**	**Not Tested**

***100% of decoupling caps removed**

Summary

- **Surface mounted discrete capacitors are ineffective above 1 GHz**
- **Embedded capacitance power-ground cores can replace a large number of discrete decoupling capacitors from the board surface**
- **Tools/methods for determining capacitor removal are lacking**
- **Results presented today suggest:**
  - **~3 to 6 decoupling caps per square inch can be removed with the use of very thin, ceramic filled materials**
  - **~20 to 40 decoupling caps can be removed per each 100 nF of very thin, ceramic filled materials**

Cost Considerations

Cost Drivers of Embedded Passives

	Cost Adders	Cost Reducers
Board	• Material cost (laminate) • PWB processing costs • Yield	• Board size reduction • Reduced layer count • Fewer vias
Board Assembly		• Eliminate capacitors • Reduce assembly cost • Yield/rework (component count)
System/ Design	• Cannot rework embedded	• Fewer design cycles • Faster layouts • Eliminate other EMI measures • Improve reliability, service life

Cost Conclusions

- **Bare board costs will almost always increase**
- **System costs may increase or decrease**
  - **Design dependant**
  - **Higher component densities favor embedding**
- **As technology and supply chain infrastructure matures, costs of embedded approaches will decline, and opportunities for system cost reduction will expand greatly**

PCB Compatibility and Reliability

PCB Processing - 1

- **Compatible with all rigid and flex PCB processing (including laser ablation)**
- **Material handling is most significant issue (compares to bare 2 ounce copper)**
- **A sequential lamination process is recommended**
  - **Pattern 1st side copper**
  - **Laminate patterned side to another layer of prepreg**
  - **Pattern 2nd side copper**

PCB Processing - 2

- **If a sequential lamination process is utilized, there are no design limitations**
- **Many high end fabricators have successfully fabricated numerous prototype lots**
  - **Over 40 board designs have been manufactured by over 20 fabricators for over 25 different OEMs**
  - **Additional fabricators have demonstrated process capability (over 50 fabs have used the product to-date)**

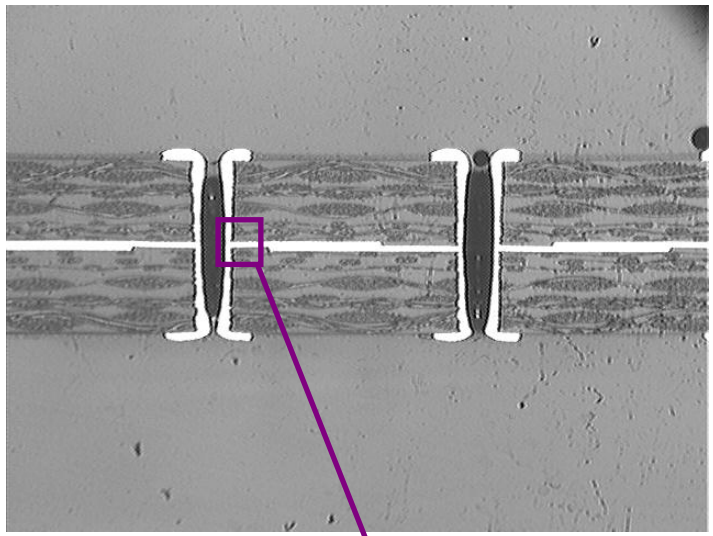
Tested Materials

- Low and high Tg FR-4 (Epoxy-Glass)
- BT/Epoxy
- Nelco 4000-13/4000-13SI
- PPO/Epoxy (Megtron/Getek)
- Embedded Resistor Materials
  - **Ohmega-Ply**
  - **Gould TCR**
  - **MacDermid M-Pass**
  - **DuPont Interra Ceramic**
- Polyimide Film (Kapton)
- Thermount (Polyimide)
- Polyimide-Glass
- Rogers 4450 and 4003
- Gore Microlam 630
- APPE

*** Materials are in the same stackup but not always adjacent to 3M material**

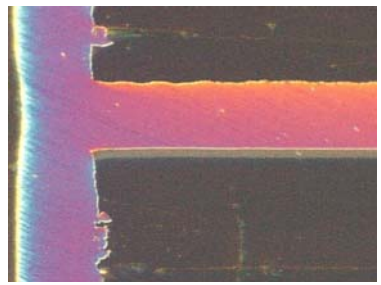
PCB Processing

4-Layer Board Cross Section



Embedded Capacitor Layer

Through-hole connection to top electrode of embedded capacitor layer

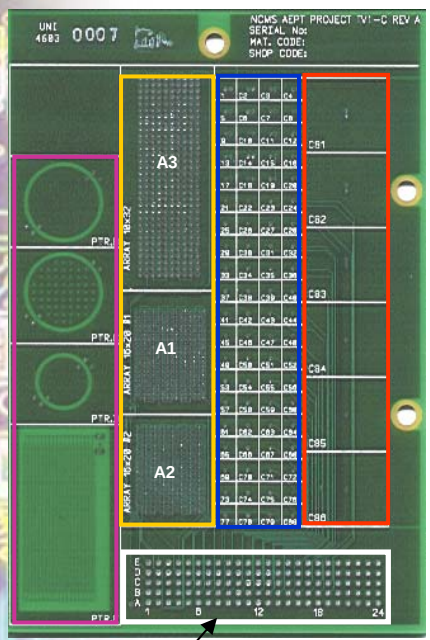


Reliability Testing on 16um Dielectric

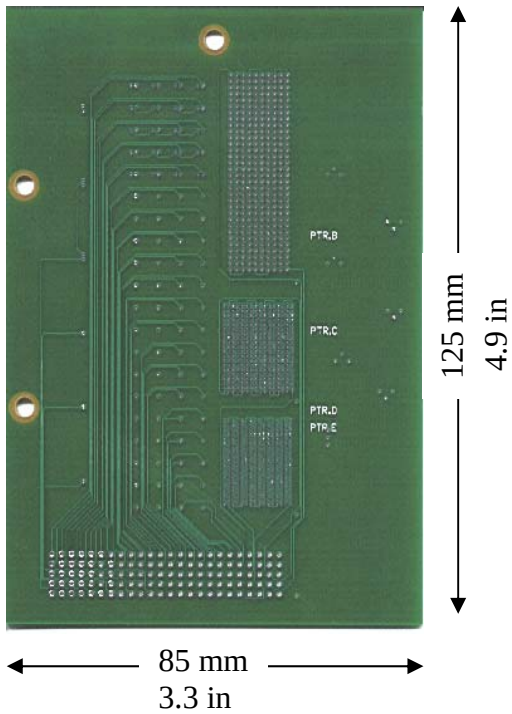
- **Testing performed in Q1 2004**
- **Board Materials: multilayer FR4 board including 3M Embedded Capacitor Material**
- **Variables:**
  - **2 Board types**
    - **4 layer, .062” (approx.), 1 embedded capacitance core (layers 2/3)**
    - **8 layer, .093” (approx.), 2 embedded capacitance cores (layers 2/3, 6/7)**
  - **3 Fabricators**
  - **2 Dielectric thicknesses (16 um, 8 um)**
- **Tests:** ***Thermal cycle*** ***THB*** ***Thermal shock*** ***Reflow*** ***Life*** ***Solder float*** ***TMA***

Test Vehicles

TV-1C Side A



TV-1C Side B



4 Layer Stackup:

Signal
ECM { Power
ECM { Ground
Signal

8 Layer Stackup:

Signal
ECM { Power
ECM { Ground
Signal (“dummy”)
Signal (“dummy”)
ECM { Ground
ECM { Power
Signal

Air / Air Thermal Cycling

Test Condition: -40C to +125C, 1000 cycles, 15 minute dwell

Test Standard: JESD22-A104-B
IPC-TM-650-2.6.7

Preconditioning: Air bake, 125C, 24 Hr
Convection reflow, 250C peak (Pb free), 3X

Failure Criteria: Capacitance change > 10%

Test Results: PASS

Fabricator	Metal Layers	Dielectric Thickness	Number Boards	ΔC
A	4	16um	4	<3%
A	8	16um	4	<1%
B	8	16um	4	<3%
C	4	16um	4	<4%

ΔC = Maximum change in capacitance from initial to final measurement

Liquid / Liquid Thermal Shock

Test Condition: -40C to +125C, 1000 cycles, 7 minute cycle

Test Standard: JESD22-A106-A

Preconditioning: Air bake, 125C, 24 Hr
Convection reflow, 250C peak (Pb free), 3X

Failure Criteria: Capacitance change > 10%

Test Results: PASS

Fabricator	Metal Layers	Dielectric Thickness	Number Boards	ΔC
A	4	16um	4	<9%
A	8	16um	4	<1%
B	8	16um	4	<1%
C	4	16um	4	<2%

ΔC = Maximum change in capacitance from initial to final measurement

Life

Test Condition: **125C, 50 VDC, 1000 Hr**

Test Standard: **MIL-STD 833, method 1005**

Preconditioning: **Air bake, 125C, 24 Hr**

Failure Criteria: **Capacitance change > 10%**

Test Results: **PASS**

Fabricator	Metal Layers	Dielectric Thickness	Number Boards	ΔC
A	4	16um	2	<2%

ΔC = Maximum change in capacitance from initial to final measurement

TMA – Time To Delamination

Test Condition: 10C/min ramp, room temp to 260C

Test Standard: IPC-TM-650-2.4.24.1

Preconditioning: Air bake, 105C, 2 Hr

Failure Criteria: Time to failure < 5minutes

Test Results: PASS

Fabricator	Metal Layers	Dielectric Thickness	Number Boards	Time to failure
A	4	16um	1	7.47 mins*
A	4	16um	1	7.77 mins*
* Delamination occurred in FR4 layers				

THB

Test Condition: 85C, 85% RH, 9.5V, 500 Hr

Test Standard: JESD22-A101-B

Preconditioning: Air bake, 125C, 12-24 Hr

Failure Criteria: Insulation resistance < 10 Mohm

Test Results: PASS

Fabricator	Metal Layers	Dielectric Thickness	Number Boards	Minimum IR
A	4	16	5	>200 Mohm
B	4	8	1	>200 Mohm

Reflow Oven Testing

Test Condition: **Air reflow, 250C peak, 3X**

Test Standard: **IPC/ JEDEC J-STD-020B**

Preconditioning: **Air bake, 125C, 24 Hr**

Failure Criteria: **Capacitance change > 10%**

Test Results: **PASS**

Fabricator	Metal Layers	Dielectric Thickness	Number Boards	ΔC
A	4	16um	12	<2%
A	8	16um	8	<1%
B	8	16um	8	<1%
C	4	16um	8	<3%

ΔC = Maximum change in capacitance from initial to final measurement

Solder Float Test

Test Condition: 288C Solder pot, 10 second float, 6X

Test Standard: IPC-TM-650-2.4.13.1

Preconditioning: Air bake, 125C, 6 Hr

Failure Criteria: Visual inspection per IPC-6012A Section 3.6, MIL-PRF-31032

Test Results: PASS

Fabricator	Metal Layers	Dielectric Thickness	Number Boards	# Floats	Result
A	8	16	2	6	PASS
A	4	16	2	6	PASS
B	8	16	2	6	PASS
C	4	16	2	6	PASS

Solder Float Test
Detailed Inspection Results

Sample No.	A2/B2	C2/D2	E2/F2	G2/H2
Board Thick. (mils):	102	61	104	56
PTH Cu Thick. (mils):	1.3/1.3	0.4/1.2	1.4/1.4	1.6/1.6
Drill Hole Size (mils):	10	10	10	10
Aspect Ratio:	10:1	6:1	10:1	6:1
Desmear Type:	Plasma	Plasma	Wet Chemical	Wet Chemical
Lamination Type:	Sequential	Sequential	Standard	Sequential
Metallic Cracks:	None	None	None	None
Conductive Interface Separations:	N/A*	N/A*	N/A*	N/A*
Subsurface Imperfections:	0.0018 max	None	None	None
Pad Lifting:	.001 max	None	None	None
Resin Recession:	None	None	0.0004 max	0.0003 max
Hole Wall Pullaway:	10%	<5%	10%	None
Wicking:	.0005 max	.0005 max	.0004 max	.0005 max
Laminate Voids:	None	None	None	None
Etchback:	N/A*	N/A*	N/A*	N/A*
Resin Smear:	None	None	None	None
Negative Etchback (Cu):	N/A*	N/A*	N/A*	N/A*
PTH Cu Voids:	None	None	None	None
Nailheading:	None	None	None	None
*All .010" sectioned vias do not make electrical connect to interior layers of the board				
***Criteria are per MIL-PRF-31032, and are for 1X solder float (not 6X)				

Reliability Testing Conclusion

- 16 um results, like previous 8 um results, indicate that very thin, ceramic filled material passes standard industry requirements for:

Thermal cycle	***THB***
Thermal shock	***Reflow***
Life	***Solder float***
TMA	

Environmental Testing Summary

Test	*Property*	*Result*
High Temp (125°C/50V)	Capacitance Dissipation Factor (D.F.)	No Change (1000 hrs)
Thermal Cycle (-55/125C)	Capacitance/D.F.	No Change (2000 cycles)
Thermal Shock (-40C/125C)	Capacitance	No Change (1000 cycles)
TMA (T260)	Life	>5 minutes
THB (85C/85%RH/15 V)	Life Capacitance D.F.	>1000 hrs 10-15% Increase* 0.4% to 0.9%*
ESD (2-8 kV)	Capacitance/D.F.	No change
Bend Test	Capacitance/D.F.	No change (200 cycles)
Multiple Reflow (250C; 3X)	Capacitance	No change
Solder Float (288C; 3X and 6X respectively)	Capacitance/D.F PTH Quality.	No change Pass (MIL-PRF-31032)

***Returned to pre-test level after bake**

UL Testing

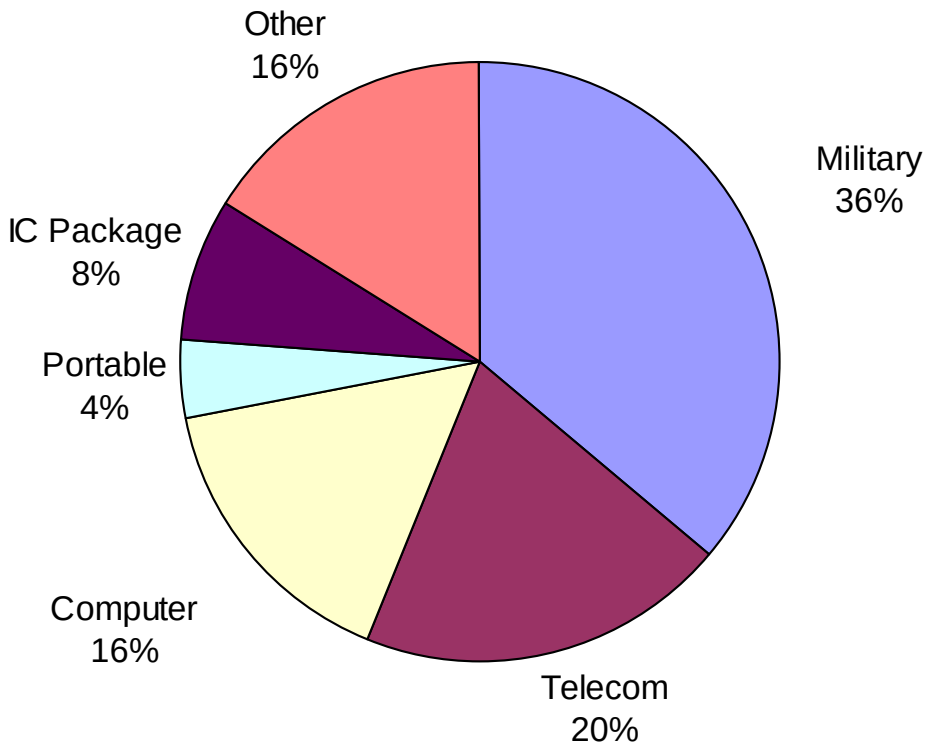
Test	*Property*	*Result*
Laminate	Flammability	94V-0
Laminate	Solderability Limits	288C/30 sec
Laminate	Relative Thermal Index	130C
Board	Flammability	94V-0
Board	Max Operating Temp	130C

Commercialization Status

Availability

- **Commercially released in April 2004**
- **High volume production capability in place**
- **Lead times (order-to-ship) < 5 days**
- **UL approval complete**
- **Fabricator base is increasing in size and expertise**
- **Several OEM's have internally qualified 3M Embedded Capacitor Material for potential use in their products**

OEM Evaluations by End Application



- OEMs include: Sun, HP, Delphi, Nortel, and IBM
- Large number of military applications/evaluations

Key Contacts

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