Simulation of Resonance Reduction in PCBs Utilizing Embedded Capacitance

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Introduction

The number of applications using Embedded capacitor technology on Printed Wiring Boards (PWBs) is increasing. One of the increasing applications using embedded capacitor is high-speed digital application and another is module for hand held devices.

For high-speed applications, design of Power Distribution System (PDS) is becoming challenging and solution for EMI is becoming more difficult. Traditional method to cope with these challenges was to use discrete capacitor components by optimizing component type, amount and location. As LSI technology scales to faster transistors and lower voltage, this traditional method is becoming ineffective, inefficient and costly. Embedded Capacitor technology has proven to be effective to overcome these issues by contributing to provide low impedance PDS and reduce EMI. In this paper, we have studied effectiveness of Embedded Capacitor using commercially available simulation software.

For module for hand held devices, the demand for higher HDI is endless. One of solution for higher HDI is to embed capacitor function inside PWB. Although there are various embedded capacitor materials proposed, the challenge still lies in the PWB fabrication to form uniform and reliable capacitor cost effectively. In this paper, we propose practical method of forming embedded capacitor and discuss what can affect tolerance of capacitance value.

Embedded Capacitor for High-Speed Digital Application

Power and Ground Noise Simulation

One of the major issues that electrical designers of high-speed digital equipment are facing is PDS and EMI. These phenomena are caused mainly by Power/Ground resonance noises. Many simulation softwares to support electrical designer have been marketed from various vendors. We have chosen EMISTREAM[1] developed by NEC corporations to investigate the impact of reducing Power/Ground resonance by PWB with embedded capacitor. EMISTREAM simulation is based upon SPICE model and provides accurate simulation of power and ground resonance noise in a short calculation time, around few minutes. The parameters that is required for the ground and power planes are, dielectric thickness, dielectric constant and thickness of copper.

Simulation results with discrete capacitor components

The design of the board for simulation was provided from NEC corporations. The board is constructed from 4 layers, 2nd and 3rd layer being used as a power and ground layer. As a default design, 0.6mm FR-4 (Dk=4.6) with 1oz copper was used as a power and ground layer. 35 decoupling capacitor components (0.1uF) were mounted on the surface to supply power to LSIs.

Figure 1 shows the power/ground resonance simulated result using default design. Excitation point (source of noise) was chosen at LSI indicated as U2 in the figure. The magnitude of noise level is listed in Figure 1 as well. As you can see from the figure, there are areas where significantly high noise area resulted from power and ground resonance, higher than 0 dB is colored in red, are observed. With conventional method of placing capacitor components on the surface, it is necessary to decide the type, amount and location of capacitor components. Figure 2 is the result of placing minimum amount of capacitor components to reduce the resonance voltage to below 0dB. Although it was possible to achieve 0 dB by adding 44 capacitor components (all 0.1µF), it was necessary to violate the placement location in the circled area of the Figure 2. In this circled area, since LSI is already mounted, it is necessary to mount capacitor components on the back side of the board, which will cost additionally for surface mounting.

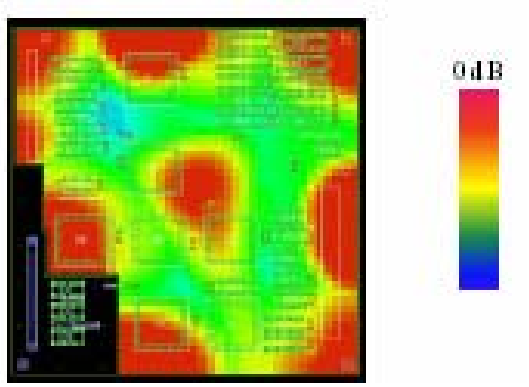

Figure 1 - 0.6mm FR-4 (Dk=4.6) Used as P/G Plane (Red>0dB)

Figure 2 - 0.6mm FR-4(Dk=4.6) with 44 Additional Capacitors (Red>0dB)

Simulation Results with Embedded Capacitor

Next, we have selected a set of embedded capacitor materials as listed in Table 1 to substitute as a power and ground plane. The embedded capacitor material has thickness range of 8 to 24µm and Dk ranging from 4.4 to 30. This Embedded capacitance materials, *FARADFLEX*, are commercially available and used in volume for high-speed digital applications. The detail material properties and processing are described in previous publications.[2,3]

First we have conducted a simulation using parameters of BC24, dielectric thickness 24µm, Dk=4.4. Simulated result is shown in Figure 3. The result showed that power/ground resonance can be reduced dramatically without any additional placement of capacitor components and achieve 0dB noise level.

Table 1 - Properties of Embedded Capacitance Material

Property	Unit	*FARADFLEX*					
		BC24	BC16	BC12	BC8	BC12TM	BC16T
Dielectric Thickness	µm	24	16	12	8	12	16
Cp @1kHz	pF/cm^2	190	260	310	500	660	1700
Dk @1kHz	-	4.4	4.4	4.4	4.4	10	30
Df @1kHz	-	0.015	0.015	0.015	0.015	0.019	0.019

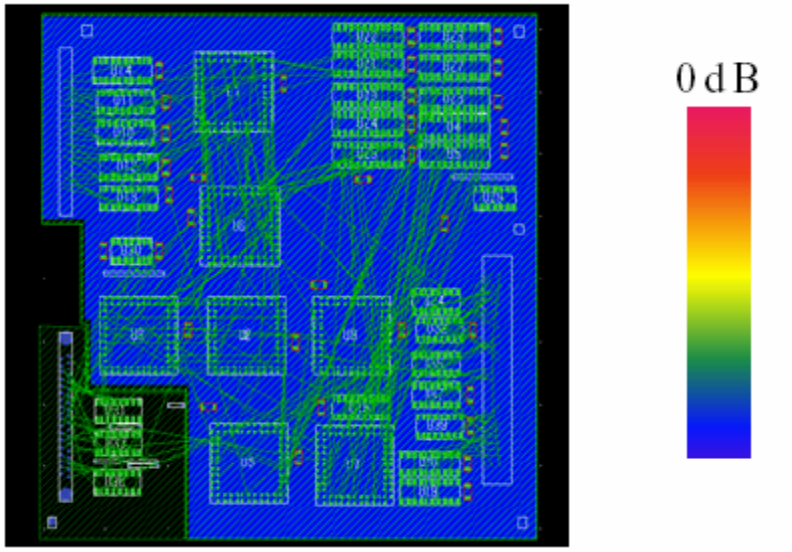

Figure 3 - BC24 (Dk=4.4) Used as P/G Plane

This implies that not just much less noise level can be achieved using embedded capacitor used in the power and ground planes but possible solution for reducing cost by eliminating surface mount capacitors.

In this case, total of 44 capacitors was able to removed from this board, of which is equivalent to 1100 capacitors per square meter.

For certain high-end application, achieving 0 dB is not enough, but requires as low as –26 dB noise level. This is due to less margin allowance resulted from lower operating voltage of LSI. It is generally said that allowed voltage fluctuation is 5%. This is –26dB noise level as calculated in following formula.

dB = 20*LOG(0.05) = – 26

Figure 4a shows a result with the default condition (P/G 0.6mm FR-4, Dk=4.6) with 44 additional capacitor components. The whole board area showed noise level of higher than –26dB. In this case, it was impossible to reduce noise level less than –26dB by adding capacitor components.

Figure 4b and Figure 4c shows a result with BC24 and BC12TM used as power and ground planes without any additional capacitor components other than 35 default capacitors. With BC24 used in power and ground planes, it was possible to achieve –26dB noise level. With BC12TM in use, much less noise level was achieved. This result implies that in the application where it requires very low noise level, traditional placement of capacitor components becomes obsolete and the role of embedded capacitor technology becomes important.

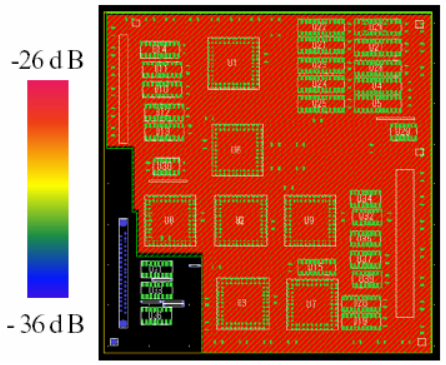

Figure 4a - 0.6mm FR-4 (Dk=4.6) used as P/G plane

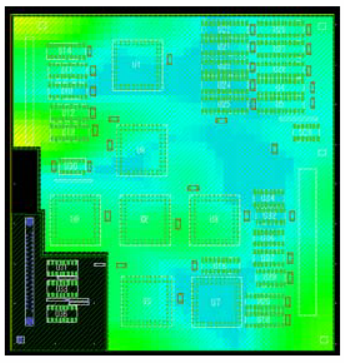

Figure 4b - BC24 used as P/G plane

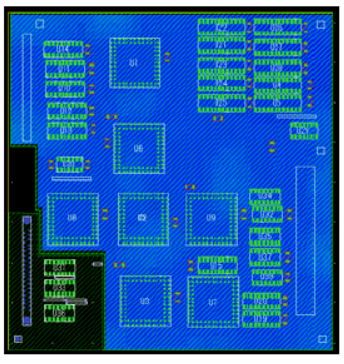

Figure 4c - BC12TM used as P/G plane

Influence of dielectric thickness of embedded capacitor

In order to understand what property of embedded capacitor affects the power/ground noise level, simulation was conducted to see the impact of dielectric thickness of embedded capacitor material. As shown in Table 1, by comparing embedded capacitor material with same Dk value and different thickness, BC24, BC16, BC12 and BC8, influence of dielectric thickness can be observed. In Figure 5, maximum voltage noise level in each frequency from 1MHz to 1GHz is shown. With 0.6mm FR-4 used in P/G plane, even with additional capacitor component placement, it was difficult to achieve less than –5dB. With embedded capacitor material used in P/G plane, -26 dB was easily achieved. It was found that the thinner the embedded capacitor material being used, the lower noise level was achieved. For instance, at resonance noise around 550MHz, noise level of PWB using BC24 was around –30dB, BC16 –38dB, BC12 –42dB, BC8 –50dB respectively. This implies that by selecting appropriate thickness embedded capacitance material, target noise level can be achieved.

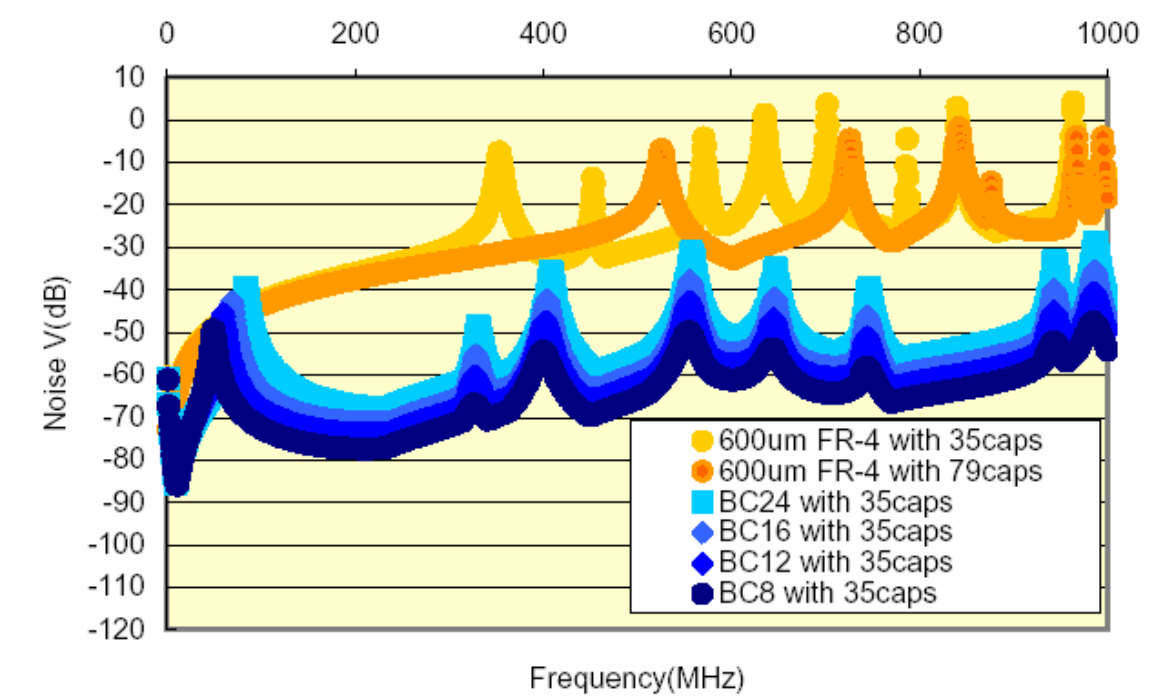

Figure 5 - Maximum Noise Level at each Frequency Using Different Thickness of Substrate Used in Power and Ground Plane

Influence of Dielectric Constant of Embedded Capacitor

Another approach is to use higher Dk embedded capacitor material on P/G plane. In Figure 6, maximum voltage noise in each frequency from 1MHz to 1GHz is shown. There are two sets of comparison shown in this Figure. First set is a comparison between BC12 and BC12TM, in which both materials have same thickness of 12µm but have different Dk of 4.4 and 10 respectively. In this comparison, not just suppression of noise was observed with higher Dk material, but shift in resonance frequency was observed. Second set of comparison was between BC16 and BC16T, in which both materials have same thickness of 16µm but have different Dk of 4.4 and 30 respectively. In this case too, with high Dk material, suppression of resonance noise and shift in resonance frequency were observed.

From above results, using higher Dk material has merit of reducing noise level and shall be useful to alternate the resonance frequency to avoid interference with specific frequency of interest without changing the thickness of P/G plane.

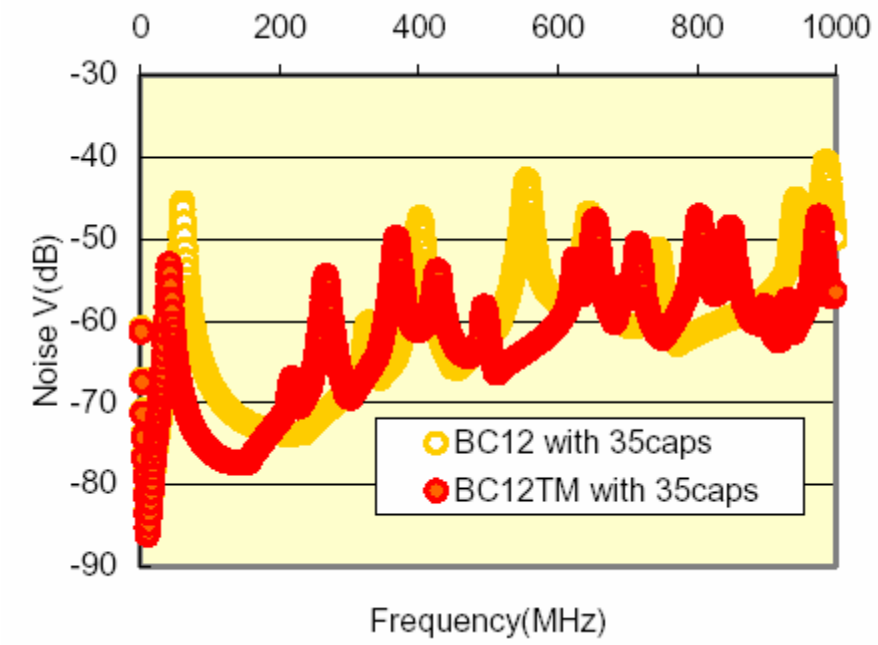

Figure 6a - Maximum Noise Level at Each Frequency of Different Dk Material, BC12 and BC12TM Used in Power and Ground Plane

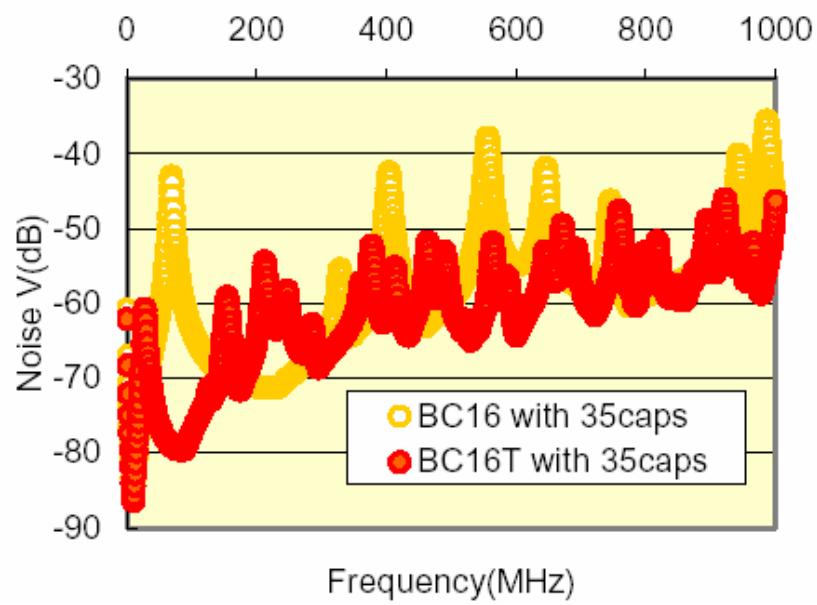

Figure 6b - Maximum Noise Level at Each Frequency of Different Dk Material, BC16 and BC16T Used in Power and Ground Plane

RCF Type Capacitor Material and it's Processing for Module/SiP Application

One of the important issues of forming embedded capacitor for module application is uniformity of capacitance. We have developed a practical and economical process using RCF type capacitor material.

RCF capacitor material is prepare by mixing high Tg epoxy resin with high Dk ceramic nano powder and uniformly coated the mixed resin on the very low profile copper foil. It is supplied in B-stage as standard RCF for HDI application and it is very easy to laminate with core materials and to form thin high Dk capacitor layer inside FR-4 multi-layer PWB boards. Though it has relatively high ceramic content, the high Dk dielectric material shows enough insulation resistance, heat resistance and robustness required for standard PWBs. The material is also free from any halogenated substance in which may cause environmental hazard and is available within a thickness range of 8 to 16 µm. No special refrigerated storing condition is required. (See Table 2.)

Table 2 - RCF Type Capacitors[4]

Characteristics	Condition	Unit	MC16TR	MC12TR	MC8TR
Capacitance	1kHz	pF/mm^2	17	22	33
Df	1kHz	N/A	0.019	0.019	0.019
Dielectric Thickness	Nominal	μm	16	12	8
Dk	1kHz	N/A	30	30	30
Peel Strength	IPC M-650 2.4.9	kN/m	>0.7	>0.7	>0.7
Thermal Stress	@ 288℃	times	>10	>10	>10

Formation of Singulated Capacitor with Sand Blasting Process

Although thin and uniform high Dk dielectric layer is formed inside PWB by laminating RCF capacitor on the core materials, in order to utilize this layer as singulated capacitors, we need to formulate appropriate size of the capacitor to realize necessary capacitance, then, electrically connect the capacitor with other devises, and encapsulate the capacitor to protect from various environments. Especially, to increase the rate of utilization of the precious boards area and allow more freedom for board designers, removal of unnecessary high Dk dielectric is very important. There are several methods historically utilize to remove unnecessary resin in PWB industry. They are laser ablation, plasma etching, dissolving by organic solvent and degradation by desmear solution. Authors had actually done several attempts with some of the above traditional methods. However, we had reached a conclusion that sand blasting process (also called as Jet scrubbing or Wet blasting), is the easiest, the most economical and the most environmentally friendly process. Sand blasting machines are also very popular in PWB industry for mechanical surface cleaning process and many board shops are already equipped with sand blasting machine of which can be converted into the process of removing high Dk dielectric.

Figure 7 shows the process with sand blasting. As curing rate of high Dk dielectric is adjusted almost similar as FR-4 prepreg, standard FR-4 press profile can be generally used for lamination process. The thickness of dielectric is substantially stable and unchanged during and after lamination, because the flow of RCF capacitor is almost nothing through the lamination process. Upper electrode is formed by etching process, and the upper electrode act as a resist while the board is being sand blasted. After sand blasting, lines and vias can be formed by standard HDI process.

As described, RCF capacitor does not require any special equipments or machinery to process, therefore we believe this is the easiest, the fastest and the most economical way to embed capacitor inside PCBs and/or packages.

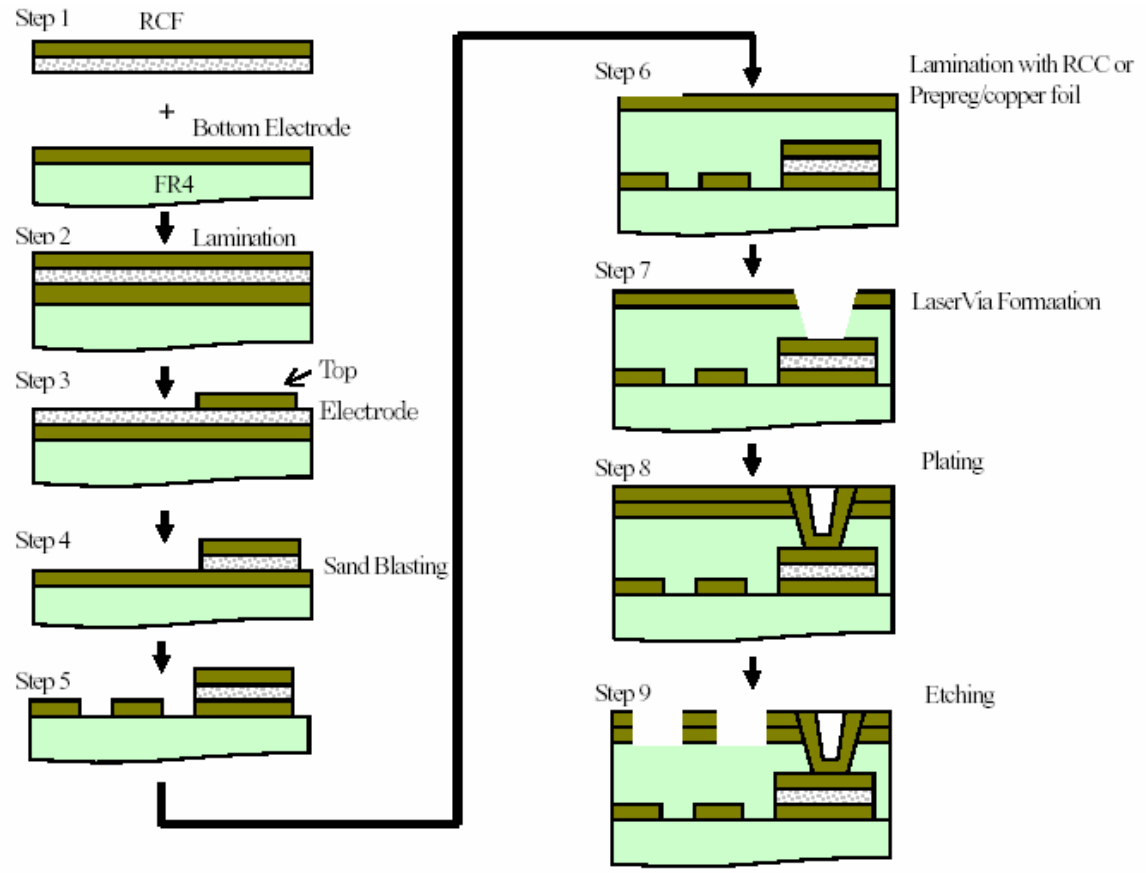

Figure 7 - Capacitor Embedding Process Using RCF Capacitor Material and Sand Blasting Method

Capacitance Tolerance Study of RCF Capacitor

Capacitance Measurement

For embedding singulated capacitors, one of the most important performances that need to be achieved is a capacitance tolerance. Application such as bypass capacitors may allow +/-20%, but applications such as for filter may require +/-5%. In order to achieve these tolerances, it is very important to understand how to control the tolerance by embedding capacitors.

Test was conducted to investigate tolerance of capacitor formed by using RCF capacitors. Various sizes of capacitors, from 0.0625mm2(250x250µm) to 4mm2(2x2mm), were formed using test vehicle shown in Figure 8. Capacitance measurement was conducted using flying probe capacitance measurement equipment.[4] Measurement result is shown in Table 3. Regardless of the size differences, all of the capacitors were in less than 10% variation.

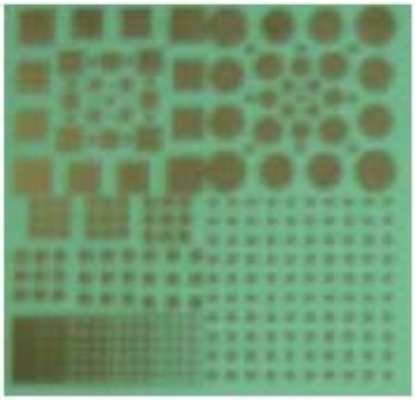

Figure 8 - Capacitance Pattern

Table 3 - Results

Cap. size(mm^2)	Measurements	Tolerance %
0.0625	576	8.9
0.25	15696	5.5
0.5	576	2.9
1	576	2.9
2	576	2.4
3	1152	2.3

Discussion of capacitance tolerance

The tolerance of capacitance is determined by mainly two reasons. One of the variations of capacitance is due to un-uniformity of capacitance material itself and another is variation associated with etching variation when forming electrode for capacitors. The total tolerance of capacitance can be expressed in following equation.

Total tolerance of capacitance (%)
=V1 (Capacitor material variation, thickness, Dk) + V2 (Etching pattern variation) eq.1

V2 can be expressed in functions of D(Target electrode size in mm) and d(Etching variation in µm)

Expected tolerance of capacitance (%)
= V1 (Variation by dielectric coating) + V2 (((D+d)*(D+d)-D*D)/D2/106*100) eq.2

With this equation, expected capacitance tolerance can be calculated depending on the size of target capacitor electrode and etching variation. Figure 9 shows the simulated results of expected capacitance tolerance in the case of +/-5% capacitance material variation. Each simulate line indicates variation in certain etching variation. For instance in Figure 9, with capability of etching patterns in +/-5µm (circle plot), it is assumed that +/-6% can be achieved when forming 1mm2 capacitors and +/-8% can be achieved when forming 0.1mm2 size capacitors. In the case of etching capability of +/-15µm (square plot), the expected tolerance would be worse, +/-8% at 1mm2 size capacitors and +/-14% at 0.1mm2 size capacitors. From these results, not only the uniformity of capacitance material is important to achieve tight tolerance, but also etching capability is important, especially in forming small size capacitor.

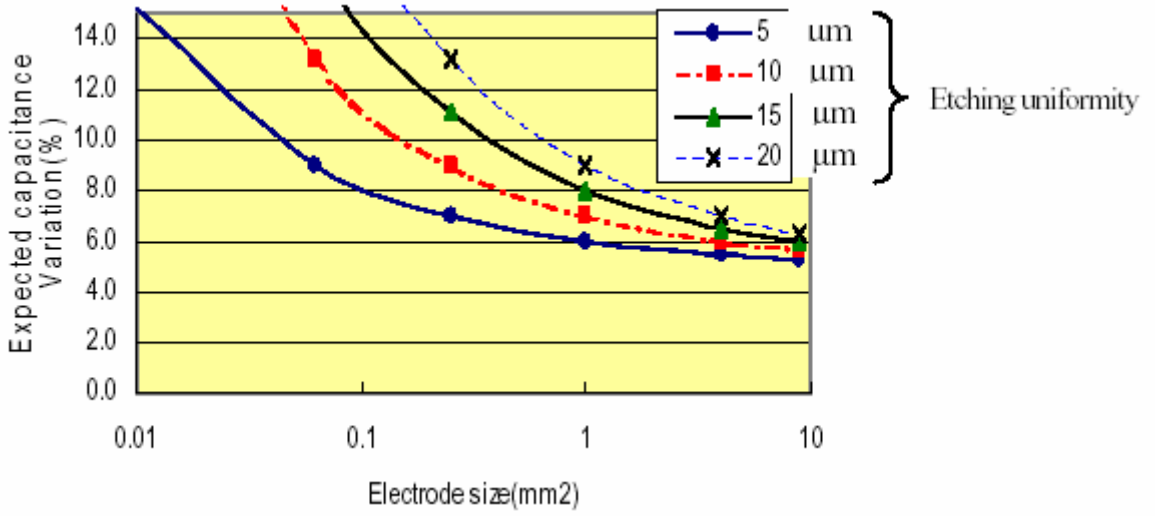

Figure 9 - Simulation Result of Expected Capacitance Tolerance

Comparison between simulated result and measurement result

Test was conducted to compare simulated result and actual tolerance of capacitors in different capacitor sizes. The capacitor material used in the test was MC16TR with 12micron Cu. In Figure10, it shows actual measured tolerance result from

capacitance size of 0.0625mm2(250x250µm) to 4mm2(2x2mm). Actual measured capacitance tolerance matched quite well with simulated result using +/-7µm as an etching variation. This implies that etching capability of PCB manufacturer where this test board fabricated has an etching capability of +/-7µm.

In this case, +/-10% tolerance was achieved at the capacitor size even as small as 0.0625mm2 (250x250µm).

Each PCB manufacturer should have different etching capability. Once etching capability of PCB facility is known, it is possible to estimate what the expected tolerance of capacitance at each capacitor size would be using the calculation method described here.

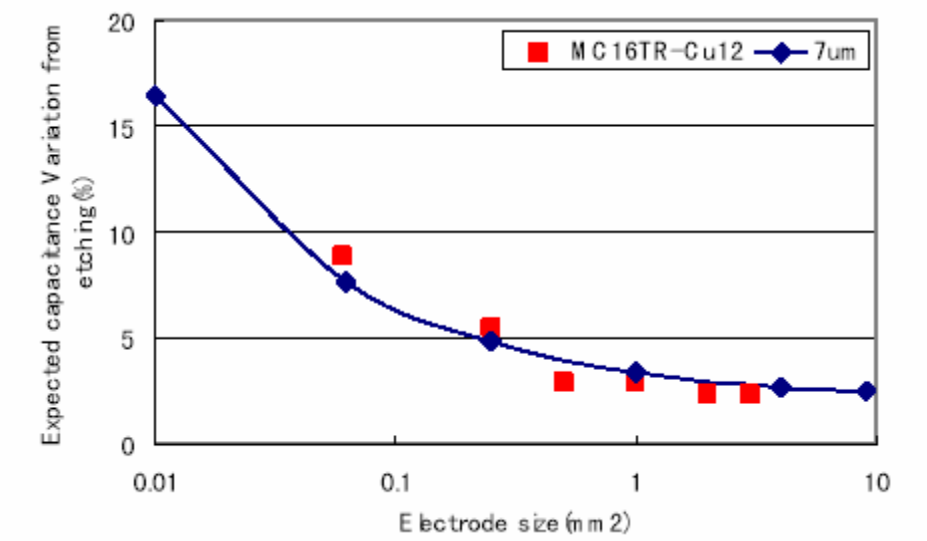

Figure 10 - Comparison of Actual Result with Simulation Result

Conclusion

For high-digital applications, usage of embedded capacitance in power and ground plane was proven to be very effective to reduce noise by simulation software, EMISTREAM. As LSI speed increases and as operation voltage decreases, embedded capacitor PWB technology can offer cost effective solution to meet the requirements. By using simulation tool like EMISTEAM, electrical designer can easily understand the advantage of using embedded capacitor in PWBs to reduce power and ground noise and improve power distributions. We hope these simulation tool will accelerate the usage of embedded capacitor for PWBs.

For forming singulated type capacitors, we have demonstrated that RCF type capacitor material with sand blasting process would be practical, reliable and economical method. To form uniform capacitance, not just uniformity of capacitance material is important, but etching uniformity plays an essential role especially when forming small size capacitor.

Acknowledgement

We appreciate Dr.Tint of HDI solutions for cooperation of capacitance measurement.

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