A Low Cost Option to Laser Trimming of Resistors

Dennis Fritz, Dave Sawoska, Frank Durso and Ted Martin
MacDermid, Inc.
Waterbury, CT

This paper is the second concerning the use of existing electrical test equipment being programmed to first measure the values of plated additive resistors manufactured on circuit board inner layers. Next, this value information is programmed into the software of a laser routinely used to drill microvias for circuit boards. A computer routine calculates the amount of the resistor that needs to be removed to adjust each resistor to the required design value. The trimming is then conducted on the actual inner layer.

Advantages of this technology include eliminating the manufacture of probe cards for each new circuit design, and utilizing existing machines for this new technology task. While accuracy of trim with this "off-line" machine may not be quite as precise as active trimming with probe cards, the accuracy is sufficient for many of the 5-10% resistor values needed for such design applications as digital signal termination. Plated additive resistors, with their uniform thickness across each resistor, are particularly easy for this technology combination to trim.

Background

Embedded resistors have been used in circuit boards for over 20 years. Embedded resistors have traditionally been fabricated at values of plus or minus about 15% of nominal resistance. While this is not the same accuracy as surface mount resistors, some OEMs have been able to design products where this accuracy is fine.

However, in the last three years interest has been expressed in trimming these resistors to values more accurate than those "as produced". Laser trimming of resistors is well known, as surface mount resistors are typically trimmed to value, while still in the format of mass production. Probe cards are typically used in this application, as these probe cards easily and rapidly trim sheets of "all the same" resistors in mass production.

The location of embedded resistors on circuit board inner layers does not usually follow a grid pattern, standard when resistors are mass-produced. Resistors embedded in circuit boards are located near the electrical components in their net. This means that embedded resistors are not in arrays that are easily probed with cards. As an alternative, "flying probe" resistor test technology has not yet been commercially demonstrated for large format epoxy circuit board inner layers. While the technique is well developed for ceramic circuits, the much larger format of organic boards presents a major machine modification problem.

While circuit board innerlayers are more commonly optically inspected before lamination, full electrical test is easily done on these same layers. Finished bare circuit boards are routinely electrically tested, with data accumulation of resistance values in various circuit nets. Establishing the desired electrical resistance measurements for embedded resistors is done interactively with the plotted artwork of the inner layer through simulation of laser trimmed resistor values.

Thus, the investigation of this report was undertaken – to see if commonly available PWB electrical test equipment and laser microvia drilling equipment could be used in combination to trim embedded plated additive resistors for circuit boards.

Summary of Prior Work - Scouting Runs

During the initial scouting runs, the following problems were identified when using a laser microvia-drilling machine to trim resistors:

1. Cut smoothness
2. Absolute location
3. Machine problems
4. Software problems
5. Correct energy for trim, without damaging resin
6. Non-uniformity across laser spot for this application

The following was done to improve the test vehicle and give better test results:

1. Decrease travel between pulses – more overlap, correct beam energy.

2. Fix software issues and recognize machine table limitations.
3. Insure data portability, DXF and Gerber software version compatibility.

This paper will continue to demonstrate methods to solve these problems.

Program Test Parameters

To demonstrate the combination of independent electrical test and laser trim, a desirable circuit geometry was selected, and incorporated into a test vehicle of "four-up" circuit boards with repeating resistor designs (Figure 1). The size of the circuit board chosen was 125mm by 175mm, and the boards were manufactured "four–up" in a panel size of 400mm by 600mm. Nominal resistor size was from 1.6 x 3.2 mm down to
0.3 x 0.6 mm. – the dimensions are given in the resistor labeling.

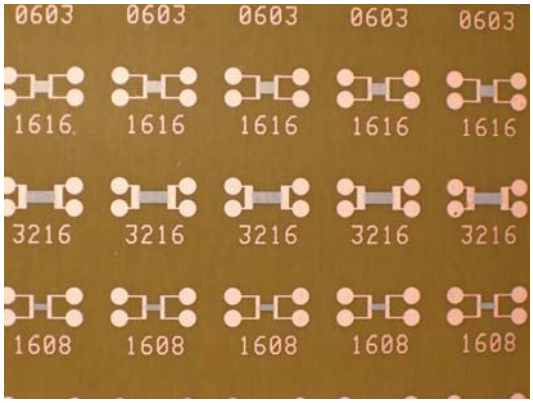

Figure 1 – Test Panel Section

A fiducial location system was set up at the corners of the panel for alignment of the microvia drilling laser and the electrical test fixture. In this test, the global fiducial system served as the orientation for both the probe testing and the laser activation. In final practice, it will be desirable to have a fiducial system that is more localized.

Next, a software routine for laser trim was developed, based on mathematical modeling of the electrical results expected upon trimming. Since the trim is not interactive, it is possible to set the trim to minimize the plunge cut effect on cross sectional area. Also, the plunge cut undertaken was set at some distance from the terminations, also to minimize resistor-heating effects. Since the cut is mathematically derived, the "L" cut is frequently longer than would be expected in an interactive cut. Figure 2a is a picture of the graphical model of the trim undertaken on 1.6x1.6mm resistors, and Figure 2b is a picture of the graphical model of the trim undertaken on 3.2x1.6mm resistors. Both of these figures show the electrical path expected after trim.

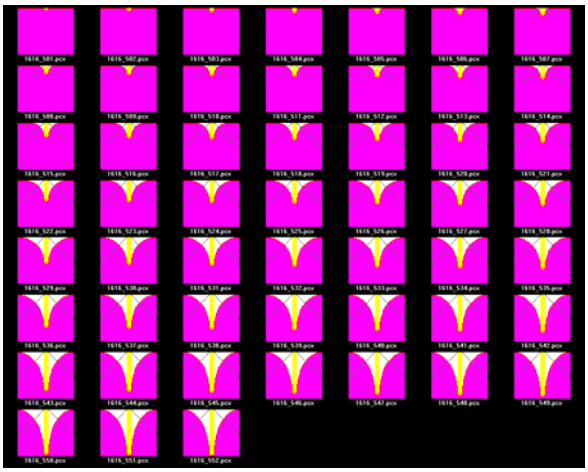

Figure 2a - Modeling of Trim of 1.6x1.6 mm Resistors

Figure 2b - Modeling of Trim of 3.2x1.6 mm Resistors

Key undertakings of the trim model were as follows:

1. Evaluating the dimensions of the "L" cut to get the resistor value desired (see Figures 2a and 2b).
2. Modeling of the spot size for trim – based on the capabilities of the laser drill.
3. Modeling of the travel of the pulsing laser source to determine movement between each pulse.
4. Modeling of the desired resistor starting value range to give acceptable final resistor values.
5. Summarizing parameters for the laser via drill to cut the resistor to give the desired value.

Algorithm Development

The process requires some basic information and data for the algorithm to proceed without problems.

1. The co-ordinate location of all resistors to be trimmed and their orientation - this is obtained from the Board Design.
2. The length and width of each format resistor - this is obtained from the "Parametric Design" from the CAD tool.
3. The starting value of each resistor with a key to the co-ordinate location - this is obtained from the measurement of the initial value, based on electrical test reading.
4. The resolution limits for the laser trim table - this is developed from the experience with each laser drill. It can be quantified based on drill model number after several installations of the same equipment are made.
5. Fiducial locations on the Gerber for proper alignment to the pinning system - this is now given from the software source, but may be optimized at each shop and with each board design.
6. The desired resistor value for each resistor or set of resistors - this is from the schematic that generates the layer design.
7. The actual diameter of the cut that the laser is tuned to create. Right now, this is based on experience with individual lasers. However, this should become standard with more installations.

The system uses a proprietary algorithm to calculate the 'Plunge' cut and 'L' cut that will give the desired resistance and use the minimum length of 'Plunge' cut to reduce the effect of hot spots and non-linearity.

A file is created for each side of each panel that has resistors to be trimmed. The cut for each resistor is individually calculated by the program using the pre-measured resistance, the custom algorithm, and a set of look-up tables that provide information for each resistor size and format. This results in the closest final resistance to the desired value with a single set of resistance readings.

This file, when fed to the aligned laser co-ordinate system, will instruct the laser where to start each cut and how to proceed with each cut for the associated panel.

A given panel type needs to be set up the first time that it is run to link the proper files and tables needed for the different resistors and their placements.

The system is currently a work in progress based on an algorithm that has shown itself to be highly responsive, versatile and accurate.

Microvia Drilling Equipment

Existing laser microvia drilling equipment – a custom designed machine at Photomachining, and an ESI unit at Tech Circuits both successfully were "turned down" to the intensity needed to ablate thin films of embedded resistors, such as those from

the plated additive technology. This drilling equipment does not significantly decompose the epoxy underneath, or alongside, the resistor plating.

Plating can successfully give a consistent deposit across inner layer panels, as shown by the “as plated” data (Figure 5 and 6 before data). Also, the use of existing laser microvia drilling equipment has shown the capability to trim resistor formulations, such as plated additive resistors, to an accuracy of about 7%.

Global Alignment

The global alignment format is accurate to 25 microns, giving an expected trim accuracy of 8% on the smallest resistors (2% on the largest 3.2x1.6mm) and a 3% final error due to resistor plating. This total could be as much as 5% on the larger resistors used in this study.

The same Gerber plot of resistor locations gave the test points for the electrical test equipment. Many of the resistor pictures here will show the mark from either manual or automated test probes. All resistor terminations could be tested with the ECT equipment, using a standard probe test fixture.

Figure 3a and b show the 1.6x1.6 resistor before and after trim, and Figure 4a and b show the actual 3.2x1.6 resistor before and after trim.

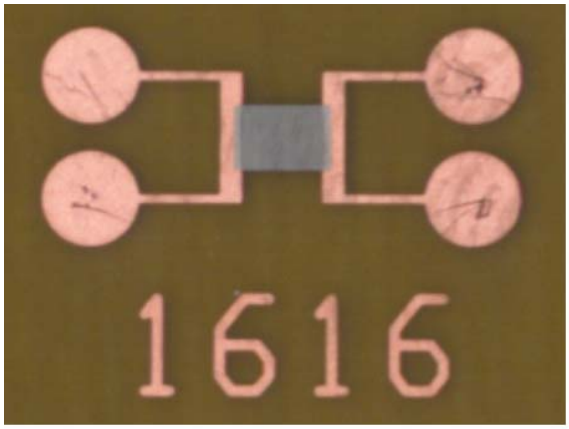

Figure 3a - 1.6x1.6 Resistor before Trim

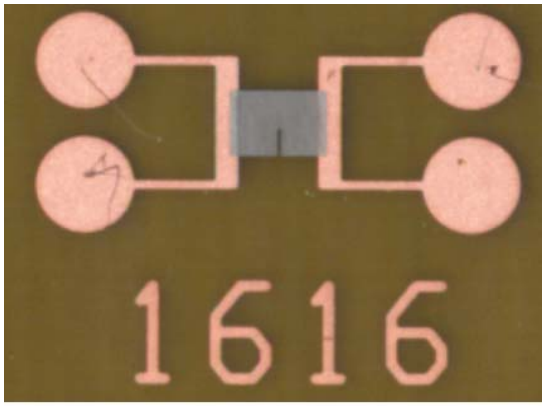

Figure 3b - 1.6x1.6 Resistor after Trim

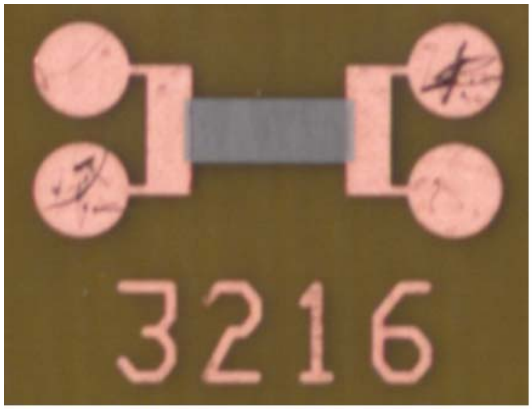

Figure 4a - 3.2x1.6 Resistor before Trim

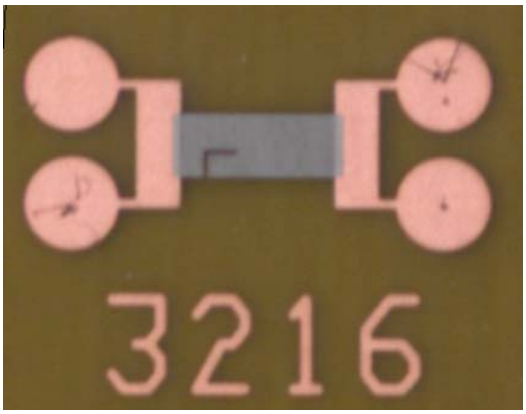

Figure 4a - 3.2x1.6 Resistor after Trim

First Trial Run

Statistical plots of the values of the initial run of trimmed resistors are shown in the plots.

Figures 5 and 6 contain electrical test results from an Everett Charles A6S before and after trim to a depth of about 0.5 mm. This was compared to the measured electrical starting and ending values of these resistors.

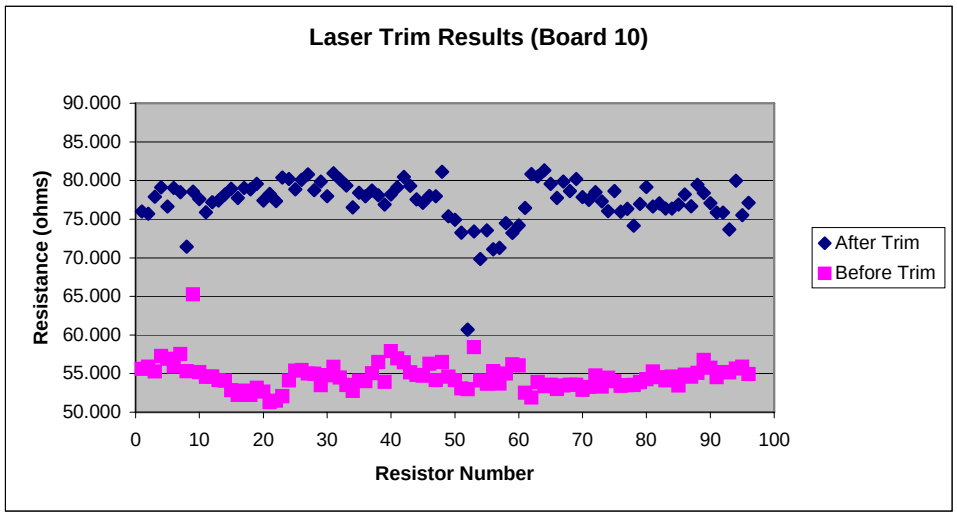

Figure 5 – Results for Board 10 – 55 Ohm Resistors Trimmed Up – Target 75 ohms

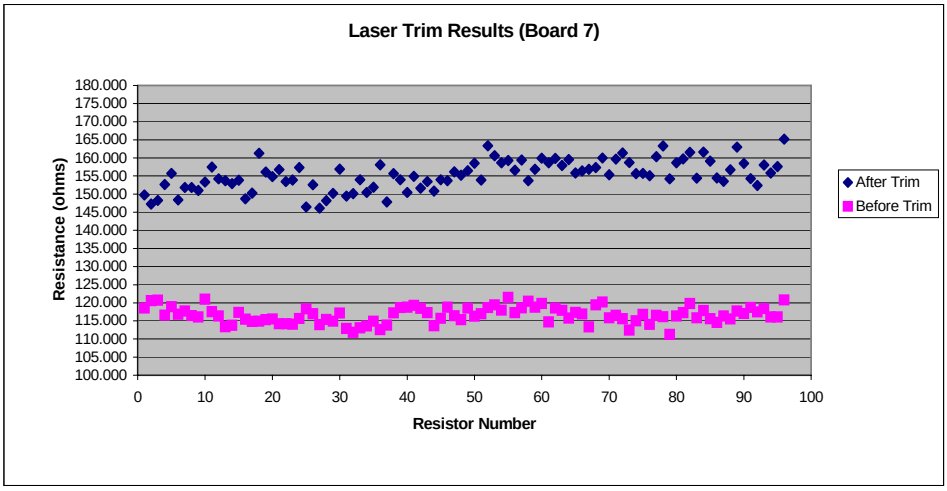

Figure 6 – Results for Board 7-110 Ohm Resistors Trimmed Up – Target 150 Ohms

Second Trial Run

A second trial run was made with improved tooling holes and an optimum alignment of the resistors on the test panels. The results were significantly improved, as shown in the Figures 7 and 8.

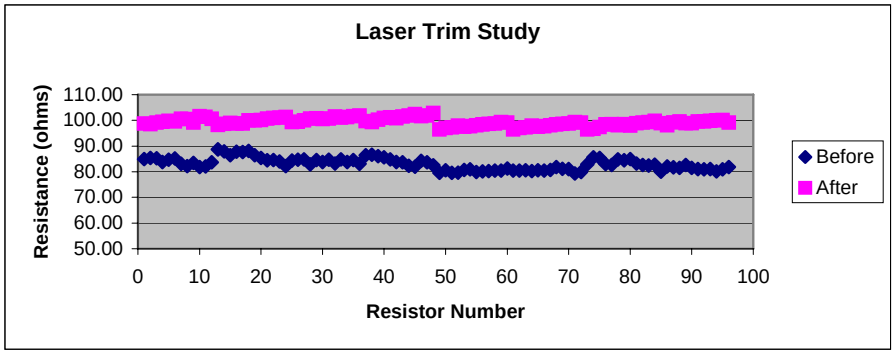

Figure 7 - Second Trial Run, before and after Trim – Target 100 ohms

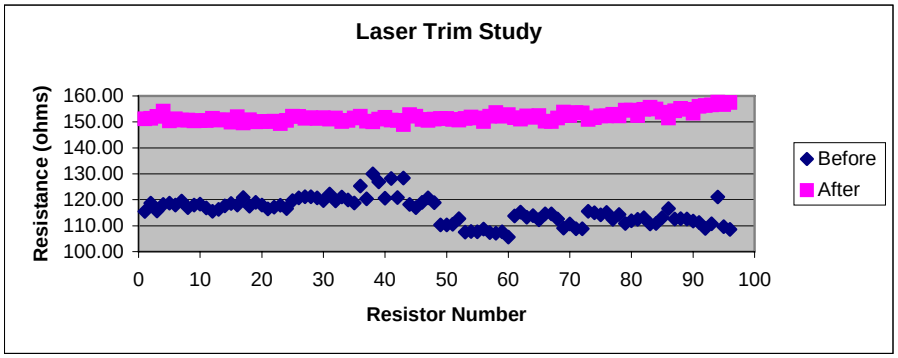

Figure 8 – Second Trial Run, before and after Trim – Target 150 ohms

Laser Trim/Electrical Test Summary

The results of the laser trim runs show that:

1. The principle of using existing circuit fabrication equipment for resistor laser trim was demonstrated as feasible.
2. Accuracy is reasonable for the beginning test work – trim to about 5 % accuracy.
3. The plan to improve the accuracy by exploring both location/fiducial issues, and by improving the laser operation in this application was successful.
4. The system is ready for field test by an interested board fabricator.

Plan Forward

Existing printed wiring board microvia drilling and electrical test equipment has been shown capable to produce trimmed resistors in the accuracy range of 5-9% range. This is better than a previously expected “as manufactured” range of 15%

It is intended to solicit a field evaluation of the resistors trimmed with the “in-house equipment” process. The key piece of that demonstration will be functional operation of the electrical device, based on resistors more accurate than those “as plated”. However, these resistors are not expected to have the accuracy of purchased surface mount discrete components.

The marketing plan for the software for this “in-house trimming” of embedded plated additive resistors is being determined. It is expected to be made publicly available.

Acknowledgements:

Tech Circuits, Wallingford, CT

References

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