A Study of Implementing Lead free Soldering Process with Organic Solderability Preservative Coating In a High Volume Production Environment

Michael Yuen
Foxconn, CMM-AMBD
Houston, TX

Rockey Q. Luo
Foxconn, CMM-AMBD
LongHua-Shenzhen, China

Abstract
As the global electronic industry marches toward the brave new world of environmentally conscious electronic manufacturing, lead free soldering has made some fundamental shifts in the processing approaches to print wired assembly (PWA). With the popular adoption of Tin Silver Copper (SAC) alloys, advancements have been made in packaging designs, soldering materials, processing equipment, and surface finishes. Historically, Hot Air Solder Leveling (HASL) has dominated the PWB market as the preferred choice for many applications. In recent years, Organic Solderability Preservative (OSP) and some precious metal finishes, namely immersion Silver and Immersion Tin, have regained momentum in Lead free electronic assemblies. Although OSP has been used in electronic assembly for over 25 years, the conversion of Lead free technologies has presented some unique challenges to manufacturability, testability, and reliability. The focus of this article is to explore the challenges posed by OSP in a high volume, Lead free production environment and how different techniques can be utilized to optimize and improve the process windows.

Introduction
The drive for green electronics started gaining momentum in Japan during the 90s, and is slightly ahead of the Restriction of Hazardous Substance (RoHS) directive which is becoming a household buzz word within the electronics community. Published reliability data and characterization efforts have mostly supported the selection of 96.5% Tin 3.0% Silver 0.5% Copper (SAC 305) alloy for Lead free application in recent years. Understanding the impacts of increased process temperatures on soldering materials, laminate materials, and surface finish is paramount to a smooth transition into manufacturing RoHS electronic products. For surface finish, one study shows the combined use of OSP in Asia grew more than 25% in the 90s making it a major player early on in the far-east. Low process complexity and cost effectiveness make OSP an attractive alternative for the many RoHS assemblies. Should the current trends continue, the projection is that OSP will remain a strong contender in the years to come.

As aforementioned, OSPs are nothing new to electronics manufacturing. By the same token, the OSP process challenges faced by the electronic manufacturer are not completely new. In fact, numerous technical articles have documented the pros and cons of OSP finish. Table 1 summarizes the basic pros and cons of OSP finish.

Table 1 - Pros and Cons Summary of OSP Finish

OSP Pros	OSP Cons
• Provides coplanar surface for soldering fine pitch devices • Solid solder joint strength compared with other finishes • No significant long term reliability risks associated with coating • Acceptable solderability when processes and soldering materials are properly optimized and controlled • Most cost effective compared with popular Lead free finish alternatives • Ease of recoating and reworking without extreme thermal excursion	• Challenging to achieve desired barrel fill for plated through hole (PTH parts), especially after multiple reflow cycles in normal atmospheric conditions • Time between processing can impact solderability • Testability issues remain for probing bare copper • Sensitive to handling • Limited shelf life compared with alternative finishes • Cleaning misprinted PCB can degrade the coating integrity • Interleaving paper needed to lower the risk of abrasion damage between stacked PCBs • Provides poor surface contact for wire bonding and RF applications • Difficult to detect imperfections or solderability issues visually prior to processing • Finish integrity can be at risk with baking process

OSP Quality

The first step to implement a robust OSP oriented manufacturing process is to control the coating quality. For the newer generations of OSP, the combination of Benzotriazole (BTA) and Imidazole are being modified to allow increased thermal resistance for multiple reflow cycles at higher temperatures. If not controlled properly, there can be concern of cleanliness reliability issues when using some rosin/resin-based OSP coatings (prefluxes). Hence, statistical process control (SPC) must be in place to monitor and control all critical process parameters during the board fabrication process.

Depending on the chemistries selected by the PCB fabricators, high temp OSP coating can typically range from 0.2 to 0.6 micron. If the thickness is too high, the excessive coating can be difficult to remove during soldering. For insufficient coating thickness, oxidation on under-protected copper surfaces can impair solderability, especially after multiple reflow cycles. Since incoming inspection cannot measure the coating thickness effectively, board houses are required to submit thickness measurements using specialized test coupons to ensure constant thickness. Besides coating thickness, uniformity is an equally important attribute; Figure 1 shows the random discoloring of OSP at PTH locations after only one Lead free reflow. It is recommended that PCB houses to take samples and simulate at least one Lead-free reflow cycle to visually verify if there is any localized discoloring at final inspection.

Although OSP has been considered as safer than other surface finishes, cleanliness and soldering material compatibility should still be validated and monitored closely. Similar to other surface finishes, if the OSP process is not being controlled and monitored properly, OSP can be a nightmare for both reliability and solderability. Figure 2 shows an example of corrosion on a test vehicle after accelerated aging. The root cause is determined to be the residues left behind from the etching process.

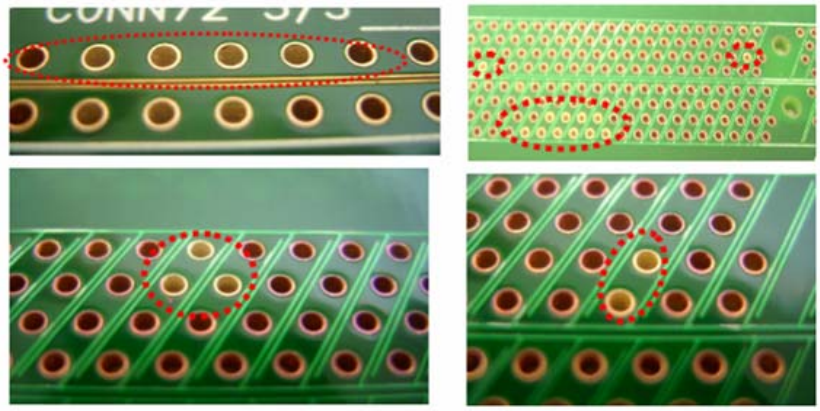


Figure 1 - OSP Coating Discoloring Randomly at Different PTH Locations

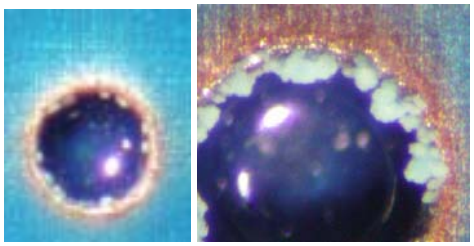


Figure 2 - Corrosion noted on OSP Coated PCB after Accelerated Aging

Manufacturability

Even in the Tin Lead world, OSP is regarded as having a smaller process window than other alternative finishes. Figure 3 shows a graphical representation of process window perceived on OSP vs Im-Ag based on historic data and engineering experience. In principle, OSP manufacturability is influenced strongly by surface finish conditions, flux activities, design and process parameters. To be successful in processing OSP, one must strive to achieve a perfect balance in aforementioned areas.

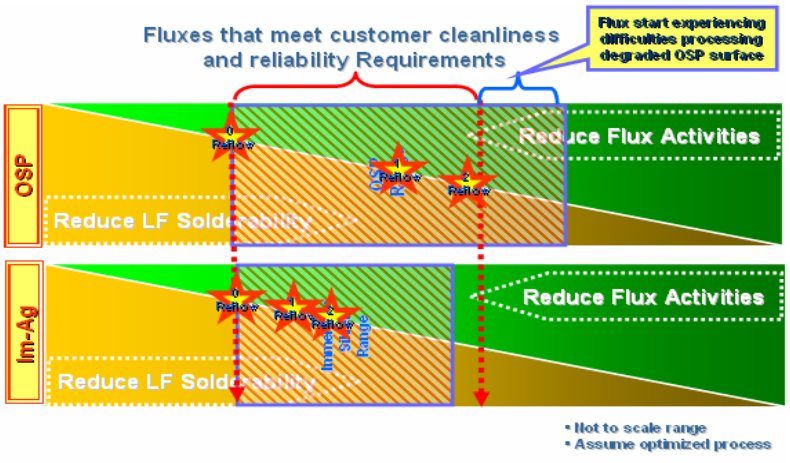


Figure 3 - Process Window Illustration

Surface Finish Conditions

Preserving coating integrity is one of the keys to implement a successful OSP process. In a highly automated production environment, proper training of operators in handling OSP coated PCB is still very critical. Fingerprints and other contaminants accidentally transferred to the SMT pads can spell trouble down the road. Thus, handling PCBs by the long edges and wearing gloves or finger cots should be common practice in preserving OSP coating integrity through out the whole manufacturing process.

For screen printer with frequent setup and changeover, dummy boards should be allocated and utilized whenever possible. Even with the new and improved high temp OSP coating, common cleaning solvents can remove a portion of the very thin OSP coating during the removal process. Although cleaning will not endanger the solder coated areas, it can easily ruin the solderability of areas remain to be soldered. In a high volume manufacturing environment, misprints can occasionally occur. When misprinted boards require cleaning, it should be reintroduced back into the production line as quickly as possible right after drying to reduce prolong exposure to atmospheric conditions.

One of the most commonly asked question from OSP user is how long the post reflow PCB can be exposed before solderability will be impacted adversely. In a high volume low mix production scenario, this may not be as critical as a batch run production line. With a fully optimized wave soldering process, 100% barrel fill can still be achieved for a double sided reflow assembly even after 24 hrs in a controlled environment.

Beside solderability, OSP surface conditions can sometimes impact equipment settings. Under normal conditions, optical registration cameras should have no problem registering the contrast on the OSP coated fiducials. As the coating thickness and oxidation conditions changes, the color of the fiducials can change significantly and may require adjustment in fiducial recognition in some rare occasions.

Flux Activities

The three main focuses for selecting Lead free fluxes are testability, solderability, and reliability. To verify the long term reliability and cleanliness of the materials used on Lead free PWA, extensive Surface Insulation Resistance (SIR) and Electromigration Chemical Migration (ECM) testing were conducted to ensure both the individual material and combination meet or exceed both industry and customer requirements. Only fluxes that are capable of meeting the reliability requirements were selected in the first round of flux evaluation. Using a dummy test vehicle, these fluxes were tested and evaluated for their ability to achieve optimum results in barrel fill, bridging and solder balling.

An interesting pattern emerges upon closer comparison of these Lead free compatible fluxes (Table 2). To address the demanding thermal endurance requirements in Lead free soldering, some flux suppliers are taking the path of higher solid contents to ensure more robust performance at higher temperatures. Barrel fill capabilities can be vastly improved with longer dwell and higher temperatures, however, the residues left behind create testability concerns for bed and nail tester. Moreover, the robustness and capability of the spray fluxer is being tested with such extreme solid content. The lower solid content fluxes work well within a smaller process window. Excessive preheat and pot temperatures should be avoided to prevent fluxes from burn-off and premature deactivation. In this case, more is not necessary better when it comes to flux deposition. Extra attention should still be paid using flux pattern test fixture to ensure no over fluxing.

Table 2 - First Round Flux Evaluation Candidates

	A	B	C	D	E	F	G	H	I
VOC Free	N	N	Y	Y	N	N	Y	N	Y
Resin	Y	Y	Y	Y	Y	Y	Y	N	Y
Sold content	15.00%	4.60%	4.50%	6.00%	7.00%	4.10%	7.00%	3.50%	3.76%
Acid number	18.00	30.00	38.00	27.00	16.50	18.00	40.00	17.00	34.20
Halide Content	0.08	0.00	0.00	0.00	< 0.05	0.00	0.00	0.00	0.00
Classification Per JEDEC 004	ROMO	ROMO	ROLO	ROLO	ROL1	ROLO	ROMO	ORLO	ROLO

Printing

There is no major change in stencil design needed unless full pad coverage is the mandated requirement. In such case, development work should be performed to ensure that the reflowed Lead free solder will fully cover surface of the pads.

In general, the wettability of OSP is not as robust as Hot Air Solder Leveling (HASL), especially after a reflow cycle, the overall poor spreading of Lead free solder makes the occurrence of exposed copper more common (See Figure 4). In particular, exposed copper can easily occur when Lead free solder does not fully wet into the corners of SMT pad or up onto the topside of the PTH annular ring. Rounding the corner of the SMT pad is sometimes used to reduce the appearance of exposed areas.

The most common concerns for the exposed area are oxidation and corrosion. For test point and test vias, serious oxidation can result in an impenetrable layer that hinders testability. Therefore, ensuring solder coverage on all test points is highly recommended. In terms of corrosion, substantial testing to date by industry and internal evaluation on cleanliness and reliability has concluded that exposed copper is technically acceptable using qualified processing materials.

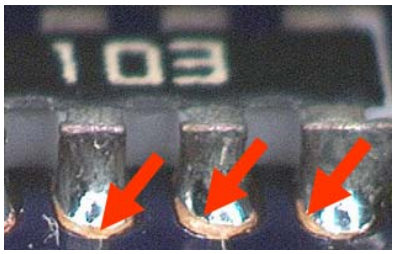


Figure 4 - Exposed Copper on SMT Pads

Reflow Soldering

The ingredients of forced convection mechanisms are given by Newton's Law of Cooling,

$Q/A = h*(To - Ts)$ <– Equation 1

Q/A = Convection heat transfer per unit area (W/m^2)
h = Convective film coefficient (W/m^2-K)
Ts= Surrounding temperature (K)
To = Object temperature (K)

Equation 1 illustrates the rate of heat transferred to the surrounding fluid is proportional to the object's exposed area (A) and the difference between the object temperature (To) and the surrounding temperature (Ts). With exposed area (A) being constant, the oven's ability to control temperatures across the PWA accurately and repeatedly is dictated by the convective film coefficient (h) or temperature difference (To - Ts). Depending on the thermal transfer characteristic of the oven and the PWAs, an oven upgrade may not be necessary; however, to retain throughput and allow maximum flexibility in profiling, more heating zones with longer heating length is highly desired.

Internal studies concluded that the overall impact of exposure time becomes more obvious as the board temperature gets closer to the peak temperature. The general rule of thumb to reduce the degradation of OSP coating during reflow is to lower the peak temperature and reduce the thermal exposure time as much as possible. This in turn can reduce the hardening of flux residues and make it easier to probe for ICT testing.

Figure 5 shows an example of the linear Lead free reflow profile adopted. Generally speaking, the linear ramp to peak model offers moderate ramp slope, reduced void formation, and maximum amount of flux available for solder wetting during the critical liquidus phase. The only drawback is that the temperature difference between smaller and bigger surface mount components will typically be more than other profiling scenarios. Therefore, it is mostly used for low complexity PWA with less demanding thermal characteristics.

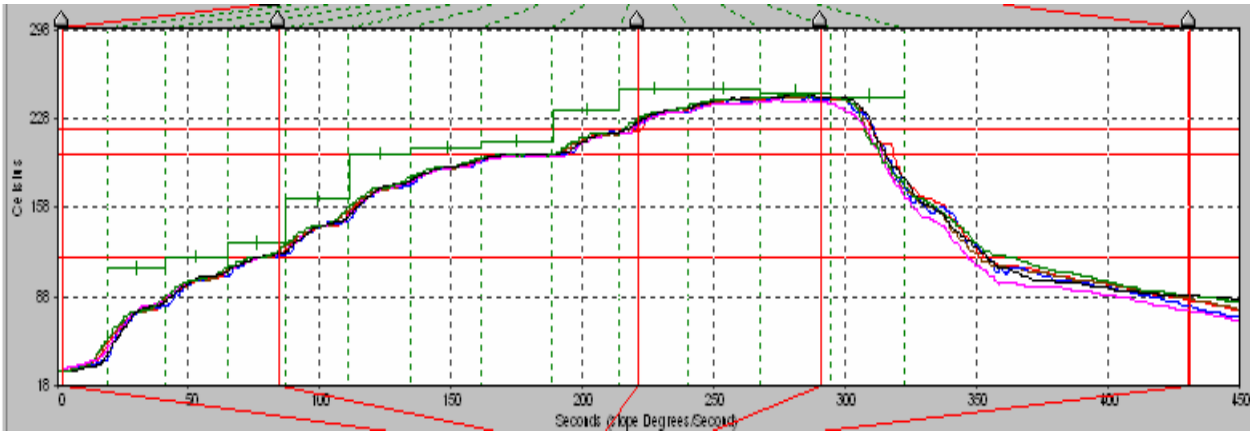


Figure 5 - Linear Lead free Reflow Profile

For years, Nitrogen has been well known for changing surface energy and reducing surface oxidation during the reflow process. Many published studies on Lead free soldering have provided supporting evidence of improving wetting, smoothing solder fillet formation, reducing flux residues, and lowering reflow peak temperatures by as much as 10^{o}C. Typically, high volume consumer electronic products are more cost sensitive. Consequently, the adoption of Nitrogen as standard reflow environment has been very slow and limited, especially in low cost manufacturing regions. To allow sufficient flexibility in deployment strategies, it is suggested that all Lead free assemblies be qualified under regular atmosphere without Nitrogen.

Based on first hand Lead free production experience, OSP performs relatively well in SMT areas. The importance of Lead free inspector training to avoid unnecessary rework and touch-up cannot be stressed enough. Initially, due to the duller and grainer appearance of the Lead free solder joints, some false failing calls reported by inexperience inspectors might be inevitable. The most common issues reported at SMT are voiding. As seen on Figure 6, the OSP coated PCB tend to have higher occurrence of voiding. By optimizing paste volume and reflow profiles using the right solder paste, regular macro voiding issues should not be difficult to control or minimize.

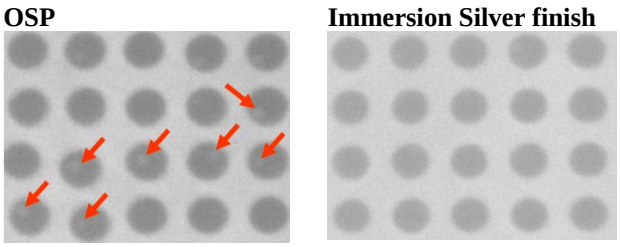


Figure 6 - X-ray images of SAC BGA voiding Solder Joints (OSP vs Im-Ag)

Wave Soldering

In the 90s, some predicted wave soldering would demise with the increase popularity of surface mount technology and intrusive soldering. Not only did the reality of this assumption prove to be wrong, it appears wave soldering will be here to stay transitioning into the Lead free world. After all, wave soldering remains one of the most cost effective manufacturing processes for forming solder joints. As new materials and equipment evolve, the smaller Lead free process windows will demand tighter process control and monitoring in critical parameters namely preheat, flux deposition, contact time, pot temperature, immersion depth, parallelism, conveyor speed, convey angle, and cooling.

In a high volume Lead free wave soldering environment, solder pot content must be verified and monitored closely. The wave parameters (i.e. contact time, wave dynamic, and pot temperature), component plating, and PCB finish can play a pivotal role in influencing the correct balance of Tin Silver and Copper. Because of the higher dissolution rate of copper from both the PCB surface and component leads, copper content is typically the one to increase the fastest.

Barrel fill

Achieving satisfactory barrel fill on PTH component is more challenging as the surface tension of Lead free solder is higher than Tin Lead molten solder. In addition, the solderability of OSP is not as robust as other surface finishes, especially after multiple reflow soldering cycles under normal atmospheric conditions. The known good design practice of adding thermal relief must be strictly followed at all times. From the design standpoint, increasing the finish hole-size has proven to reduce the hole-fill difficulties. With more solder volume in the barrel, shrinkage cracks are more prone to occur without proper control of solidification.

To simulate the actual Lead free production and design conditions as close as possible, a high volume computing product coated with high temp OSP coating was used as the test vehicle. The PCBs were reflowed twice using actual Lead free reflow parameters. Only PTH components, such as headers, E-Caps, DIMM sockets, and connectors were populated to reduce cost and processing time. Before commencing the experiment, the quantity of flux applied was optimized and verified using a standard flux pattern test fixture. Utilizing the best performing Lead free no-clean flux in the first round flux evaluation, a design of experiment (DOE) was created to optimize the Lead free wave soldering process. Based on the results obtained from previous experimentations, the following factors were selected. An automated 3D X-ray inspection system was used to eliminate any uncertainties when ascertaining the barrel fill data.

Factor	High (+)	Low (-)
No of reflow	2 cycles	0
Use of selective pallet	Yes	No
Contact time	3-4 s	5-6 s
Preheat	110-120 oC	80-90 oC

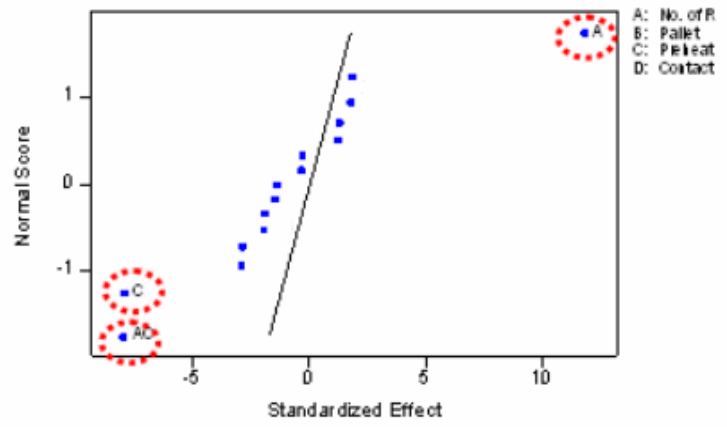


Figure 7 - Normal Probability Plot of Barrel Fill Response

The probability-plot in Figure 7 shows reflow cycles and preheat are the significant factors influencing barrel fill performance. As expected, the added reflow cycles significantly degraded the solderability of the OSP finish. On the other hand, the prevalence of lower preheat temperature is very much driven by the lower solid content of soldering flux. The two factor interaction of preheat and reflow cycle reaffirmed the significance of these two factors. As reflowing the assembly twice is part of the worse case scenario in soldering both top and bottom side components, the only significant factor left that can be modified is the preheat temperature. By lowering the preheat temperature, a small confirmation run was scheduled to validate and quantify the test results using three different OSP coatings. Figure 8 shows the actual wave soldering thermal profile used in the run. It is preferred that the areas directly opposite of the BGA component be protected during wave soldering. For PWA requiring the utilization of open carrier, detail thermal profiling should be done on affected BGA to ensure no damage on component caused by overheating during soldering.

The results from the confirmation run reveal some variation in OSP coatings performance. Assemblies coated with thicker measurements achieve slightly better results within the group (Figure 9). Overall, the Lead free barrel fill performance of OSP matches the result obtained from immersion Silver with up to 99.95% of PTH achieve more than 75% barrel fill. Additionally, X-ray, cross sectioning and pull-test were performed to confirm that both reliability and workmanship are meeting expectations (see figure 10 and11).

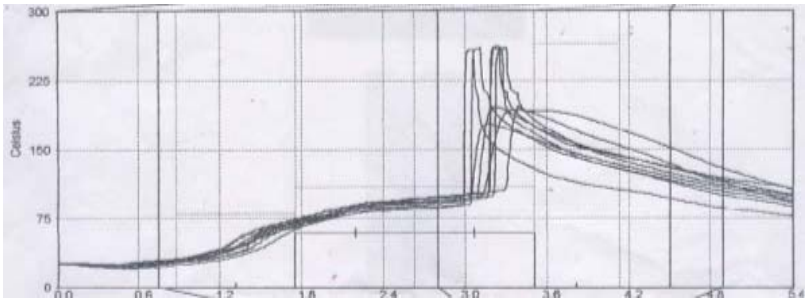


Figure 8 - Wave Reflow Profile

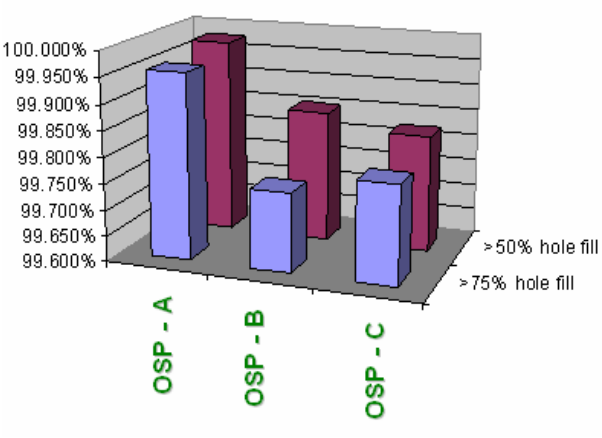


Figure 9 - Barrel Fill Performance of OSP

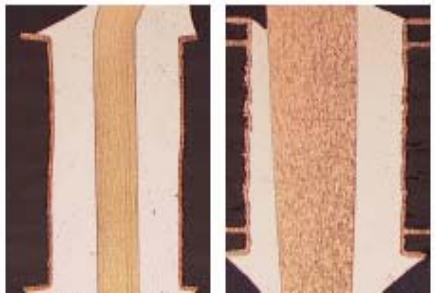


Figure 10 - Cross Sectioning of PTH Solder Joints

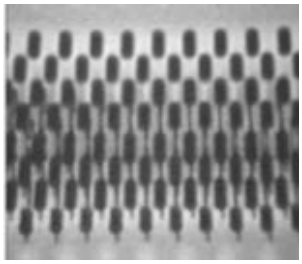


Figure 11 - X-ray image

Testability

Figure 12 illustrates that many factors impacting testability. Robust test performance at circuit test (ICT) is mostly determined by the contact quality between the test probe and test pad. It has been a well known issue that the OSP coating makes ICT test probes more challenging to make contact with test pads. In order to resolve the testability concerns, different methods have been proposed. Table 3 highlights three conditions commonly encountered by OSP coated PCB.

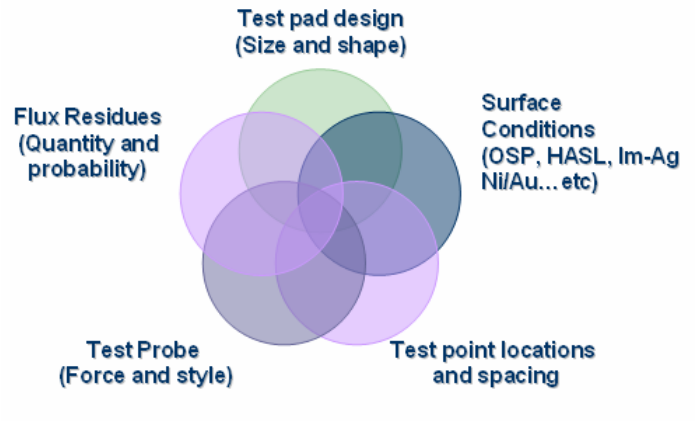
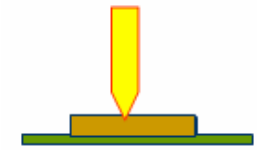
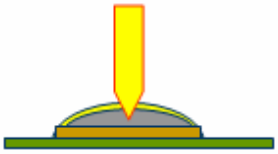
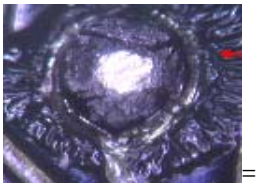
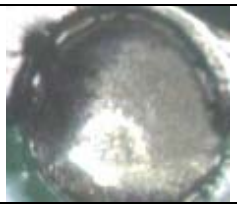


Figure 12 - Factor impacting testability

Table 3 - Test conditions Summary

Condition	**A**	**B**	**C**
Illustration			
Appearance			
Process	None	Add Solder Paste	Expose to Wave soldering
Remarks	Bare copper, prone to OSP thickness and surface oxidation conditions	No-clean Lead free solder paste residues reduce probability	Low solid no clean flux, left behind little residues
Testability	Poor	Marginal (Paste dependent)	Good

It appears that exposing the test pads to wave soldering directly (condition C) is the most logical solution to the testability issue. This allows both test pads and test vias to form a nice, round solder dome surface for test probes to make good contact (see Figure 13); however, getting every test point coated with Lead free solder at wave soldering alone can be tricky (see Figure 14).

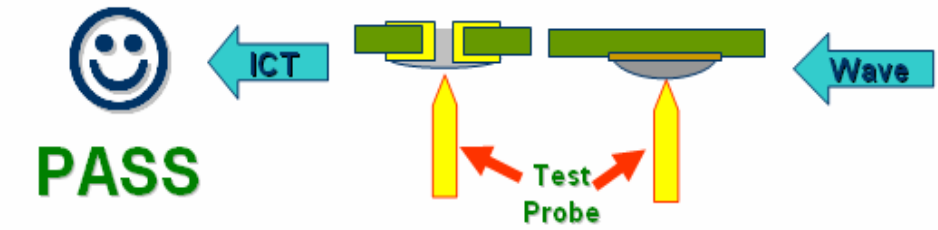


Figure 13 - Test Pads and Vias Forming Dome Shape

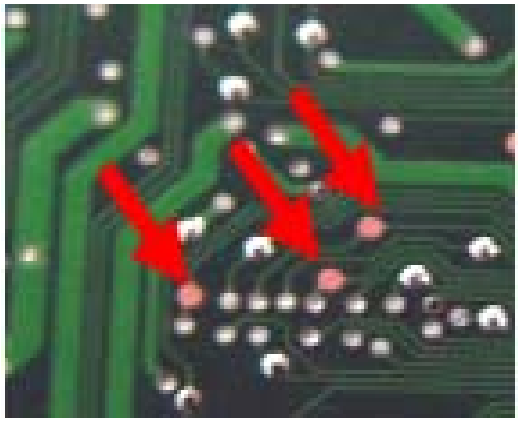


Figure 14 - Test Points without Solder Coating can Lead to False Contact Failure

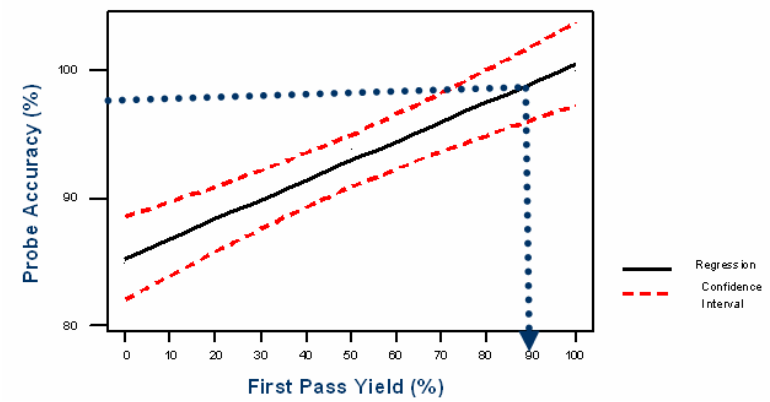


Figure 15 - Regression Chart on FPY and Probe Accuracy

To better understand the relationship between accuracy and first pass yield, a regression study was conducted. As shown in Figure 15, the results indicate the probe must reach at least 96% accuracy before it becomes capable of achieving 90% first pass yield. Two alternative techniques were explored to improve the solder coverage of the test points; Table 4 summarizes the effectiveness and the outcomes after exposing all test points to wave soldering directly using an open wave carrier.

Table 4 - Testability Improvement Summary

Option	Issues	Results
1. Add solder paste to all test points to ensure 100% full coverage	Additional process step for assembly with only single sided reflow	Significant improvement in test point coverage With some paste residues left behind on test point that require more frequent cleaning to test fixture
2. Use dual wave to improve test pad coverage	The added contact time burn-off and deactivate some flux prematurely.	Slight increase in flux deposition with improvement sometimes influenced by surface finish conditions

Conclusion

As observed in this case study, a high volume Lead free production solution for OSP coated PWAs is highly achievable. As one of the leading Lead free finish embraced by the industry, the use of OSP is sometimes unavoidable. With more RoHS electronic assemblies currently in the product development cycle, the improvement in material performance and process know-how are anticipated to increase rapidly. At the same time, new challenges with more complex assemblies will continue to surface. The development works presented in this article demonstrate the systematic approach needed when facing these new, formidable huddles.

The progresses in Lead free process knowledge, material and equipment have come a long way in the past few years. Converting to OSP finish in a high volume Lead free manufacturing environment requires careful research. Existing good manufacturing practices will need to be strengthened and revised as new Lead free soldering lessons are being learned. Although OSP is not a simple drop in replacement for existing processes, it is still a highly viable surface finish option for high volume manufacturing provided proper checks and balances are in place. With that said, there is “no one size fit all”

solution when selecting the right PCB surface finish. In the Lead free transition cross road, the key is to balance the risks associated with manufacturability, testability, design, reliability, cost, and supply chain partner capabilities.

Acknowledgment
The authors would like to thank the entire China AMBD team, specially, Jim Ma, Bob Goa, Xiao Wang, Luli Bun and Michael Burner, in supporting the development activities