## Bob Wettermann

President
**BEST Inc.**
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**Biography:**
Bob is an MIT and president of BEST. Bob is an electrical engineer and has experience in applications and design. He holds several patents in the fields of surface science, factory automation products and PCB rework/repair. In addition he is a member of IPC and SMT.

**Title:**
NPI Step Stencils-A New Approach

**Executive Summary:**

There are a variety of stencil approaches in which the new product process engineer can deal with the assembly of both high solder paste and low solder paste volume in an SMT assembly environment. Traditional approaches have heretofore favored aperture manipulation, multiple stencil printing and chemically or mechanically altered stencils which include a “step”. Some of these approaches present either a compromise or a non-workable option for building new products reliably and quickly. This paper presents a new approach delivering on the need for fast delivery and enough solder paste volume differential between the low solder paste and higher solder paste volume requirements. Presented will be the method and the results of an initial printing study determining amongst other things the solder paste volume delivered to the areas of different stencil height.

## Jim French

**BEST Inc.**
jfrench@solder.net


**Biography:**
Jim brings very practical knowledge to his classroom teaching. He has been involved in various manufacturing, PCB repair, rework and electronics repair assignments in his career spanning 12 years. Having been in the contract manufacturing environment responsible for pick and place, solder paste printing, reflow oven profile development and cleaning processes Jim has experienced firsthand some of the challenges in PCB assembly. Jim has experience with several Chicago-area contract manufacturers and currently leads BESTs' test and PCB rework/repair operations. Jim is a certified instructor in both IPC JSTD-001 and IPC A-610.

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# NPI Step Stencils-
# A New Approach

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# Stepped Stencils for NPI

- Requirement for Stepped Stencils
  - High Component Mix
  - Pin in Paste
  - Glue Stencils
  - Other Issues
- Existing Solutions
  - Electroformed Stencils
    - Additive, Subtractive

# Stepped Stencils for NPI

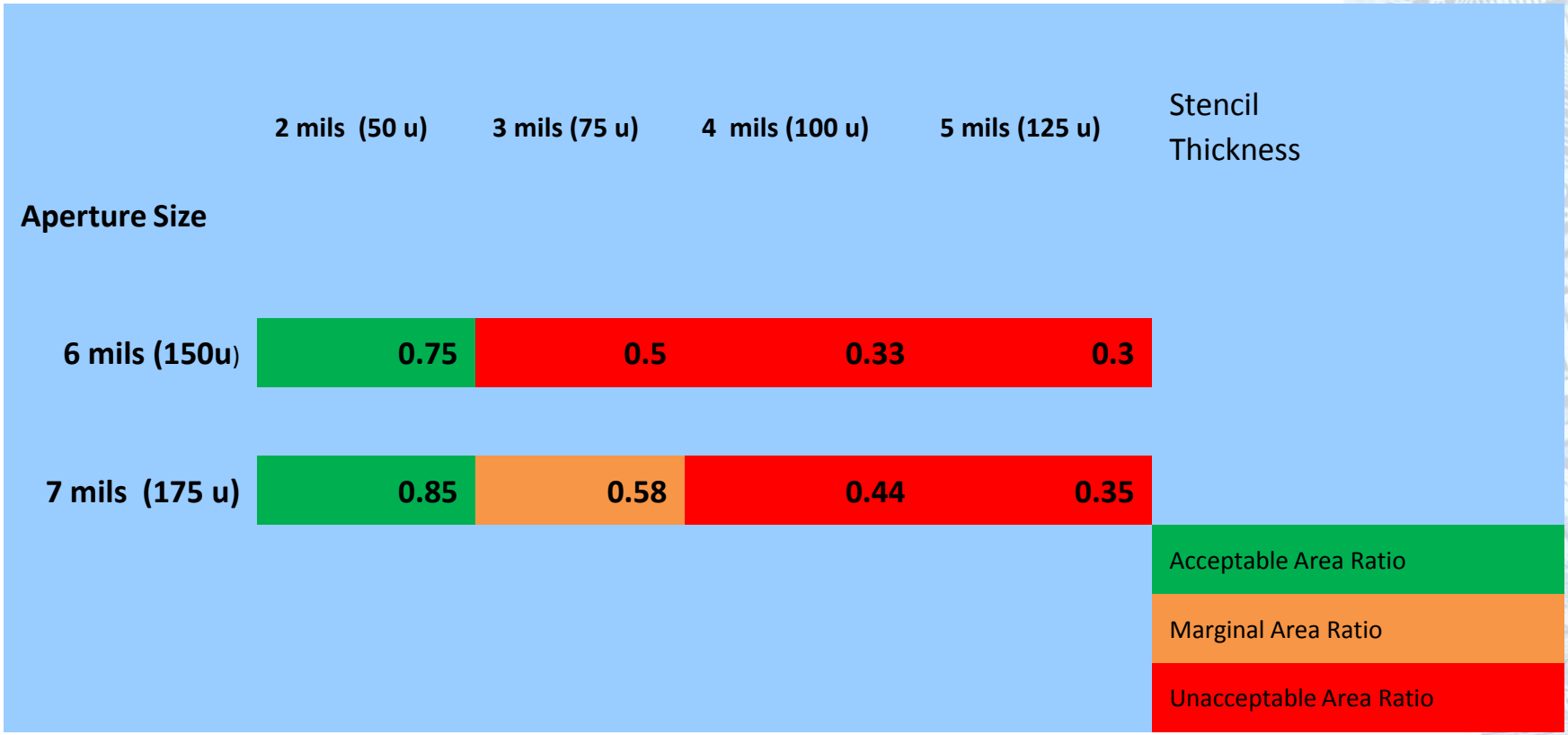
**Existing Solutions (continued)**

- **Milling**
- **Combination**

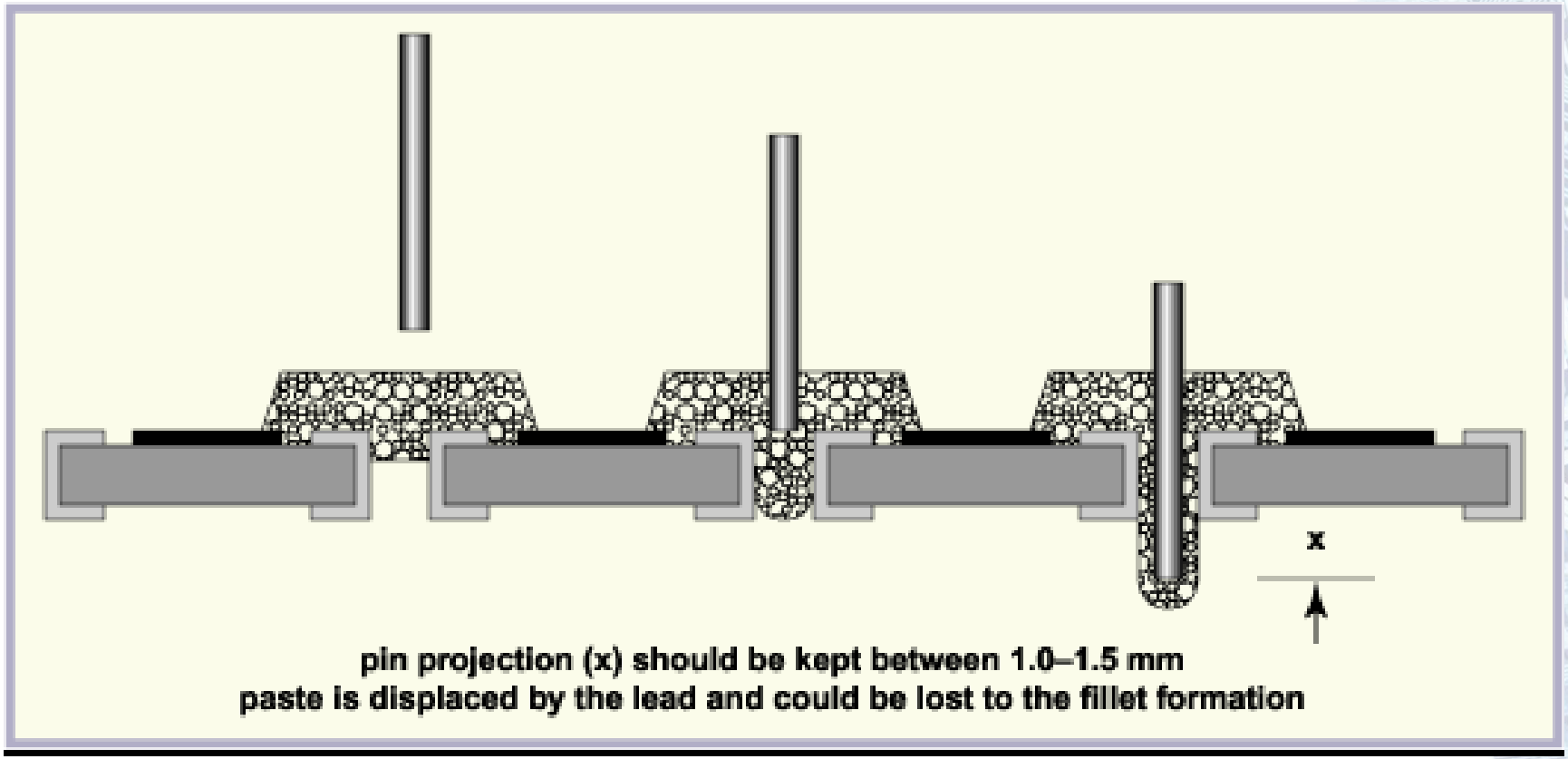
**New NPI Stepped Stencil**

- **Concept, Testing, Results+Conclusions**

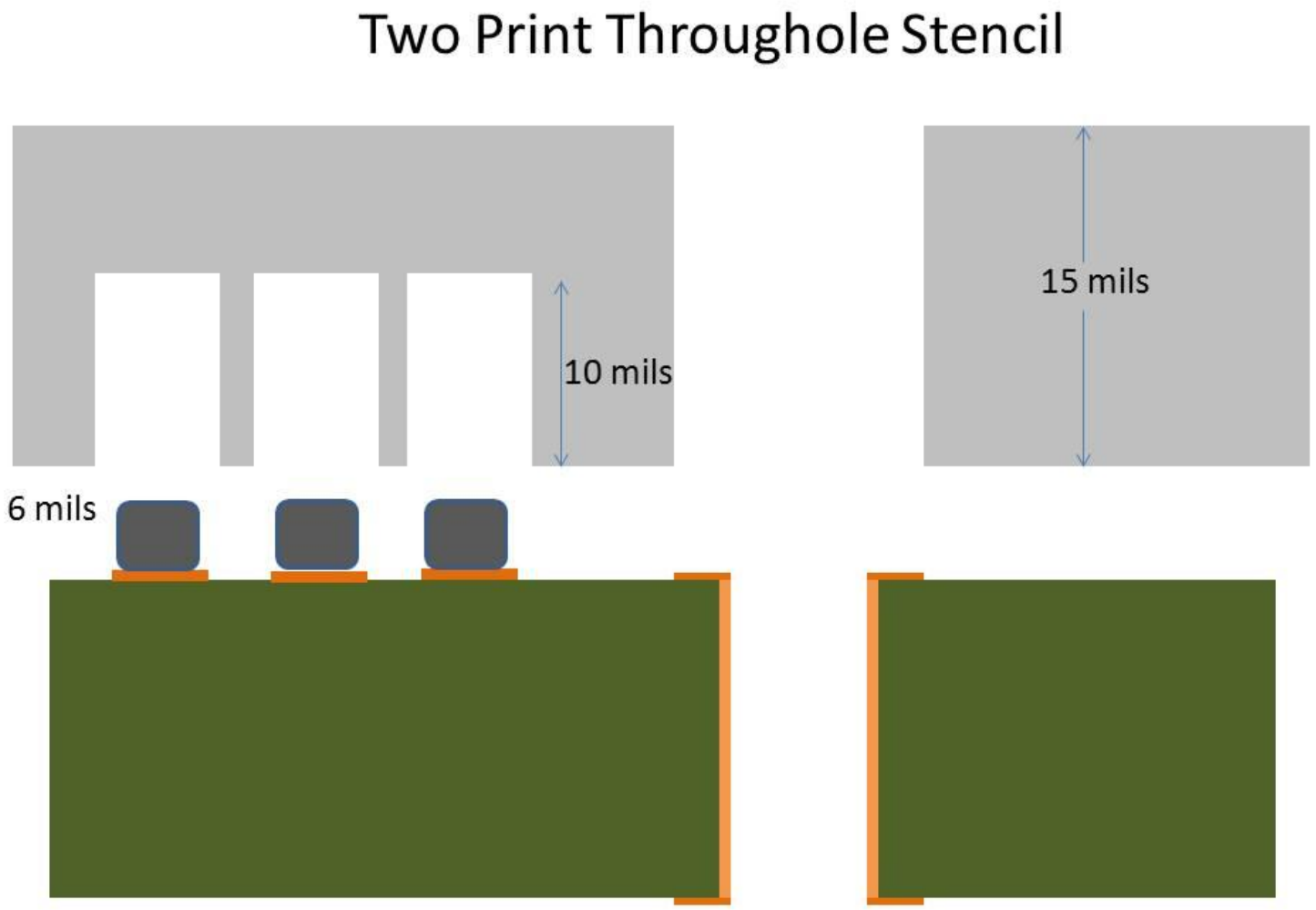
# Area Ratios


2 mils (50 u)
3 mils (75 u)
4 mils (100 u)
5 mils (125 u)
Stencil Thickness
Aperture Size
6 mils (150u)
0.75
0.5
0.33
0.3
7 mils (175 u)
0.85
0.58
0.44
0.35
Acceptable Area Ratio
Marginal Area Ratio
Unacceptable Area Ratio

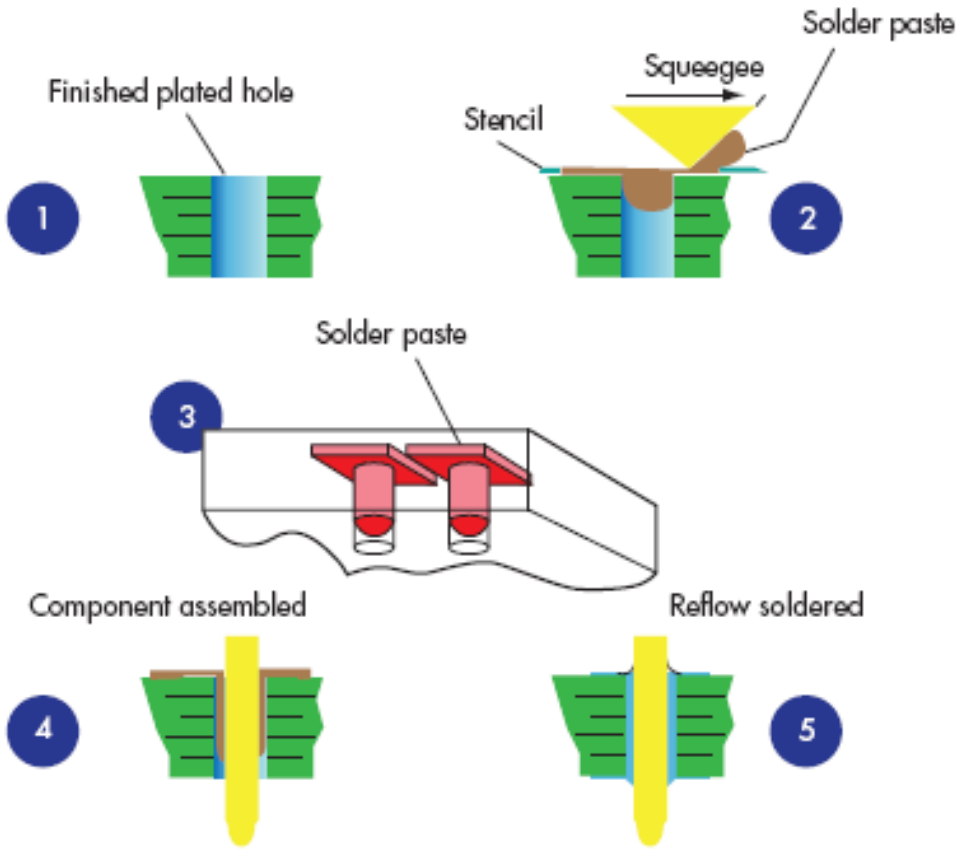
# Glue Stencil
# Pin in Paste/Intrusive Soldering



# Two Print for Pin-in-Paste (2nd print)

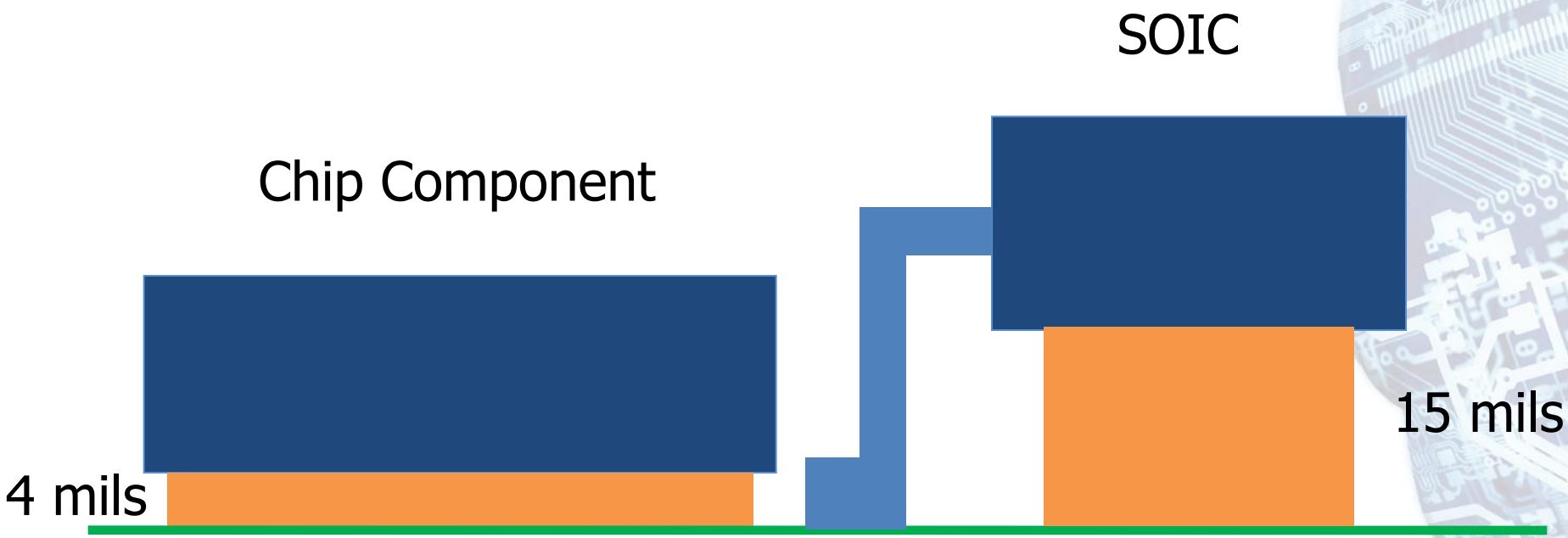


# Glue Stencil
# Pin in Paste/Intrusive Soldering

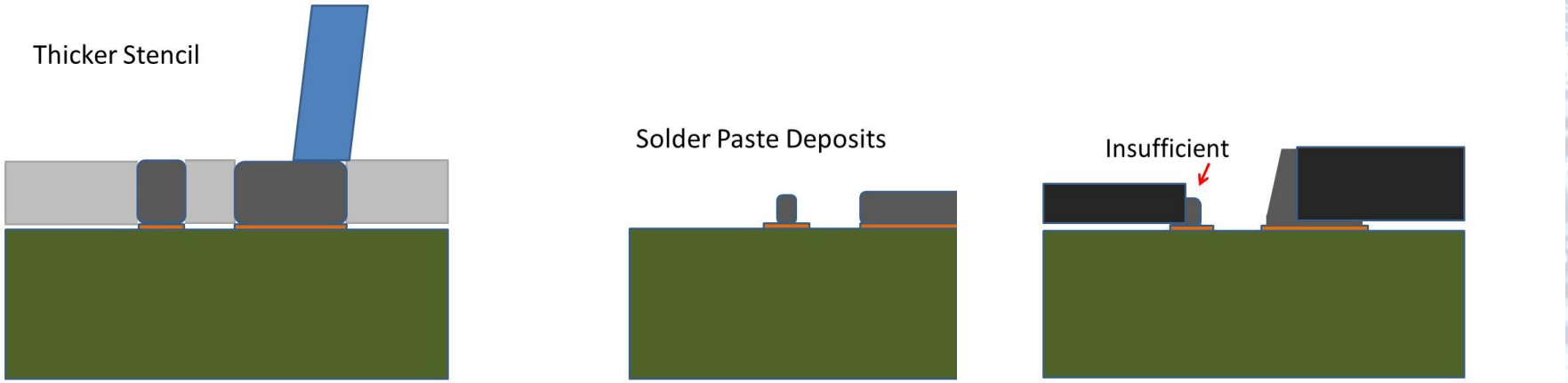



1. There are five steps for mounting components in a PiP rendering.

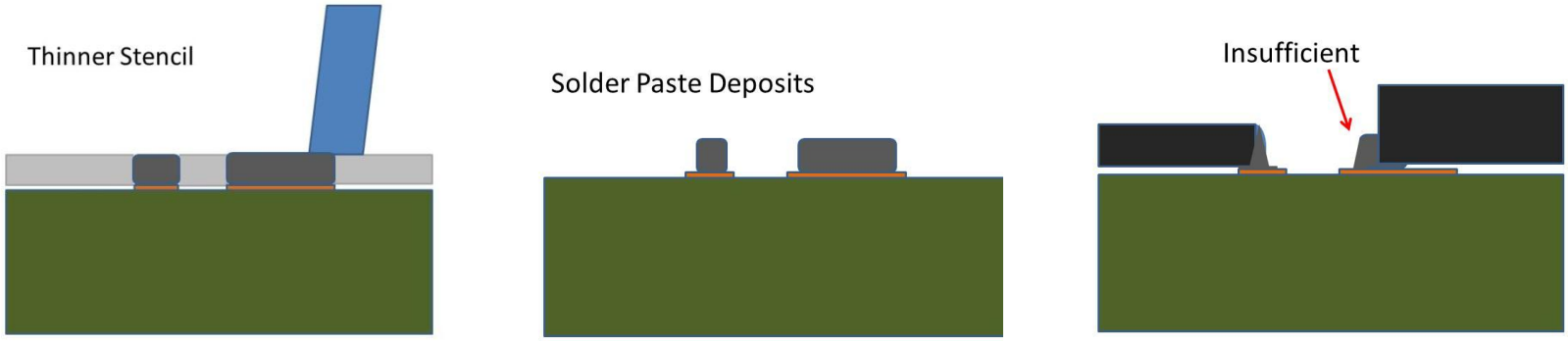
# Glue Stencil
# Diverse Volume Requirements



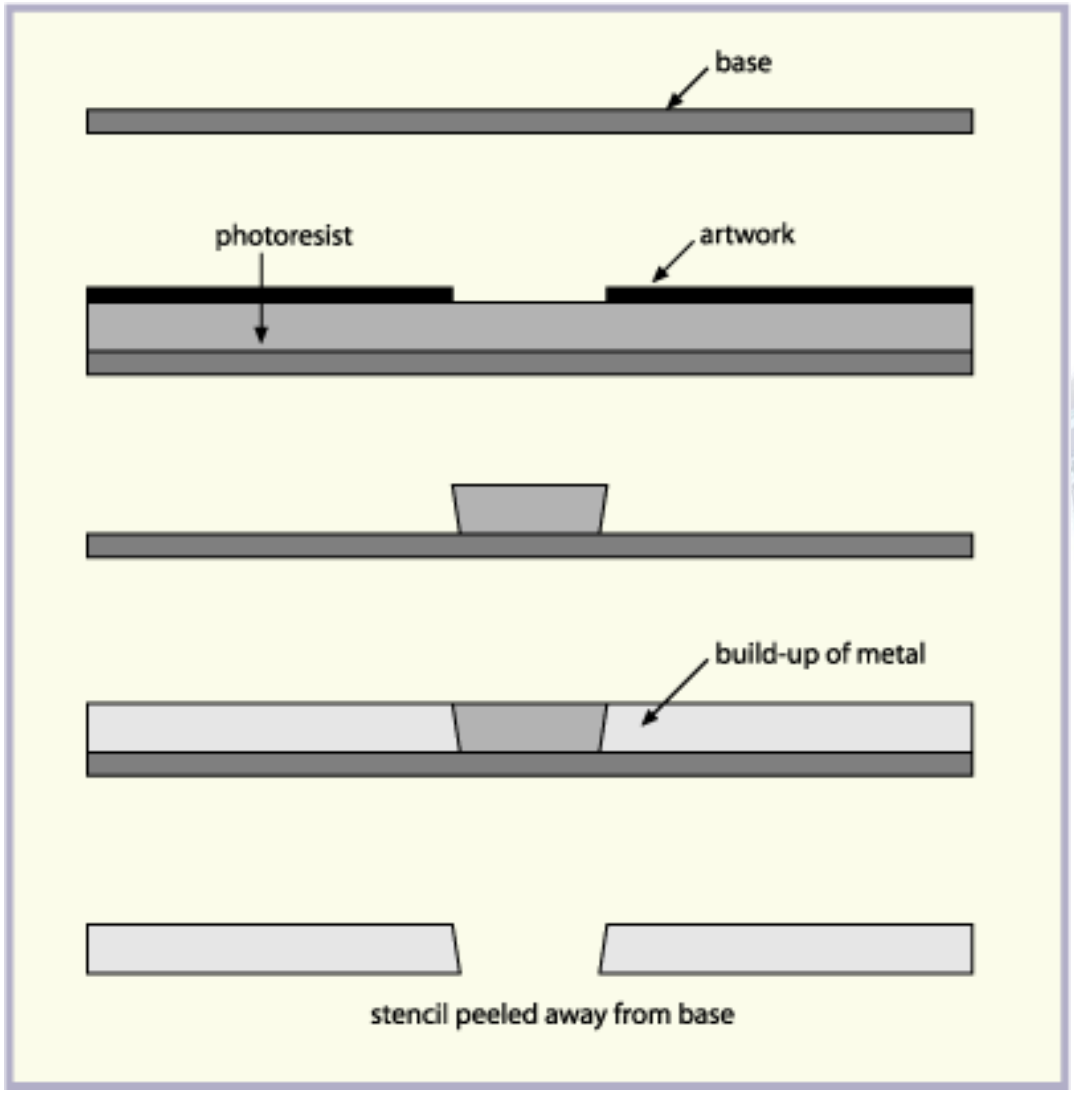
# Compromise for Diverse Volume Requirements Thicker Stencil



# Compromise for Diverse Volume Requirements Thinner Stencil

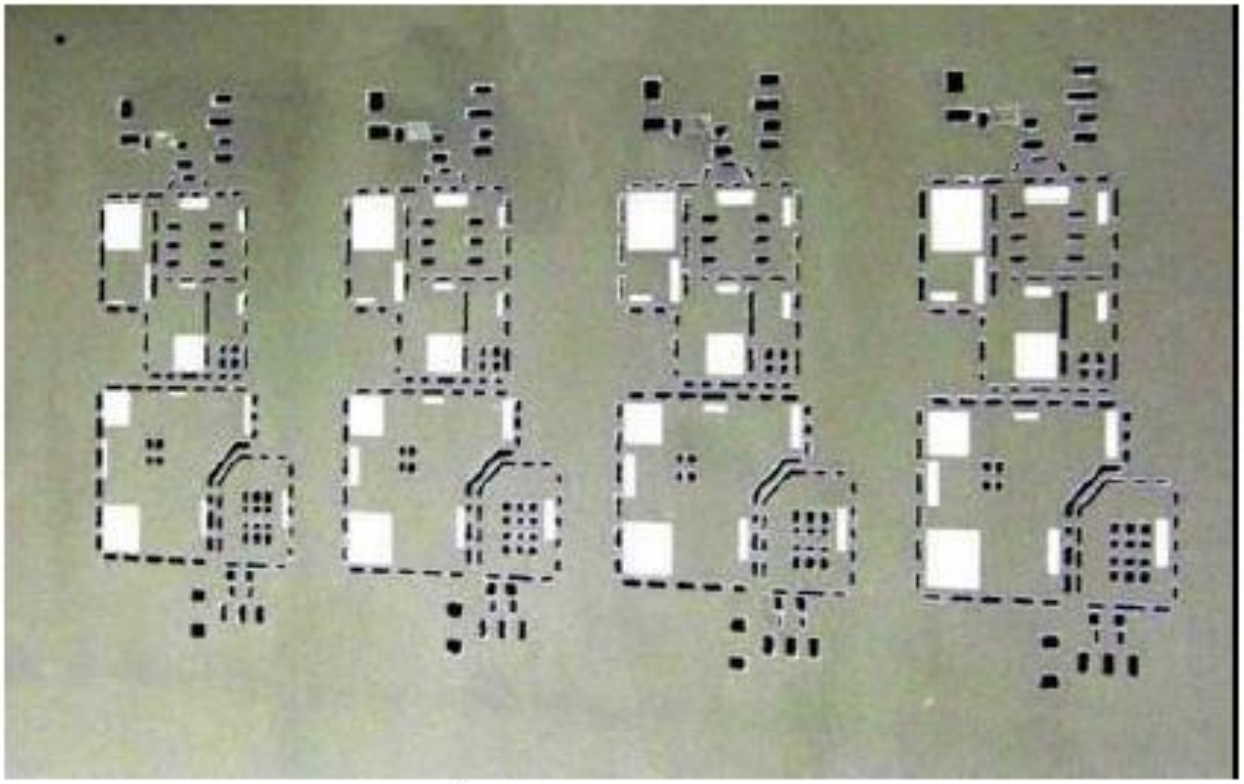


# Chem Etch

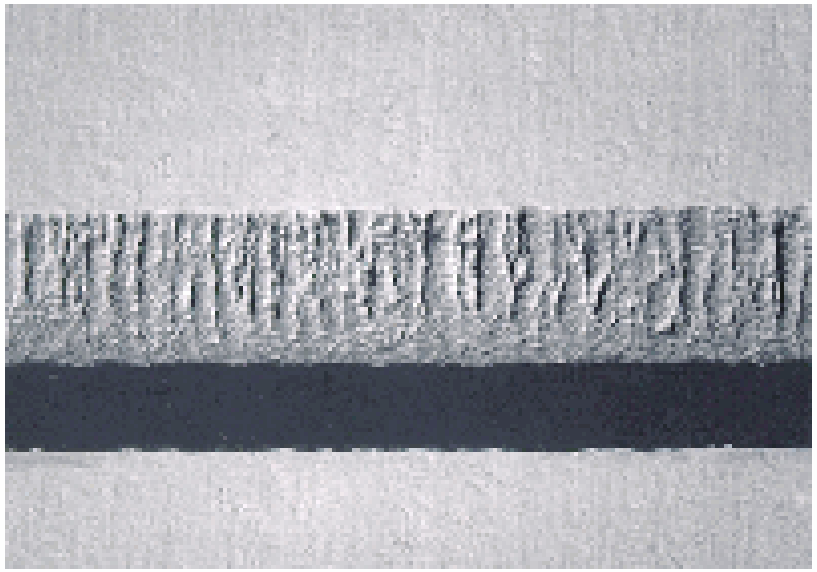

base
photoresist
artwork
build-up of metal
stencil peeled away from base

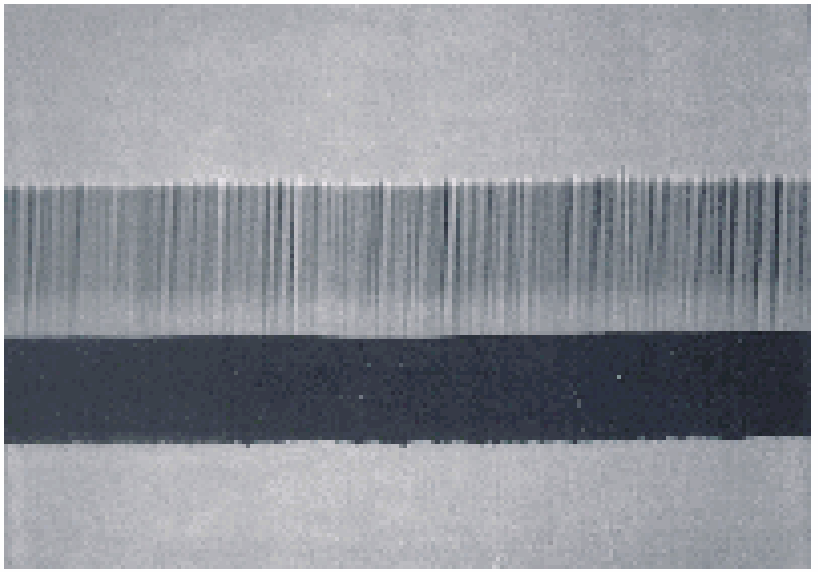
# Chem Etch

# Step Stencil
# Relief Pocket

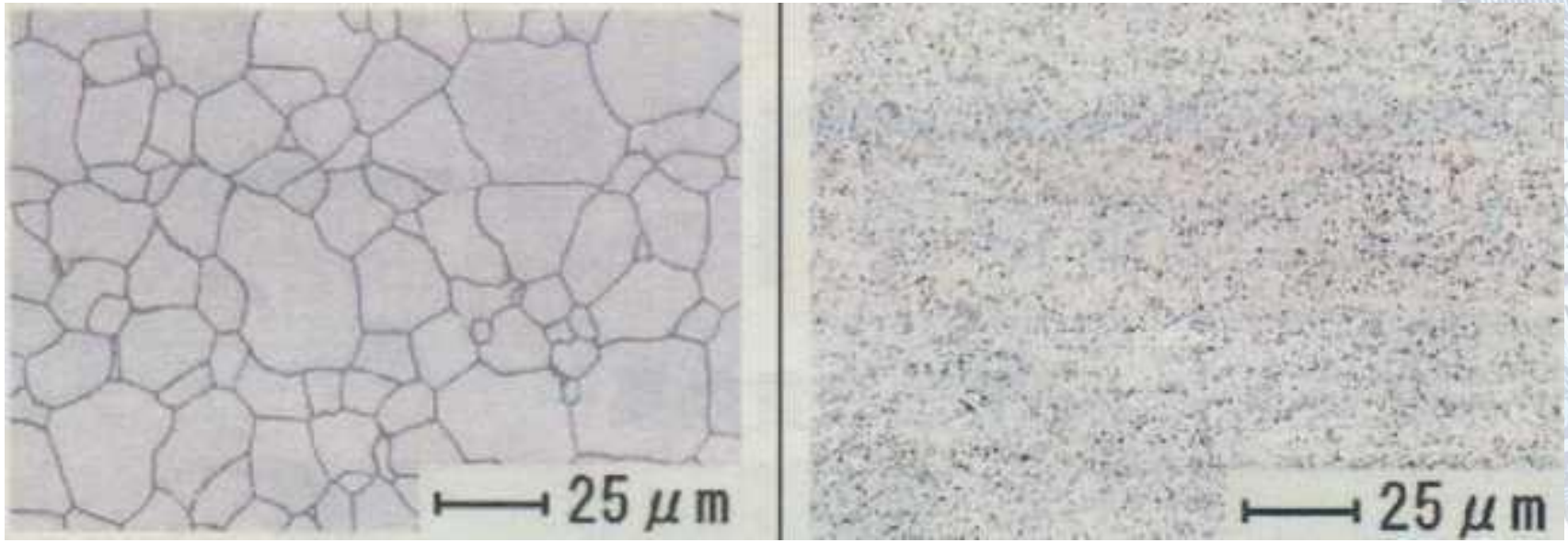


# PHD Material Side Wall

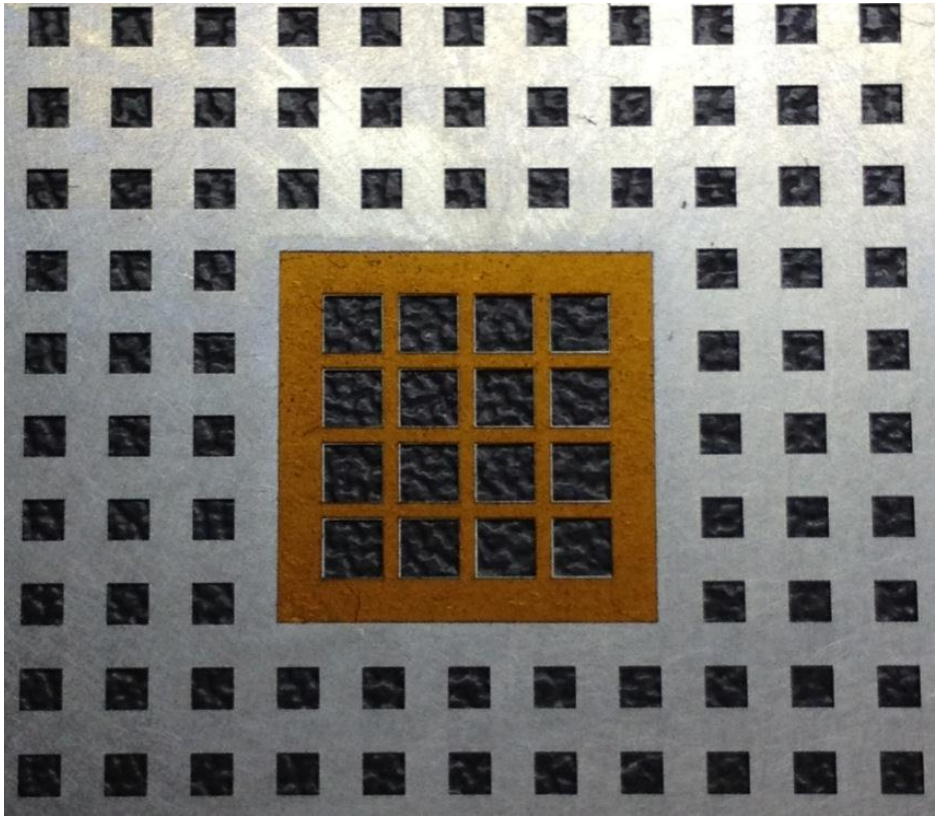




# PHD Material
# Grain Structure



# QuikStep – A New Approach



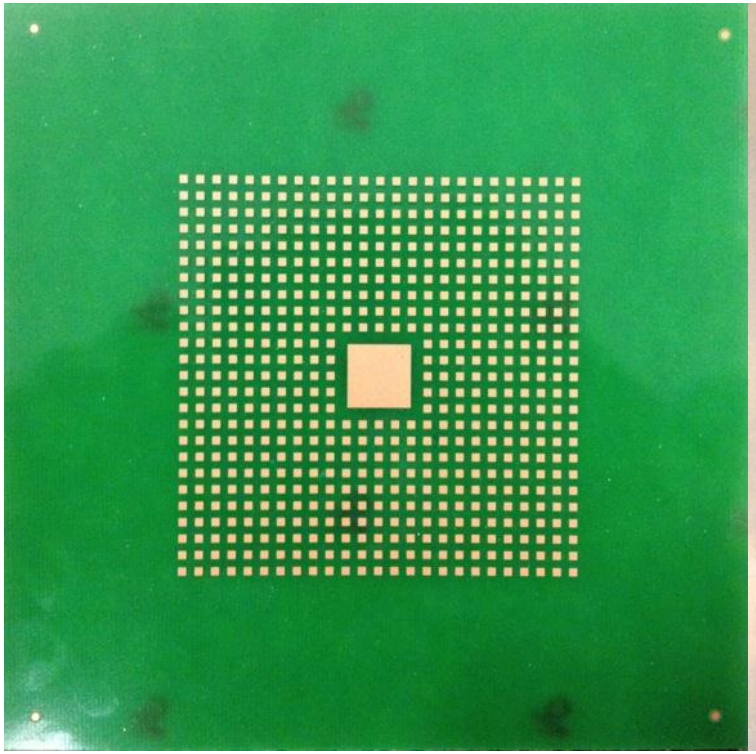
# What is QuikStep

**An adhesive backed polyimide stencil that is applied to a laser cut metal stencil creating a step in selective areas of the stencil.**

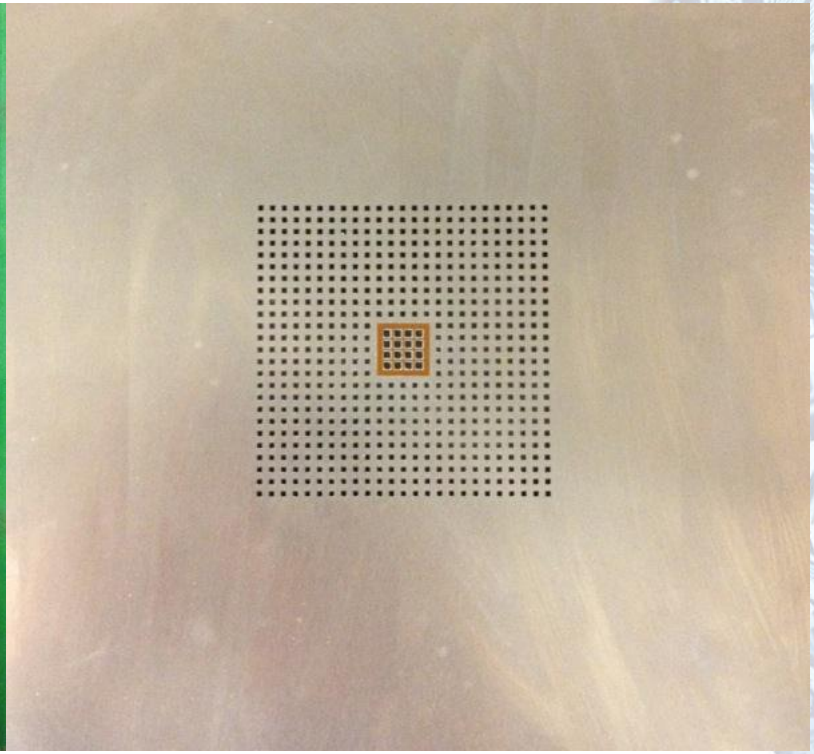
# QuikStep Advantages

- **Quick Turn**
- **Cost Effective**
- **Replaceable**
- **Similar Characteristics as other Step Up Stencils**

# Development

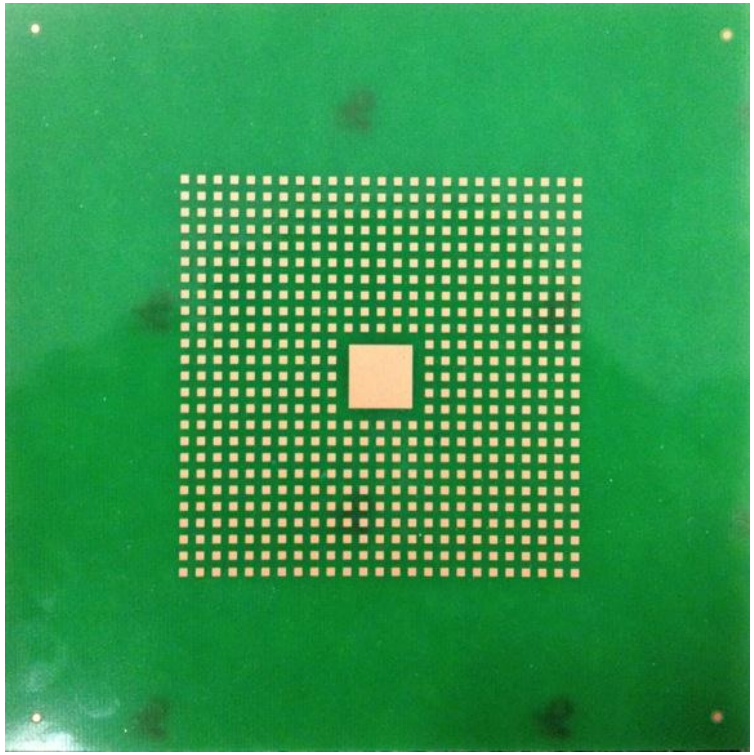


Test PCB



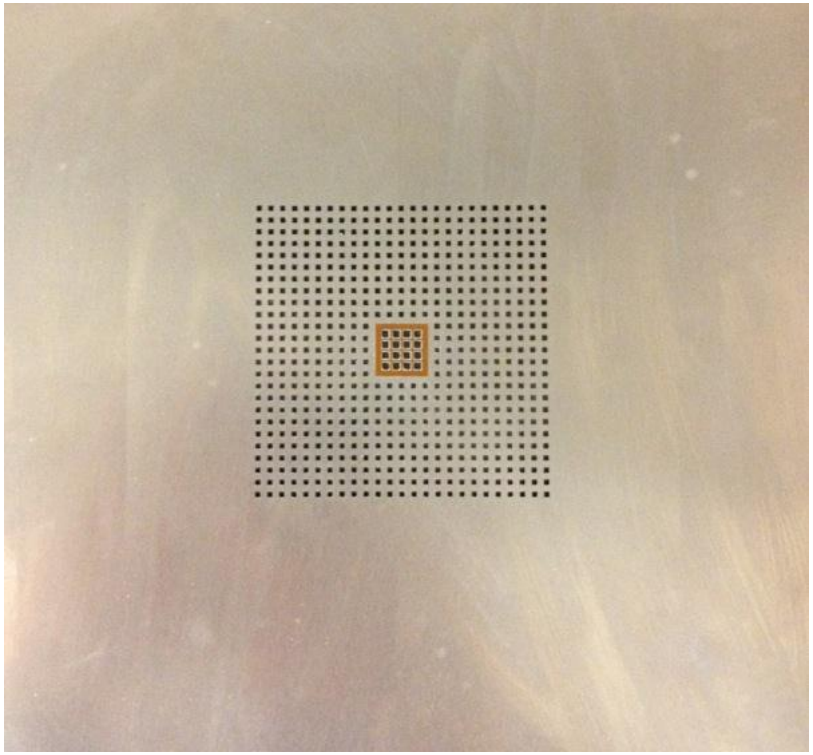
Test Stencil

# Test PCB Specifications



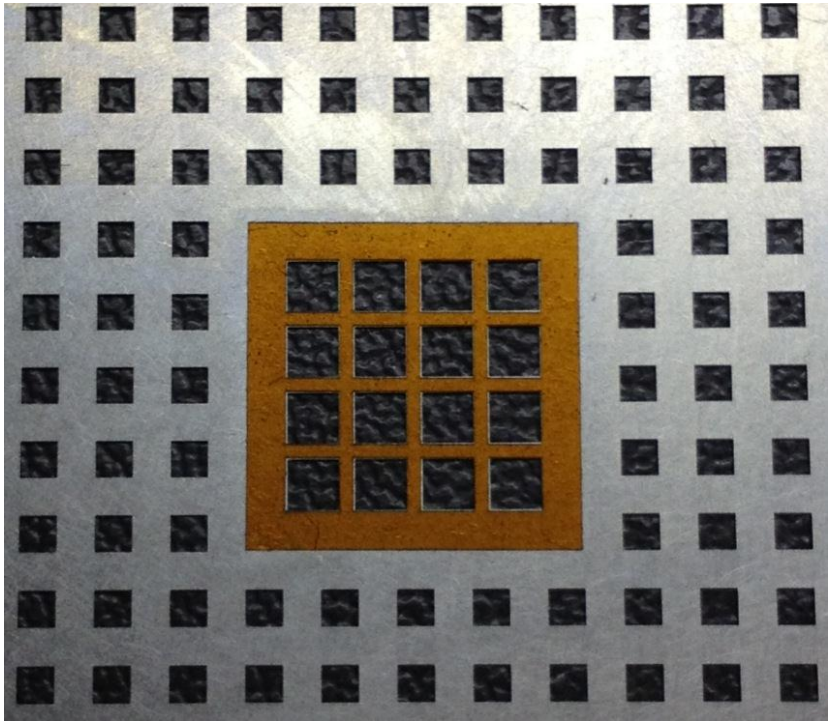
- **Test PCB – .062” thick FR4 laminate with a copper OSP finish.**
- **Test PCB – Pads .060” x .060”, pad spacing .060” with center pad of .470”**

# Test Stencil Specifications



- **TEST Stencil – 5 mil stainless steel**

# Test QuikStep Specifications



- **Test QuikStep – 4 mil polyimide window paned to step up the center pad of PCB.**

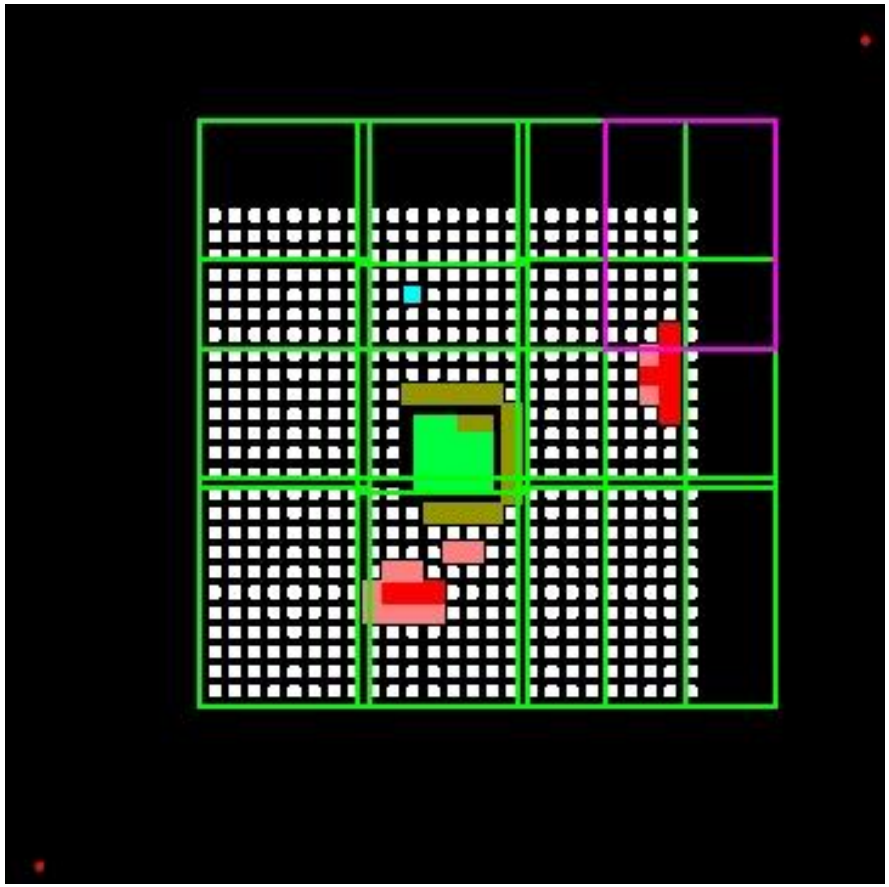
# Test Procedure

- **5 PCBs that were not stepped were paste screened.**
- **10 boards using QuikStep were screened**
- **PCBs were measured for paste volume using a 3-dimensional solder paste inspection system.**

# Results

- **Non stepped boards had a nominal paste height of 5.3 mils in all areas.**
- **Boards using QuikStep had a nominal paste height of 8.7 mils in the stepped up area.**

# Results (cont.)



Paste Volume Measurements

# Keep Out Area Specifications

- **Print direction - leading edge: 20 mils per 1 mil**
- **Print direction - trailing edge: 33 mils per 1 mil**
- **Transverse direction: 35 mils per 1 mil**

# Thanks!

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