

Effect of Voiding on Lead Free Reliability

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ABSTRACT

This paper had as an aim to correlate the degree of voiding with reliability. Here the a purpose designed test vehicle was used, in which seven different solder pastes from three manufacturers were evaluated through a range of reflow profiles. In spite of strenuous efforts we had the surprising result of only producing limited voiding. Hence, end-users can have a high degree of confidence that voiding levels in lead-free solder pastes can be kept below the IPC specified maximum of 25% by area. No paste exhibited voids in any PBGA joint greater than 15% despite attempts to produce higher voiding levels.

Three different voiding levels were produced and samples subsequently subjected to 2000 thermal cycles (-55 to +125°C). Despite these samples having higher voiding levels than those stipulated for class 3 of the IPC's BGA Assembly and Inspection Guidelines, no adverse effect on reliability was seen. The shear strength deterioration during thermal cycling of chip resistors also with these levels of voiding, was also unaffected.

INTRODUCTION

European legislation will eliminate lead in solders from main-stream electronics manufacture. The current preferred solder replacements are based on the tin-silver-copper (SAC) system, which have melting points of 217 °C and above. This 34 °C increase in melting point from the established SnPb solder alloys, necessitates a similar increase in processing temperature for both reflow and wave soldering. Some users have reported increased voiding levels associated with these higher temperatures (Reference 1) and this has led to a general belief within the electronics industry, that the change to lead-free soldering will mean an increase in typical voiding levels and potential consequential reductions in solder joint reliability.

For SnPb alloys, a good deal of work on assessing reliability of soldered joints with known voiding levels has been undertaken. Voiding has been shown to reduce solder joint reliability in a number of ways. Large voids cause reductions in effective cross-sectional area of the soldered joint (Reference 2). This results in higher joint stresses as any shear strain on a void-containing joint is experienced over the reduced cross-sectional area. The voiding may also reduce the distance fatigue cracks have to propagate to cause failure, although alternatively, voids may act as crack arrestors, stopping the propagation of a crack and requiring additional energy to initiate a continuing crack through the remainder of the joint (References 3 and 4).

The effect on reliability of smaller voids is more complicated and can depend on where the voids are located within the joint. The latest IPC BGA assembly guidelines (Reference 5) specifically differentiate between voiding within the bulk of the joint and voids at the interface between component and solder, or between solder and PCB. Voids at the interfaces tend to be more detrimental and have therefore been given a lower permitted level in these guidelines than voids in the bulk of the joint.

Voids have been shown to have a direct effect on reliability, with several workers (References 4 and 6) reporting premature thermal cycling failures and significant loss of electrical integrity, as well as device failure due to voiding. The device failure may be related to loss of device thermal performance due to voiding, which can result in device over-heating and subsequent premature performance failure.

Smaller voids in the bulk solder of the joint may have less effect on reliability. Banks et al (Reference 3) have reported no reduction in the reliability of plastic ball grid arrays (PBGA) with up to 24% voiding by area. Indeed, their work showed an improvement in PBGA reliability with voiding levels up to 16%. In these samples the route taken by cracks within the solder balls, was not affected by the presence of voids. Banks et al suggested several possible reasons for this improved reliability. As discussed above, the voids may be acting as crack arrestors. The inclusion of voids within the joint does increase the height of the solder joints (possibly by as much as 4%). This will reduce the stress on a taller joint for the same joint strain, compared to a shorter joint. It may simply be that the mechanical properties of the joint are affected by the inclusion of the voids, making the structure more flexible. The improved reliability of joints with limited voiding levels is probably a result of a combination of some or all of these three suggestions.

The belief that voiding is likely to be greater for lead-free solders is consistent with many of the known causes of voiding, for example solvent retention within the molten solder of the joint can cause voiding. This may be more likely in lead-free soldering, as there may be insufficient preheat in a poorly developed profile, which is particularly likely to occur during

initial transition to lead-free soldering. Lead-free solders have higher surface tensions (Reference 8) than SnPb equivalents, which may also result in to increased solvent retention. Air Liquide (Reference 9) have reported that increased oxidation at the surface of joints can inhibit out-gassing of volatile molecules. Such increased surface oxidation is likely to occur with the higher processing temperatures of lead-free soldering. Lea reported increased voiding in SnPbAg solder joints (Reference 10) where the solder paste had experienced increased oxidation during the assembly process. Again, the increased processing temperatures of lead-free soldering are consistent with this scenario.

At the higher lead-free processing temperatures, increased out-gassing of the component parts may occur, leading to increased voiding in the joints. Out-gassing may be caused by insufficient laminate or solder mask cure (Reference 2). Moisture absorption or surface contamination may also increase voiding in the soldered joint. Several workers have reported problems with vias within pads (References 11 and 12), an increasingly common aspect of high density PCB designs. Such vias may be more prone to out-gassing at higher processing temperatures.

Eckel et al (Reference 4) have also reported that increased processing temperatures may affect the out-gassing of electroless nickel/immersion gold (ENIG) surface finishes. The out-gassing may be caused by organic contaminants within the gold finish, with hot air solder levelled (HASL) finishes performing better. Similar issues may exist with organic solderability preservative (OSP) on copper finishes.

The vast majority of the work cited above, has been conducted on SnPb systems. But the results clearly provide a link between voiding, soldering and reliability of the joint. In consequence, it is reasonable to question the nature and extent of any link between voiding and reliability for lead-free soldered joints. However, there is very little work in the open literature concerning lead-free systems. Thus the work reported here was designed to investigate some of these issues for lead-free systems, specifically for the SnAgCu alloy.

A complete description of this work can be found in Reference 15

EXPERIMENTAL

The work took three component styles, chip resistors, SOICs and BGAs. Different reflow profiles and solder pastes were evaluated to give suitable voiding levels.

Table 1 - Reflow temperature profile details

Thermocouple position	Profile 1			Profile 2			Profile 3		
	Max Temp °C	Time above 217°C	Time to Max Temp (min)	Max Temp °C	Time above 217 (min)	Time to Max Temp (min)	Max Temp °C	Time above 217°C	Time to Max Temp (min)
PBGA Inner	245	00:54	03:24	240	00:45	03:17	249	00:57	02:45
PBGA Outer	239.5	00:47	03:29	234	00:36	03:13	243	00:47	02:43
SOIC	241.5	00:43	03:25	231.5	00:29	03:06	243	00:44	02:35
R0603	253.5	00:50	03:14	251	00:44	02:59	259	01:03	02:30
R1206	233.5	00:39	03:22	225	00:22	03:06	238	00:34	02:38

Table 2 - Lead-free solder paste details

Paste	Manufacturer	Alloy	Flux Type	Particle Size	Metal Content wt%
A	X	95.5Sn3.5Ag0.7Cu	No-clean A	Type 3	88.5
B	X	95.5Sn3.5Ag0.7Cu	No-clean A	Type 3	88.0
C	X	95.5Sn3.5Ag0.7Cu	No-clean B	Type 3	88.5
D	X	95.5Sn3.5Ag0.7Cu	No-clean C	Type 3	88.5
F	Y	95.5Sn3.8Ag0.7Cu	No-clean E	Type 3	89.8
G	Z	95.5Sn4.0Ag0.5Cu	No-clean F	Type 3	88.0
H	X	95.5Sn3.5Ag0.7Cu	Water-Soluble	Type 3	88.5

After assembly, voiding levels were measured using Dage XIDAT 6000 X-ray system. The system was set up with identical parameters for each inspection run so that the results obtained are directly comparable. For the BGAs, an auto inspection routine was utilised, which calculates the total area of voids in each PBGA solder joint. Figure 3 presents a typical image. Representative images were also acquired of resistors and SOICs for each condition.

After soldering, all the non-BGA joints on the assemblies were 100% visually inspected by a single operator using a 10X to 30X stereo microscope. The assemblies were inspected to IPC A610 Rev C class 3 (Reference 13). No rework was undertaken. Any defective solder joints were logged and removed from subsequent test results.

The thermal profile used to condition the samples was -55 to +125°C with 5min dwells and a ramp between dwells of 10 °C/min, and is shown in Figure 1.

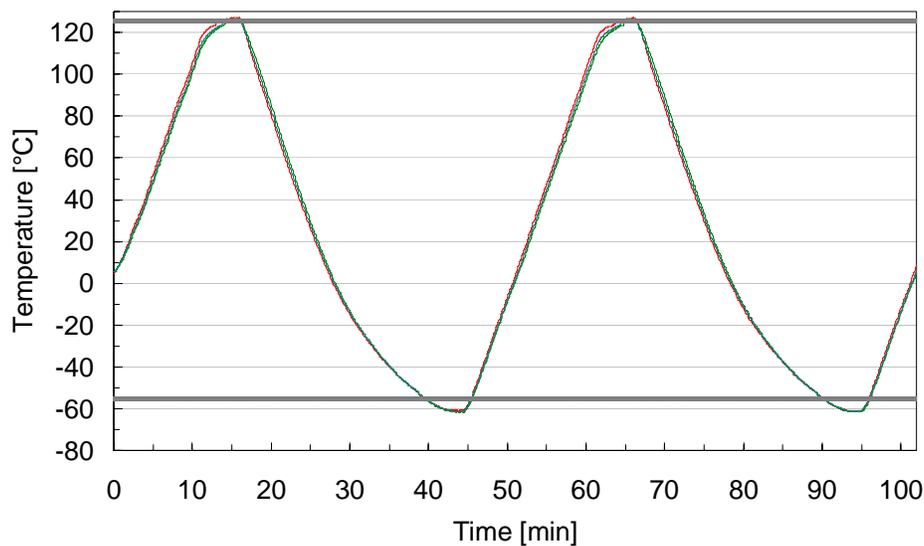


Figure 1 - Thermal cycling profile (-55 to 125°C, 5min dwells, ramp 10°C/min)

DEFINING DIFFERENT VOIDING LEVELS

The initial phase of the solder paste trials were intended to identify three levels of voiding appropriate for the reliability evaluation, in which three sets of samples were to be assembled at these voiding levels. The desired voiding levels were intended to be very low (or zero) average voiding, moderate average voiding levels around 10%, and a high average voiding

level around 20+%. However, in this work generating average voiding levels above 5% proved impossible. **Figure 2** demonstrates the effect of profiling on the voiding levels in a BGA of three different paste types from a single manufacturer. Profiles 1, 2 and 3 have progressively faster times to peak temperature, the intention being to reduce the amount of pre-heat on the paste and increase the level of volatiles present during reflow. There was little difference between the pastes or the profiles with average voiding levels only varying between 1.8 and 3.3%, with the largest voiding in any ball varying between 9 and 13%. Again all of these voiding levels are well below the 25% maximum voiding level specified by IPC (Reference 13).

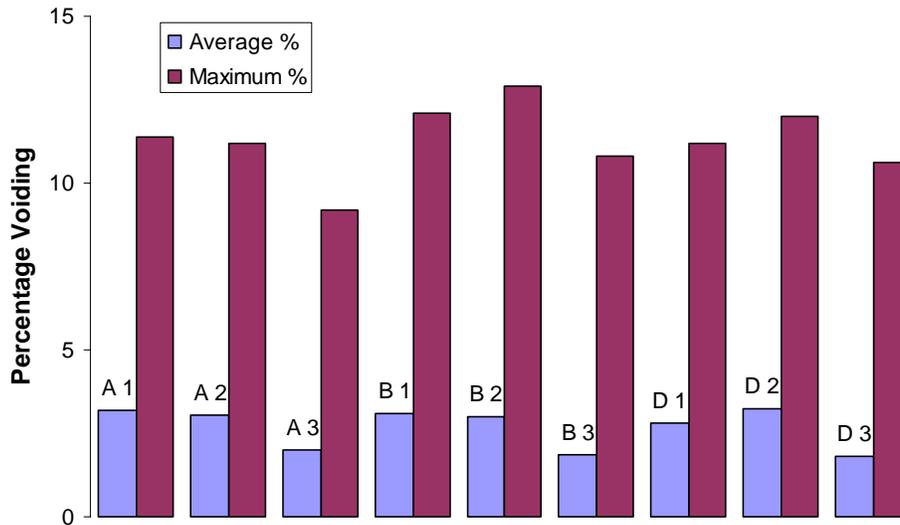


Figure 2 - Comparison of average and maximum BGA voiding for three pastes using profiles 1, 2 and 3

As a result of this work, in which seven different solder pastes have been evaluated with 3 reflow profiles, end-users can have a high degree of confidence that voiding levels in lead-free solder pastes can be kept below the IPC specified maximum of 25% by area.

TEST VEHICLE VOIDING LEVELS

From the earlier phase three different profiles were chosen to give low, medium and high voiding levels.

R1206 Voiding Levels

Example images for the L, M and H assembly sets are presented in **Figure 3**. As with the R0603 components, autocalculation was not possible, but again it is clear that in common with the R0603 and PBGA results, voiding levels in the R1206 components were generally low, with voiding levels increasing from L through M to H levels.

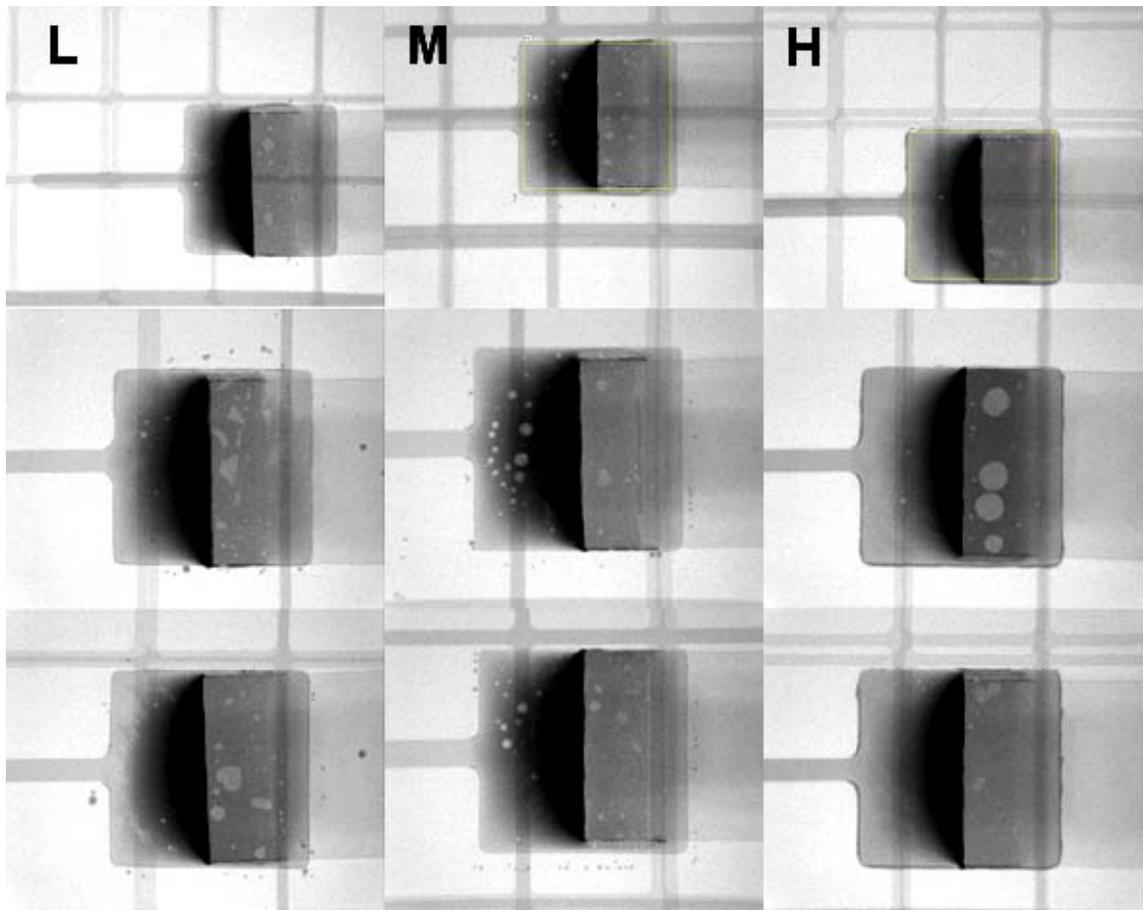


Figure 3 - Example images of R1206 for L, M and H voiding levels

With SOIC voiding levels voiding levels were generally low, with little difference between the L, M and H levels.

PBGA Voiding Levels

The results for the PBGA components from the three profiles in manufacturing ten identical assemblies are shown in **Figure 4**. All these profiles produced voiding levels less than the maximum 25%, permitted by the IPC A610 visual inspection guidelines (Reference 13). IPC 7095 (Reference 5) assembly and inspection guidelines for BGAs, call for a more stringent maximum voiding level than IPC A610. This maximum level is 9% on a sample basis for voids within the joint after reflow. Using angled transmission X-ray inspection, the location of the voids created in these samples was determined to be in the bulk solder of the joints. Thus from **Figure 4**, it can be seen that all three sets of samples contained individual voids greater than 9%, but the occurrence of these is infrequent, and being less than 1% of all voids for each set. Set H has the highest level of voiding over 9% with 0.5% of voids being above this figure. Example images of PBGAs from each voiding level are presented in Figure 7.

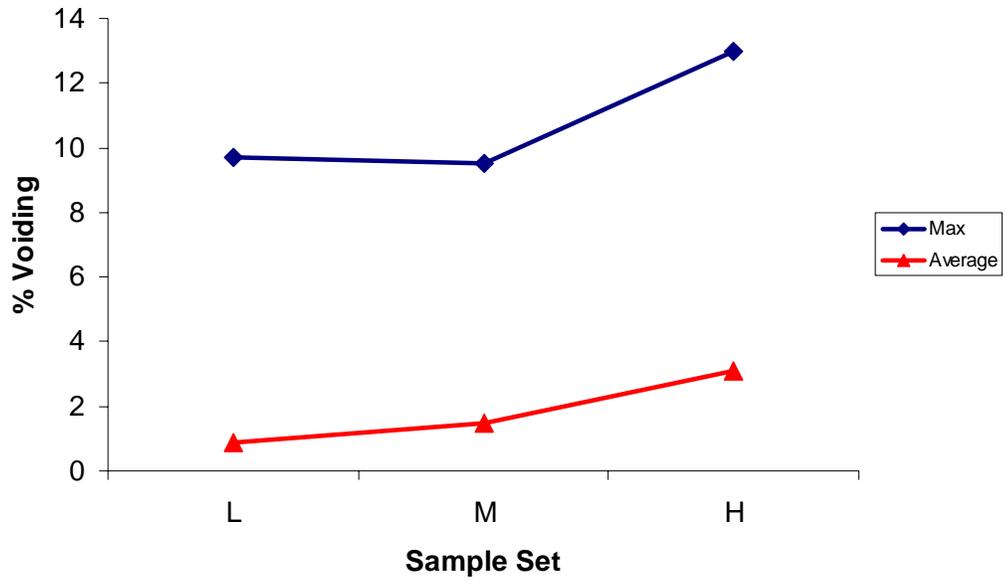


Figure 4 - Comparison of average and maximum voiding levels for phase 2 samples

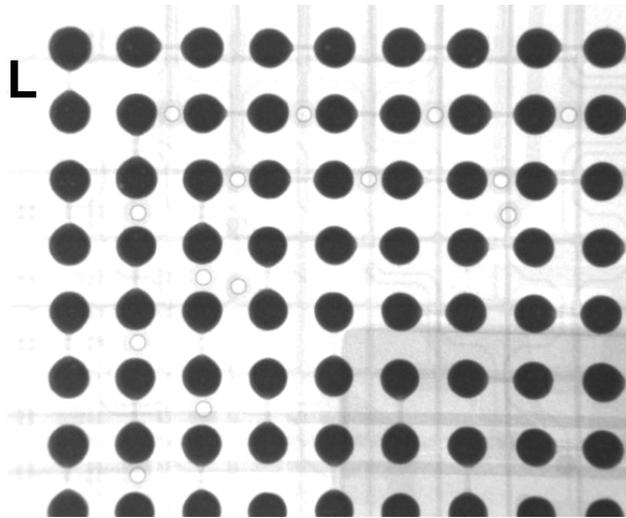


Figure 5a - Example images of PBGA for L voiding levels

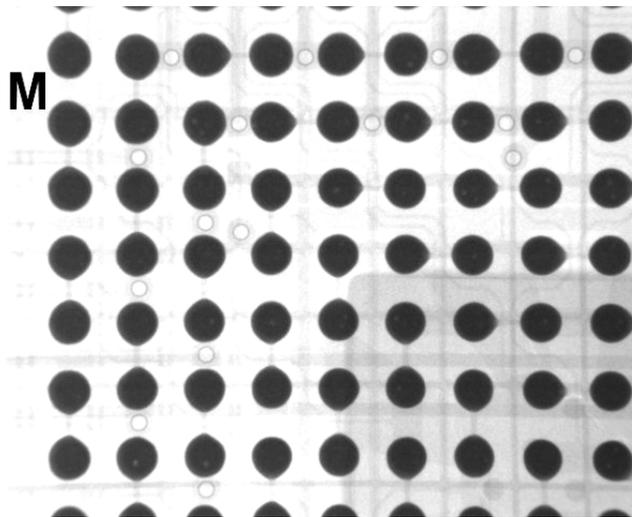


Figure 6b - Example images of PBGA for M voiding levels

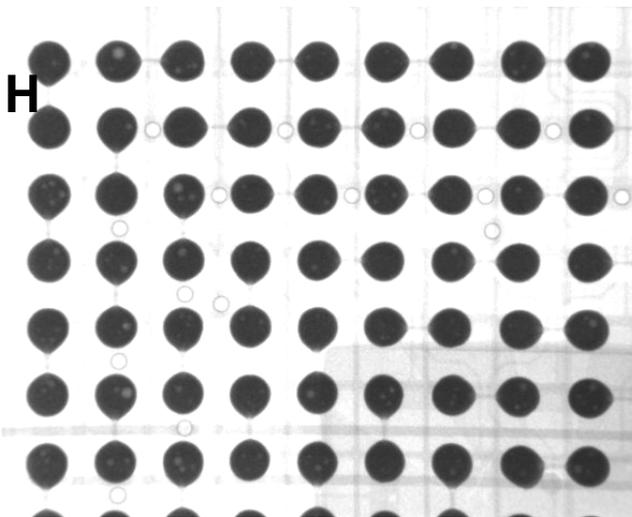


Figure 7c - Example images of PBGA for H voiding levels

RELIABILITY TEST FAILURES

R1206 Failures

Figure 8 shows the comparison of the electrical failures for R1206 components. These three data sets show very little difference, indicating no apparent change in reliability for the voiding levels generated.

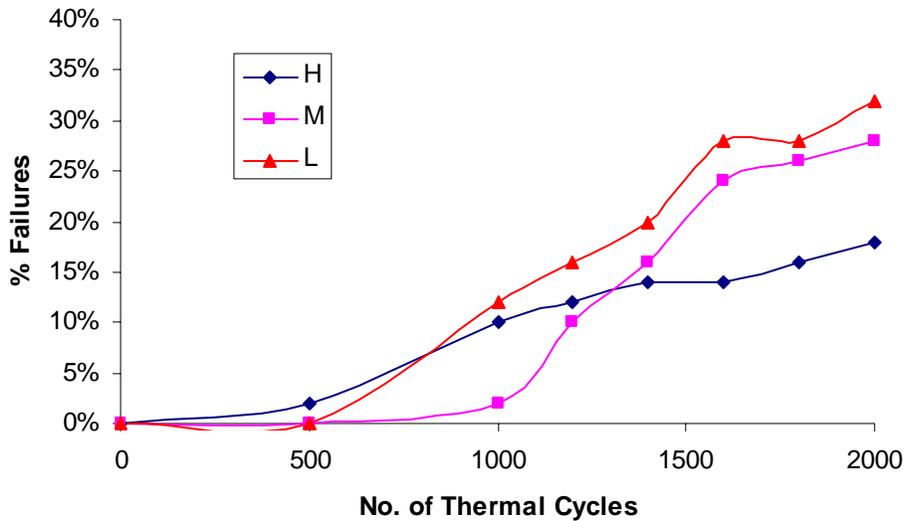


Figure 8 - R1206 electrical test failures

R0603 Failures

The failures for these components were somewhat higher than would normally be expected for this component type after 2000 thermal cycles. This may be due to via failures, which could not be eliminated from the data as the vias within the electrical test circuit were sited close to the component joints and could not be probed reliably without affecting the soldered joints.

PBGA Failures

All PBGA failures occurred in the rings of ball interconnects immediately adjacent to edge of the silicon die. Sets of interconnects of increasing radius were daisy chained into four circuits, the C-ring straddled the edge of the die. Here the TCE of the device is constrained by the low TCE of the die, and the difference is at a maximum from the TCE of the substrate. Because of this difference and the distance from the centre of the device, joints in this region are subjected to the most strain, and are therefore likely to be the least reliable. These results are shown in Figure 7. However, after 2000 thermal cycles, there is little difference between the reliability of the PBGA components in the three data sets. An attempt was made to correlate the occurrence of large voids (greater than 10%) with failures in C-rings of the PBGAs. However, joints with large voids occurred in both failed and reliable interconnection rings. Therefore, the position of a joint and its proximity to the edge of the die, have much greater significance than the levels of voiding investigated in this work.

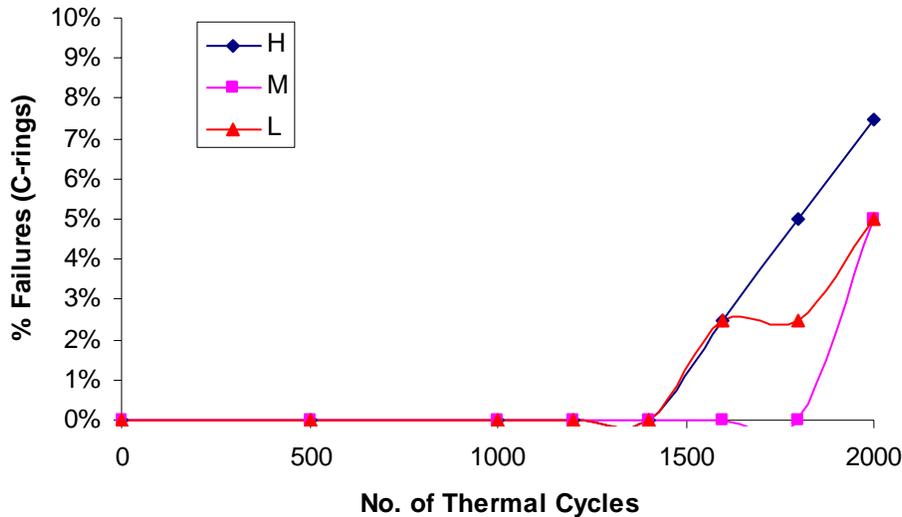


Figure 9 - PBGA Electrical Test Failures

SHEAR TEST RESULTS

Shear tests results for both the R1206 and R0603 components there were no significant differences between the shear strengths for any of the three voiding levels.

CONCLUSIONS

- *SM assembly using lead-free solder technologies processed under a wide range of conditions has not produced high levels of voiding.* This robustness of the lead-free technologies will be welcomed by industry and ease its current worry that lead-free solder joints might be prone to high voiding levels.
- Earlier work (Reference 14) had demonstrated that with solder joints assembled using conventional SnPb alloys, it was possible to incur high levels of voiding (<20% by area). However, in the present work it has not been possible to produce such high levels of voiding. *All the voiding levels recorded were well below the permitted levels (25% by area) in IPC A610 revision D.* Average values were in the range 2-4%, although individual values reached 13%.
- These low voiding levels were consistently encountered across a wide range of lead-free solder technologies. The evaluation involved seven solder pastes (six no-clean; one water-soluble) from three suppliers processed through a range of reflow profiles. In addition, some of the PCB test boards had been subjected to artificial ageing, and the water-soluble paste had been subjected to damp-heat ageing, in an attempt to produce “worst case” conditions.
- The three levels of voiding available for Phase 2 were in the range up to 13% by area, and test boards were subjected to extensive thermal cycling (2000 cycles from -55 to +125°C). However, there were no discernable differences in the reliability of the joints as monitored using (a) electrical resistance, (b) shear strength, or (c) shear strength deterioration during thermal cycling. Since the IPC 7095 guidelines for class 3 BGAs call for a maximum voiding level of only 9% (cf 25% for IPC A610) the results clearly suggest that if the IPC maximum voiding levels are adhered to, there will be no adverse effect from voiding on the reliability of lead-free solder joints – a conclusion that will be welcomed by manufacturers and end users of lead-free assemblies.

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ACKNOWLEDGMENTS

The authors are grateful for the support of the DTI as part of its MPP Programme, and of AMS, Goodrich, Matra BAe, BAe Systems, TRW Automotive, Loctite Henkel, Heraeus, ESL and Dage Group for their contributions throughout this project. The authors are also grateful to members of the projects industrial advisory group for useful discussions throughout the work.