Assembly Verification of an Immersion Silver Finish with Enhanced Tarnish Inhibition

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Abstract
New ROHS standards are forcing the electronics industry to find a replacement for leaded surface finishes. Even more rapidly than the legislative decision to move away from lead, electronics were moving to much smaller, faster and higher function applications. Not only does the new surface finish have to be lead free but it will have to perform with circuit designs that are increasingly challenging. A flat, planar surface is an obvious and minimum requirement. Beyond this, a preferred finish should be simple to apply, consistent in performance, and durable/resistant to aggressive and corrosive environments.

A final finish that has been able to deliver a planar surface for the solderability of fine components as well as maintain ease of use for fabricators is immersion silver. In recent years, immersion silver has grown as the final finish of choice for a large variety of end use applications. Immersion silver has a wide variety of fabrication/manufacturing and functional advantages over other lead free surface finishes. One shortcoming of immersion silver is its potential to tarnish in sulfur and sulfide environments. A post treatment has been developed which delivers significant tarnish inhibition to thin silver coatings, translating to a more robust and corrosion resistant finish. This work investigates and verifies the effectiveness of a tarnish inhibited coating, with focus on confirming the coating's compatibility in modern, fine-pitch assembly applications. Controlled assembly studies focus on wetting characteristics, solder paste compatibility, and bridging risks are discussed.

Introduction
Immersion Silver continues to grow as a final finish of choice for a diverse variety of end use applications. Originally, immersion silver was formulated as a hot air solder level replacement. A great amount of maintenance was associated with HASL. Fabricators were continually fixing the HASL machine. Then as technology improved, circuit boards became smaller, thinner and contained finer pitched devices all more densely populated. The application of HASL became more critical. There was a strong push to make the surface flat for placement of the components but an even greater issue was that thin board designs were warping and twisting under HASL temperatures. The shortcomings of HASL became too great. Many fabricators and OEM's knew that the need for better final finishes was a must. At the time, the driving forces made organic solderability preservatives (OSP), electroless nickel/immersion gold (ENIG), immersion tin, and immersion silver potential replacement choices.

As time progressed, to current day applications, the demand placed on the surface finish has become even more challenging. Surface features are smaller and the ROHS regulations have pushed leaded solders out of assembled products completely. The move to lead free solder has been a major undertaking for the electronic industry. A few lead free alloys are now commonly used; these various alloys require different peak temperatures for the solder to liquefy. During assembly, circuit boards are reaching higher temperatures than ever before, greater than 20°C above leaded solder liquidous. Not only does the laminate itself have to hold up to these elevated temperatures but the surface finish must be able to withstand multiple reflows before final assembly is completed. The final finish must be able to withstand the high temperatures and remain solderable.

These extreme temperatures have pushed conventional OSP out of the market. Chemical suppliers are forced to reformulate OSP baths to resist change to high reflow peak temperatures. Even the new formulation can suffer from poor performance after multiple reflow due to breakdown of the coating which leads to oxidation of the underlying copper. Immersion tin suffers the inherent problem of losing pure tin to the intermetallic layer. As the reflow temperatures increase, the lose of tin is more rapid, the resultant intermetallic is unsolderable.

Immersion silver does not suffer from solderability problems inherent to OSP and immersion tin. The silver coating is largely unaffected by heat cycles, neither significantly degrading nor forming a harmful intermetallic with the underlying copper. As a result, the silver finish has very good wetting characteristics. Silver does, though, have one commonly discussed shortcoming: limited tarnish resistance.

The effect of tarnish on the practical functionality of a silver finish has been covered in prior work, "Surface Tarnish and Creeping Corrosion on Pb-Free Circuit Surface Finishes" by Cullen[1] and "Enhancing the Tarnish Performance of Immersion Silver Finishes" by Swanson and Norwood[2]. In the majority of environments, a minimal to moderate amount of silver tarnish, largely due to silver sulfide and sulfate, maybe observed between board fabrication and assembly. These levels of tarnish have been shown to be extremely thin and largely innocuous to the functional performance of the surface. As silver proliferates as a finish of choice, though, it may be deployed in a wider variety of geographies and board fabrication environments, some of which are more aggressive to the silver finish. Beyond this, standard packaging and handling errors increase the risk of tarnish growth. These threats to the silver surface highlight the benefit that a functional, low-cost, and tarnish-inhibiting protective layer may bring to some applications.

Metal Deposition

Immersion silver has become a very successful alternate final finish in the electronics market. Its attributes are seen during fabrication, at the assembly house, and in its final end-use application.

Fabricators enjoy the ease of use and low maintenance of immersion silver. The cycle time is short in comparison to other final finishes like electroless nickel/immersion gold and immersion tin. These final finishes can run in an excess of 50 and 30 minutes, respectively. Standard immersion silver cycle time ranges about 22min in vertical processing and 10min horizontal processing. Immersion silver baths are very stable and easily analyzed. Immersion tin working baths as well as bath make up components continuously suffer from oxidation of Sn^{2+} to Sn^{4+}. ENIG has a lengthy, complex analysis cycle which makes the chemistry more difficult to control.

To make the silver finish even more robust, a simple and effective tarnish inhibitor has been developed and deployed commercially in high volume. Application of the tarnish inhibitor simply involves the addition of one tank or module to an already existing line, or a simple and separate post-treatment following immersion silver plating. The standard dwell time runs from 30 seconds to one minute. Bath analysis is quick and easy, the process chemistry is stable and environmentally benign. In brief, the tarnish inhibitor selectively forms a protective film over the silver finish, leaving other parts of the circuit board untouched. Though the film is very effective at repelling corrosive agents in the environment, it is also extremely thin. This film, which is on an Angstrom level of thickness, has been shown to have no effect on contact resistance, nor any significant effect on the solderability of the silver coating[2].

Resistant to Aggressive Environments

The following sections will discuss the effects of aggressive environments on the immersion silver finish and immersion silver with the tarnish inhibitor. Experiments will also be discussed that display the solderability performance of the immersion silver deposit and help to depict the increased protection supplied by the tarnish inhibitor. The results will help to display its resistance to the aggressive environments without sacrificing solderability.

One specific experiment used to test the tarnish resistance and functional performance of immersion silver versus immersion silver with the tarnish inhibitor was to subject the boards to different contaminated environments. The boards were than analyzed for tarnish resistance and solder performance.

Sets of samples were plated with immersion silver and with immersion silver plus the tarnish inhibitor. The samples were then exposed to three different environments. The first set was wrapped in sulfur free paper, this set is considered the control. The second set was exposed to a manufacturing atmosphere where all board fabrication chemical processes were being used. Samples were kept in this environment for 36 hours. The final conditioning step was to expose the third set of coupons to a sulfur rich environment. A mixture of sodium bisulfide, hydrochloric acid and water are enclosed in a heated chamber with the presence of humidity for 15 minutes.

Visual appearance of the metal area on all samples was observed optically. Every sample wrapped in sulfur free remained unchanged; they maintained a silver appearance. Samples exposed to the manufacturing environment displayed differences between the two surfaces. Samples plated with silver only turned uniform yellow. The samples with the tarnish inhibitor were unchanged. Finally, the samples exposed to the sulfur rich atmosphere displayed similar appearance changes to those left in the manufacturing atmosphere. The immersion silver surface turned yellow where as the inhibited finish was unchanged.

To determine the effects of the environments described above on the surface, a solder spread test was conducted. The specific solder paste test used varied the aperture openings of a quad flat pack design. A 22 by 88 mil pad was reduced in increments along all four sides of the component (Figure 1). After printing lead free solder paste through a 6-mil stencil and reflowing the samples through a convection oven, the boards could be analyzed for solder spread. The percent solder spread was measured as the smallest amount of paste printed to flow the entire length and width of the pad. Four sides per quad flat

pac were analyzed as well as three replicates for each condition. The data bars in Figure 2 represent a total of 12 data points per bar. It was determined that the surface finish and the conditioning had no effect on the wetting of the samples, overall, solder spread was very consistent.

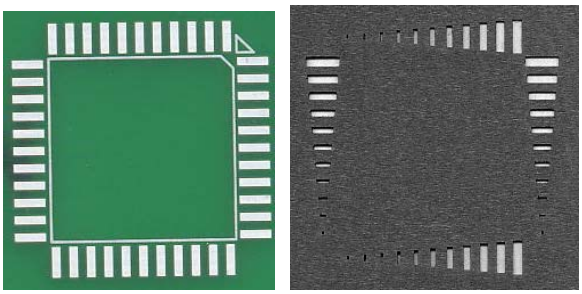

Figure 1 - Varied Aperture Quad Flat Pack Board and Stencil

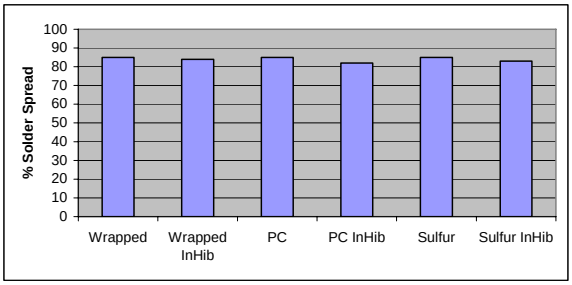

Figure 2 - Solder Spread Data

The IPC and JIS Hot Slump test

Additional solder spread tests were used to assess the performance characteristics of immersion silver versus immersion silver with the tarnish inhibitor. These tests included variations on an IPC slump test, a JIS hot slump test and standard wetting balance testing. The IPC Solder Paste Slump Test[3] (IPC-TM-650 2.4.35) and the JIS Hot Slump[4] (Annex 7) test are normally used to determine the characteristics of a solder paste. The term slump is used to understand the change in shape of a pasted area when exposed to drying or heating[4]. By running this test with an established solder paste under identical conditioning for two substrates, one can determine the differences between the surfaces. In this case, the two samples tested were immersion silver only and immersion silver with the tarnish inhibitor. For both test types an 8 mil stencil was used.

In the first experiment the IPC stencil pattern was printed on each of the coated surfaces. The samples were then placed in a batch oven at 150ºC for 10 minutes. The data was recorded as the distance between two pads that are joined together by solder flow. All measurements were recorded in mm. The spread data (Table 1) did not show differences between the two surfaces. The test was then repeated with the JIS Hot Slump stencil design. This test showed a variation in solder slump distances (Table 2) which indicated a difference in surface tension of the two coatings. The immersion silver alone displayed more slumping than silver with the inhibitor. This indicated that the surface coated with the tarnish inhibitor had a higher surface tension than silver alone. This point may help to explain its resistance to the effects of surface contaminates.

Table 1 - IPC Hot Slump Test

Board coating	IPC Hot slump	
	Paste 1	
	0.33x2.03mm pad	0.63x2.03mm pad
Inhibitor	0.1 - 0.15	0 - 0.33
	0.1 - 0.15	0
Immersion Ag	0.15 - 0.2	0 - 0.33
	0.15 - 0.2	0

Table 2 - JIS Hot Slump Test

Board coating	JIS Hot slump	
	Paste 1	
	3x0.7mm pad	3x1.5mm pad
Inhibitor	0.2	0
	0.2	0
Immersion Ag	0.3	0.4
	0.3	0.4

To further understand the functionality of the surface finishes a second variation on the JIS slump test was used. For this test, the two surface finishes were separated into two groups. One set was kept as plated and the second was processed through one lead free reflow excursion. Soldering the two groups would help to simulate first and second side assembly. The JIS stencil design was used to print solder onto the board surfaces. The samples were then processed through a standard reflow profile. The samples were run in duplicate for reproducibility. The analysis was the same as used above. The data indicated (Table 3 and 4) that there is no statistical difference in solder spread between the two surfaces.

Table 3 - as Plated Solder Spread

Board coating	Wetting As Plated									
	Paste 1									
	3x0.7mm pad					3x1.5mm pad				
	row 1	row 2	row 3	row 4	row 5	row 1	row 2	row 3	row 4	row 5
Inhibitor	0.4	0.4	0.4	0.5	0.4	0.4	0.2	0.2	0.2	0.2
	0.4	0.4	0.5	0.4	0.5	0.2	0.2	0.2	0.4	0.6
Average	0.43					0.28				
Std Dev	0.048					0.140				
Immersion Ag	0.3	0.4	0.4	0.4	0.4	0.5	0.5	0.5	0.5	0.5
	0.3	0.3	0.3	0.3	0.4	0.5	0.5	0.4	0.5	0.6
Average	0.35					0.5				
Std Dev	0.053					0.047				

Table 4 - Solder Spread After Reflow Excursion

Board coating	Wetting After One Reflow Excursion									
	Paste 1									
	3x0.7mm pad					3x1.5mm pad				
	row 1	row 2	row 3	row 4	row 5	row 1	row 2	row 3	row 4	row 5
Inhibitor	0.3	0.5	0.5	0.3	0.4	0.6	0.7	0.5	0.5	0.6
	0.5	0.5	0.5	0.3	0.3	0.5	0.5	0.5	0.5	0.7
Average	0.41					0.56				
Std Dev	0.099					0.084				
Immersion Ag	0.3	0.3	0.3	0.5	0.4	0.6	0.6	0.6	0.6	0.6
	0.5	0.3	0.3	0.5	0.4	0.4	0.5	0.5	0.6	0.6
Average	0.38					0.56				
Std Dev	0.092					0.070				

The next lab test run was a standard wetting balance test. It was hypothesized that the wetting balance is the most discerning tool when considering small changes in surface wetting. The standard wetting balance testing was conducted on the two finishes using a lead free SAC alloy solder paste. Samples were tested on a Multi Solderability Tester SWET 2100. The flux used was specific to the type 1 pasted used in the previous solder spread tests. The samples tested were 0.6mm by 30mm copper wires that had been plated in silver and silver with the tarnish inhibitor. The solder paste was placed in a small cup below the hanging wire. The solder paste was then heated to liquidious. Once the solder was melted, the samples were inserted at a speed of 2mm/sec to a depth of 2 mm and held in the solder pot at 250ºC for 10 seconds. Nine replicates of each surface are averaged in the Table 5 below. Results were based on time to bouyance (Tb), total wetting time (T2) and force max (Fmax). The wetting balance data for the two surface finishes were very similar. Figure 3 clearly shows similar time to bouyance, total wetting time, and force max. They are statistically the same.

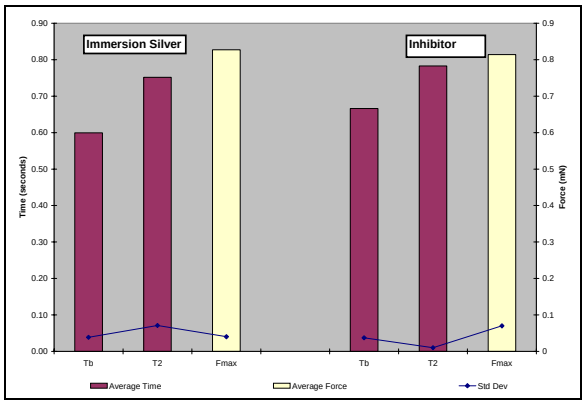

Figure 3 - Wetting Balance Data

Assembly

MacDermid has implemented the silver tarnish inhibitor in a high volume production environment. The finish has been running well for a variety of board designs. As a more extensive look at the effects of the coating on the plated surface, a design of experiments was executed to better understand any differences between the surface finishes and also determine the effects of varied assembly conditions.

Figure 4 - Assembled 16-mil Pitch QFP Device with Silver Inhibitor Finish

The design focused on the lead free assembly of a 16mil-pitched quad flat pack plated with immersion silver and immersion silver with the tarnish inhibitor. Factors of the experiment included two paste types, three aperture openings, and varied reflow pre-heat lengths. Both pastes were lead free but with different flux packages. The aperture openings to be pasted varied from 90 % of the pad length to 100 and 110%. The aperture openings were tested at both 7 and 7.5 mil wide on a 10-mil surface pad. The main portion of the reflow profile that was varied was the length of the pre-heat. The three levels included 128, 148, and 178 seconds. All other conditions of the reflow profile were kept as consistent as possible.

Production board designs were automatically printed; the boards then traveled to a pick and place machine where the fine pitch component was positioned. For each board, two quad flat pack areas were printed. A component was placed on one of the areas and the other was left as paste on pad. Both areas were analyzed for bridging prior to component placement and after reflow. Solder spread was analyzed on the surfaces pads in two ways. The first was to identify the amount of spread over a reduced printed area. The second was to observe any wetting defects such as de-wetting or non-wetting. All responses were analyzed using statistical software.

The solder spread was recorded as a numerical scale to show variation in flow observed. A 1 indicated that there was no movement of paste from where it had been printed. A 2 designated spread to the edge of the pad on the left and right side

(width) but no spread in the length of the pasted area. A 3 rating, thought similar to a #2 indicated further spread of the paste along the length of the pad. Finally, 4 represented full solder coverage over the entire pad. Figures 5 and 6 show the effect aperture opening had on the amount of solder spread. As to be expected, the quantity of paste printed on the pad surface had the largest effect on the amount of solder spread. For example 90% pasted areas displayed the least amount of spread throughout the experiment. Figures 5 and 6 are identical though they represent the wetting differences of the two finishes. Comparison of the two graphs indicates that the surface finish has no effect on the solder spread, the two behave exactly the same. The largest influence was seen in the length of the pre-heat. Figures 7 and 8 show the pre heat effects on the solder spread. Comparison of the two graphs shows that with a longer pre heat (Figure 8) has greater solder spread. The black and red lines within the charts represent immersion silver and the inhibitor, respectively. Assemblers should fully understand the effects of proper profiling to the surface finish performance.

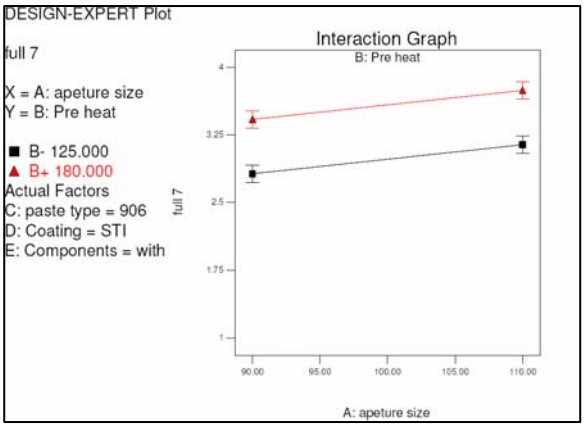

Figure 5 - Spread Data on Inhibitor

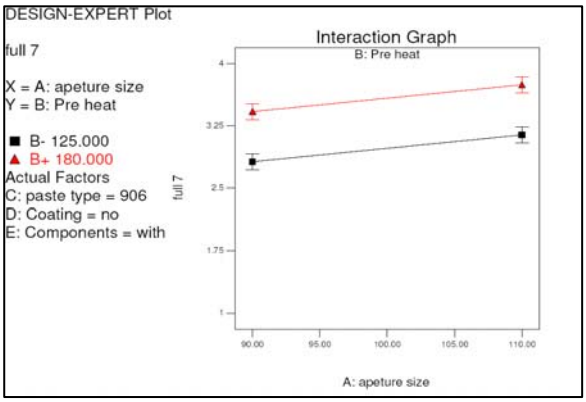

Figure 6 - Spread Data on Immersion Silver

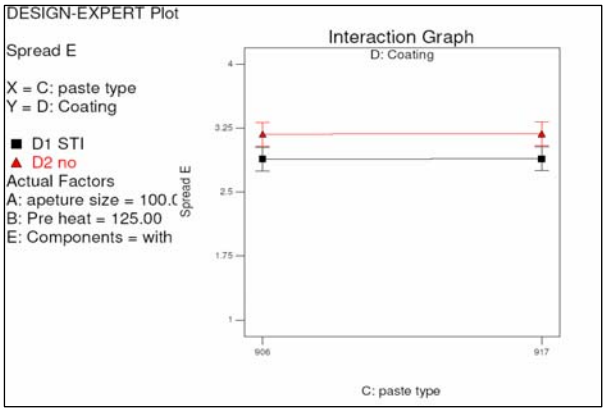

Figure 7 - Spread Data Using 125 sec Pre-heat

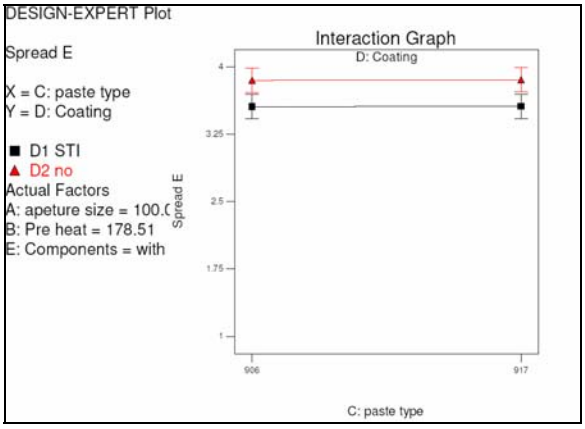

Figure 8 - Spread Data Using 178 sec Pre-heat

The other pasted areas observed all displayed uniform wetting over the entire pads. Statistical analysis of this response could not be tabulated because there was no observable difference between any of the samples. The result does indicate again that there is no wetting difference between the two surfaces.

Because fine pitch components can be prone to bridging, the final response was to observe any bridging that may have resulted during the reflow process. Similar to the solder spread data, the percent of the pasted area was shown to have the greatest effect on bridging. Where 110% of the pad had been pasted there was a stronger occurrence of bridging. Also the designs with the component placed had more occurrences of bridging. Along the same lines, the width of the pasted area had a large effect on the presence of bridging. Samples that were printed 7.5mil wide on the 10mil pad had a slightly higher level of bridging. Out of 3080 analyzed areas there was a total of 19 bridge sites on the 7.5mil prints and 14 on the 7.0mil prints.

Conclusions

As electronic assemblies have transitioned into a Pb-free world, Immersion Silver has emerged as one of the most preferred final finishes for printed circuit boards. Its popularity is attributable to its versatility and strong performance in fabrication, assembly, and end-use environments. One drawback commonly discussed for immersion silver is its susceptibility to tarnishing. This paper has described the benefits of a simple and easy to use tarnish inhibitor post treatment for immersion silver; it shows this tarnish inhibitor to effectively stop the growth of tarnish films between board manufacturing and assembly, even in harsh environments. Furthermore, this paper communicates a body of work in which the tarnish inhibitor had no negative effect on the solderability and overall functionality of the silver-plated board. This work shows assembly parameters such as solder paste footprint and pre-heat cycles to be more influential on assembly yield.

References

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