Application Assessment of High Throughput Flip Chip Assembly for a High Lead-Eutectic Solder Cap Interconnect System Using No-Flow Underfill Materials

David Milner and Daniel F. Baldwin, Ph.D.
Packaging Research Center
The George W. Woodruff School of Mechanical Engineering
Manufacturing Research Center
Georgia Institute of Technology
Atlanta, GA

Abstract
Flip Chip on Board (FCOB) is one of the most quickly growing segments in advanced electronic packaging. In many cases, assembly processes are not capable of providing the high throughputs needed for integrated Surface Mount Technology (SMT) processing.[1] A new high throughput process using no-flow underfill materials has been developed that has the potential to significantly increase flip chip assembly throughput. Previous research has demonstrated the feasibility and reliability of the high throughput process required for FCOB assemblies.

The goal of this research was to integrate the high throughput flip chip process on commercial flip chip packages that consisted of high lead solder balls on a polyimide passivated silicon die bonded with eutectic solder bumped pads on the laminate substrate interface.[2] This involved extensive parametric experimentation that focused on the following elements: no-flow process evaluation and implementation on the commercial packages, reflow profile parameter effects on eutectic solder wetting of high lead solder bumps, interactions between the no-flow underfill materials and the package solder interconnect and tented via features, void capture and void formation during processing, and material set compatibility and the effects on long term reliability performance.

Introduction
Several processing and reliability concerns were considered during these experiments. Eutectic solder wetting on high lead solder was provided with 100% interconnect yield by using an additional process step utilizing an light abrasive removal of over-developed eutectic solder oxides combined with thermal cure cycles optimized for each tested no-flow underfill. The optimized thermal cure cycles further improved the assembled packages by limiting outgassing from tented vias and eutectic solder bumps on the substrate during the thermal ramp-up. Accelerated reliability testing was conducted on the two no-flow underfills with the best results and one was determined to satisfy company reliability criteria.

The high throughput flip chip assembly process shown in Figure 1 utilizes newly developed underfill material systems to effect improved assembly throughput.[3,4,5]

The process begins with known good substrate and die. A controlled volume of no-flow underfill material is dispensed or stencil printed onto the substrate bond site. The chip is aligned and placed onto the bond site using a high-speed flip chip placement system. The chip compresses the underfill forcing the formation of partial underfill fillets. Finally, the solder interconnects are reflowed simultaneously while the no-flow underfill is cured in a single thermal cycle. The underfill both fluxes the solder bumps promoting interconnect formation and cures to provide a mechanical bond between chip and substrate following reflow leveraging the unique latent cure characteristics of the no flow underfills.[3,4,5] The process therefore excludes underfill capillary flow and the secondary thermal process steps present in conventional flip chip assembly techniques thereby resulting in an increased chip production throughput.

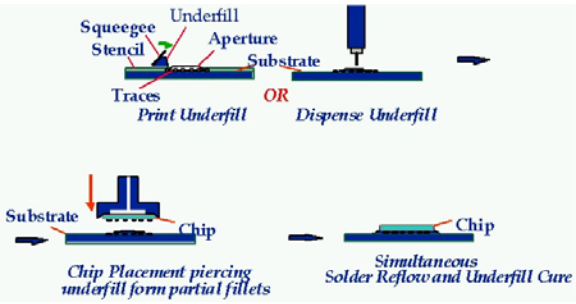


Figure 1 - High Throughput Flip Chip Process

The high throughput flip chip-attach process, also know as the "no-flow" process, has significant potential to replace the conventional flip chip attach process. Reasons for this include the elimination of several processing steps, the reduction of process complexity, reduction of capital equipment requirements, reduction of equipment maintenance,

and enhancement of process robustness. Cost modeling and analysis comparing a typical industry flip chip process, the low cost high throughput (no-flow) process, and surface mount assembly[3,4] quantitatively describe how the no-flow process has the potential to greatly enhance profit margins. Therefore, much research has been conducted to develop the process and the corresponding materials to make the technology transparent to current assembly lines.[3,4,5]

This study focused on the development and analysis of the no-flow process on a commercial flip chip package. This assembly consisted of 97/3 Pb-Sn bumps (high-lead solder) on the chip interface and 37/63 Pb-Sn caps (eutectic solder) on copper metallization on the board interface as shown in Figure 2. This interconnection composition showed inconsistent results in obtaining yield in preliminary tests relative to homogeneous eutectic solder interconnect systems, leading to the detailed testing.

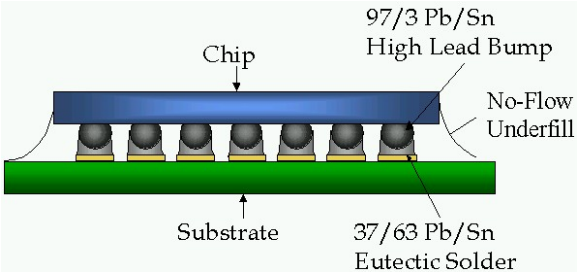


Figure 2 - High Lead on Eutectic Solder Interconnects

Experimental Procedures

The experiments focused on the development and application of the high throughput process on commercial packages utilizing the high lead on eutectic solder interconnect systems. Two sets of experiments were conducted to determine the effects of thermal reflow cycle settings (experiments 1a and 1b) and pre-assembly solder surface treatments (experiments 2a and 2b) on interconnect yield and underfill voiding in packages assembled with no-flow underfills. The final experiments (experiment 3) were conducted to determine the accelerated reliability performance of no-flow underfill materials utilizing process settings that provide optimal interconnect yield and underfill voiding characteristics.

Experiment 1a

Prior experimentation revealed inconsistencies in eutectic solder wetting of high lead solder and subsequent interconnect formation in the assembled packages utilizing conventional no-flow underfills. The first experiment 1a was used to determine the main effects of four reflow process variables on interconnect yield in test vehicles using no-flow underfill materials. The experiment examined the effects of reflow profile ramp rate, peak temperature, time above 183ºC, and soak time between 120ºC and 170ºC varied parametrically as shown in Figure 3. The purpose was to determine the impact of these reflow process variables on the relative amount of solder wetting of eutectic solder and high lead solder interconnects of test vehicle 1.[6,7] Seven no-flow underfill materials A, B, C, D, E, F, and G were tested with reflow profiles and relevant parameter setting levels based upon precedented reflow settings derived by manufacturers and previous research for each underfill.

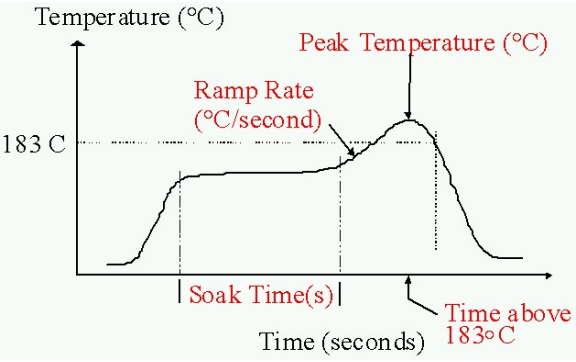


Figure 3 - Reflow Profile Varied Parameters

Experiment 1b

The primary goal of this experiment was to determine the effects of thermal reflow profile parameters on both interconnect yield and underfill voiding in commercial packages of test vehicle 2. Commercial packages were assembled using select no-flow underfill materials in an experiment varying thermal reflow profile parameters as in experiment 1a. Four additional underfills were added to this experiment, two variations each of underfill C and F with varying flux activity. Interconnect yield and underfill void efficiency were examined for each underfill to determine the correlations between substrate feature and void locations.

Experiment 2a

The purpose of this experiment was to determine the effects of surface treatment and cleaning steps relative to the eutectic solder interconnect surfaces prior to package assembly. The experiment tested several potential procedures to remove excessively thick oxide layers on the eutectic solder surfaces that inhibit solder wetting and thus interconnect formation. The experiment involved construction of test vehicle 2 parts with replicates for each of the following process conditions:

1. Control assemblies using the high throughput process (no treatment steps)
2. Assemblies using substrate organic pre-clean step prior to chip attach
3. Assemblies using a substrate UV-ozone pre-clean prior to chip attach

4. Assemblies using an underfill pre-wipe step on the bond site prior to chip attach.

The organically pre-cleaned components were cleaned using a series of 3 minute sequential ultrasonic cleaning steps of acetone, methanol, isopropanol, and de-ionized water followed by an 8 hr, 130C pre-bake of the parts. Ozone cleaned parts incorporated a UV-ozone-cleaner to strip off organic contaminates on the substrate prior to assembly. The pre-wipe method involved a standard no-flow underfill dispense onto the substrate followed by its removal by manually wiping the site clean. All pre-clean steps were conducted within 20 minutes of the no-flow assembly except those with the organic pre-clean, which required a pre-bake step before assembly. All assemblies were constructed using underfill F in a parametric series of multiple runs including replicates and utilizing underfill F's optimized reflow profile. Each treatment was conducted in a randomized order.

Experiment 2b
The purpose of this experiment was to determine processing feasibility of the pre-treatment methods to promote the desired assembly results in three specific underfill materials. The underfills were commercial underfills A, F, and G were assembled using optimized reflow profiles and replicates of each pre-treatment method to determine which methods could be effectively utilized in final test assemblies. The tested methods included underfill pre-wiping of the substrates, flux-refire pretreatment of the substrates, and flux removal methods for the flux-refire pretreatment.

The underfill pre-wipe method incorporated a wipe removal of the pre-dispensed underfill. The flux-refire method was a newly developed processing idea more easily implemented into present-day assembly lines because it lacks the wipe component of the previous method. The flux-refire method incorporated the deposition of a water-soluble flux and reflow followed by reflattening of the bumps on the substrate. This was followed by one of two cleaning steps. The cleaning step for the flux-refire method was either a water jet rinse of the substrates with no bake out, or a 30 second ultrasonic bath clean with a 30-minute convection oven bake-out to remove absorbed water.

Experiment 3
The purpose of this experiment was to test the no-flow underfilled commercial packages in accelerated reliability testing. Packages were assembled using underfills F and G and optimized thermal reflow parameters with the underfill pre-wipe pretreatment step, which provided robust interconnect yield and minimal underfill voiding. The reliability test matrix included 35 parts in Liquid-to-Liquid thermal shock (JESD22-A106-A) and 25 parts in Level 3 preconditioning (IPC/JEDEC J-STD-020A) for each underfill material.[8,9] Both groups were comprised of 5 electrical parts supplemented by mechanical parts to complete the sample sets. The electrical parts were used to approximate sample interconnect life through the testing regime. The mechanical parts were used to provide replicates of the sample set and to reveal specifically mechanical failures in underfill cracking or delamination as inspected by C-SAM and microscope inspection.

Packages tested by Level 3 IPC/JEDEC J-STD-020A preconditioning (60% Relative Humidity, 30°C for 192 hours followed by 3 reflow cycles) had failure defined as a 10% variation in electrical resistance in any of three daisy-chained interconnected loops, 10% delamination of underfill from the silicon chip, or any parts experiencing die cracking. The material acceptance criterion was no failures before 192 hours at 60% relative humidity at 30°C. Groups passing J-STD-020A are then subjected to LLTS, but no criterion is specified. Packages tested by JESD22-A 106-A Liquid to liquid thermal shock also had failure defined as 10% variation in electrical resistance in a daisy-chained interconnect loop. Material acceptance criterion was no failures before 1000 cycles of 5 minute sequential dwells at -55ºC and 125ºC. Each test set was evaluated for primary failure modes for the given package systems.[10,11]

Test Vehicles
Test Vehicle 1
Test vehicle 1a was comprised of high lead (90 Pb/10 Sn) 0.035" diameter solder spheres and a ~1 mil eutectic lead-tin solder coating on a 0.5 oz copper coated FR4 substrate cut to 1" X 1". These coupons were designed to simulate the high-lead bump on eutectic cap interconnect system of the commercial package. Test vehicle 1 was used in experiment 1a.

Test Vehicle 2
Test vehicle 1b was a commercial flip chip package module. The package consisted of a 10 mm X 14 mm silicon die attached to a 13 mm X 20 mm FR4 substrate with copper traces throughout. The interconnect system comprised 127 ?m diameter high lead (97 Pb / 3 Sn) bumps on the silicon chip interface and eutectic solder (37 Pb / 63 Sn) caps on copper pads with solder mask passivation on the substrate interface. The ball-limiting metallurgy (BLM) was TiW/CrCu/Cu with polyimide passivation. The laminate was Driclad (r) composite with Taiyo PSR4000 solder mask. The bumps numbered approximately 130 and were arranged in 6 rows, 4 in across the short distance through the center of the footprint and 1 on each side. The bumps were spaced at a 250-micron pitch and provided a 150-

micron offset height between the substrate and chip post-reflow. The substrate was populated with over 100 copper plated through vias throughout the surface of the footprint of the chip. Test vehicle 2 was used in experiments 1b, 2a, 2b, and 3.

Assembly Process

The test vehicles were assembled using a consistent chip attach process for each experiment. Experiments 2a, 2b, and 3 included an additional solder surface pretreatment step conducted immediately prior to package assembly. Assembly began with a fixed mass of underfill dispensed by a Camalot 3700 onto the substrate bond site. The substrate was then placed in a Kulicke and Soffa 6900 flip chip placement machine where the bond head picked up and placed the die upon the substrate. The placement parameters were a placement force of 1000 g at a speed of 0.1 mm/s. The assembly was then reflowed in a BTU Paragon 98N convection reflow oven. A Sonoscan D6000 Scanning Acoustic Microscope was performed on assembled packages to examine underfill continuity. A Keithley 210 multimeter was used to make quality measurements on electrical packages based on a two point resistance measurement.

Results

Interconnect yield is defined as the percentage of total interconnects that successfully wet and form an electrical and mechanical interconnection during the reflow step. Underfill voiding was defined as the total amount of voids formed in the underfill material during chip placement and underfill cure. Interconnect yield was determined by electrical continuity testing of the chip to substrate interconnect loops combined with X-Ray microscopy images of the solder interconnects. Underfill voiding was determined by a count of total voids within the underfill following processing, measured with CSAM images.[12]

Experiment 1a

Experiment 1a utilizing test vehicle 1 was analyzed using analysis of variance relative to a defined solder wetting response. Solder wetting was defined in terms of a wetting parameter based upon a combination of relative fillet rise and internal diffusion of eutectic solder upon the high lead solder sphere. Ratios of the respective terms were defined relative to the total sphere half circumference and sphere cross-sectional area as shown in Figure 4. The tested no-flow underfill materials showed significant effects to the varied reflow parameters allowing determination of optimized reflow profiles combining the most successful settings of each reflow parameter that provide relative maximums in solder wetting. The results of these optimized reflow profiles were compared to the best cases of solder wetting experiments to provide verification of the results. Table 1 shows the parameter settings providing the relative maximums in solder wetting and the wetting parameter response relative to the best cases for each underfill in the experiment.

$$M1 = \left(\frac{s}{s^*}\right); \; M2 = \left(\frac{A}{A^*}\right)$$

$$M = \left(\frac{s}{s^*}\right)\left(\frac{A}{A^*}\right) = M1 * M2$$

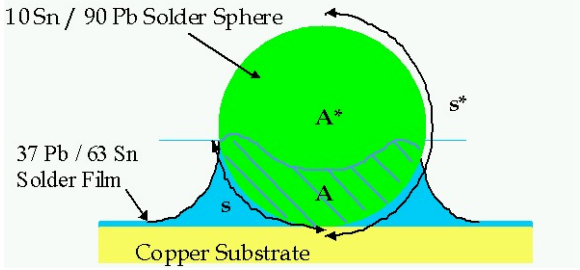


Figure 4 - Experiment 1a Wetting Response Parameter

Table 1 - Solder Wetting Experiment and Verification Results

Underfill	Ramp Rate (°C/s)	Peak Temp. (°C)	Time > 183°C (s)	Step Soak Time (s)	Optimal Profile M-Factor	Best Case Old M-Factor Measurement
A	1.4	225	90	0	0.13	0.12
B	2.5	240	90	0	0.28	0.27
C	2.5	240	90	0	0.57	0.37
D	1.8	220	65	120	0.14	0.15
E	2.5	240	90	0	0.55	0.21
F	1.5	220-235	50	120	0.16	0.13
G	1.5	220	50-65	120	0.12	0.11

Experiment 1b

Test vehicle 2 packages were examined for thermal reflow profile effects on solder wetting and underfill voiding after assembly. Results indicated both package interconnect yield and underfill voiding were significant relative to the tested parameters. None of the underfills provided acceptable interconnect yield and underfill voiding throughout the experiment. Table 2 shows interconnect yield and underfill voiding results for the optimized reflow profiles (best cases) of the tested underfills. Note "None", "Very Low", "Low", "Moderate", and "Very High" Voiding corresponds with 0, 1-5. 5-20, 21-50, and 100+ total void counts, respectively.

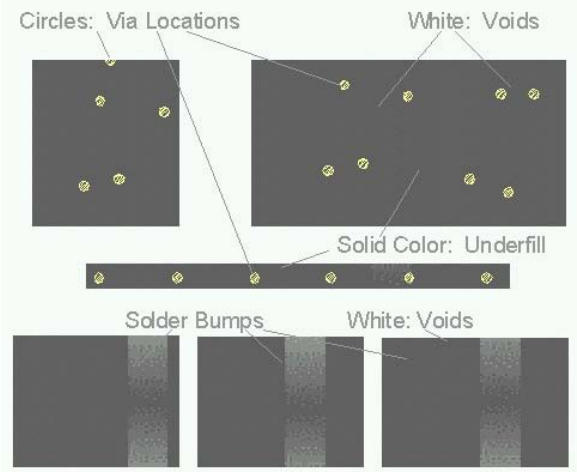
Voids were observed in the experiments to originate from substrate tented vias and eutectic solder capped pads. Figure 5 shows segments of CSAM images overlaying a maps of the substrate footprint revealing the apparent direct correlation between underfill voids and substrate features of tented vias and solder pads. Direct in-situ observations of assembled packages during the reflow process revealed gas emanations occurred from both the tented vias and

the eutectic solder. In addition, the experimentation revealed the amount and rate of gas emanations were directly proportional to the ramp rate and peak temperature parameters of the reflow profile.

Table 2 - Experiment 1b Interconnect Yield and Underfill Void Results

Underfill	Ramp Rate (°C/s)	Peak Temp. (°C)	Time > 183°C (s)	Step Soak Time (s)	Interconnect Yield %	Underfill Voiding
A	1.4	225	90	0	85.6	Low
B	2.5	240	90	0	33.6	Low
C	2.5	240	90	0	93.2	Moderate
C1	2.5	240	90	0	86.7	Moderate
C2	2.5	240	90	0	53.5	Moderate
D	1.8	220	65	120	33.1	High
E	2.5	240	90	0	79.6	Moderate
F	1.5	220	50	120	85.9	Very Low
F1	1.5	220	50	120	90.1	Very Low
F2	1.5	220	50	120	90.9	Low
G	1.5	220	50-65	120	72.1	Low

Figure 5 - Observed Locations of Underfill Voids Near Substrate Features



Experiment 2a

Solder precleaning steps provided varying degrees of success in promoting interconnect yield. The underfill pre-wipe method provided the most consistent interconnect yield in packages with nearly 100% yield. The organic preclean and UV-ozone precleaning both provided improved interconnect yield however inconsistent over the control process. The experimental finding provided evidence that inconsistent solder oxide layers on the eutectic solder bump surfaces adversely affected interconnect yield in assembled packages. The pre-wipe method was the most effective in disrupting the solder oxide layer and thereby promoting interconnect yield.

Experiment 2b

Solder pretreatment steps were further analyzed for their effect on interconnect yield in this experiment. The pre-wipe method again provided the most consistent interconnect yield of the tested steps averaging with ~99% interconnect yield as shown in Table 3. The Flux-refire steps provided inconsistent yield and voiding results except for underfill F in which yield was approximately 99% and voiding was very low.

Table 3 - Experiment 2b Pretreatment Step Results

Underfill	Level	Pre-Clean Method	Interconnect Yield (%)	Underfill Voiding
A	1	Pre-wipe	98.43	Low
	2	Flux-refire-bump reflatten-rinse	62.81	Low
	3	Flux-refire—bump reflatten-ultrasonic clean	47.07	Low
F	1	Pre-wipe	99.70	Very Low
	2	Flux-refire-bump reflatten-rinse	98.60	Very Low
	3	Flux-refire—bump reflatten-ultrasonic clean	91.64	Very Low
G	1	Pre-wipe	99.24	Low
	2	Flux-refire-bump reflatten-rinse	69.70	Low
	3	Flux-refire—bump reflatten-ultrasonic clean	47.38	Low

Experiment 3

Underfills F and G utilizing the high throughput process with optimized reflow profiles and the pre-wipe solder treatment steps as shown in Figure 6 were found to provide acceptable interconnect yield and underfill voiding results. These materials and process settings were thus selected for final accelerated reliability testing by liquid to liquid thermal shock (LLTS) and Jedec Level 3 preconditioning.

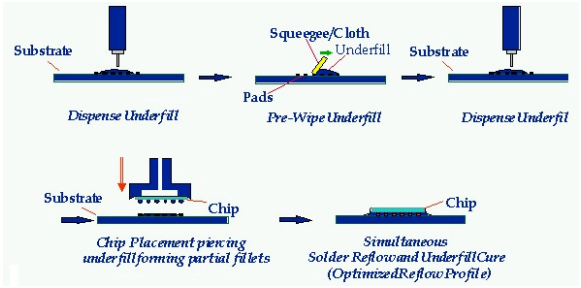
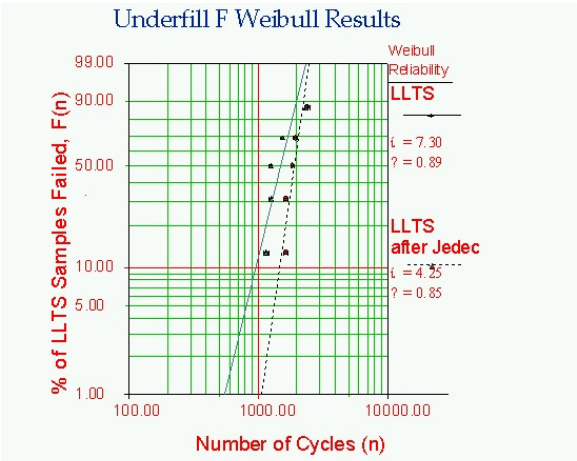


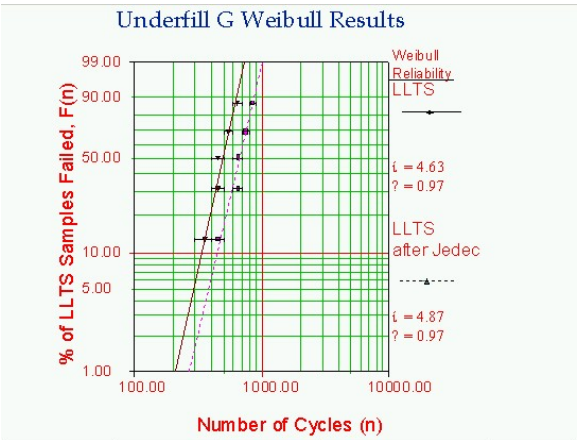
Figure 6 - Final Flip Chip Process With Pre-Wipe Step

Both underfill materials passed Level 3 preconditioning with no failures occurring within either sample set for 192 hours at the prescribed settings. Underfill F also passed the LLTS criterion with the first failure occurring at 1700 cycles. Underfill G did not pass the LLTS criterion with first failure at 500 cycles. Packages cycled in LLTS testing following level 3 preconditioning had first failure at approximately 80% of the non-preconditioned groups for both underfills with a similar rate of failure. Cycle results are shown for each underfill material relative to a Weibull distribution in Figures 7 and 8 for Underfills F and G respectively.



Test Procedure	First Failure	Last Failure	Mean Time of Failure	Slope
LLTS only	1700	2500	1894	7.30
Jedec Level 3 plus LLTS	1200	2400	1487	4.25

Figure 7 - Weibull Results for Underfill F



Test Procedure	First Failure	Last Failure	Mean Time of Failure	Slope
LLTS only	500	900	667	4.63
Jedec Level 3 plus LLTS	400	700	487	4.87

Figure 8 - Weibull Results for Underfill G

Discussion

Experimental results revealed reflow profile parameter settings are critical elements affecting interconnect yield and underfill voiding. The thermal reflow profile required considerable research to provide thermal energy load requirements to provide solder wetting, but must be carefully regulated to prevent premature gelation of the underfills during processing that would inhibit solder wetting. The ramp rate and peak temperature are also directly proportional to gas emanations from substrate features that result in underfill void formations.

The solder surface is an additional element that must be treated to provide robust interconnect yield. The underfill pre-wipe method was found to be an effective, albeit difficult to automate, pre-assembly step that can disrupt excessive Sn-oxide layers and help promote solder wetting.

The reliability results of the final two underfills provided additional insight into no-flow underfill performance. Underfill F was found to provide sufficient resistance to temperature and humidity environmental loading as well as thermal shock testing. Underfill G was resistant to temperature and humidity environs, but susceptible to thermal shock failure. Both package groups failed primarily due to solder fatigue induced crack propagation that traversed through defects in the solder interconnect. Such defects were typically microvoids within or adjacent the eutectic solder interconnect as shown in the SEM image in Figure 9. Packages assembled with underfill G possessed significantly greater amounts of voiding in the solder interconnects as well as the underfill material adjacent to the interconnect. The relatively larger amounts of defects provided increased concentrations of stress and promoted earlier interconnect failure.

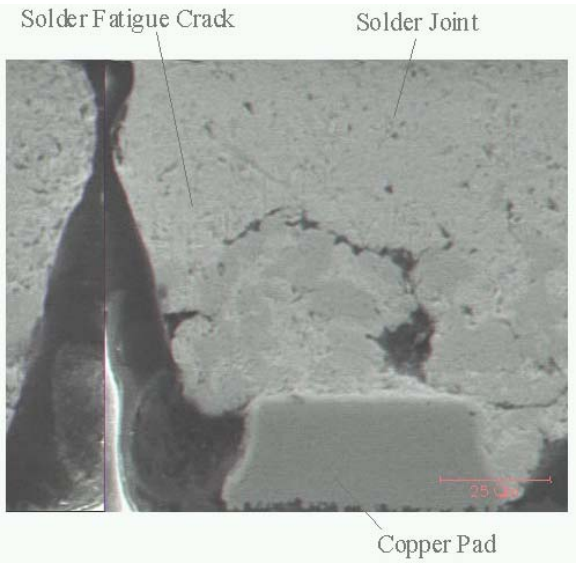


Figure 9 - SEM Image of Fatigue Crack Propagation Through Solder Defects

Conclusions

This research has demonstrated a successful application of the high throughput flip chip assembly process and no-flow underfills on a commercial package. The no-flow underfill F and high throughput assembly process was successfully developed and applied to a commercial package consisting of test vehicle 2. The principal inhibitors to successful package assembly with robust interconnects and minimal underfill voiding were effectively removed by a combination of reflow profile optimization and solder preconditioning modifications. This effectively shows the applicability of this and future no-flow underfill materials on packages utilizing both high lead on eutectic solder interconnect systems and/or multiple substrate vias populating the board surface. Future underfill and package experimentation will require

consideration of these two hurdles, but is obtainable through similar process development steps.

Acknowledgements
The authors would like to thank the Georgia Institute of Technology's Packaging Research Center for support in this work. The authors would also like to thanks Sonoscan Incorportated for use of the model D6000 CSAM, BTU International for use of the Paragon 98N reflow oven, Speedline Technologies for use of the CAM/ALOT 3700 underfill dispense system.

References

1. R. Tummala, E. Rymaszewski, A. Klopfenstein, "Microelectronics Packaging Handbook", Second Editon, Part I, II, III, 1997.
2. J. Qi, "Manufacturability Issues in Flip Chip on Laminate Assembly," The International Journal of Microcircuits and Electronic Packaging, Volume 22, Number 3, Third Quarter, 1999, pp. 270-279.
3. D.F. Baldwin Ph.D and N.W. Pascarella, "Advanced Encapsulation Processing for Low Cost Flip Chip Assembly-A Cost Analysis," 3rd Intl. Symp. Adv. Pack. Matls. Proc. Prop. and Inter., Braselton, GA, March, 1997.
4. D.F. Baldwin Ph.D and N.W. Pascarella, "Advanced Encapsulation Processing for Low Cost Flip Chip Assembly-A Cost Analysis," Proc. of INTERpack '97, Mauna Lani, Hawaii, June 1997.
5. L. P. Thorpe. "High Throughput Flip Chip Assembly Process and Reliability Analysis Using No-Flow Underfill Materials," MSME Thesis, School of Mechanical Engineeringm, Georgia Tech, Atlanta, GA. 2000.
6. C. Delott, "Thermal Process Optimization and Monitoring," Circuits Assembly, May 2000, pp. 50-56.
7. F. Yost, F. Hosking, and D. Frear, The Mechanics of Solder Alloy Wetting and Spreading, 1993, p. 234.
8. IPC/JEDEC J-STD-020A, "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices", April 1999.
9. JEDEC Standard, "Thermal Shock", JESD22-A106-A, Electronic Industries Association, April 1995.
10. P. Houston, B. Smith, D. F. Baldwin Ph.D, and B. Lewis, "Failure Mode Analysis of Advanced Electronics Packaging," Proceedings of the Technical Conference, APEX, March 12-16, 2000.
11. P. Viswanadham and P. Singh, Failure Modes and Mechanisms in Electronic Packages, Chapman & Hall, 1998.
12. IPC/JEDEC, J-STD-035 Acoustic Microscopy for Nonhermetic Encapsulated Electronic Components, Electronics Industries Alliance, May 1999. 6