Methodology to Predict Mechanical Strength and Pad Cratering Failures under BGA Pads on Printed Circuit Boards

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ABSTRACT
In the past few years, several papers, test methods and methodologies have been developed to estimate pad cratering under Ball Grid Array (BGA) pads in Printed Circuit Board Assemblies (PCBAs).

However, almost all the tests and methodologies proposed so far have the following shortcomings:

1. They are destructive. The samples tested are broken and the failure mode(s) observed to determine the propensity for cratering
2. They require testing several samples using different test methods (bend, shock, pull, shear or acoustic), but there is no easy correlation between the different test methods.
3. They can be used for relative comparisons, but there is no easy way to translate the correlations into failures in actual functional board level assemblies.

While these tests have helped mitigate pad cratering significantly, the industry still needs the following:

1. A non-destructive way to predict whether a certain PCBA design (BGA and PCB combination) is likely to result in mechanical strain induced pad cratering failures, long before the product has been built.
2. An easy to use way to correlate PCB level pad pull tests done per IPC-9708 and monotonic bend tests per IPC-9702, so that the design can be optimized to mitigate pad cratering failures during qualification testing.
3. An easy to implement design to detect pad cratering in a functional assembly, so that if a failure is observed in the field, it is easy to determine if the failure is due to pad cratering. Detecting a failure as soon as it occurs is critical in identifying the source of the mechanical strain that resulted in the failure, which in turn can help quickly resolve the issue.

In this study, using extensive experimental data, a detailed methodology is outlined to show the relationship between board strain, solder joint strain and force to failure in monotonic bend testing and pad pull testing. In addition, the correlation between monotonic bend testing and pad pull testing is shown, such that the results of pad pull testing can be used to estimate the likelihood of observing pad cratering failures in PCBAs during bend testing and manufacturing operations. The methodology can be used by designers to estimate the optimal combination of package and PCB design variables to minimize the likelihood of pad cratering and other solder joint failures during testing and field operation.

Finally, methodologies to predict and determine pad cratering failures quickly in field operations are also discussed and outlined.

INTRODUCTION
The exponential growth of the internet and smart connected devices is driving a need for faster, smaller and more efficient devices. This exponential growth is being propelled by the indomitable Moore's law, which has aided the rapid miniaturization of transistors. To support the shrinking of transistors, the density of interconnects from the silicon to the system has been rapidly increasing. This increase in density requires reducing the size of interconnects, ranging from the flip chip bumps connecting the chip to the substrate, to the connectors connecting line cards to backplanes to drive networking equipment.

Key to this rapid shrinking of devices and interconnects is achieving an acceptable level of reliability during the expected assembly, manufacturing and use of these devices. The smaller and thinner the device, the more susceptible it could be to mechanical loading conditions (bend, drop, shock, vibration etc.). Over the past several years, the industry has developed

multiple test standards to evaluate and benchmark the reliability of devices under different use conditions. Device suppliers are required to demonstrate that their device passes the required tests before the device is accepted as part of a finished system.

However, given the wide range of potential failure modes that could occur, a whole plethora of test methods are currently being used, and suppliers have to perform more standard tests to demonstrate reliability. For example, suppliers need to pass IPC/JEDEC 9701 (Accelerated Temp Cycling), 9702 (Monotonic Bend), 9703 (Shock), 9708 (Pad Cratering) etc. to demonstrate that a Ball Grid Array (BGA) component can be reliably mounted on a Printed Circuit Board (PCB). While the approach of defining test methods and requiring suppliers to meet test standards is fairly common, it poses several challenges:

1. The tests are expensive and time consuming. The added cost and time required to perform the tests inevitably gets transferred to the OEM making the system, and eventually to the consumer
2. Since the tests require physical samples, by the time the tests are performed, several aspects of the device have already been designed. If a device fails the test, more time and cost is involved in root causing the failure and iteratively redesigning and testing the device to pass the test
3. There is little correlation between the tests, so each test is usually performed sequentially. Consequently, passing one test could invariably mean failing another, making design optimization even more difficult and time consuming. With rapidly shrinking design cycles, repetitive testing and optimization is a luxury most device suppliers can ill afford.
4. There are several "test escapes" because there is virtually no way to guarantee that each potential failure mode can be captured for rapidly evolving devices by the established test methods. Moreover, end use conditions rapidly evolve too, and even after passing all the tests, when a field failure occurs, it is almost impossible to determine the root cause of the failure (unusual use conditions or a design flaw).

Given all these challenges, there is a growing need to develop ways to predict failures during the design phase, and to correlate failures from one test condition to another test condition. If designers know *a priori*, the tradeoffs in the design that they need to consider, the design time and optimization can be improved significantly.

In this study, we present the analytical correlations derived between two test standards: IPC/JEDEC-9702 and IPC/JEDEC-9708, and how those correlations could be used to predict a potential failure much earlier in the design process. Moreover, the predictions can be used to estimate the optimal design to mitigate potential failures both during testing and in the field. Finally, we present potential ways to detect a failure real time in field use conditions.

MONOTONIC BEND TEST (IPC/JEDEC 9702) [1]

The monotonic bend test standard was developed specifically to address interconnect failures in BGA components mounted on PCBs, subjected to flexure loading conditions. As many as seven potential failure modes could occur in the immediate vicinity of the BGA interconnects during monotonic bending conditions. The test method strives to derive a single damage metric (board strain) that could result in failure. Board strain can then be used to determine how much flexure a given BGA/PCB combination can handle, and to establish minimum strain levels that a given assembly can be expected to withstand.

In a recent publication [2], we have demonstrated using extensive numerical analysis that a combination several design variables could be used to *predict* board strain to failure, with reasonable accuracy, and to help designers optimize the parameters to achieve a target board strain. The prediction equation is shown in (Table 1 and Figure 1).

Variable	Description	Category	Value
A	Package Type	FCBGA 1pc Lid	-276.14
		FCBGA No Lid	-176.21
		Wirebond PBGA	-1137.23
B	Package Size (mm)	-	
C	PCB Thickness (mils)	-	
D	PCB Pad Size (mils)	-	
E	Pkg Pad Size (mils)	-	
F	Ball Pitch (mm)	-	
G	Joint Top Strain (με)	-	

Table 1 PCB Strain Prediction Model

$$PCB\ Strain(\mu\varepsilon) = A - 22.02 \times B - 28.43 \times C + 184.74 \times D + 323.14 \times E - 5062.76 \times F + 277445 \times G \quad (1)$$

This model can be used to estimate the PCB strain to failure for a given package and PCB combination during the design phase even before samples are built. A few important caveats to note:

a. The model itself does not give the definition of a failure. It provides the correlation between design variables and joint strain. The typical Joint Top Strain (G) values observed are approximately 20,000 $\mu\varepsilon$ for an electrically open solder joint failure. This value can be used to estimate the PCB strain to failure with an appropriately selected safety margin.
b. The model is based only on the failures associated with joint top strain (such as brittle solder joint fracture), so it is applicable only to packages in which the ratio of joint top and bottom strain is equal to, or close to 1.

Details on how this relationship was derived are outlined in [2]. However, we still need to develop a similar predictive capability for the Pad Cratering test method (IPC 9708).

PAD CRATERING TEST METHOD (IPC-9708) [3]

The IPC-9708 test method was developed to address a specific failure mode: pad cratering. Pad cratering is known to occur as a cohesive failure in the PCB laminate directly underneath a BGA at the corners, when subjected to mechanical loading conditions (Figure 1).

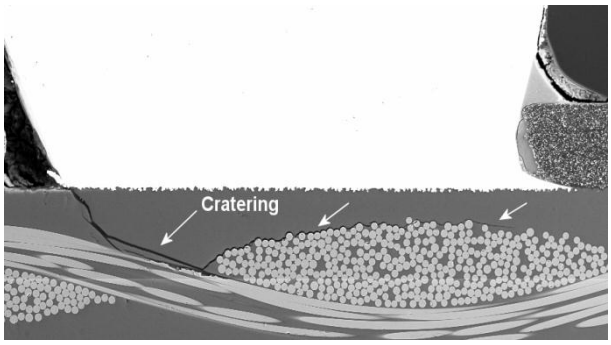

Figure 1: Example of a Pad Cratering Failure [4]

The IPC-9708 test method comprises of three different test methods: a Pin Pull Test, a Cold Ball Pull Test and a Shear Test. Each test is aimed at determining the force it takes to induce a pad cratering failure underneath a BGA pad, but each test has different tradeoffs.

In this study, we focused specifically on the Pin Pull Test because it minimizes the effect of the solder from the test by attaching a pin directly to the pad.

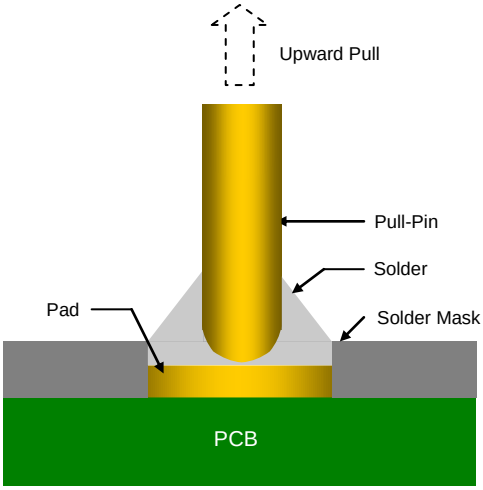

Figure 2: Test Setup Schematic [4]

The experimental pin pull data derived from the testing is shown in Figure 3.

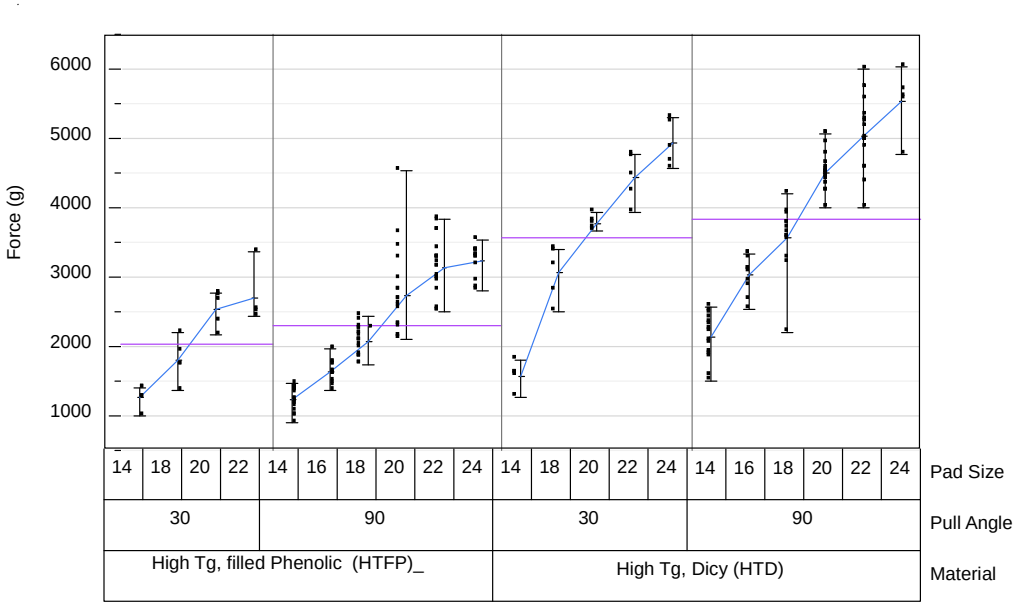

Figure 3: Effect of Pull Angle (5 mil stencil, 5mm/sec pull speed, 500um pin size) [4]

The results of this testing indicate a clear and strong relationship between pad size and the average pull force (for the case of a 90° pull). Given the strong correlation of the average pull force to pad size, we can determine if the stress underneath the PCB pads is the same for each pad size. If the postulation is valid, then the stress-to-failure for the experimentally derived pull forces-to-failure should be constant for all the pad sizes tested.

NUMERICAL MODEL

Consequently, a set of numerical models were developed, to estimate the stress underneath the PCB pad corresponding to each pad size. A detailed numerical model was built to simulate the pin pull test. BGA pads of varying diameter were simulated and pulled to estimate the tensile stress built underneath the pad. Quarter symmetry was used to model the pads, as shown in Figure 4. The force applied in the model corresponded to the forces applied to the pad sizes shown in Figure 5.

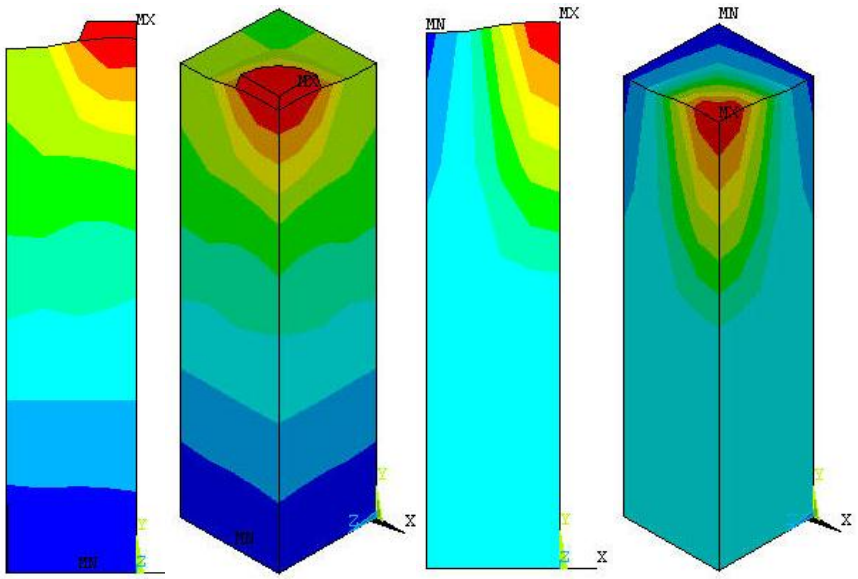

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Figure 4: Numerical Analysis Results (a) Vertical Deformation (Front View) (b) Vertical Deformation (Isometric View) (c) Vertical Tensile (SY) Stress (Front View) (d) Vertical Tensile (SY) Stress (Isometric View)

The results of the numerical analysis are shown in Table 2. SY represents the vertical tensile stress, while VM represents the Von Mises Stress (max and min values). The % Change is the difference between the max and min values.

Table 2: Pull Force and Stresses underneath PCB BGA Pad

Pull Test Modeling Results										
Pad Size (mils)	**Force (g)**	**U_Y (Inch)**	**SY_{min} (PSI)**	**SY_{max} (PSI)**	**SY_{max} - SY_{min} (PSI)**	**% Change**	**VM_{min} (PSI)**	**VM_{max} (PSI)**	**VM_{max} - VM_{max} (PSI)**	**% Change**
24	**5500**	7.17E-04	2.20E+04	6.68E+04	4.48E+04	0	1.92E+04	5.73E+04	3.81E+04	0
22	**5000**	6.67E-04	1.86E+04	6.68E+04	4.82E+04	-0.00449	1.68E+04	5.84E+04	4.16E+04	9.35
20	**4500**	6.16E-04	1.56E+04	6.76E+04	5.20E+04	1.179994	1.47E+04	5.98E+04	4.52E+04	18.65
18	**3500**	4.95E-04	1.13E+04	6.03E+04	4.91E+04	-9.63462	1.12E+04	5.38E+04	4.26E+04	11.998
16	**3000**	4.40E-04	9.05E+03	6.06E+04	5.16E+04	-9.18389	9435.7	5.43E+04	4.48E+04	17.804
14	**2100**	3.22E-04	5.92E+03	5.10E+04	4.50E+04	-23.6912	6558.2	4.57E+04	3.92E+04	2.8442
Average				**6.22E+04**	**4.84E+04**	**-6.88904**	**1.30E+04**	**5.49E+04**	**4.19E+04**	**10.10862**

The simulation results show that the stresses (SYmax – SYmin) underneath the PCB pad are within 20% of each other, and about 6% on average. This variation is within the experimental data variation for pull force values as shown in Figure 3. Consequently, one can use the average Delta SY value to establish that the threshold stress-to-failure underneath the PCB pad for this material (Dicy Cured High Tg FR4 (HTD)) is approximately 333,706 Pascal (48,400 PSI).

From Figure 3, it can also be seen that for the High Tg Filled Phenolic (HTFP), the pull force values are also linear (for the 90° pull) and scale linearly with the values of the HTD. A comparison of the two sets of pull force values yields a ratio of 0.6. Consequently, it can be estimated that the threshold stress-to-failure underneath the PCB pad for the HTFP material is roughly 199,285 Pascal (28,903.93 PSI).

Now that we have the estimated failure threshold stresses for the two materials from the pin pull test, we can re-run the Monotonic Bend Test analysis and extract the typical stresses seen under the BGA pad on the PCB during bending.

CORRELATION BETWEEN MONOTONIC BENDING AND PIN PULL TESTING

The entire monotonic bend model was re-run to derive the correlation between board strain and stresses under the BGA PCB. The PCB material assumed for the analysis was the HTD material. Guidelines for HTFP could be derived from the same analysis, by using a de-rating factor of 0.6. These guidelines could also be used for any new material other than HTD and HTFP, as long as the de-rating factor of the new material relative to HTD can be derived. The de-rating factor can derived from pin pull tests performed in accordance with IPC-9708 for the new PCB material(s) and compared with HTD data.

Since the board strain can be predicted by the assembly design variables (Table 1), all we need to do is derive the relationship between board strain and PCB BGA pad strain. That way, we can predict what amount of board strain can result in pad cratering failures. It is important to note that 3 strain gages are attached to a PCBA during monotonic bend testing per IPC/JEDEC 9702: (1) at a location far field from the package perimeter (global strain), (2) underneath the cornermost BGA (local strain) and (3) underneath the package center (local strain). Since local strain is very difficult to measure accurately, the global strain has been used to derive all the guidelines. The results of the analysis are shown in Figure 5.

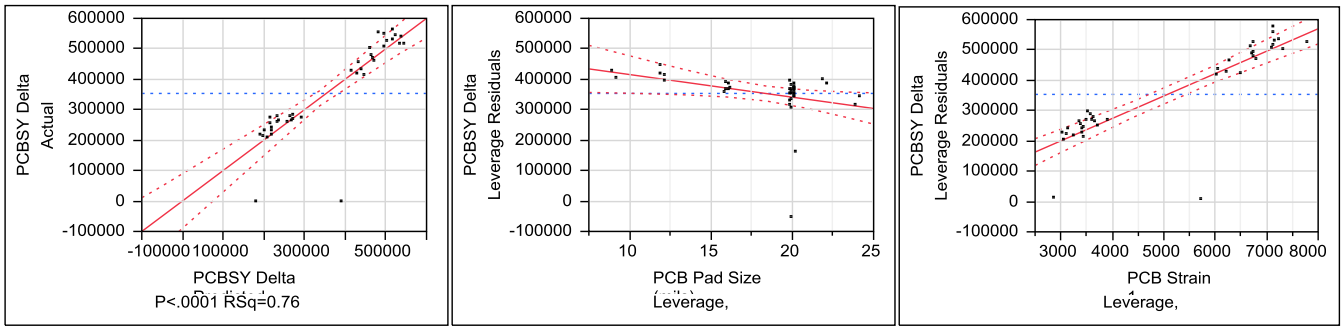

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Figure 5: (a) Accuracy Estimate of Prediction Model (b) Correlation between PCB SY and PCB Pad Size (c) Correlation between PCB SY and PCB Global Strain

The prediction equation relating PCB Pad Size, PCB Global Strain and PCB Pad Cratering Stress is shown below:

$$PCB\ Pad\ Cratering\ Stress = 114506.246 - 7432.648 * PCB\ Pad\ Size\ (mils) + 73.96825 * PCB\ Global\ Strain\ (ue)$$

From the results, one can conclude that a stress-to-failure threshold stress under the BGA pad of 333,706 Pa (HTD) translates to a global PCB strain of about 5000 $\mu\varepsilon$ (Figure 5). That means that if a given package assembly is subjected to more 5000 global microstrain, it could result in complete pad crater rupture. It is important to note that this is strain to *complete* rupture, not partial pad crater. Similarly, for the HTFP material, the global PCB strain to crater translates to 3000με (corresponding to a threshold stress of 199,285 Pascal).

It can also be seen from Figure 5 that the selected pad size can significantly alter the PCB strain. For pad sizes that are 20 mils and below, the PCB stress is higher than the threshold stress value. This is borne out in experimental bend test results, where for pad sizes 20 mils or below, the failure mode is predominantly pad cratering. In addition, it has been shown in experimental tests that increasing the pad size from 20 mils to 25 mils significantly reduces the propensity for pad cratering [4].

DETECTING PAD CRATERING FAILURES

Now that we have a criterion for acceptable PCB strain (3000 – 5000με), we face another challenge. How do we determine if this threshold has been exceeded in a real assembly? It is impractical to place strain gages on live boards because they cannot be calibrated to reflow temperatures and cannot easily be assembled on every location on every board in production. We need some way to indicate when the strain threshold has exceeded the 3000 – 5000 με range. The indicator does not have to be as precise as actual strain gages, but accurate enough to give an estimate that the strain exceeded the design threshold.

One possibility is to design the trace from the cornermost BGA pad to fail at a preset strain threshold. The trace could be narrowed down to create a stress concentration that could result in the trace cracking at a level corresponding to the failure threshold (Figure 6).

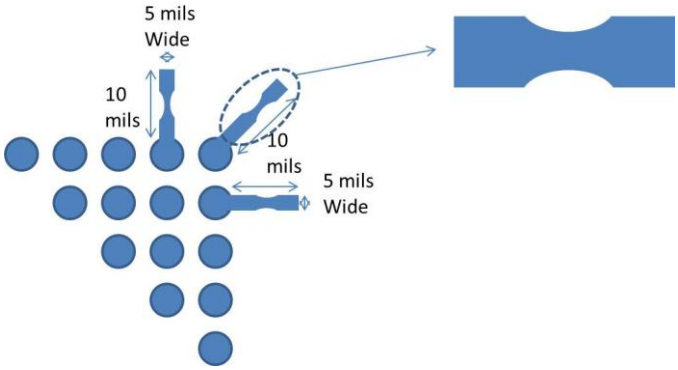

Figure 6: "Mousebite" Trace Design To Fail At Preset Strain Threshold

However, in looking at the stress/strain curve of the typical trace copper material used in PCBs (HTE, Figure 7), it is clear it will take an applied strain of 60,000με (6% elongation) to cause complete rupture. Making a trace that could rupture at a strain level in the 3000 – 5000με strain range without significant process/design modifications does not appear to be practical for high volume manufacturing.

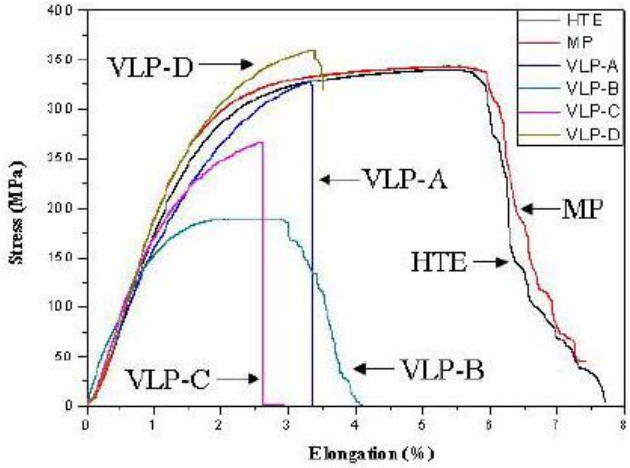

Figure 7: Stress/Strain Curve of Different PCB Copper Trace Materials. The Most Commonly Used is High Temperature Electrolytic (HTE) [5]

Consequently, a different solution was sought, that was easier to implement in high volume production and could be scaled easily and cost effectively. While other techniques for in-situ monitoring have been proposed, they require custom connectors and designs that are not very easy and cost effective to deploy on hundreds of components on linecards in production [6]. It has been known for quite some time in the industry, that ceramic capacitors are prone to mechanical strain related failures. In fact, the strain-to-failure of ceramic capacitors under flexural loading has been very well characterized for a whole range of capacitor sizes (Figure 8).

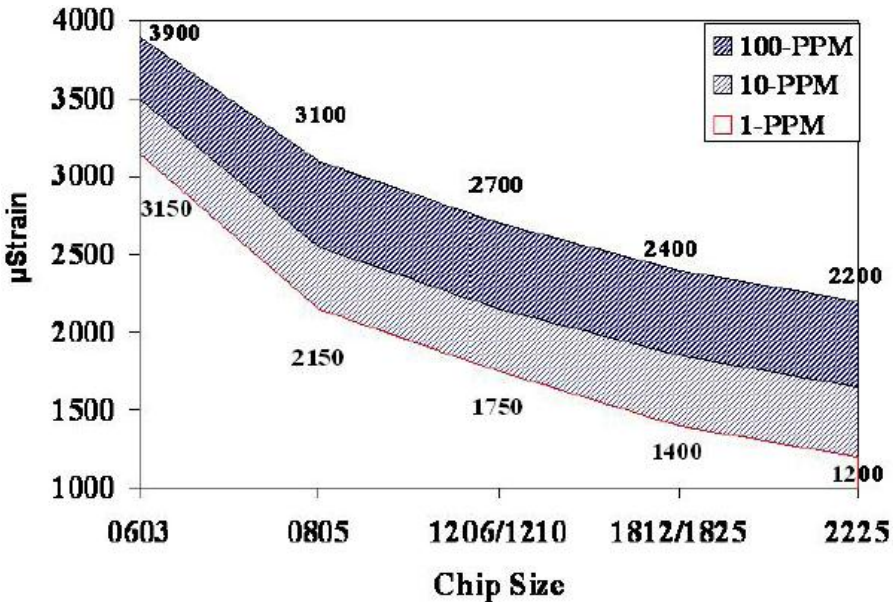

Figure 8: Chip Size Versus Strain Required to achieve 100, 10, and 1 PPM Failure Rates (Typical) [7]

It can be seen from Figure 8 that if a 2225 capacitor is mounted at the diagonal location closest to the corner of a BGA, it is likely to fail at strains in excess of 3000 – 5000 ue. The failure rate is expected to be high enough to reliably detectable. An electrical circuit such as that shown in Figure 9 can be used to monitor the capacitor in real time, and to determine the precise time at which it has failed. Knowing the time of failure is critical to a root cause analysis: if it failed during assembly, the precise assembly process step that caused the failure can be identified. If it failed during use conditions, the specific instance of usage could be identified.

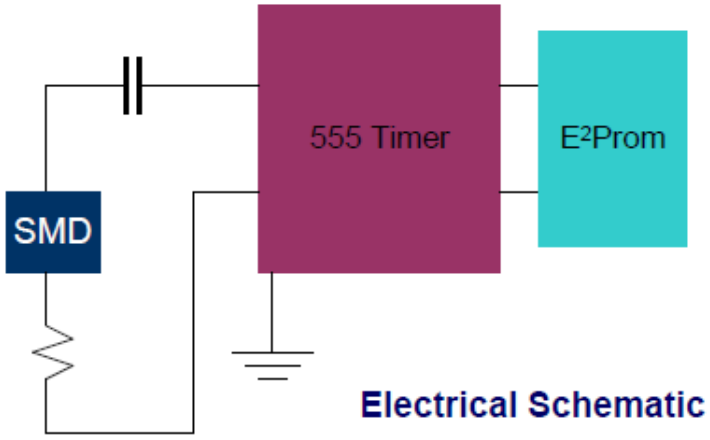

Figure 9: Electrical Schematic of Circuit To Detect Capacitor Change (Capacitor is Strain Monitoring Device (SMD))

The methodology for detection involves connecting the capacitor (SMD) to a 555 Timer Circuit and an Electrically Erasable Programmable Memory (E^2PROM). The memory register will be set to First-In-First-Out (FIFO), to record x-minutes of data. This will serve as a "black box". A threshold value of baseline capacitance can be preset or programmed into each board based on the T_0 capacitance value. The circuit will log the time vs. capacitance over time and will show any changes in capacitance over time – caused by a crack in the capacitor. The timer and memory could be located at a convenient distance away from the part(s). Several devices can be connected in parallel to the same Timer/E^2PROM circuit, to give the effective capacitance change. If any device fails, the circuit will record the event.

Relatively simple cross section analysis can also be performed later to reveal the classical flexure-induced failure mode as shown in Figure 10, thus verifying the failure.

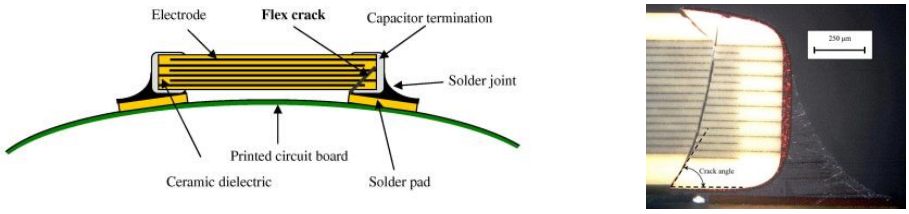

Figure 10: Typical Crack Signature of Chip Capacitor Under Flexural Loading [8]

Thus, a commonly known and understood failure mode in ceramic capacitors could actually be turned into an easy to implement detection method for excessive strains in PCB assemblies. Ceramic capacitors are cheap, easy to mount and require no significant changes to the standard SMT assembly process. The region around the diagonal of a BGA is generally known to be a high strain region and no active components are recommended for mounting in this region. Mounting the sensing capacitor in this location should not result in significant loss of board real estate either.

CONCLUSIONS

A detailed methodology for correlating pin pull testing with monotonic bend testing metrics has been presented. With the data presented in this paper, the threshold stress in the PCB material for creating full pad craters has been derived. In addition, the global PCB strain range to reach the threshold stress in the PCB material has been derived. Thus, the amount of strain it could take to cause a full pad crater in a PCB material can be estimated upfront. The prediction can be used to optimize the package and PCB design variables required to minimize the likelihood of pad cratering. Finally, a methodology for real time detection of high strains, which could result in pad cratering failures has been outlined.

FUTURE WORK

A detailed test vehicle to validate the correlation between monotonic bend testing, pin pull testing and capacitor sense testing is currently being developed. The results of the experimental data will be used to further refine the results presented in this paper.

ACKNOWLEDGMENTS

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