

# **The Evolution of ICT: PCB Technologies, Test Philosophies, and Manufacturing Business Models Are Driving In-Circuit Test Evolution and Innovations**

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## **Abstract**

*Many manufacturers employ one or more In-Circuit Test (ICT) systems in their PCB manufacturing facilities to help them detect manufacturing process and component defects. These “bed-of-nails” electrical test systems are highly valued for providing the qualities of simple program generation, high fault coverage, fast test throughput, low false fail rates, and exceptional diagnostic accuracy as compared to other available test and inspection techniques.*

*Advancements in PCB technologies, along with changing test philosophies and manufacturing business models in recent years have created new and diverse requirements for manufacturers of in-circuit test systems. Particular challenges that ICT manufacturers have had to address include the erosion of test point access in certain product sectors; the progression of ultra-low voltage components; the variable test requirements of different product applications; the varying test philosophies of different market segments and different manufacturing regions; and the demanding throughput requirements of high volume production facilities.*

*This paper highlights how in-circuit test systems have evolved in recent years to include innovations and advancements to address these challenges and trends. Topics that will be covered include boundary scan and functional test integration strategies; advancements in vectorless test techniques; incorporation of limited access electrical test techniques; test strategy analysis tools; high accuracy pin drivers and sensors; concurrent test throughput improvement options; scalable test performance capability architecture; and program development accelerators.*

*The paper describes how these new ICT advancements contribute to lowering overall manufacturing test costs by improving the fault coverage, reliability, and throughput of in-circuit production tests.*

## **Introduction**

When in-circuit test systems were first introduced in the late 1970's, the world was a different place. Printed Circuit Board Assemblies (PCBAs) used through hole technologies, spacing between pins was typically 100 mils, components were only placed on a single side, the largest components rarely had more than 14 pins, the prevalent voltages used to power the boards were 5, 12, and 15 volts, manufacturing occurred in the highly industrialized regions where the products were consumed and manufacturing test consisted primarily of the execution of complex and time consuming functional tests.

The introduction of in-circuit test systems revolutionized the PCB manufacturing process by changing the test paradigm from testing the functionality of the board to testing the functionality of the parts along with the integrity of the assembly process. In-circuit test systems accomplished this by using a bed-of-nails test fixture to make electrical contact to every net on the PCB allowing each component to be individually stimulated and measured. With such electrical test access and innovative guarding and voltage forcing techniques - which allowed each component to be tested individually without the influence of its surrounding parts - ICT systems could quickly detect shorted and open pins, missing components, incorrect analog component values and tolerances, and faulty digital component logic. The theory behind in-circuit testing is that manufacturers can be confident that the board will operate correctly if they verify that all the components are operating correctly and have been properly assembled.

The real breakthrough with in-circuit testing was the benefits it provided compared to traditional functional tests. The complexity of test generation was greatly simplified because test developers no longer had to understand the functionality of the board and could automatically generate programs in days that used to take weeks. The quality of the test coverage improved with ICT as well because direct access to every net eliminated the functional test complexity of trying to propagate faults from internal nets to externally observable test points. Finally, in-circuit test systems provided faster test throughput and exceptional diagnostic accuracy that were not possible with functional tests. All these benefits resulted in fast adoption of in-circuit test systems and they quickly eclipsed complex functional test systems and became the test system of choice for most high volume manufacturers.

In-circuit test systems have had to evolve throughout the years to keep up with the demands of ever-changing PCB technologies, the advance of global manufacturing capabilities, and the diversity of testing philosophies for different product and market segments.

### Addressing Erosion of Test Point Access

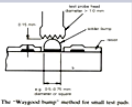
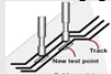
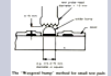
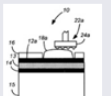
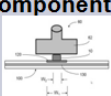
The cornerstone of traditional in-circuit testing has been the ability to gain electrical test access to all of the nets on the PCB using electrical test probes. In-circuit test providers use comprehensive CAD analysis and probe placement solutions to analyze circuit board designs and generate wiring instructions that fixture fabricators use to assemble bed of nails in-circuit test fixtures.

Increasingly it is becoming more challenging to find probe placement solutions that provide full electrical test access to all the nets on the PCB. This is because shrinking packaging technologies, greater IC integration and functionality, higher pin counts, faster I/O speeds and reduced product footprints have lead to ultra-miniaturization. To support this trend, manufacturers are designing increasingly complex high density interconnect boards that make use of blind and buried vias, smaller tracks with tighter spacing and with less copper available on the board surface for electrical test access. This trend is more pronounced for high volume consumer products which place a premium on small size, fast performance, and low power consumption.

One way that designers and fixture fabricators have addressed these challenges is through the use of more advanced probe technologies. Traditional ICT probe technology which consists of a small probe contacting a larger test pad target on the Unit-Under-Test (UUT) is restricted to a target diameter of .024 inches with center spacing of .0395 inches between probes. New highly accurate probe fixturing technologies developed by the fixture fabricators are available that make it possible to design ICT fixtures that can reliably contact test points as small as .012 inches with pitch of .020 inches. [1]

To provide access to even smaller test points, manufacturers can use what are called micro-access test technologies. Instead of using a small point test probe in the fixture to contact a large test pad on the board, micro-access test technologies use a large head test probe in the fixture to contact a small test point on the board. Micro-access test technique concepts have been around since the 1990's and Table 1 describes the general concepts behind 5 different implementations. Micro-access technologies allow manufactures to get electrical test access to test points that are as small as the signal traces themselves; however, their use is only viable on signal traces that can be accessed from the top or bottom layer of the UUT and the micro-access test points must be spaced appropriately to avoid conflict with the large head probes that are used in the test fixture.

**Table 1 – Micro-Access Comparison Matrix**

Micro-Access Technique	Date	General Concept	Benefits	Considerations
<b>Waygood Bump [2]</b> 	1990	Place small solder bumps on test pads and contact them with large head probes	Improves probing accuracy by targeting small solder bumps with large test probes rather than large test pads with small test probes	Size of test pad may hinder performance and probe placement for high speed/high density PCB designs
<b>Vaucher [3]</b> 	1996	Open small apertures in solder mask above signal traces and contact them with deformable tipped probes	Allows direct access to signal traces with special probes that do not require solder bumps	Contact reliability depends on deformable probe performance
<b>Prasad Bump [4]</b> 	1997	Same as Waygood Bump, except proposes that solder bumps be placed on significantly smaller test pads	Better suited than Waygood Bump for high speed signals and high density interconnect designs	Smaller test pads and solder bumps may reduce mechanical performance
<b>Bead Probe [5]</b> 	2003 + 2007	Place small solder bumps directly on signal traces through open apertures in solder mask and contact them with large head probes	Also good for high speed signals and high density interconnect designs	Licensed technique limits which test equipment Mfgs can use / Less robust mechanical performance
<b>TestAccess Component [6]</b> 	2007	Place small conductive Surface Mount Components directly on top of signal traces and contact them with large head probes	Very robust mechanical performance compared to other Micro-Access techniques	Need to place extra SMT component which can add costs

Despite the advances in ICT fixturing technology, manufacturers sometimes find it challenging to get complete physical test access to the boards they are testing. The effectiveness of the ICT solution diminishes as physical test access is lost, so some ICT test systems have evolved to augment physical test access with virtual test access techniques. Table 2 shows the reduced access tools that are available on some ICT test platforms.

**Table 2 – Limited Access Tools Augment ICT**

Technique	Description	Benefit
<b>Boundary Scan / Embedded Test</b>	Many boards today have components with built-in testability features like boundary scan that can be activated during in-circuit testing to run board self tests or provide virtual access to signals on the board when the ICT system does not have physical test access.	Detects faults on nets that do not have physical test access. Uses ICT resources and board testability features in concert for maximum test effectiveness. Consolidates tests on single manufacturing test solution.
<b>Combined BSCAN + Framescan [7]</b>	Combines BSCAN and capacitive opens test techniques. BSCAN devices provide digital stimulus, probe sensor plate in fixture detects stimulus signal.	Identifies open pins on connectors, sockets and IC devices that do not have physical test access.
<b>Indirect Testing</b>	Indirect stimulus of inaccessible pins through low value resistors or buffers on the board.	Allows ICT system to indirectly test nets that do not have direct physical test access using physical nails on the other side of low value resistors and buffers.
<b>Cluster Testing</b>	Groups of two or more components are tested as a single entity to verify proper operation	Allows testing of functions like RC Networks and filter circuits without access to all pins in the cluster.
<b>Functional Test [8]</b>	Application specific circuit board functional tests are executed using add-on functional test instrumentation.	Some ICT systems have ability to plug in industry standard PXI instrumentation which allows ICT to be integrated with functional test in a single test stage.
<b>Adaptive Test Generation</b>	Intelligent test generators and device models are designed to automatically adapt to circuit constraints and missing test access.	Faster test generation and program debug; less time modifying tests to account for different wiring configurations.
<b>Distributed Test [9]</b>	Intelligent analysis tool that can analyze test access, objectively report fault coverage, model alternative test strategies, and recommend optimal test strategies based on manufacturer preferences.	Simplifies the task of understanding ICT fault coverage and the alternative inspection methods that could be used to detect defects other than ICT.

The tools highlighted in Table 2 extend the capabilities of the ICT system allowing manufacturers to still maintain high fault coverage even on boards that do not have full physical test access. It must be noted however that the tradeoff for using these tools is often an increase in programming complexity, less accurate diagnostics at the repair station and longer test execution times. Given these tradeoffs, it is in the best interest of designers and manufacturers whenever it is possible to provide physical test access to every pin they can.

### Addressing Ultra Low Voltage Technologies

As Moore's Law predicted, the number of transistors in integrated circuit packages has approximately doubled every two years over the last two decades. The greater the number of transistors in a package the more power it requires. The amount of power a transistor requires is calculated using the formula ***Power = Frequency x Capacitance x Voltage<sup>2</sup>***. Designers have discovered that the most effective way to reduce the power requirements for their products and satisfy the reduced power consumption and environmental concerns of their customers is to lower the voltages at which they operate. As a result, many boards now contain devices that operate with a combination of low voltage logic levels of 1.8V and below.

The challenge for many in-circuit test systems is that their pin electronics were originally designed when 5V was the predominant logic technology and many of them do not have the required accuracy to test these ultra low voltage components accurately, reliably, and safely.

Some in-circuit test systems have evolved to address this low voltage testing challenge by updating their digital pin electronics with dramatically improved drive and sense accuracy (as low as 15mV). Other capabilities added to ensure safe and reliable testing include real-time backdrive current measurement and control features (to prevent devices from being harmed by electrical over-stress conditions); automatic driver verification (to guarantee that drivers reach their programmed logic levels); dual-level sensor thresholds (to ensure device output drivers are within published specifications); and programmable per-pin logic levels (to support devices that require multiple independent logic levels). [10]

In-circuit test systems equipped with these advanced digital test capabilities can confidently perform powered-up digital testing of the latest low voltage technologies. However, if manufacturers are using in-circuit test equipment that do not have these advanced digital test capabilities they may not be able to reliably or safely test low voltage components, or they be forced to resort to unpowered vectorless test strategies of their low voltage digital parts which are slower, more expensive, and less comprehensive. [11]

### **Addressing Diverse Test Requirements**

In addition to evolving to meet the technology requirements previously described, manufacturers of ICT systems have had to evolve to meet the shifting testing philosophies and business economic drivers of their customers. ICT vendors have struggled to satisfy the demands of different manufacturers who specify different requirements for their ICT systems and who have different expectations as to what they need the system to do.

The factors that drive these expectations include:

- PCB complexity - simple or complex board; low or high pin count; full or limited test access?
- Product cost – low margin consumer product; high cost server, communication, or military/aerospace board?
- Reliability & Regulatory obligations – what safety standards are required for automotive, medical, and industrial equipment?
- Manufacturing strategy – Outsourced vs internal manufacturing; multi-site manufacturing; frequent manufacturing location changes?
- Product volume and mix – high mix/low volume; dedicated high volume production lines; automated vs operator driven operation
- Manufacturing skill levels – experienced vs inexperienced developers and operators; trained vs un-trained personnel

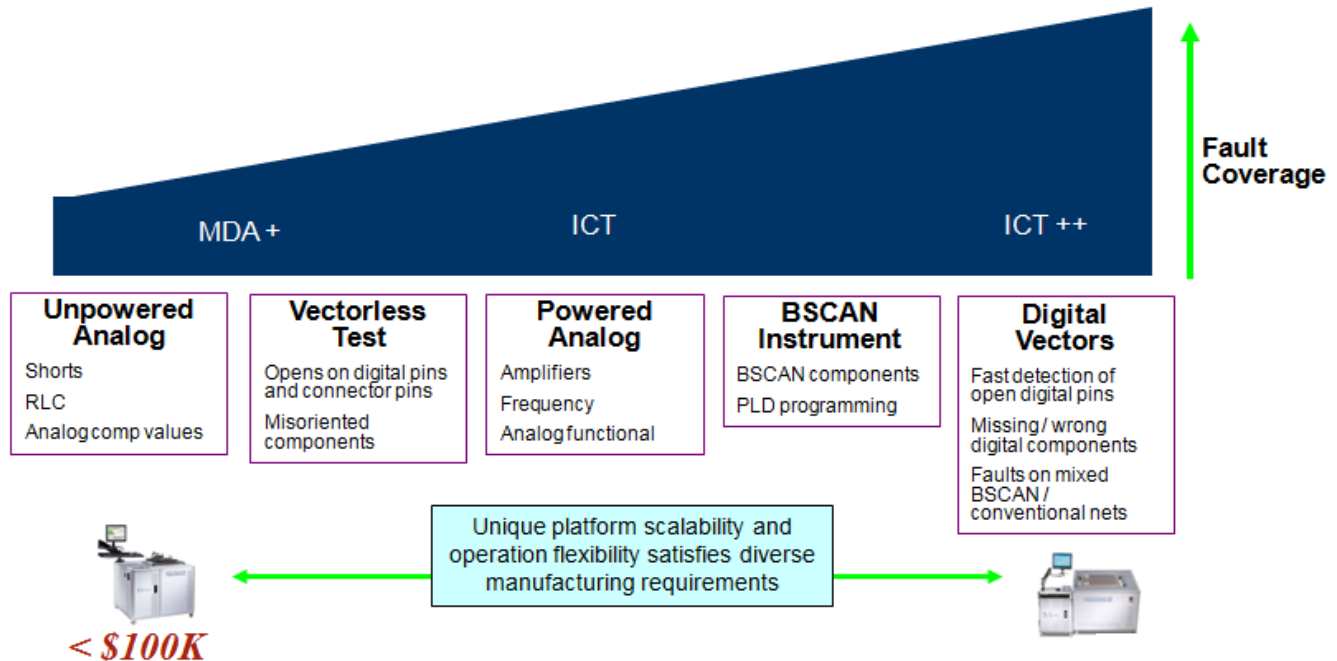
All these factors combine to place conflicting demands on ICT systems. Low margin manufacturers demand low cost ICT; manufacturers of high reliability, highly complex products demand high fault coverage and high pin count capacity; untrained operators demand simple and easy to use operation; highly skilled test engineers demand powerful programming capabilities; high volume manufacturers demand ever higher test throughputs; manufacturers using outsourcing business models demand equipment compatibility. To further complicate matters for ICT vendors different market segments and different geographic regions implement different test philosophies.

Historically, ICT vendors have addressed these conflicting demands with different classes of ICT systems. Manufacturing Defect Analyzers offered low price and simple test operation, but provided limited test capabilities and low fault coverage. High performance In-Circuit Testers offered extended test capabilities and high fault coverage, but were expensive and complex to program. In the middle were a variety of standard in-circuit test systems that offered more performance than an MDA class system at a lower price than high performance class ICT systems.

Given the different classes of test systems, many manufacturers now have production floors with multiple incompatible classes of ICT systems, often from different ICT vendors. There can be a hidden cost to this multi-system test strategy because it increases system training and service costs, increases program maintenance costs, and reduces flexibility in test equipment utilization.

If a manufacturer decides to only use an MDA class tester, then they may not be able to adequately test complex PCB assemblies due to its limited capabilities. On the other hand, if a manufacturer decides on a high performance ICT platform solution, it can be overkill for simple PCB Assemblies where the high performance ICT features are not always needed and the program development requires higher skilled operators.

To account for this dilemma, some ICT vendors have evolved their ICT test systems to be highly scalable to satisfy diverse test requirements in a single compatible platform that supports multiple pin board types and independent hardware options and software plug-ins that can be used to expand the capabilities of the tester. Figure 1 shows how this approach can be used by manufacturers to buy only the test capability they need and grow or reduce test capabilities without changing the tester. The benefits include lower training and programming costs because operators only have to learn one test system and develop one test program, higher equipment utilization rates because a single test system can be used for multiple test applications and higher equipment value because the tester can be configured as an MDA+ system all the way to a high performance digital ICT system. To facilitate test program compatibility and equipment utilization, the test executive on these ICT systems will adapt to run only those tests in the program that can be supported with the given hardware and software configuration of the target tester. No more need to create custom test programs designed for the configuration of each tester on your production floor!



**Figure 1 – Scalable ICT Platform Satisfies Diverse Manufacturing Requirements**

#### Addressing High Volume Manufacturing Requirements

High speed assembly equipment continues to improve resulting in ever faster beat rates on the production line. The beat rate for today's high volume production lines is often less than 30 seconds. In-circuit testers can become the bottleneck in the production line when their test times exceed the beat rate of the assembly equipment and place a limit on the number of boards that can be manufactured per hour.

When this happens manufacturers can choose to add additional test equipment to increase their test capacity or they can reduce test times by eliminating tests until the test time is below the target beat rate. Neither of these options is considered ideal as adding additional test equipment is expensive, requires extra test fixtures, and is not always possible because production facilities often have limited floor space. Eliminating tests requires extra program maintenance and reduces the amount of defects that can be detected by the ICT system.

A better approach is to increase the execution speed of the tester until it no longer is the bottleneck on the production line. Some ICT systems have evolved to support concurrent testing of more than one component at a time. This is accomplished by duplicating instrumentation in the test system so that the test executive can test multiple components in parallel (typically on boards manufactured as part of a panel). How concurrent test is implemented differs for different ICT vendors and the amount of concurrency depends on many factors, but ICT systems with concurrent test features can generally test 1.5 to 2 times faster than a standard ICT tester.

In addition to increasing the test execution speed, high volume manufacturers also try to reduce or eliminate the board handling times. This can be done on non-automated lines by using dual-well fixtures so there is no delay between testing

boards, however the highest volume can be achieved by eliminating the test operator and placing the ICT system in an automated line. Some ICT vendors sell their ICT subsystems as standard 19" rack mount components so that they can be easily integrated into the automated handler solution that is preferred by the manufacturer.

Finally, some manufacturers provide test throughput analysis and optimization software that can modify test parameters to ensure that the test program is optimized for the fastest test throughput. This software reduces test times by an average of 15% and identifies test inefficiencies in the program that could be corrected to further reduce test times.

## **Conclusion**

ICT systems have evolved to address the technology and business challenges of modern PCB manufacturing and their capabilities have advanced far beyond when they were first introduced. Reduced access test techniques, integration of boundary scan and embedded testability tools, advanced pin electronics capable of testing low voltage technologies, concurrent test capabilities, functional test capabilities, and scalable test system configurations have all combined to extend the life of ICT systems and make them one of the tools that is still most valued by high volume PCBA manufacturers.

Taking into consideration how the in-circuit tester has evolved since its introduction and all the electrical test capabilities that are now at its disposal that do not require actual physical test access, it may be time for the industry to stop categorizing these test systems as "In-Circuit Testers" because that name no longer reflects all the things that the tester has evolved to do.

It may be more appropriate to now start categorizing these versatile test systems as "Electrical Test Controllers" because the most capable ones can support in-circuit, boundary scan, PLD programming, cluster and functional testing techniques all in a single consolidated test platform.

## **References**

- [1] Gary St Onge, "Zoom Fixtures for ATE", IPC/APEX Conference, April 2010
- [2] David Boswell, "Surface Mount & Mixed Technology PCB Design Guidelines", Technical Reference Publications Limited, 1990, pg 28
- [3] Vaucher, C; "Analog/Digital Testing of Loaded Boards Without Dedicated Test Points", Proceedings of the International Test Conference, IEEE 1996, pp. 325-332
- [4] Ray P. Prasad, "Surface Mount Technology – Principles and Practice", Chapman & Hall, 1997, sec 332
- [5] Doraiswamy/Grealish, "Implementation of Solder-bead Probing in High Volume Manufacturing", Proceedings of the International Test Conference, IEEE 2006, Paper 5.4
- [6] Anthony J Suto, "Micro Access Technologies on PCB Assemblies", SMT Magazine, August 2011
- [7] Anthony J Suto, "Virtual Access Technique Augments Test Coverage on Limited Access PCB Assemblies", IPC/APEX Conference, Feb 2012
- [8] Michael J. Smith, "Integrated Electrical Test Within the Production Line", IPC/APEX Conference, Feb 2012
- [9] Robinson/Verma, "Optimizing Test Strategies During PCB Design For Boards with Limited ICT Access", Proceedings of the Telecom Hardware Solutions Conference, May 2002
- [10] Alan J. Albee, "Issues & Challenges of Testing Modern Low Voltage Devices on Conventional In-Circuit Testers", IPC/APEX Conference, 2004
- [11] Albee/Smith, "Vector vs Vectorless ICT Techniques", Evaluation Engineering, March 2011

# The Evolution of ICT

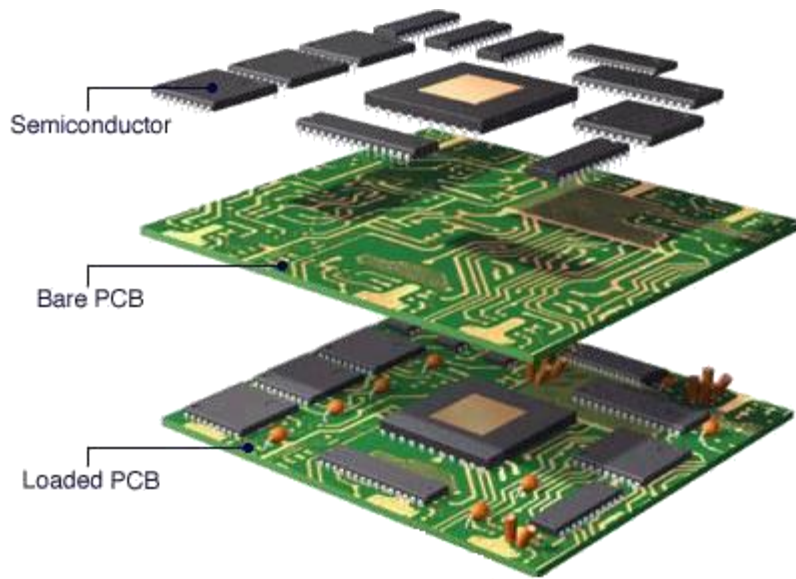
*PCB technologies, test philosophies, and manufacturing business models are driving in-circuit test evolution and innovations*

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# What is In-Circuit Testing (ICT)?

- In-Circuit Test uses electrical test methods on printed circuit board assemblies
- ICT uses various guarding and voltage forcing techniques so each component can be tested individually without the influence of its surrounding parts



## Test Coverage

- Full Shorts Test Coverage
- Open Device Pins
- Analog Component Value and Tolerance
- Digital Component Functionality
- Boundary Scan and Built-In Self Tests
- Memory tests
- PLD Programming

## ICT Strengths

- Simple Test Generation
- Good Fault Coverage
- Fast Throughput
- Excellent Diagnostics



# ICT Covers Broad Range of Electrical Test Steps

## ICT Hardware Blocks

### Power Block

- UUT Power Supplies
- PC Controller
- PCI Instrument Slot

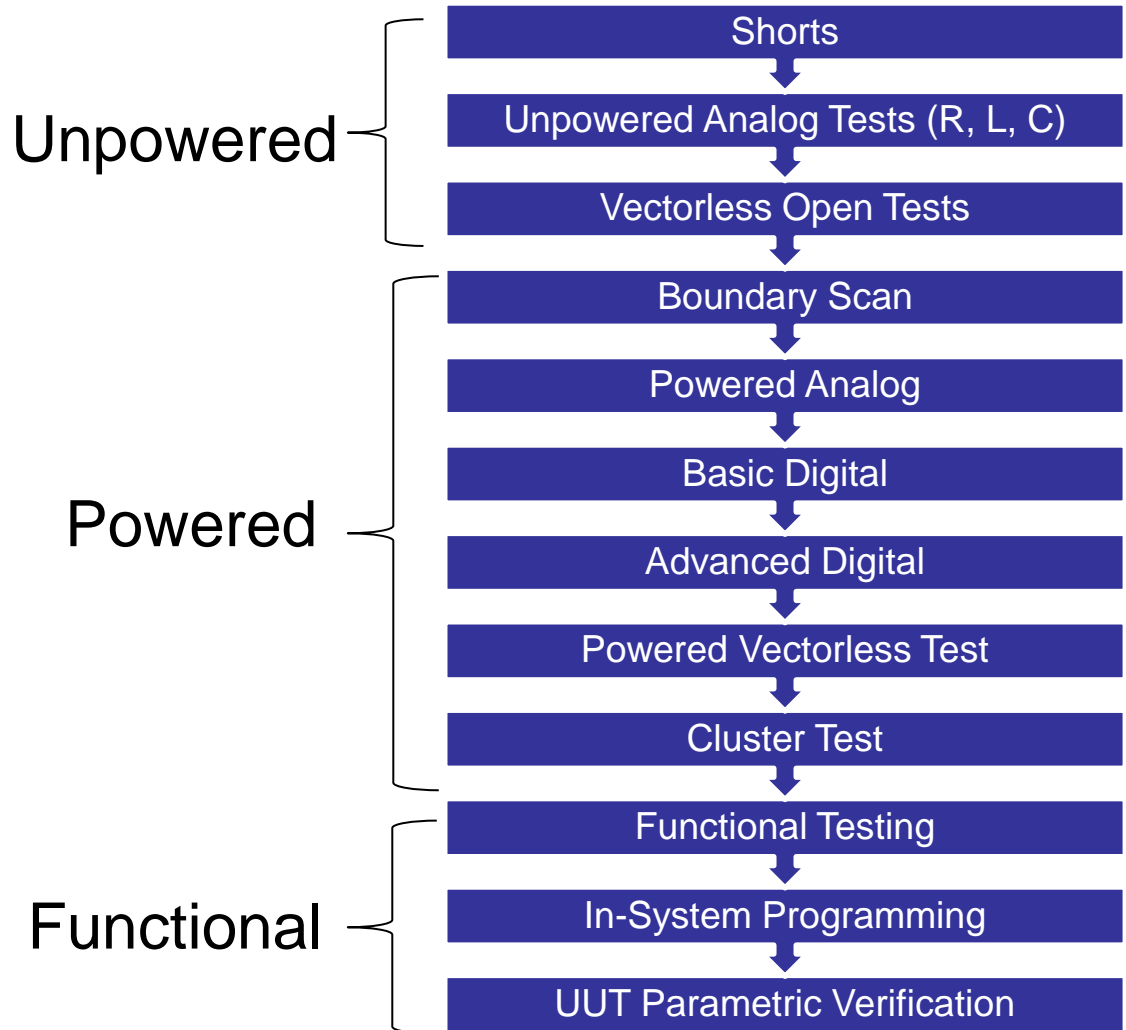
### Instrument Block

- In-Circuit Analog Module
  - AC/DC Source / Measure
  - High Voltage Source
  - Arbitrary Waveform Generator
- Digital Drivers & Sensors
- Clock / Sync / Trigger Pins
- Frequency / Time Measure
- Functional Test Instruments
  - PXI & GPIB Instruments
  - Application Specific

### Control Block

- Relay Drivers
- Vacuum Control

## Typical ICT Tests



# ICT has Evolved to Counteract Production Test Challenges

## ***Test Challenges***

Limited physical test access  
Variable test requirements  
Ultra low voltage technologies  
Shrinking package geometries  
Proliferating BSCAN & DFT  
Operator skill levels  
Increasing production beat rates

Is simple or complex test needed?  
Can it be tested safely & reliably?  
What defects can't be detected?  
Test nets without physical access?  
How to access embedded testability?  
Can I lower operational costs?  
How much time is available for test?

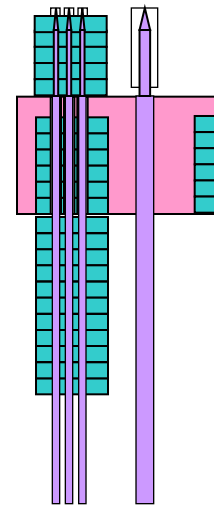
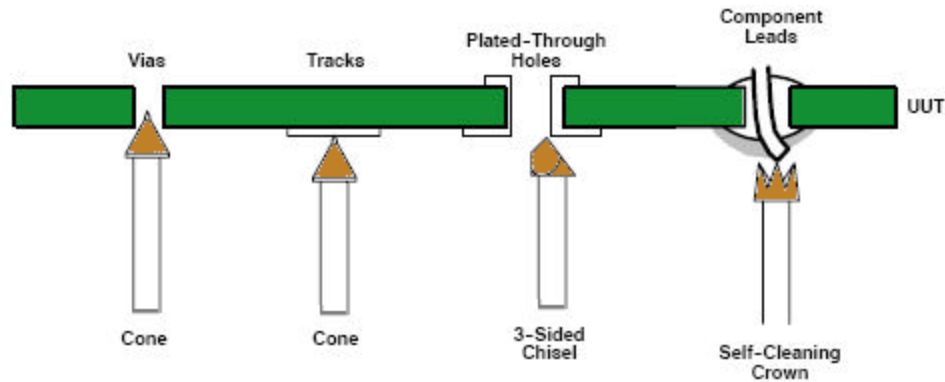
## ***ICT Solutions***

Micro-access technologies  
Combined Bscan & Vectorless Test solution  
Scalable ICT system architectures  
More accurate digital pins  
Higher vectorless test sensitivity  
Native & Partner boundary scan solutions  
Simplified operator user interfaces  
Concurrent test & automation support

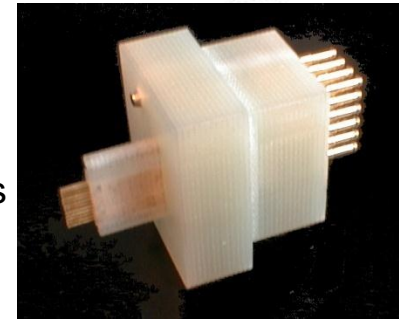
Configurable to test requirements  
Guaranteed voltage accuracy  
Advanced tech for hi fault coverage  
Extend bscan to test non-bscan parts  
Choice of bscan solutions  
Operator productivity tools  
High throughput test options

# Gaining Access with Probe Technologies

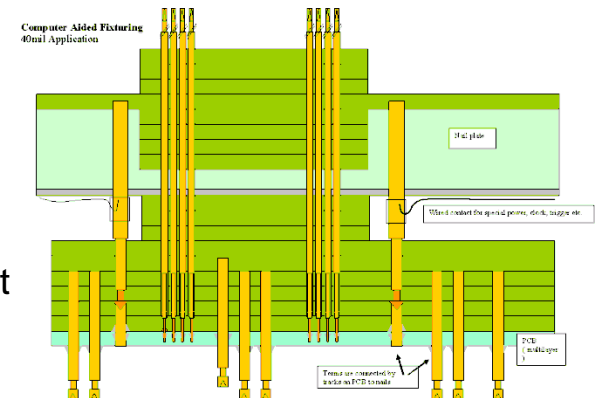
- Advanced probe technologies can help maintain test access
  - Traditional probe technology is restricted to a target diameter of about .020 to .024 in
  - Fine point probing assemblies can reliably contact test points as small as .012 in
- Micro-Access test points can be employed on the PCB to further improve test access



Fine point probing assemblies

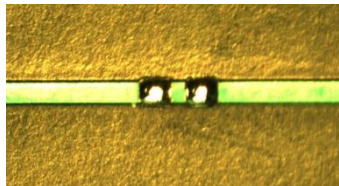


Fine point Alignment

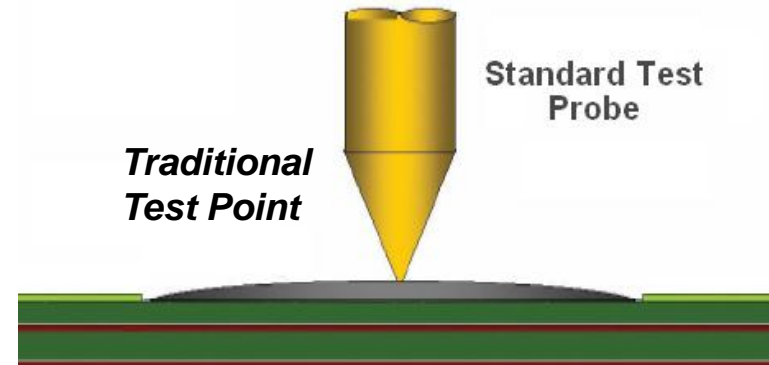


# Gaining Access with Micro-Access Test Points

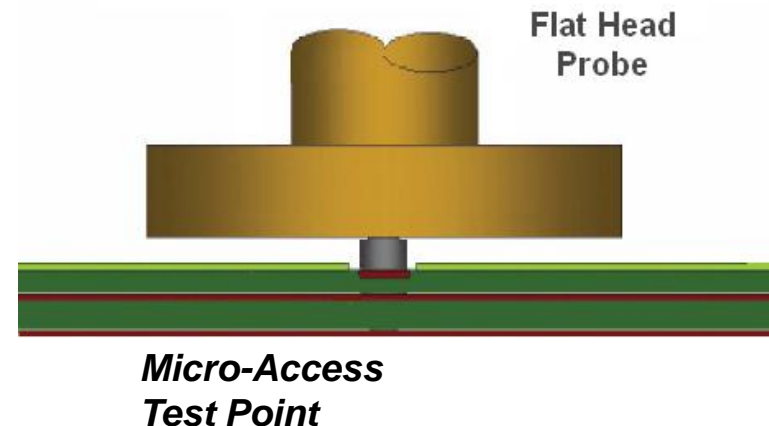
- Traditional Test Point
  - Large test point
  - Small test probe
  - Large test point size places limitations on board density
  - Probing reliability decreases as test point gets smaller
- Micro Access Test Point
  - Small test point
  - Large test probe
  - Smaller test point does not effect probing reliability
  - Test point size no longer limits board density



Before: Probing large target with a small probe



Improved: Probing small target with large probe

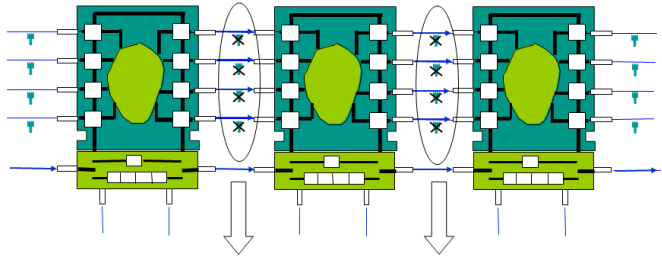


# Micro-Access Comparison Matrix

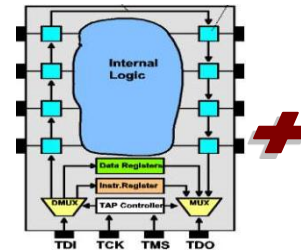
Micro-Access Technique	Date	General Concept	Benefits	Considerations
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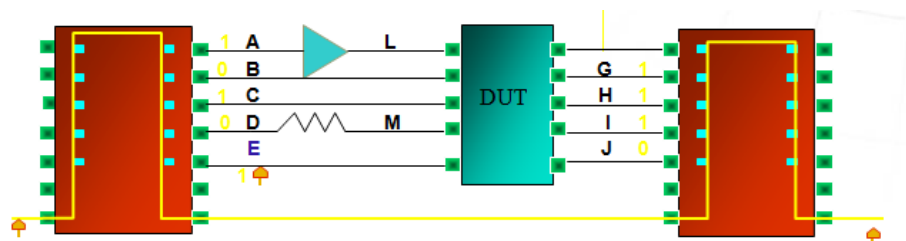
# Gaining Access with Test Techniques



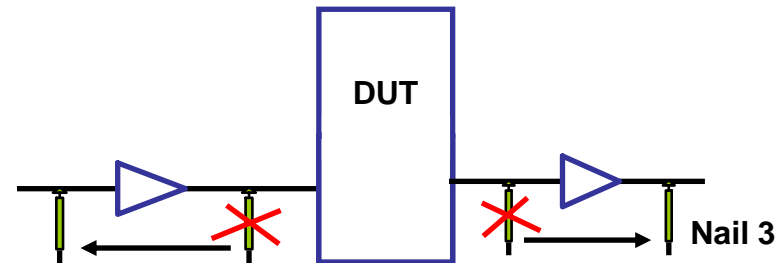
**Boundary Scan**



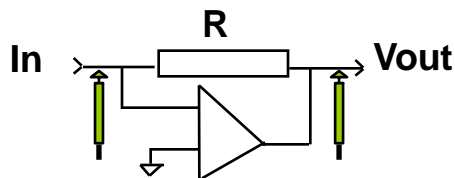
**BScan + Capacitive Opens**



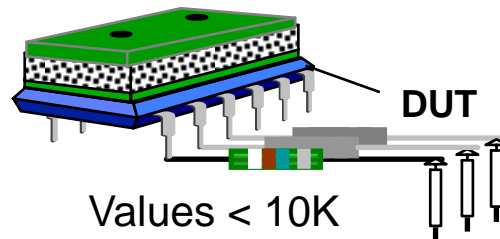
**BScan Virtual Pin**



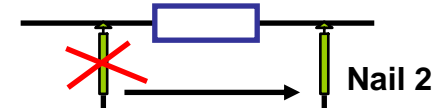
**Remote Drive/Sense**



**Cluster Test**



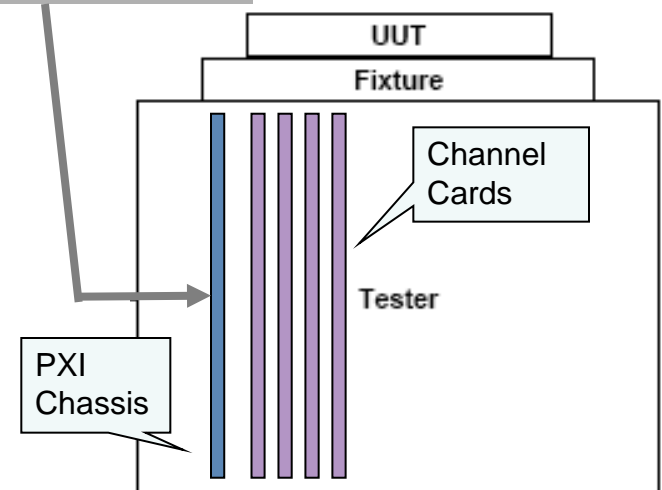
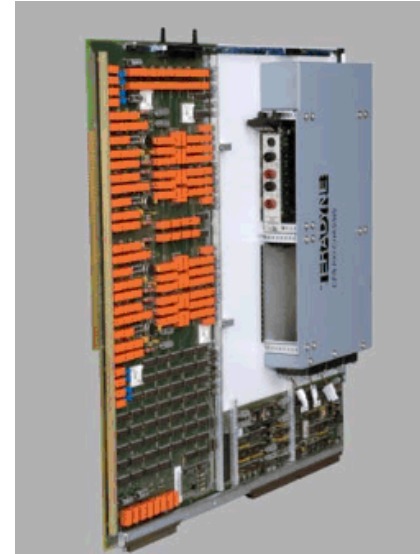
**Indirect Capacitive Opens Test**



**Digital Jumper**

# Gaining Access with Functional Test

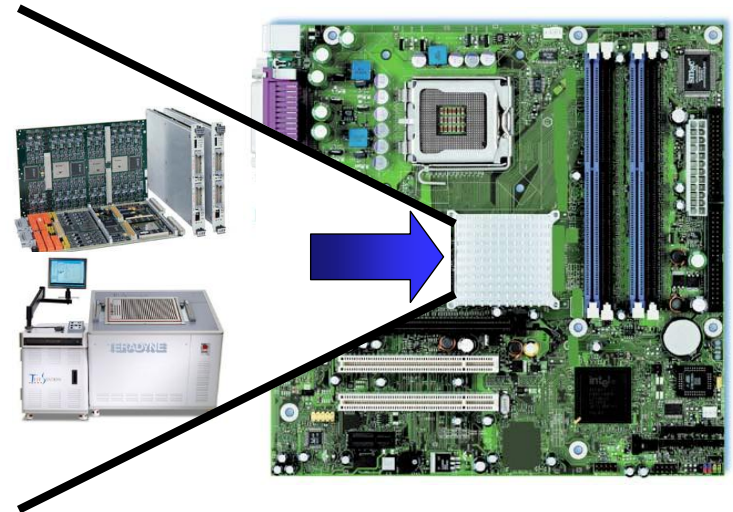
- Add power of PXI instrumentation & programming standards to ICT
  - Plugs into existing ICT backplane
  - Flexible signal distribution hub simplifies test fixture wiring
  - Small form factor that does not expand tester footprint
- Key Manufacturing Benefits
  - Reduced test stages
  - Increased test fault coverage
  - Lower capital costs
  - Faster cycle time
  - Earlier defect detection
  - Fewer test operators





# Gaining Access with Board Assisted BIST

- Many chips and boards are being designed with built-in test features
  - Test instrument Intellectual Property downloadable to PLD
  - Evolving IEEE-P1687 standard for controlling embedded instrumentation
  - Proprietary test features embedded by silicon manufacturers into their chipsets
  - At-speed processor controlled emulation tests
- ICT Impact
  - Take advantage of testability features to complement ICT
  - Pre-condition board to prepare it to execute self tests
  - Combine with traditional ICT tests to improve test coverage and diagnostics

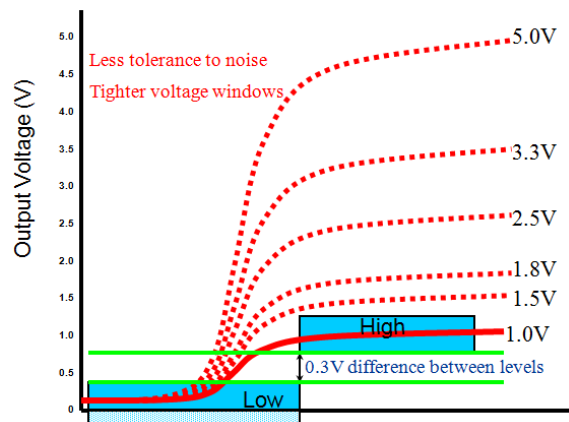


# Low Voltage Challenge for ICT

- Multiple voltage levels per IC
- Easier to expose pins to electrical over-stress
  - Voltage glitches exceed max spec ratings
  - Shared logic levels are potential risk
- Devices susceptible to damage from 'over-driving'
- I/O logic levels differentiated by milli-volts
  - Tester pins require much greater accuracy
  - High accuracy required even under load conditions
  - Voltage instability can trigger unwanted logic transitions

*Source of device stress and potential damage*

*Source of unstable tests & high false fails*

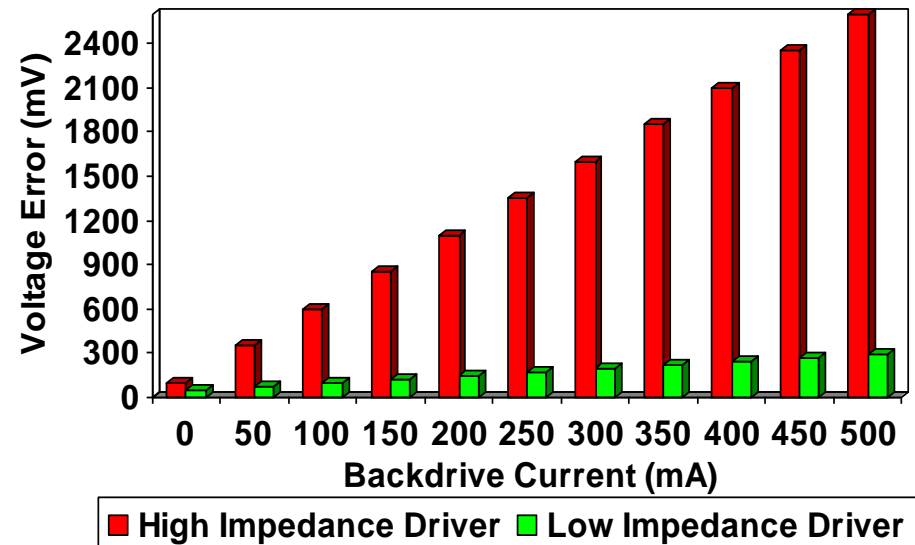


Margin for error is much smaller

# Solving Low Voltage Testing Problems

## Voltage Error vs Backdrive Current

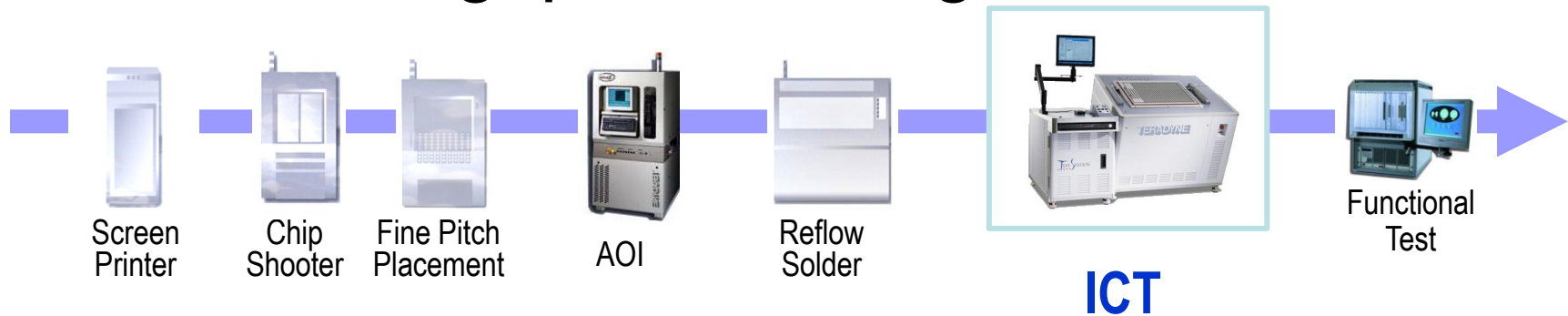
- Improved accuracy ICT pins
  - 15mV D/S Accuracy
  - Low Impedance Driver
  - Real-Time Current Measurement
  - Automatic Driver Verification
  - Programmable Per-Pin Logic Levels
  - Dual Level Sensor Thresholds
- Advanced Timing Control
  - Fast Test Execution
  - Consistent and Repeatable Timing
  - Specialized Clock and Trigger Pins
  - Concurrent Device Testing
  - Parallel Device Test Capability
- Test Analysis Software
  - Multi-Level Digital Isolation
  - Calculated Backdrive Controls



**SafeTest™**  
Protection Technology

	High Accuracy D/S	Programmable Per Pin Logic Levels	Dedicated Digital Controller	Automatic Driver Verification	Backdrive Measurement	Programmable Backdrive Control	Multi-Level Digital Isolation
TestStation	✓	✓	✓	✓	✓	✓	✓
GR228X	X	✓	✓	✓	X	X	✓
System A	X	✓	✓	X	X	X	X
System B	✓	X	X	✓	X	X	X

# Throughput Challenge for ICT



- PCB assembly equipment speeds continue to increase
  - Manufacturing beat rates can be less than 30 seconds
- In-circuit tester becomes bottleneck on manufacturing line
  - ICT test times limit the amount of boards that can be manufactured
- Manufacturing facilities often have limited floor space
  - Adding additional test equipment is not always possible

# Solving Throughput Challenges

- Concurrent Test Configuration
  - Multiple test modules in single test frame
  - Supports simultaneous testing of multiple boards
  - Doubles throughput of traditional ICT testers
  - More test capacity throughput in same footprint
  - Lower capital equipment, fixture, and operation costs
- Automation Ready Building Blocks
  - Flexible rack mount ICT subsystems
  - Easy integration into automated mfg lines
  - Turnkey partner solutions or custom implementations
  - Eliminates operator cost & handling time



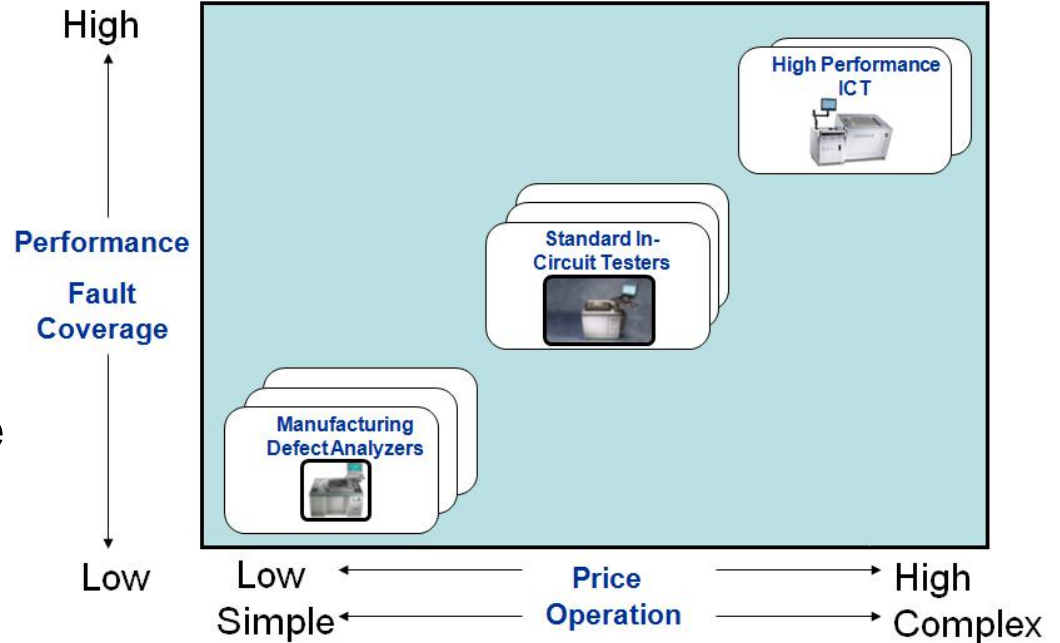


# Diverse Manufacturing Challenges for ICT

- Different PCB complexities
  - Simple vs complex technologies
  - Low vs high net count PCBs
  - Full vs limited test access
- Different product costs
  - Low cost consumer products
  - High cost server, networking, and military/aerospace products
- Different reliability & regulatory test obligations
  - Safety concerns for automotive and medical products
  - “Throw-away” consumer products
- Different manufacturing strategies
  - Outsourced vs internal manufacturing
  - Multi-site manufacturing
  - Frequent changes to location where product is manufactured
- Different product volumes and mix
  - High mix, low volume NPI facilities
  - Dedicated high volume production lines
  - Automated vs operator driven manufacturing lines
- Different operator skill levels
  - Experienced vs inexperienced operators
  - Different native languages

ICT Manufacturers have historically met diverse requirements with different classes of ICT...

But each class of testers have different fault detection capacities...



Tester Type	Shorts and Opens	Un-Powered Analog (R,L,C)	Vector-less Tests	Powered Analog	Powered Functional	Boundary Scan	Basic Digital	Advanced Digital
MDA	✓	✓	✗	✗	✗	✗	✗	✗
MDA+	✓	✓	✓	✓	✗	✓	✗	✗
ICT	✓	✓	✓	✓	✓	✓	✓	✗
ICT+	✓	✓	✓ +	✓	✓ +	✓ +	✓ +	✓



# Solving Diverse Manufacturing Requirements



**MDA +**

**ICT**

**ICT ++**

**Fault  
Coverage**

## Unpowered Analog Test

ICA Analog  
Instrumentation  
Analog Only Pin  
Boards  
PDU Option

## Vectorless Test

Framescan FX 2.0  
Cap Xpress  
Junction Xpress

## Function Testing

System Frequency  
Test Module  
Analog Functional  
Test Module  
Multi-Function  
Application Board  
PXI Functional  
Expansion Board  
Synchronized Analog  
& Digital Subsystems

## BSCAN Test Options

Native IEEE 1149.1  
Solution  
Partnership BSCAN  
Solutions  
Fast PLD  
programming  
Powered Framescan

## Digital Vector Testing

UltraPin II Technology  
15mV D/S Accuracy w/  
Dual Logic Thresholds  
Programmable Per Pin  
Real Time Backdrive  
Current Measurement  
20MHz Clock, Sync, &  
Trigger signals  
Multiple Timing Sets  
Deep Serial Memory  
Multiplexed or Pure Pin  
Digital Parallel Test  
Throughput Boost

- Buy only the test capability that is needed
- Grow or reduce test coverage without changing the tester
- Programs and test fixtures are compatible
- Operators do not need to learn different test systems
- Software adapts to tester configuration

# ICT Innovations Help Solve Manufacturing Challenges

- Shrinking test access
  - High accuracy probing & Micro-access test technologies
  - Flexible boundary scan solutions
  - Combined bscan and capacitive opens techniques
  - Functional test integration support
  - Activation of on-board built-in-test capabilities
- Smaller packages and component pins
  - More sensitive capacitive opens measurements
- Low voltage components
  - Improved accuracy ICT pins
  - Advanced timing control & safe testing analysis software
- High volume production speeds
  - Concurrent test configurations double throughput
  - Rack mount ICT block modules support inline solutions
- Diverse test requirements & testing philosophies
  - Scalable ICT system design
  - Compatible programs and fixtures
  - Common development software & tools



*Instead of “In-Circuit Testers”, today’s test systems would be better characterized as “Electrical Test Controllers”*

# Manufacturers have Diverse Electrical Test Requirements

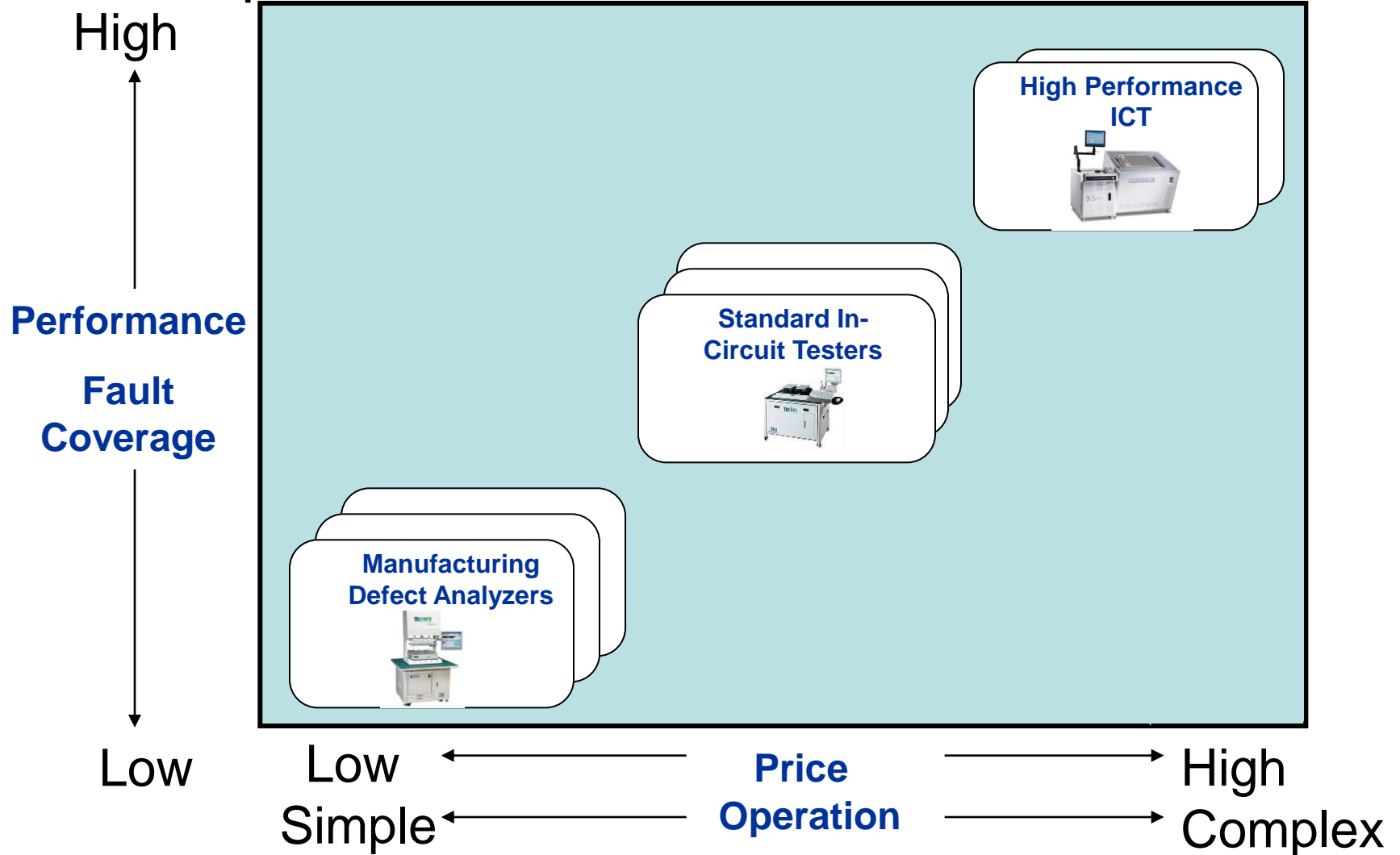
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  - Trained vs un-trained personnel

# Diverse Test Requirements Place Conflicting Demands on ICT Testers...

- Low margin manufacturers demand low cost ICT
- High reliability/high complexity product manufacturers demand high fault coverage and safe testing
- Untrained operators demand simple and easy to use operation
- Highly skilled test engineers demand powerful programming capabilities
- High volume manufacturers demand ever higher test throughputs
- Outsourcing business models demand turnkey solutions and equipment compatibility
- Complex PCB Manufacturers demand high pincount capacity systems
- Different market segments and regions implement different test philosophies



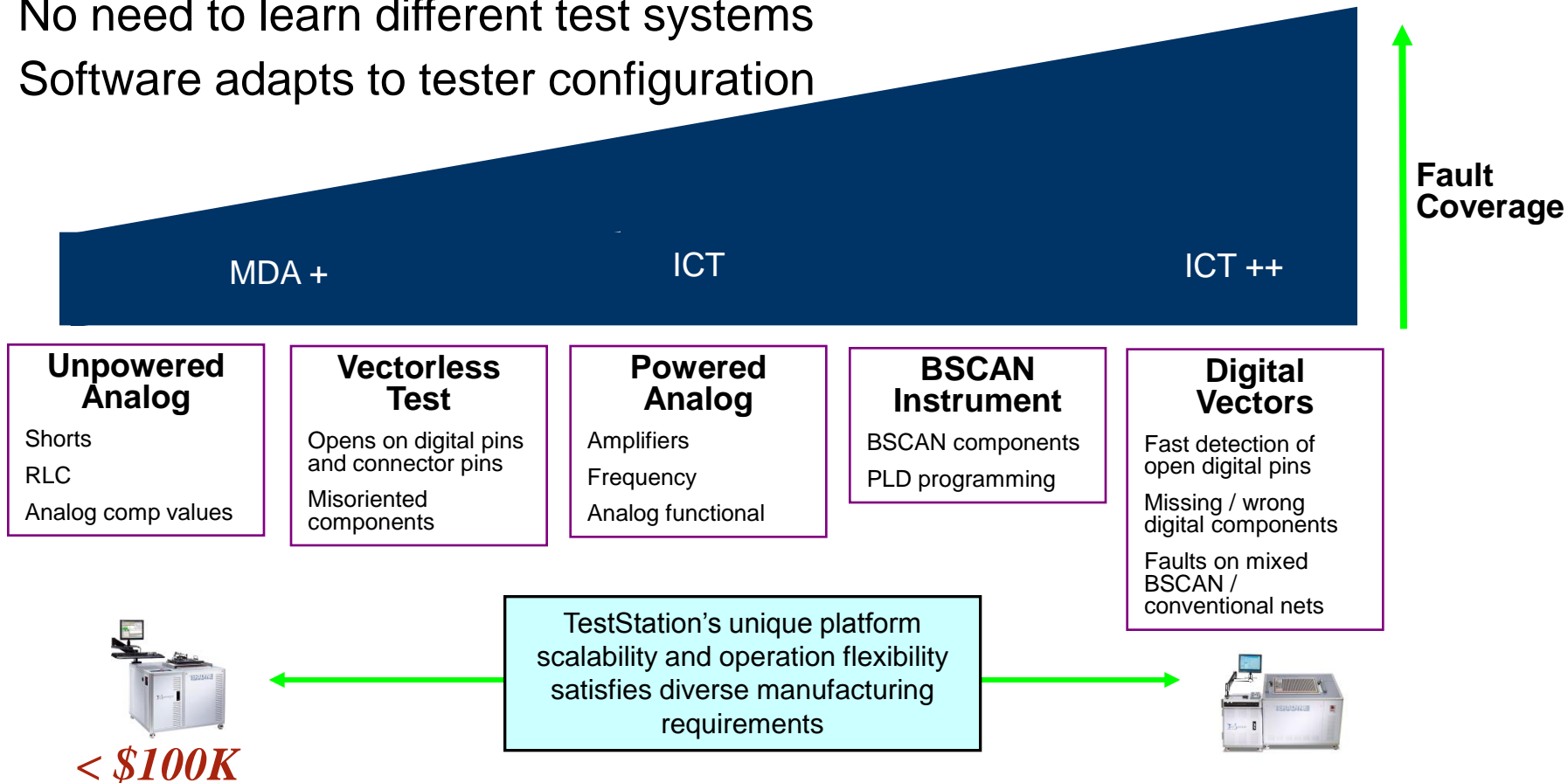
# ICT Manufacturers have Historically Met Diverse Requirements with Different Classes of ICT



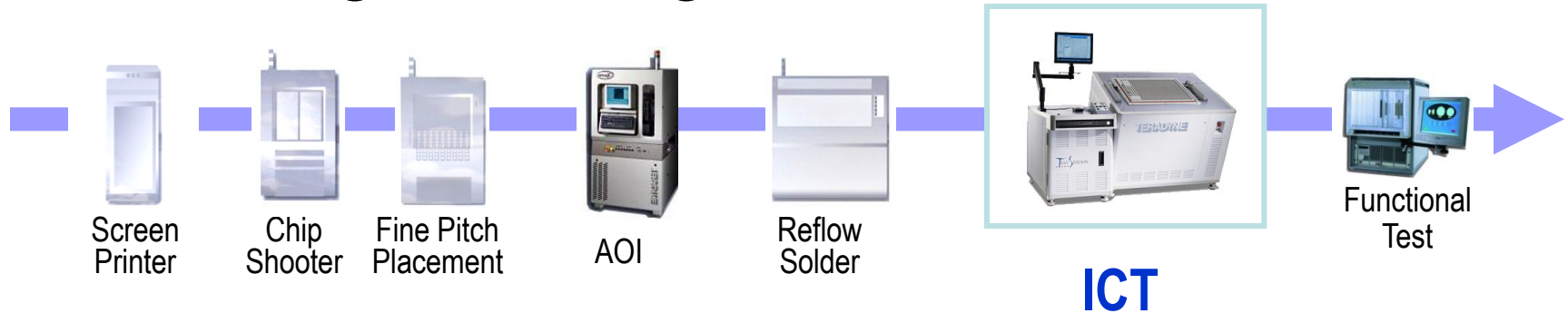


## Scalable ICT Platforms can Satisfy Diverse Manufacturing Requirements

- Buy only the test capability you need
- Grow or reduce fault coverage without changing the tester
- No need to change programs and test fixtures
- No need to learn different test systems
- Software adapts to tester configuration



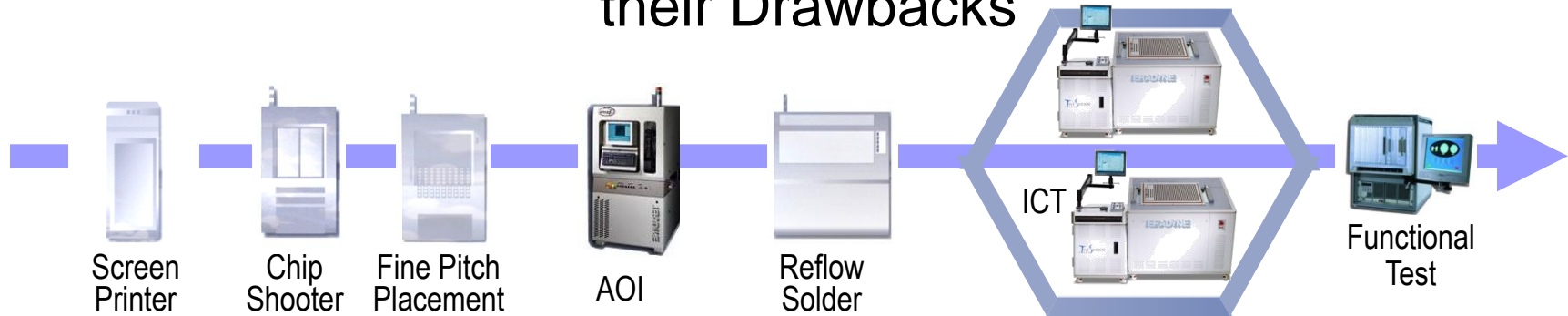
# Challenges for High Volume Manufacturers



- PCB assembly equipment speeds continue to increase
  - Manufacturing beat rates can be less than 30 seconds
- In-circuit tester becomes bottleneck on manufacturing line
  - ICT test times limit the amount of boards that can be manufactured
- Manufacturing facilities often have limited floor space
  - Adding additional test equipment is not always possible



# Methods Used to Satisfy High Volume Test Requirements...and their Drawbacks



- Add additional testers to the manufacturing line
  - Increases capital equipment, test fixture, and operation costs
  - Requires additional manufacturing floor space and test cells
- Underutilize tester by removing tests
  - Reduced fault coverage
  - Extra program maintenance
- Remove in-circuit test from manufacturing line
  - Implement less effective inspection strategy
  - Increased chance of shipping defective products

# Concurrent ICT Test Systems are Ideal for High Volume Applications

- Duplicate instruments capable of executing simultaneous tests
  - Supports parallel testing of two boards
- Up to twice the throughput of standard ICT testers
  - More test capacity throughput in same footprint as single system
- Valuable cost savings
  - Less expensive capital equipment, fixture, and operation costs



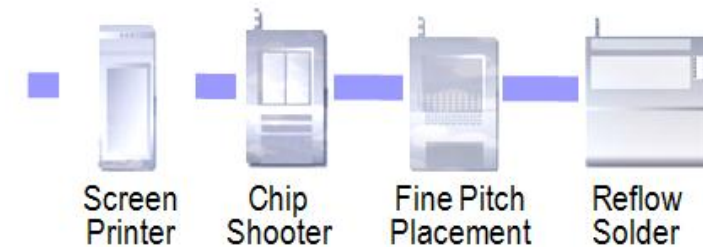
# Test Strategy Throughput Comparison

## Existing Single ICT Tester



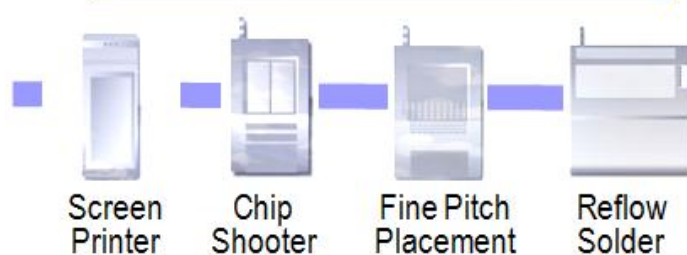
- Test Time: **130 Seconds**
- Test Cells: **1**
- Test Operators: **1**
- Test Fixtures: **1**
- Boards per Shift: **15950**
- Cost per Panel: **\$0.93**

## Two ICT Tester Solution



- Test Time: **65 Seconds**
- Test Cells: **2**
- Test Operators: **2**
- Test Fixtures: **2**
- Boards per Shift: **31901**
- Cost per Panel: **\$1.20**

## One Duo Tester Solution



- Test Time: **65 Seconds**
- Test Cells: **1**
- Test Operators: **1**
- Test Fixtures: **1**
- Boards per Shift: **31901**
- Cost per Panel: **\$0.57**



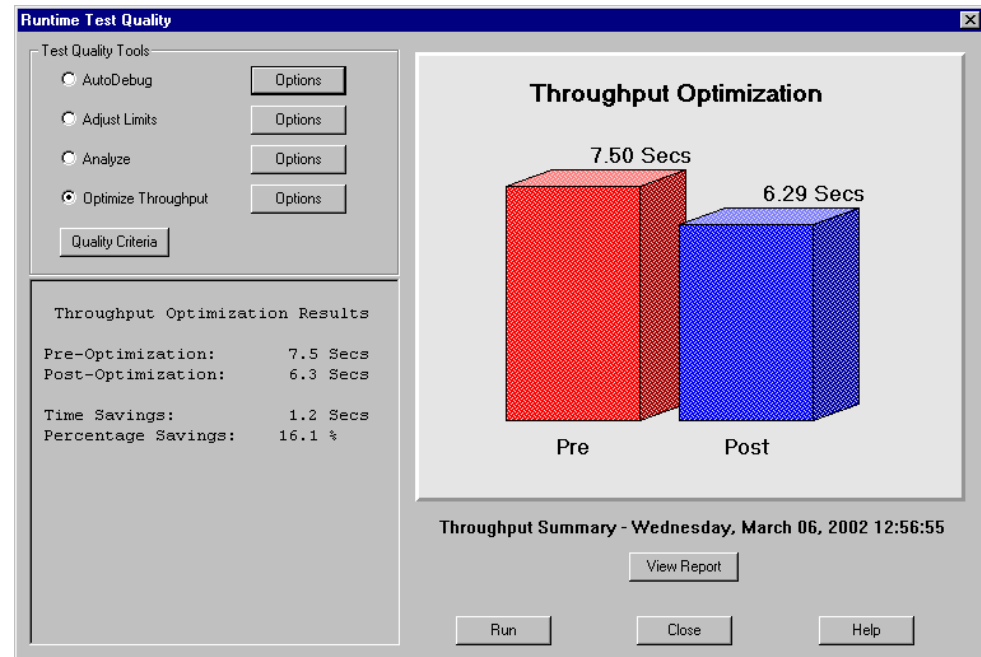
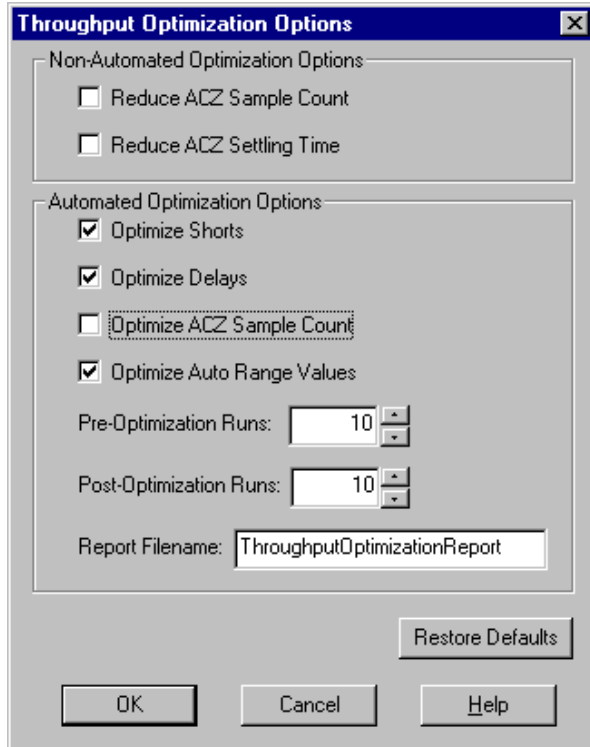
# Automated Solutions Increase Test Throughput Capacity

**ICT instruments available as Rack Mount components for easy integration into automated handler systems**

- ICT Subsystems configured for Integration
  - Tester Instruments available in 19" rack mount chassis
  - Power Controller Assembly
  - Integration Manual
- Custom Configurations
  - Three receiver options
  - Selectable multiplexing
  - Vacuum or Press-Down
- Automation partners
  - Provide turn-key in-line solutions



# Automated Tools can Optimize Test Execution Times for Best Test Throughput



- Optimizes AC measurement parameters
- Select fastest Shorts testing algorithm (linear or binary)
- Reduces program Delay values
- Optimizes expected values to minimize Instrument Autoranging

# ICT has Evolved to Meet the Challenges of Modern PCB Manufacturing

- Scalable ICT system design
  - Configurable from MDA+ to high performance / high pincount digital
- Advanced Pin electronics & Safetest technologies
  - For safe, accurate and reliable testing of low voltage technologies
- More powerful vectorless test technologies
  - For reliable testing of microBGA and small package components and connectors
- Incorporation of reduced access test techniques
  - For gaining test access to nets that do not have physical test access
  - Innovative combination BSCAN and Framescan technologies
- Specialized configurations and software for high volume applications
  - Rackmount modules support automated inline solutions
  - True concurrent test capabilities with TS Duo system
  - Throughput Optimization Toolset

