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Printed Circuit Board Reliability in High Temperature Lead-Free Processes

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Abstract

This paper will demonstrate the effect high reflow temperatures in lead free processes will have on the reliability of printed circuit boards from a broad range of laminate materials for both traditional and lead-free processes. The focus will be on 24 layer boards of high thickness (3.2 mm) and high aspect ratios (5.21:1 and 10.42:1). The test boards were preconditioned through six reflow cycles to simulate assembly and rework processes for both traditional and lead-free processes and then tested using IST.

The results showed that raising the reflow temperatures from standard tin-lead to lead-free had a significant effect on the reliability of PTVs, regardless of the laminate materials used. The results also showed that traditional and even some lead-free materials did not survive the temperature increase when measured against industry standards.

Introduction

As the electronics industry moves to become more environmental friendly, new legislations are being pushed through governments in various countries to eliminate the use of lead and other substances in electronic products. One area where lead is used extensively in electronics is the solder used in attaching electronic components onto printed circuit boards (PCB's). The obvious solution would be to replace leaded solder with lead-free solder. While the processing steps are the same for both types of solder, the peak temperature during soldering must be raised from 220°C for 63/37 tin-lead solder (melting temperature of 184°C) to approximately 255°C for tin-silver-copper solders (melting temperature of 217°C). This can potentially have a huge impact on the reliability of a product because the temperature differences are larger, causing more strains in the system. This paper will attempt to discuss the effects such a drastic change will have on PWB laminate systems, focusing on high-end electronic products such as network servers. The set up and procedure of the experiments involved will be stated and the results will be analysed. Conclusions from the study will then be presented and any future studies will be discussed.

Test Methodology Selection

In choosing a method for accelerated reliability testing, two primary methods were considered. The first method is thermal cycling in an air chamber, and the second is Interconnect Stress Testing (IST), where an electrical current is used to heat the test vehicle from within. While both methods offered similar results, IST Testing was chosen as the primary method for this study.

The major difference between the two tests is that the air chamber method will not stop cycling until the preset number of cycles is finished. So if a test vehicle fails in an early cycle, the air chamber will still constantly cycle that test vehicle, destroying the evidence of what caused the onset of failure. While it is possible to stop the air chamber and remove the failed TV, this will introduce new variables to the system (e.g. effect of cycling from a peak temperature to room temperature in addition to regular cycles). In IST, all the TVs are placed in separate compartments and thermal cycling for that compartment stops after that TV fails. This effectively preserves the cause of failure in the TV for further examination. Another advantage of IST are the relatively short thermal cycles; the air chamber cycles were 40-minute cycles while IST cycles are between 5 to 6 minutes.

There are two sets of independent circuits in an IST coupon to monitor two different failure modes. The first set, known as the "power" circuit, can be used to monitor any inner layer separations and foil cracking. The power circuit contains lower aspect ratio (the ratio between the board thickness to the drilled hole size) PTVs, and is also the circuit used by the IST system to heat the coupon. The second set, known as the "sense" circuit, is not powered, contains high aspect ratio PTVs, and can be used for monitoring barrel cracking.

After the coupons, whether they are preconditioned or not, are plugged into the IST system, the IST machine will attempt to find the appropriate amount of current to pass through the coupon to raise it to a temperature of 150˚C (above T_g of most Sn-Pb laminates) in three minutes. If the coupon is not stable enough for the system to find a constant current, then the coupon is considered to have failed before testing. During thermal cycling, as the strains begin to cause cracks in the PTVs to propagate, the resistance of the circuit will increase. Once the resistance of the coupon rises above a user defined rejection resistance, the cycling for that coupon is stopped.

It is important to select a low enough rejection resistance such that thermal cycling is stopped at the moment the failure begins to propagate. Once extended damage in the PTV is accumulated, the clues that lead to the cause of failure are destroyed. It is this ability of stopping testing at the start of failure propagation that sets IST testing apart from other conventional test methods.

An IST specification from a producer of high end servers stated that, for a product powered continually and used in a benign office environment, a minimum sample of 24 IST coupons preconditioned three times must survive these criteria:
1) All samples must survive at least 75 cycles
2) Samples must have a mean failure of at least 100 cycles

Failure times are evaluated at a 10% resistance increase as the failure criterion.

Laminate Material Properties
The following six different kinds of laminate materials, three contemporary and three new materials for lead-free applications, were tested as listed in Table 1.

Table 1 - Tested Laminate Material Properties

Material	Application	Thermal Cond. [W/mK]	T_g (DSC) [˚C]	α (z axis) [ppm/˚C]		α (x, y axes) [ppm/˚C]	
				$T < T_g$	$T > T_g$	$T < T_g$	$T > T_g$
A	Low T_g	0.3-0.4 W/mK	140	65	326	12-16	N/A
B	Pb-free	0.4-0.6 W/mK	175	60	288	12-14	N/A
C	Mid T_g	0.36 W/mK	140	50	250	15	17
D	Pb-free	0.36 W/mK	175	50	250	15	17
E	High T_g	N/A	180	N/A	120	13	N/A
F	Pb-free	N/A	180	N/A	140	11-13	N/A

While materials A and C both had the same T_g, material C was considered "Mid T_g" in the industry. This was presumably because material C's α (z-axis) was significantly lower than material A's α (z-axis) and therefore caused less stress to the PTV. Material E had comparable characteristics as material F, but material E was used for experimental reasons and material F was designed for mass production.

Materials A and B were from one supplier, C and D were from another supplier and E and F were from a third supplier. This comparison testing allowed the material suppliers to appreciate how each of their two products fared in the different temperature processes.

Test Board Layout
For each material, large 457mm (18") x 610mm (24") panels were made at Multek in Irvine, California, and each carried four test boards. They were separated and vacuum packed before being shipped to Celestica. Each test board was 267mm (10.5") x 203mm(8.0") x 3.2mm(0.125"), 24 layers thick and finished with plain copper. Every test board contained six IST coupons laid out parallel to each other. There were also square shaped sections at the top of the board. They were for tests that the laminate suppliers were going to do on their own. The test PCBs likeliness was as depicted in Figure 1.

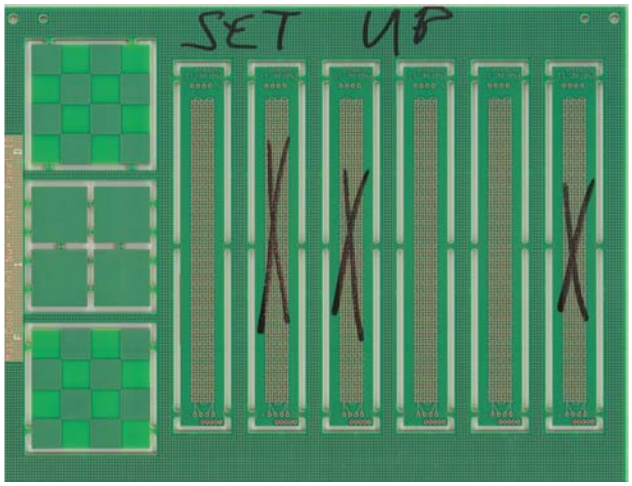

Figure 1 - Top View of the Test PCB Layout

The test board's material (A to F), large board number (1 to 8) and test board letter (A through D) identified each test board. The boards were identified were as depicted in Figure 2.

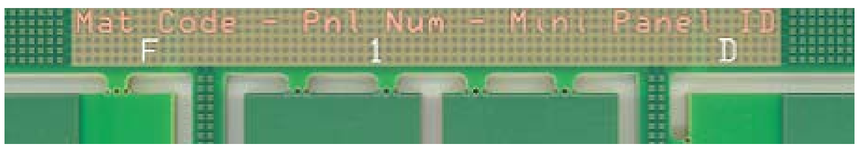

Figure 2 - Test Board Identification

The coupons on the board were identified by their test board letter and numbered 1 to 6 from left to right if the board was laid out as depicted in Figure 1.

Test Vehicle Design

The IST coupons had dimensions of 19mm (.750") x 152mm (6.000") and contained power and sense circuits, each consisting of 404 PTVs connected in series. The vias for the power circuit had drilled hole diameters of 0.60mm (0.024") and pad diameters of 0.97mm (0.038"), resulting in an aspect ratio of 5.21:1. The sense circuit had drilled hole diameters of 0.30mm (0.012") and pad diameters of 0.66mm (0.026"), resulting in an aspect ratio of 10.42:1. The grid spacing was 1.27mm (0.05") and there were no non-functional pads. Connections between the PTVs in the power circuit were on layers 2, 3, 22 and 23, while the connections for the sense circuit were on layers 1, 2, 23 and 24.

Sample Size

The total number of boards that were preconditioned at specified temperatures and number of reflows for IST testing were as described in Table 2. All of the boards were preconditioned at Celestica Inc. in Toronto, Canada. The supplier of Material E requested a study into the effects the number of reflows had on reliability. This was the reason for the proposed 3x reflow samples.

IST testing was completed in two labs due to availability of these machines. The sample size for material F was doubled because of the need to determine if there was a difference in the test results from the two labs where IST testing would be conducted. The testing sites involved were the Naval Surface Warfare Centre (NSWC) at Crane, Indiana, and Celestica in Toronto, Canada. NSWC Crane handled the samples that would be used to compare the performance of the materials at AsRcvd, 6x220 and 6x255. The number of PCBs sent to Crane was as described in Table 3.

Unfortunately, because of budget constraints, only half of the IST coupons sent to NSWC Crane were tested. The number of test boards remaining at Celestica was as described in Table 4 below.

Table 2 - Number of Test Boards of Each Material Preconditioned in Each Condition

Material	AsRcvd*	3 x 220	6 x 220	3 x 255	6 x 255	Total
A	2		2		2	6
B	2		2		2	6
C	2		2		2	6
D	2		2		2	6
E	4	2	2	2	2	12
F	4		4		4	12
Total	16	2	14	2	14	48

*AsRcvd = As Received

Table 3 - Number of Test PCBs Sent to Crane for IST Testing

Material	AsRcvd	3 x 220	6 x 220	3 x 255	6 x 255	Total
A	2		2		2	6
B	2		2		2	6
C	2		2		2	6
D	2		2		2	6
E	2		2		2	6
F	2		2		2	6
Total	12		12		12	36

Table 4 - Number of Test PCBs that Remained at Celestica for IST tesTing

Material	AsRcvd	3 x 220	6 x 220	3 x 255	6 x 255	Total
A						
B						
C						
D						
E	2	2		2		6
F	2		2		2	6
Total	4		2		2	8

Testing Procedure

The test procedures were divided into two steps: preconditioning and IST testing. The preconditioning step included reflow oven profiling, passing the boards through the reflow oven, and resistance testing to ensure the boards survived the reflow process.

Before the preconditioning step, thermocouples were attached to a test board to measure the temperature profile of the "Conceptronics Model HVN_2 155" reflow oven at Celestica. The oven had ten zones, numbered 1 to 10 from entry to exit, enabling the oven to obtain different temperatures in different zones. The speed of the conveyor belt passing the board through the oven can be manually adjusted and the atmosphere can be selected as well. Celestica had specific guidelines for the temperature profiles for standard tin-lead solder processes. These guidelines were used to construct the profiles used in standard preconditioning. For the lead-free reflow profile, a guideline titled "NEMI Position Statement Regarding Lead-Free Solder Reflow Component Temperatures" by NEMI (National Electronics Manufacturing Initiative) that was distributed for a conference call on March 12, 2002 was used to build the lead-free profile, with a peak temperature of 255˚C.

One test board from each laminate material was profiled this way to confirm that the oven settings would produce the same profile for all boards. The same test board was also used in subsequent reflow sessions to ensure that the profiles were consistent from session to session. For storage, the boards were placed in a "dry room" to reduce the possible effects moisture would have on the test PCBs.

Before the actual test boards were preconditioned, the resistances of the daisy chains were recorded and any initial opens or shorts were noted. A "BK Precision Test Bench 388A" multimeter and later a "Fluke 75 Series III" multimeter were used to take the resistance measurements when the original multimeter became inaccessible. The resistance readings were also taken after every single reflow. A micro-ohmmeter would have been more appropriate because the resistance readings were in the magnitude of 1Ω. Unfortunately, the connectors required by the micro-ohmmeter (and the IST machine) could not survive reflow temperatures. After the specified number of reflows was completed, the connector was selectively soldered on and a micro-ohmmeter was used to confirm the resistance readings of the multimeter.

A quick scan of the maximum change in the resistances revealed a gap between the resistances of the nets that obviously failed (max delta > 20%) and the ones that were not so obvious (max delta < 15%). Hence, for the IST coupons in this study, a coupon was considered to have failed if the resistance of either the power or the sense circuit increased by at least 15%. This failure criterion was also used during IST. After all the resistance readings were taken, the IST coupons were detached from the board, packaged, and sent to labs for IST testing.

The IST machines at both Celestica and Crane were used to thermally cycle the IST coupons from ambient temperature to 150ºC a maximum of 1000 times or to a 15% increase in daisy chain resistance, whatever came first. When an IST coupon failed, the number of cycles to failure and failure mode were recorded. The results were then compiled and analysed.

IST Results

The data was first tested for goodness of fit, and then data from both labs was correlated in an attempt to pool data for larger sample sizes. Additionally, an α of 0.05 and a *CI* of 95% were selected. The selection of these values did not affect the final outcome much because of the overwhelming influence small sample sizes have on the significance and confidence. Also, coupons that failed before IST testing was performed were not plotted, because of the lack of certainty of failure mode. They were taken into account at the end, when the final recommendations were made. Unless otherwise stated, all failures studied were sense circuit failures, since they were considered ideal, whereas power circuit failures were considered to be suspensions (samples that failed in other failure modes).

Goodness of Fit Results

The r^2 statistic indicated that both Weibull and lognormal distributions fitted the data well in both cases. Since Weibull data tended to fit lognormal functions, it was a strong indication that the reliability of the IST coupons did follow the Weibull function.

The A^{2*} statistic indicated that Weibull with Maximum Likelihood Estimation (MLE) estimates did not fit some samples with suspensions. However, the current version of A^{2*} was not designed to handle data with suspensions anyway. Since the r^2 statistic indicated a good fit for complete data, it was assumed that the Weibull function also fit data with suspensions. The satisfactory A^{2*} statistic in most fits also indicated that no adjust for bias was needed for the MLE estimates. This also opened up the possibilities of using likelihood ratios to calculate the confidence bounds.

Correlation of Results from Celestica and Crane

To correlate the data between Celestica and Crane, the IST results from both labs for the same material and preconditioning were analysed. While the distributions appeared to be different in the Weibull plots, the contour plots confirmed that the data from both IST labs were not statistically different. Therefore, results from Celestica and Crane for the same material subjected to the same pre-conditioning could be pooled together. For F: AsRcvd, Crane had only one coupon that survived to IST testing, so a comparison was made between Celestica's data and the pooled data instead.

Interpreting the Acceptance Criteria

From the acceptance criterion presented earlier, the most lenient criterion possible would be if all the failures came from one failure mode. Using Bernard's approximation of the median ranks, this would require a material to have a maximum 3% chance of failure before 75 cycles. Therefore, for a material to be considered fit for use, its IST results must pass the following two criteria:

1. Must have a maximum of 3% chance of failure before 75 cycles.
2. *MTTF* must be greater than 100 cycles.

Even though the criteria were based on a rejection resistance increase of 10%, having the material fail the criteria at 15% would have been even more telling. For criterion 2, the central limit theorem and *t*-distribution with *n*-1 degrees of freedom will be used to test the following hypothesis:

H_0: There is <u>insufficient</u> evidence to support the claim that $MTTF \geq 100$

H_a: There is <u>sufficient</u> evidence to support the claim that $MTTF \geq 100$

The significance level α will remain at 0.05. Unfortunately, the central limit theorem is based on large sample theory. Due to the lack of options, however, the theory was still used.

Results for "AsRcvd" Preconditioning

With the exception of five dead on arrival boards for material F tested at Crane, all of the materials without preconditioning were tested in IST. The results were as depicted in Figures 3 and 4.

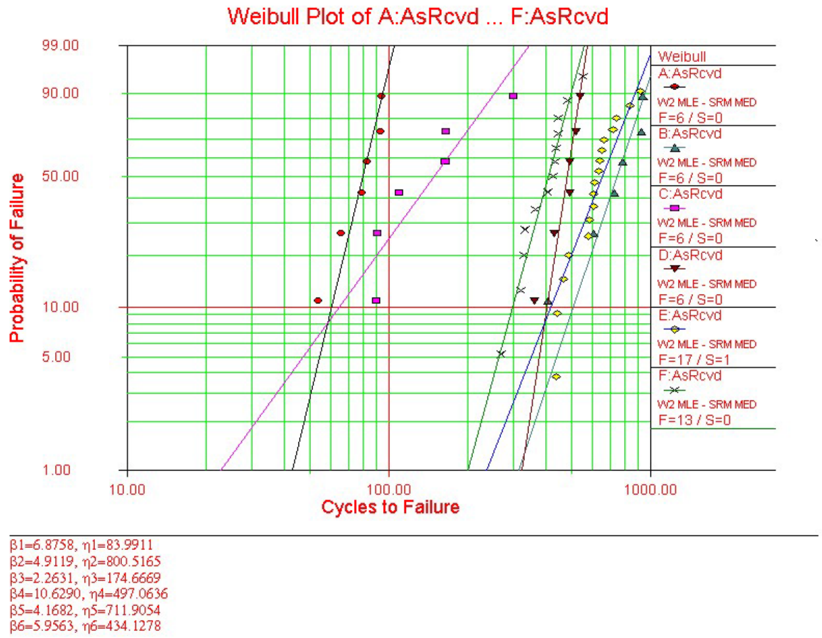

Figure 3 - Results from AsRcvd

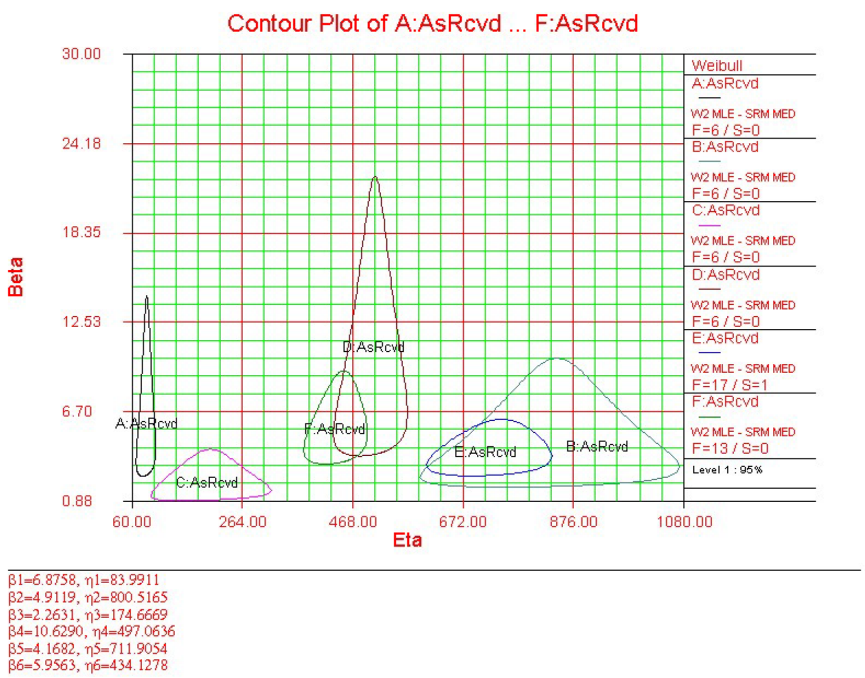

Figure 4 - *CI* Contours from AsRcvd

The evaluation of the materials' performance to the acceptance criteria was not made here, because of the clutter presented by having six distributions with confidence bounds interweaving on the graph. The acceptance check was performed when each material was studied in detail. From Figures 3 and 4, the performances of material D and F were not statistically different, and the same could be said of materials B and E. The rankings of performances were as described in Table 5.

Table 5 - Material Performance Rankings with "AsRcvd" Preconditioning.

Rankings	Material
1 (Best)	B, E
2	D, F
3	C
4 (Worst)	A

As expected, the lead-free and high T_g materials were more reliable than the conventional materials at this preconditioning level. It was surprising to note that material B performed as well as material E and better than F and C, even though the mechanical properties of B were less desirable than the others.

Results for "6x220" Preconditioning

Material A failed to survive 6x220 preconditioning and pre-IST testing failures were beginning to occur for materials B, C and D. This was a cause for concern because those materials were designed to survive reflow temperatures higher than the current tin-lead soldering process. The results from this preconditioning level were as depicted in Figure 5 and Figure 6.

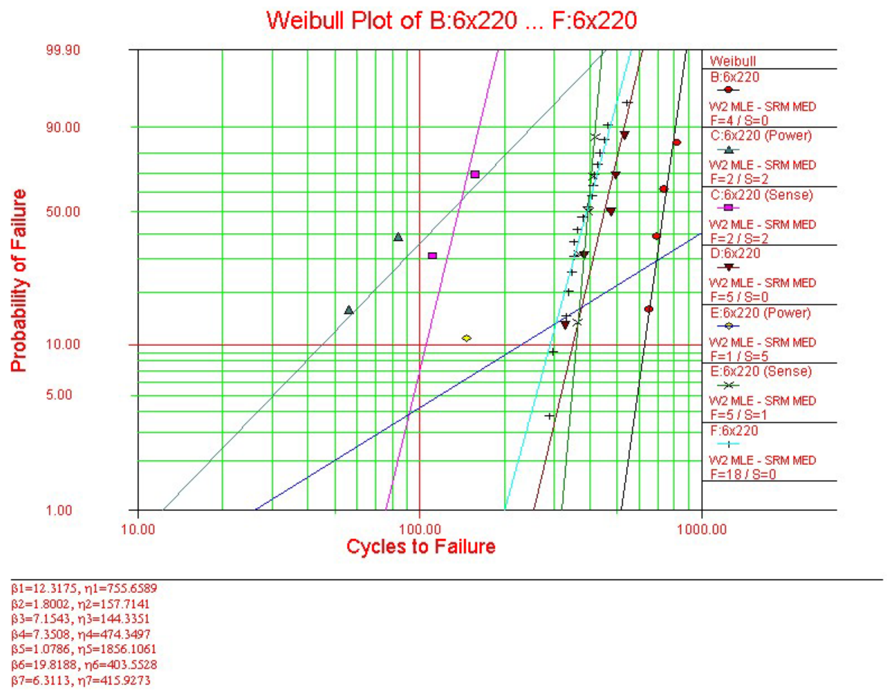

Figure 5 - Results from 6x220

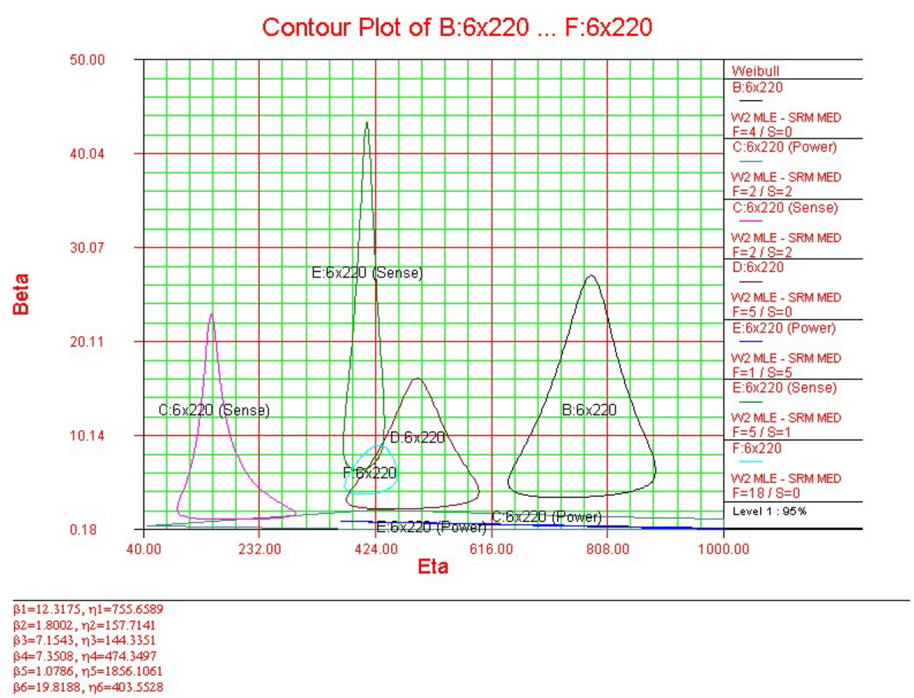

Figure 6 - *CI* Contours from 6x220

From the two figures above, the rankings in Table 6 were deduced. Material B continued to outperform the other materials for this preconditioning and the rankings were similar to AsRcvd preconditioning. Failures in the Power circuit dominated the lower failure end of the failure curve for materials C and E. The small sample sizes resulting in splitting the sample between sense and power failures had a huge effect on the confidence bounds. The resulting confidence bounds were so wide that it was impossible to extract any meaningful information from the plot.

There was an early failure in one of the samples for material B, occurring at cycle 239. While the failure mode for this coupon was in the sense circuit, the data point fell out of the confidence bounds of the fitted curve when plotted. This indicated that the point very likely did not belong in the same distribution, because the probability of a point landing outside the bounds was less than α (5%). Since it could not be concluded from the numbers that the point was a suspension or a legitimate failure, it was left out of the analysis.

Table 6 - Material Performance Rankings with "6x220" Preconditioning.

Rankings	Material
1 (Best)	B
2	D, E (Sense), F
3	C (Sense)
4 (Worst)	C (Power), E (Power)

Results for "6x255" Preconditioning

Material A and, surprisingly, material F did not survive preconditioning. Power failures in materials C and E continued to occur. The IST results were as described in Figure 7 and Figure 8.

From the two figures above, the rankings in Table 7 were deduced. Material B continued to dominate the field while variability in performances of materials C, D and E were starting to expand from a study of the contour plot.

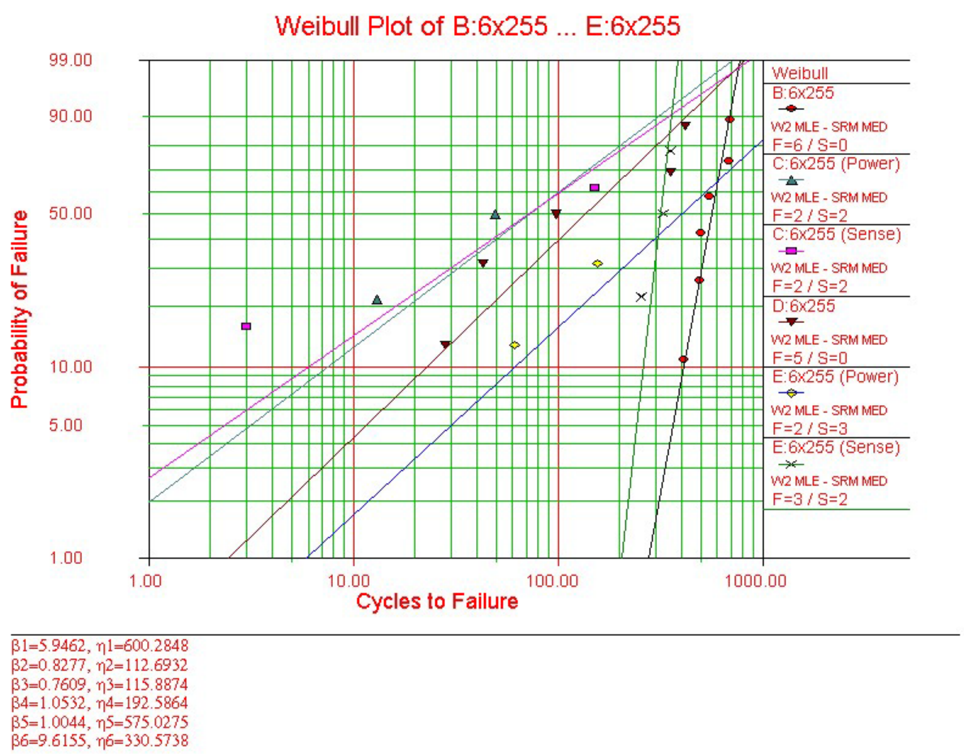

Figure 7 - Results from 6x220

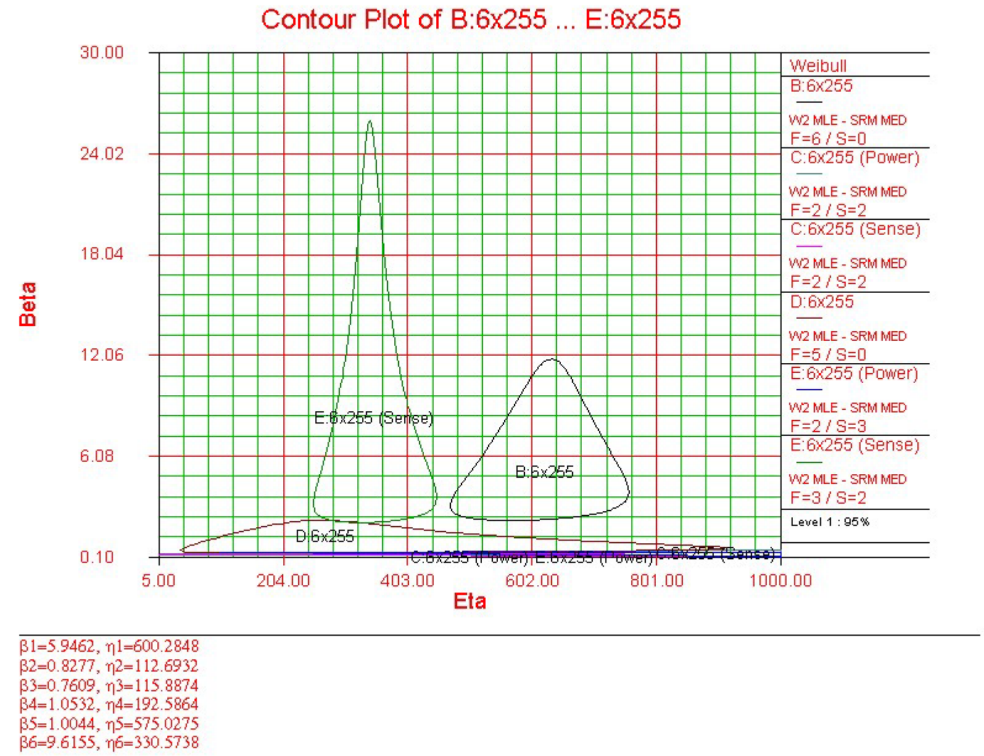

Figure 8 - *CI* Contours from 6x220

Table 7 - Material Performance Rankings with "6x220" Preconditioning

Rankings	Material
1 (Best)	B
2	E (Sense)
3	D
4 (Worst)	C (Sense, Power), E (Power)

Summary of Results

In general, the increase in the maximum preconditioning temperature from 220˚C to 255˚C decreased the reliability of the IST coupons built using the six laminate materials. In some cases, materials that would have been considered fit for use when preconditioned at 220˚C did not survive when preconditioned at 255˚C.

Increasing the number of reflows from three to six brought to light the power circuit failure mode to material E in addition to the sense failure mode being studied. This may have been the case as well for material C; unfortunately, the test matrix did not include samples at 3x reflow for that material. The distribution of power circuit failures had shape factors of 1, indicating the failures were random in nature. Failure analysis of the power circuit failures must be done, for they would provide insight on the causes of the failures and how to properly take them into account. The results from IST testing were as summarised in Table 8 through Table 12.

Table 8 - Material Performance at AsRcvd Preconditioning Level

Material	Pass/Fail
A (low T_g matl.)	Fail
B (lead-free matl.)	Pass
C (low T_g matl.)	Fail
D (lead-free matl.)	Pass
E (high T_g matl.)	Pass
F (lead-free matl.)	Pass

Table 9 - Material perFormance at 3x220 Preconditioning Level

Material	Pass/Fail
E	Pass

Table 10 - Material Performance at 3x255 Preconditioning Level

Material	Pass/Fail
E	Pass

Table 11 - Material Performance at 6x220 Preconditioning Level

Material	Pass/Fail
A	Fail
B	Pass
C	Fail
D	Pass
E (not including power failures)	Pass
E (including power failures)	Fail
F	Pass

Table 12 - Material Performance at 6x255 Preconditioning Level

Material	Pass/Fail
A	Fail
B	Pass
C	Fail
D	Fail
E (not including power failures)	Borderline Fail
E (including power failures)	Fail
F	Fail

From the above tables:

- Material B could be used in both tin-lead and lead-free processes
- Material E could be used in both tin-lead and lead-free processes if power failures were discounted
- Material D and F could be used in tin-lead, but not lead-free processes
- Material A and C were not fit for use in either tin-lead or lead-free processes

Material B performed equally well under all three preconditioning levels, although there were trends visible that the results for AsRcvd was slightly better than 6x220 which in turn was better than 6x255. A cause for the introduction of power failures in materials C and E may be due to their low $\alpha_{>Tg}$ when compared to materials of the same T_g. While the performance of material E in the sense circuit was excellent, the random nature of the power circuit failures was a cause for concern. If the power circuit failures were ignored, material E would have been fit for use in both tin-lead and lead-free applications.

As depicted in Table 1, material A had an $\alpha_{>Tg}$ of 326ppm/˚C while material C had an $\alpha_{>Tg}$ of 250ppm/˚C. This decrease in the coefficient of expansion may be enough to move the Weibull curve to the right far enough to expose the power circuit failure mode. The same could be said for material E when compared to F, providing the power failures in F were similar in nature. This would indicate that laminate material manufacturers should strive to raise T_g rather than lower $\alpha_{>Tg}$ in their design of new materials to avoid power circuit failures (foil cracking, innerplane separation) from being the dominant failures. The randomness of power circuit failures would make prediction of product life difficult.

As the hypotheses are defined, the significance level α at 0.05 and the confidence interval *CI* at 95%, there will be at most a 5% chance (Alpha Risk) that the laminate material, deemed acceptable for use for a specific process in this study, will fail the acceptance criterion of $MTTF \geq 100$ and 3% percentile failure of 75 cycles. This claim is pending thorough failure analysis of samples and the study of effects of small sample sizes on confidence intervals and hypothesis testing.

Conclusions

To reiterate, the purpose of this study was to use IST testing in conjunction with reflow oven preconditioning to provide an indication as to whether or not:

1) High-end products built with current materials would survive Pb-free processes,
2) High-end products built with new Pb-free laminates would survive Pb-free processes,
3) There are significant reliability penalties in moving from Pb to Pb-free processes.

Based on the results presented, there was a strong indication that high-end products built with current laminate materials, represented by material A and C, would not survive lead-free processes. Products built with new Pb-free laminates in general would survive Pb-free processes, but the end products would not meet OEM reliability demands. The increase in the temperature from 220ºC to 255ºC had significant reliability consequences, as both lead-free and tin-lead materials currently considered fit for use in 220ºC processes did not survive in 255ºC processing.

To summarise, if the materials tested here are representative of what is being used in the industry, then there is a strong indication that the industry is not ready yet to make the switch from tin-lead to lead-free processes. The reliability penalties in switching are heavy and high-end products built using lead free laminates will either fail significantly earlier than their tin lead counterparts, or will not survive the assembly process at all.

Future Considerations

This paper needs to be followed up in three areas as follows:

1. Failure Analysis of Failed Samples

Cross-sectioning and flat-sectioning of failed IST samples are needed to ensure there are no other failure modes hidden in the distribution (e.g., D: 6x255). Also, analysis needs to be done on the samples that did not make it to IST testing, to ensure that it was the material's mechanical properties that caused the failure, not manufacturing or other problems. Finally, there is a need to find the root cause of the power circuit failures because of its random nature. Failure analysis will provide a better understanding on how to incorporate power circuit failures into the data.

2. Effects of Small Sample Sizes

The sample sizes in this study are small compared to what is needed for traditional hypothesis testing and estimation of parameters. Therefore, the effect the small sample sizes on parameter and confidence bounds estimates must be studied. The effect of such small sample sizes on the results will provide more certainty to the conclusions drawn from the data. A further analysis by Monte Carlo simulations may be beneficial as well.

3. Test Acceptable Laminate Materials in Real Products

IST testing can only give projected performances. Building a live product from a material deemed fit for use in this study will provide actual results of reliability. These results can also be used to correlate field data to IST test data.

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8. Ms. Pooneh Vaziri, Celestica Inc.
9. Mr. Ronald Brock, NSWC Crane**References**

References

1. J. Smetana, "Plated Through Hole Reliability with High Temperature Lead-Free Soldering," The Board Authority, pp. 50-64, April 2002.
2. S. M. Bhandarkar, et al., "Influence of Selected Design Variables on Thermo-Mechanical Stress Distributions in Plated-Through-Hole Structures", Transactions of the Asme, pp. 8-13, vol. 114, March 1992.
3. J. P. Schaffer, et al., The Science and Design of Engineering Materials, 2nd ed., Boston: McGraw-Hill Companies, Inc., 1999.
4. D. Bergman, ED, "Surface Mount Council White Paper: Design for Success," [Online document], 1997 April, [cited 2003 March 29],
5. Available HTTP: http://www.ipc.org/4.0_Knowledge/4.1_Standards/smcwp004.pdf
6. J. P. Clech, "Solder Joint Failure Statistics," in Proc. EPSI Solder Joint Reliability of Surface Mount Assemblies. Toronto, Canada, 2001.
7. C. E. Ebeling, Introduction to Reliability and Maintainability Engineering, New York, New York: The McGraw-Hill Companies, Inc., 1997.
8. R. B. Abernethy, The New Weibull Handbook, 2nd ed. , North Palm Beach, Florida: Robert. B. Abernethy, 1996.
9. R. B. D'Agostino, and M. A. Stephens. Goodness-of-Fit Techniques. New York, New York: Marcel Dekker, Inc., 1986.

10. H. Hirose, "Bias Correction for the Maximum Likelihood Estimates in the Two-parameter Weibull Distribution," IEEE Transactions on Dielectrics and Electrical Insulation, vol. 6, no. 1, pp. 66-68, February 1999.
11. D. D. Wackerly, et al., Mathematical Statistics with Applications, 5th ed. , Belmont, California: Wadsworth Publishing Company, 1996.
12. G. Gavrel, "IST Technology," [Online document], 2000 Apr 12, [cited 2003 March 29],Available HTTP: http://www.pwbcorp.com/FrameDoc.html