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Decoupling with Anodized Ta

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Novel configurations of decoupling capacitors were formed by anodizing Ta, resulting in Ta_2O_5 films 2000 Å thick and k = 23, giving about 110 nF/cm^2. Since the dielectric is very thin, the parasitic inductance is almost unmeasurable, and is shown by simulation to be less than 1 pH/square. Breakdown voltages are around 30 V and leakage at 5 V is less than 0.1 μA/cm^2. The total ESR is dependent on the plate thickness, but can be less than 10 mΩ. Since the material is paraelectric, there is no significant falloff of dielectric behavior at frequencies well over 10 GHz. The capacitors are formed on flex with close-spaced, alternating contacts to minimize contact inductance. The assemblies are designed to be included in a polymer-based BGA stack to provide ultra-low inductance as close to the chip as possible. In this presentation, the reasons for using these materials and configurations are presented from the point of view of electronic performance, reliability, and manufacturability.

Introduction

The two requirements for effective decoupling are to be able to deliver enough charge to run the IC for one clock cycle and to be able to deliver the high switching current without causing a drop in power-ground voltage.[1, 2] The first requirement is satisfied by providing sufficient specific capacitance by a combination of high k and/or a thin dielectric, and the second demands low parasitic inductance (ESL). Since inductances add in series, all significant sources must be removed between the decoupling capacitor's dielectric layer and the current's point of use at the chip's boundary. With discrete components, the ESL is reduced by connecting many of them in parallel. While this does reduce the aggregate ESL, it increases the capacitance often to values much larger than required, which also means the loss of more valuable on-board real estate. Embedded capacitors are the solution to this problem because thin planar dielectrics, with plates properly connected to the chips they decouple, mean lower ESL.[3-5]

The amount of capacitance required depends on the power demands of the chip. A 30 W chip operating at 3 V with a 1 GHz clock would require 10 A on the average, or 10 nCoulombs of charge per clock cycle. If the final stage decoupling capacitor is to provide this with no more than a 10% drop in voltage, a capacitance of 33 nF is necessary. Table 1 shows the specific capacitance and required areas to give 33 nF using various embedded capacitor technologies either currently available or soon to appear on the market.[6]

Table 1 - Area Requirements to achieve 33 nF with Various Embedded Capacitor Dielectrics

Dielectric	Dielectric Constant	Thickness (μm)	Specific Capacitance (nF/cm^2)	Area Required for 33 nF (cm^2)
4 mils FR4 pre-preg	4.6	100	0.041	800
unfilled laminated polymer	4	25	0.14	240
filled laminated polymer	20	25	0.70	47
spin-on BCB	2.7	2.0	1.2	28
ferroelectric powder in epoxy matrix	90	5.0	16	2.1
Al_2O_3	9	0.2	40	0.83
Ta_2O_5	24	0.2	110	0.30
barium titanate	~2000	1.0	1800	0.018

Low capacitance density solutions, such as unfilled polymers, require excessive footprints. Ferroelectric powders dispersed into polymer carriers can provide the needed capacitance in a small footprint, but may exhibit relaxation behavior that would cause its dielectric constant to decrease at high frequencies.[7] Tantalum oxide gives one of the highest specific capacitances of any well-behaved paraelectric material, mainly due to its very thin dielectric layer. Pure ferroelectrics, such as barium titanate, give much higher specific capacitances than is possible with tantalum oxide or any other paraelectric, but require curing at >600°C in pure oxygen to achieve these values, which no organic board could withstand. However, these materials can be processed on metal foil separately and transferred to the board after curing.

The second requirement that of reducing parasitic inductance, can only be satisfied by removing inductance from both the capacitor itself and from the power-ground path between cap and chip.[8] As far as the capacitor itself is concerned, embedded dielectrics show almost two orders of magnitude less inductance than standard surface mount parts, mainly because of the way currents flow through the devices. As shown in Figure 1, currents through typical surface mount capacitors flow in the same direction and, as a result, the magnetic fields add resulting in high inductance. By contrast, currents through embedded capacitors move in opposite directions, resulting in canceling fields and much lower inductance.[1]

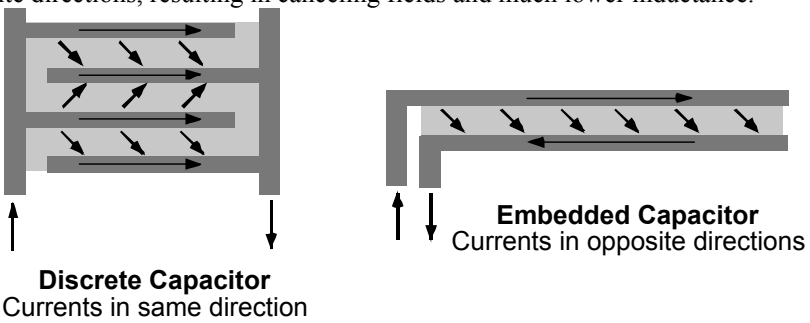

Figure 1 - Current directions through surface mount and embedded capacitors.

In addition to lower inductances in the embedded capacitors themselves, there is reduced inductance in the connections since the currents do not have to be sent up to and back from the board surface (Figure 2).

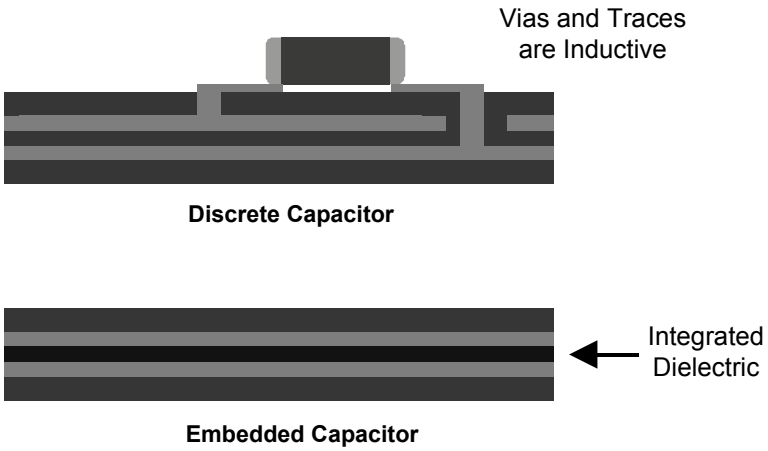

Figure 2 - Shorter current paths in embedded capacitors

Hence the reasons for using anodized tantalum thin films for decoupling can be summarized as:

- Low ESL
- Low ESR
- Saving board area in the vicinity of the chip
- High specific capacitance.

Fabrication

The capacitors are formed on flex material using not a lamination process, but a build-up process. 3 mil thick Upilex®, which is a polyimide film, was used due to ease of processing and also because Upilex® has a CTE of 20 rather than the much higher CTE of Kapton®. The Upilex® film was the planarized to obtain a smooth surface and also because studies have shown that surface roughness of the film can lead to defects in the resulting capacitors. The film was glued at the edges to 5" glass wafers using an adhesive that does not outgas in the vacuum systems used in processing. The process flow is as shown in the figure below. DC Magnetron sputtering was used at low power (1kiloWatt) to sputter the top plate, bottom plate and plating seed layer. The bottom plate is a stack-up of Titanium/Copper/Tantalum approximately 3μm thick, while the top plate is also a stack-up of 0.5μm thick Titanium/Copper/Tantalum. Low power was used so as not to overheat the substrate. Tantalum was anodized using an electrolytic solution, first at constant current and then at constant voltage. Anodization leads to the formation of a 2000Å Tantalum Oxide layer. The un-anodized Tantalum is part of the bottom plate. Reactive Ion Etch (RIE) using O_2, Argon and SF_6 was used to pattern the dielectric. Since the Flex substrate cannot withstand long process runs in the RIE tool, each run was 2 minutes long followed by a 5 minute interval before the next run. Argon is also used for the

same purpose. A passivation layer using B-staged bisbenzocyclobutene (BCB) was applied, and nickel-gold contacts were electroplated. The capacitors were then diced and mounted on a board for testing. (See Figure 3.)

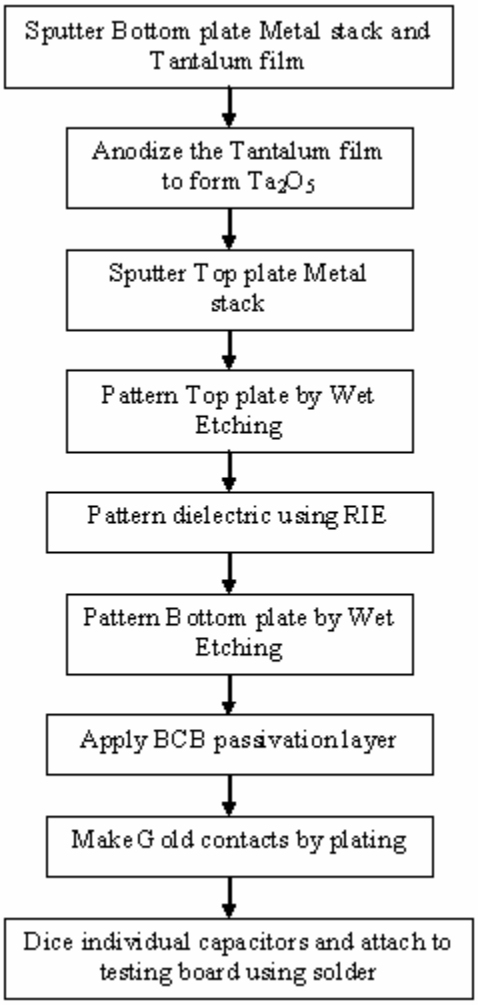

Figure 3 - Fabrication Process Flow

Configuration

Several sizes of capacitors were fabricated: areas were $1cm^2$, $0.5cm^2$ and $0.25cm^2$. Various configurations including the sawtooth structure shown in Figure 4, as well as line contacts to top and bottom plates and a single point contact were tried. A couple of different configurations are for the different probes used. Multiple point contacts to top and bottom plates are shown in Figure 4. The capacitor is referred to as Stealth™ because the extremely low inductance allows it to absorb noise like the Stealth bomber absorbs radar signals.

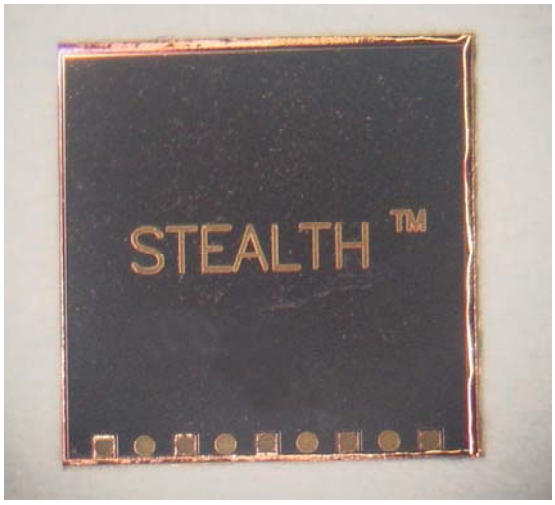

Figure 4 - STEALTH™ Capacitor with Single Row Connections

Line contacts can be used to reduce inductance. A cross section of a line-connected capacitor is shown in Figure 5. A detailed discussion of the properties of the line-contacted capacitor and its transmission line model appears in Reference 5. Either a line-contacted model or a multiple point-contacted model is appropriate for an embedded capacitor, which might be connected to a load IC with many vias and solder bumps. The precise performance in a given application will have to be simulated. Work is going on now to correlate simulated capacitor performance with measurement.

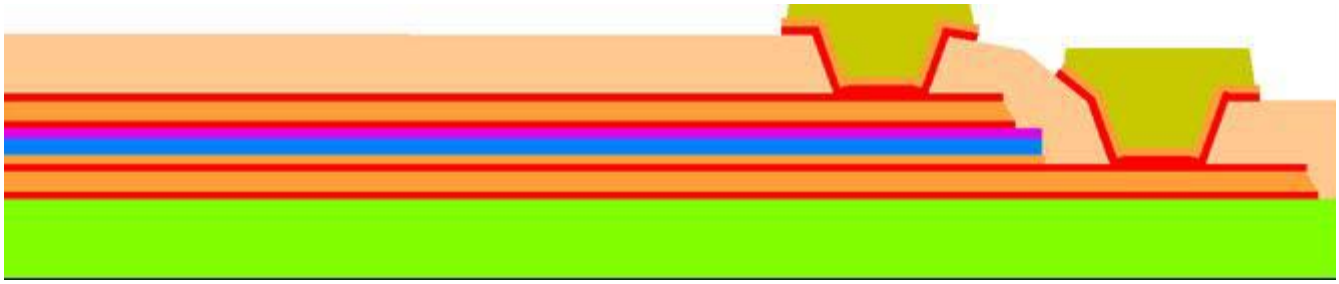

Figure 5 - Cross-Section of a Line-Connected Capacitor - Base Flex Material is Green; Copper Plates are Orange; Tantalum is Blue; Dielectric is Purple; Gold Terminal Stripes are Yellow

Electrical and Reliability Testing

Electrical tests conducted include characterization and fitting of impedance to an R-L-C model, leakage tests, and breakdown voltage measurement. Some of the results from these tests are presented in this paper. After fabrication, significant numbers of capacitors will be subjected to reliability testing. Reliability tests include thermal cycling, thermal shock, and temperature/humidity/bias testing. Samples will be attached to printed wiring board coupons either face up or face down, with either solder or conductive epoxy used to make connections to the devices. This program was begun in the Fall of 2003 and will continue through mid-2004.

Results

A plot of the impedance analyzer data for a 1 cm^2 capacitor is shown in Figure 6. The RLC equivalent circuit model for this device is 110 nF, 16 pH, and 27mΩ. A few of the results are tabulated below. The resistance was high because the process sequence had not yet been optimized. Un-anodized Tantalum which becomes a part of the bottom plate stack up might be a cause of the high resistance. The inductance is much larger than the simulated inductance of a multiply connected or line-connected device because the microwave probe is a point contact that causes current crowding and thus an increase in the measured inductance. The combined simulation and measurement program described above will confirm the effectiveness of these devices in actual in-circuit configurations.

Table 1 - Results

	Area (cm^2)	Capacitance (nF)	ESL (pH)	ESR (mΩ)
1	1	110	16	27
2	0.5	26	32	30

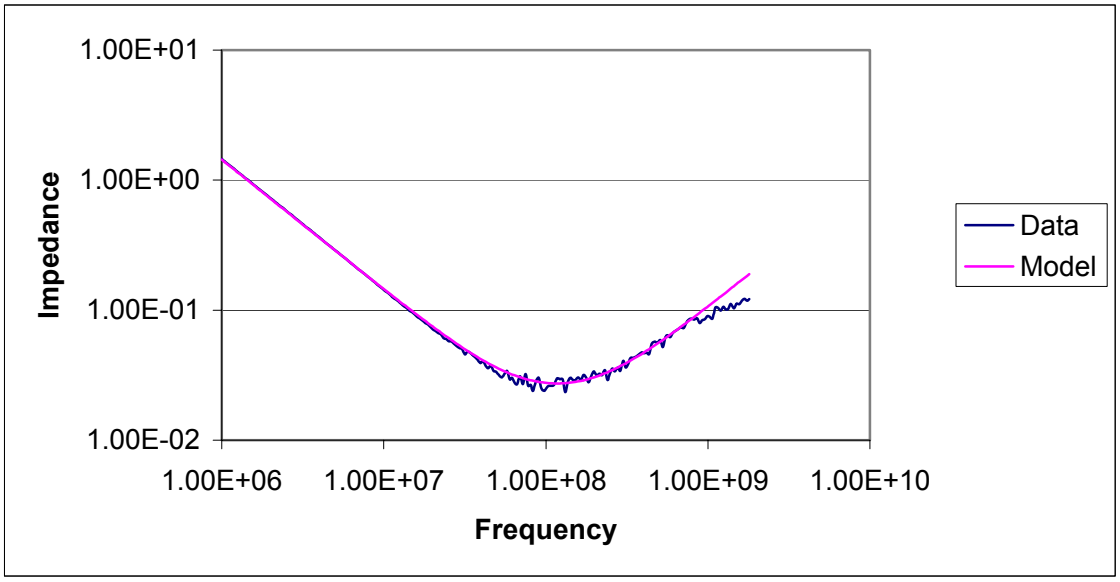

Figure 6 - Plot of Impedance Analyzer Data

Conclusion

Tantalum oxide embedded capacitors exhibit low parasitic inductance and resistance compared with discrete passives. Line contacts are better than point contacts due to the lower effective resistance and inductance of the former type. These capacitors were measured on the HP Impedance Analyzer with a 500 μm pitch probe. The measured inductance is caused by the probing method and the spacing of the pads; hence measurement is not an accurate method of determining these very low inductances. However, if they are too low to measure, they may be too low to matter.

References

1. R. Ulrich, L. Schaper, “Decoupling with Surface Mount Capacitors”, CircuiTree, June 2003, Vol 16, no. 6, p. 22.
2. L Smith, "Decoupling Capacitor Calculations for CMOS Circuits," Electrical Performance of Electronic Packaging Conference, IEEE, Nov, 1994.
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5. K. Chen, W. D. Brown, L. Schaper, S. S. Ang, and H. Naseem, "A Study of the High Frequency Performance of Thin Film Capacitors for Electronic Packaging," IEEE Transactions on Advanced Packaging, pp. 293-302, 2000.
6. R. Ulrich and L. Schaper (eds), “Integrated Passive Component Technology”, ISBN: 0471244317, IEEE Press/Wiley, June 2003.
7. R. Ulrich, L. Schaper, D. Nelms, and M. Leftwich, " Comparison of Paraelectric and Ferroelectric Materials for Applications as Dielectrics in Thin Film Integrated Capacitors," International Journal of Microcircuits and Electronic Packaging, p. 172-181, 2000.
8. I. Novak, “Lossy Power Distribution Networks with Thin Dielectric Layers and/or Thin Conductive Layers,” IEEE Transactions on Advanced Packaging, Volume: 23 Issue: 3, Page(s): 353, Aug. 2000.

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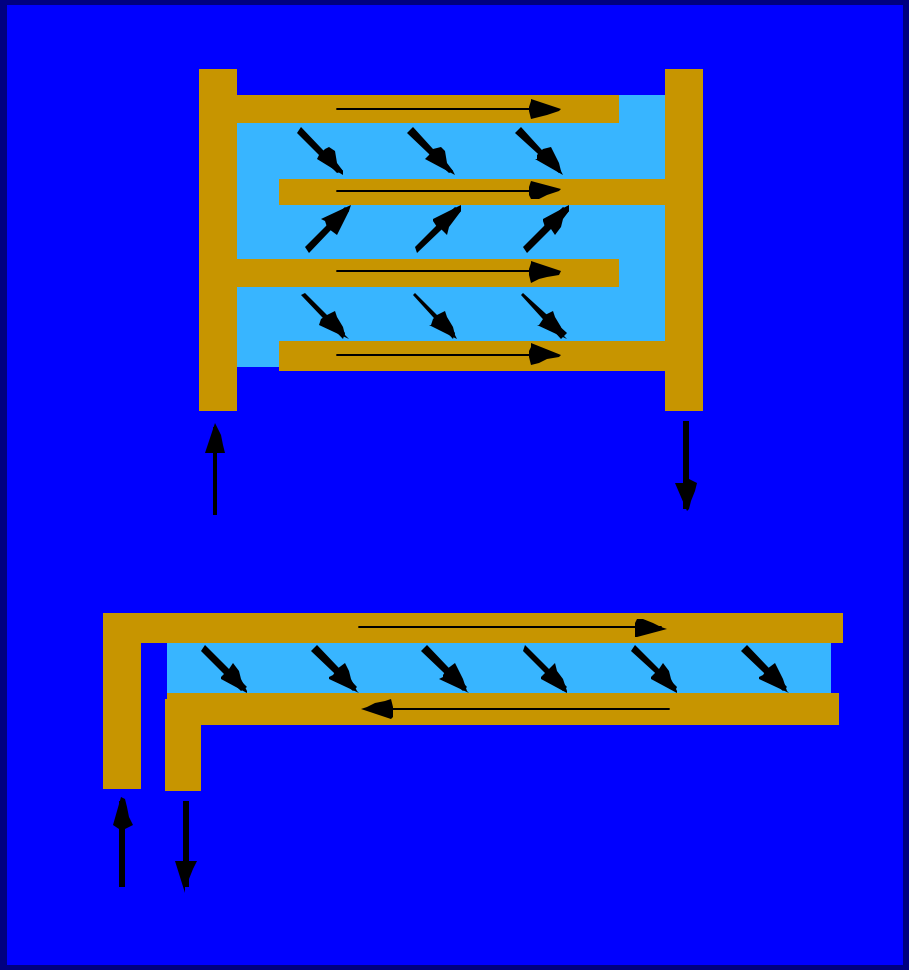

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What We're Going to Cover

What aspects are important in decoupling?

What's available for decoupling?

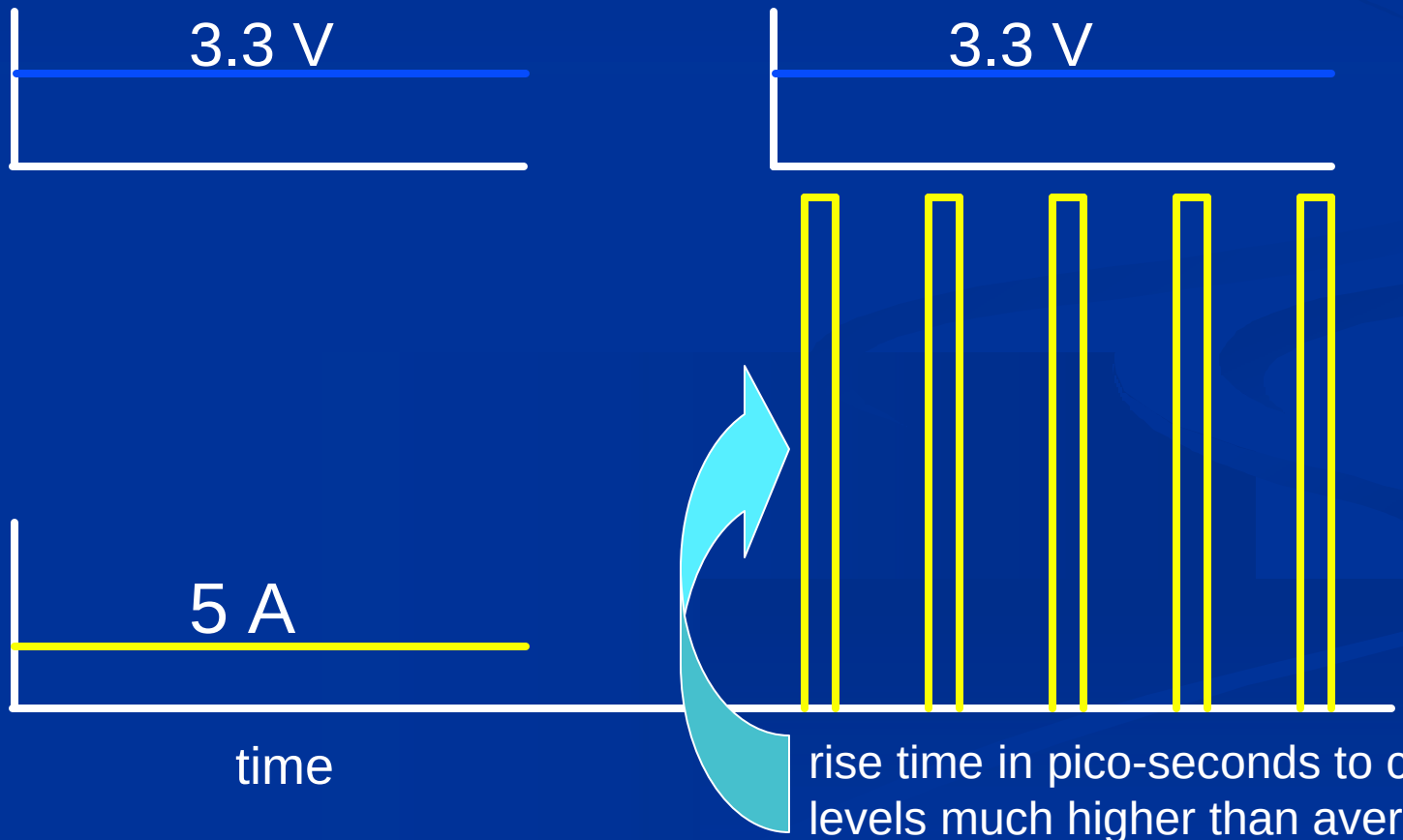
What matters more: k or thickness?

Why use and how to use anodized Ta?

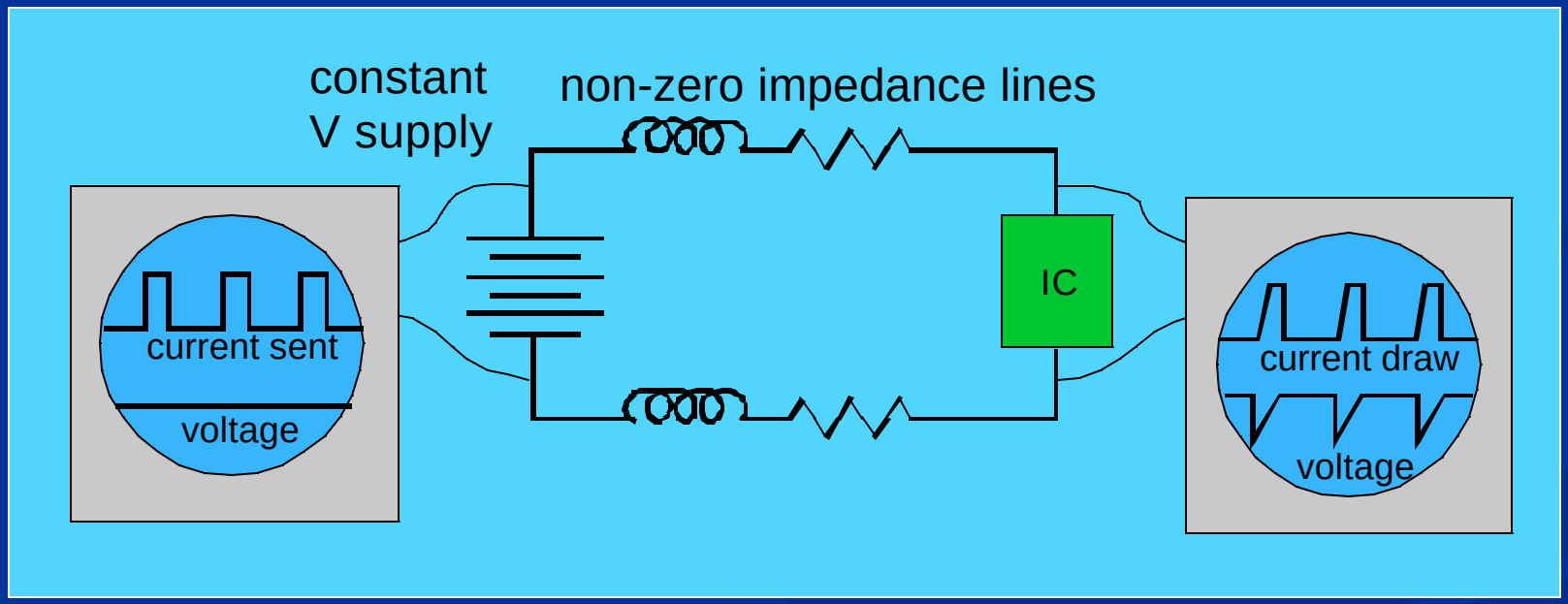
A Quick Review of Decoupling

What the power supply wants to put out

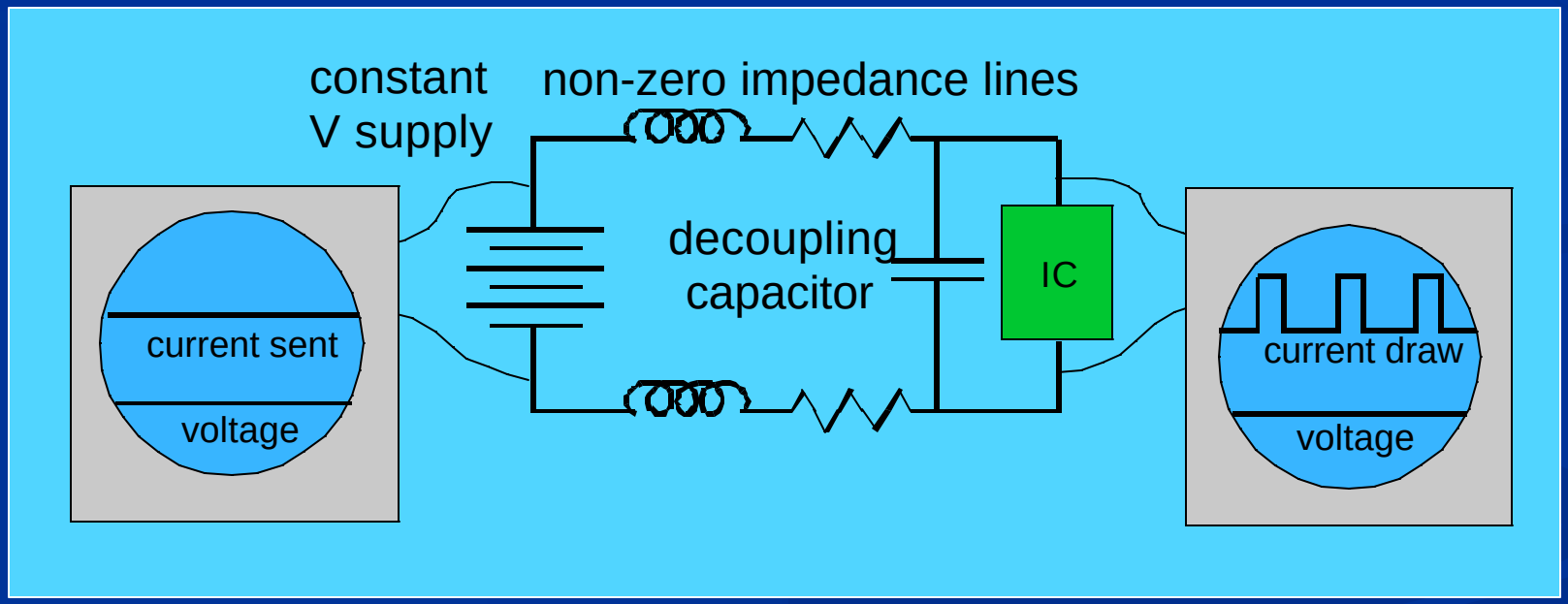
What the IC has to have

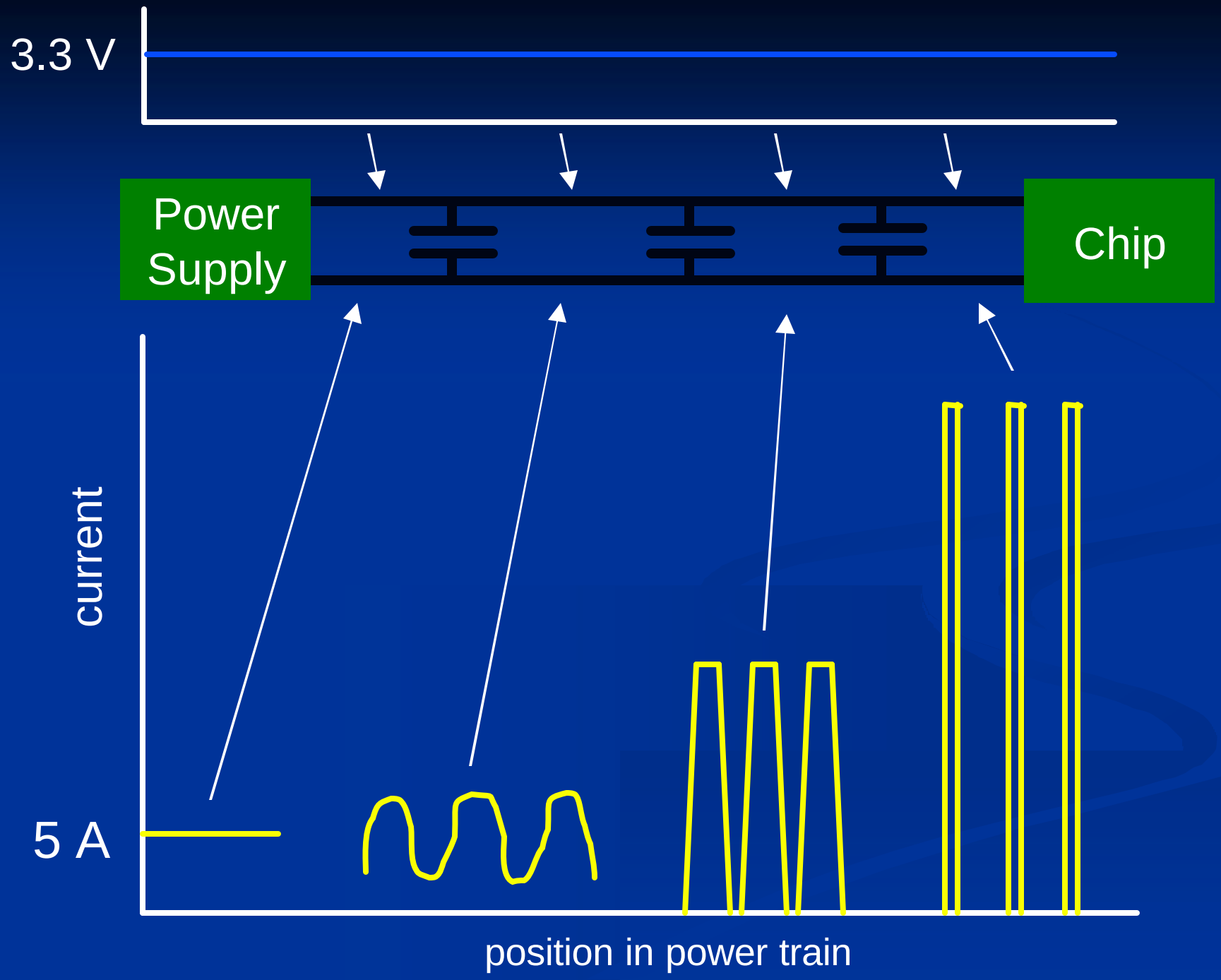


In between them, the power train has resistance and inductance, leading to distortions of both the desired current and voltage.

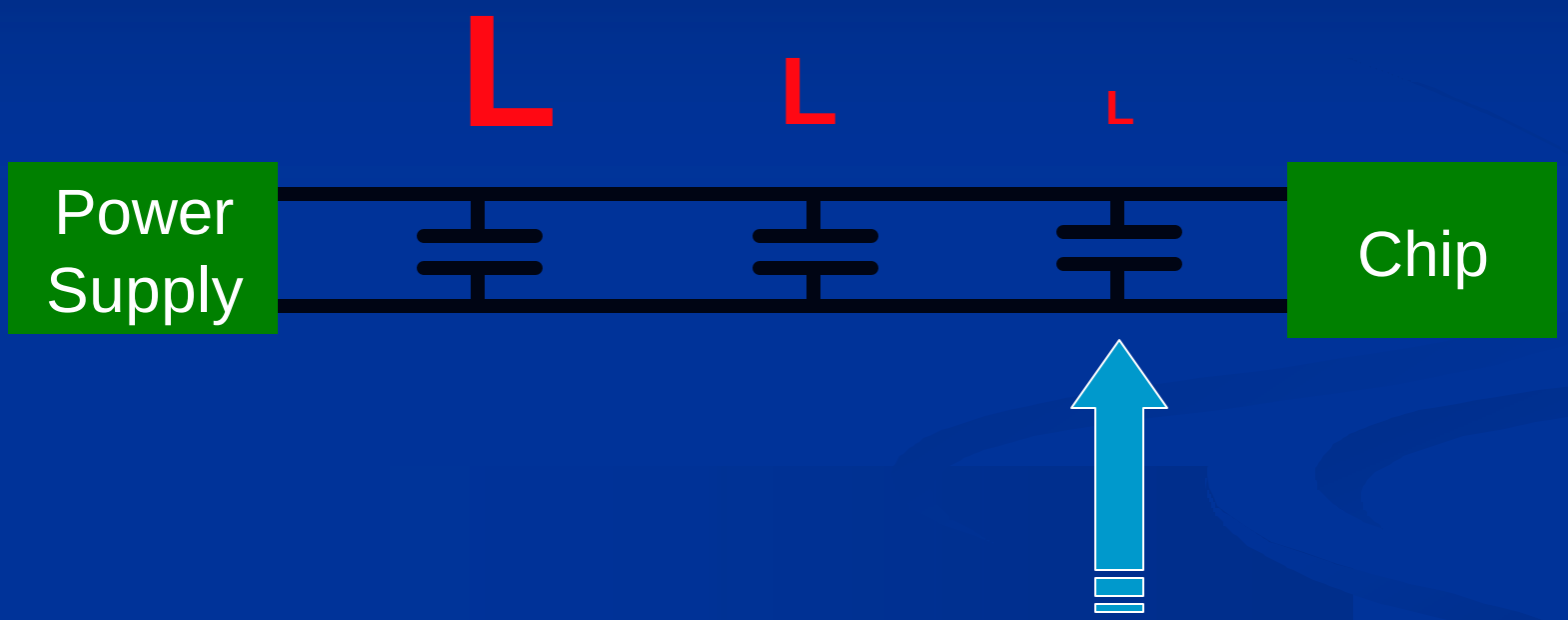


Putting decoupling caps in the power train enables the chip to have the current and voltage forms it needs while, simultaneously, relaxing the requirement for the power supply.




3.3 V
Power Supply
Chip
current
5 A
position in power train

lower parasitic inductance is required in the decoupling caps as you get closer to the chip

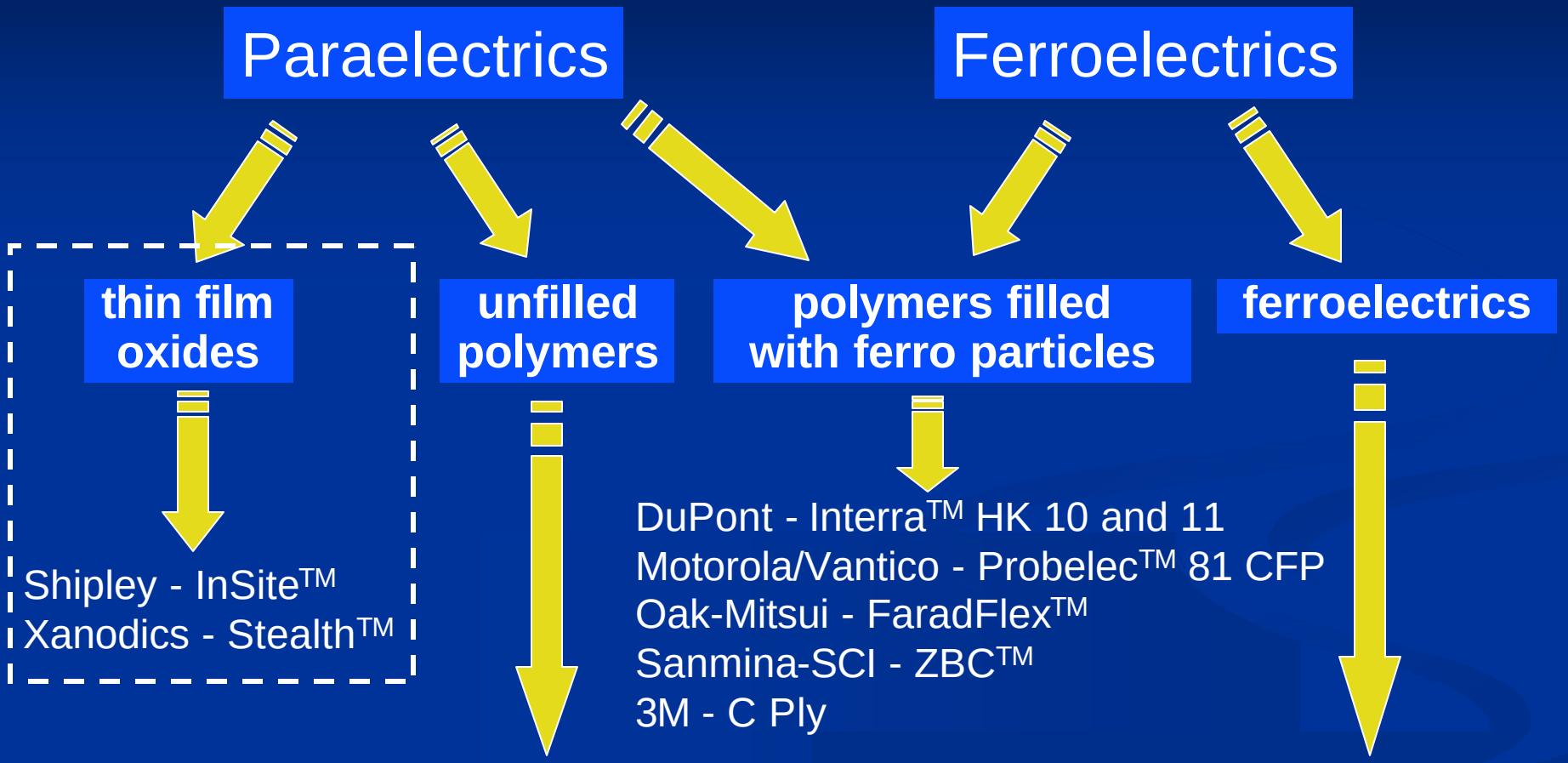


What Does a Capacitor Need In Order To Decouple Well?

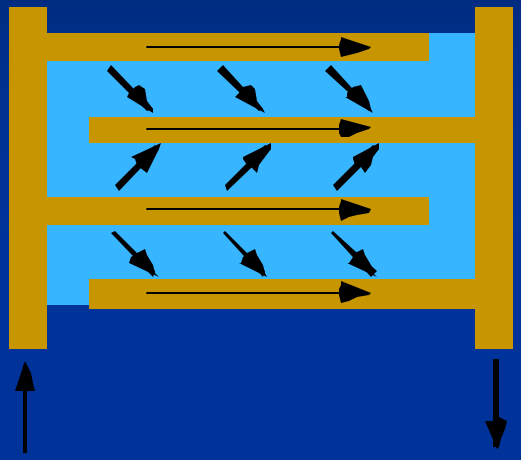
At least enough capacitance to run the chip for one clock cycle

Low inductance (and resistance) so the charge can be delivered fast enough

The Family Tree of Embeddable Dielectrics

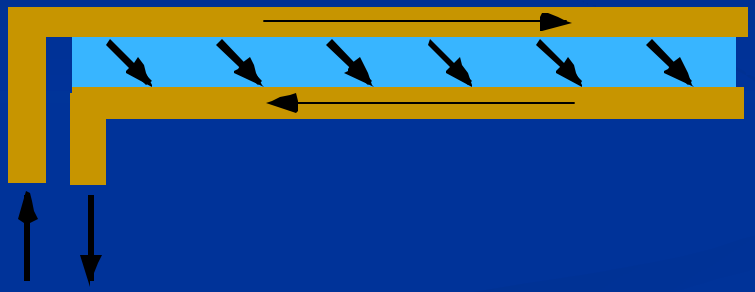


Field Cancellation in Integrated Caps



Surface Mount

Currents in same direction, fields add



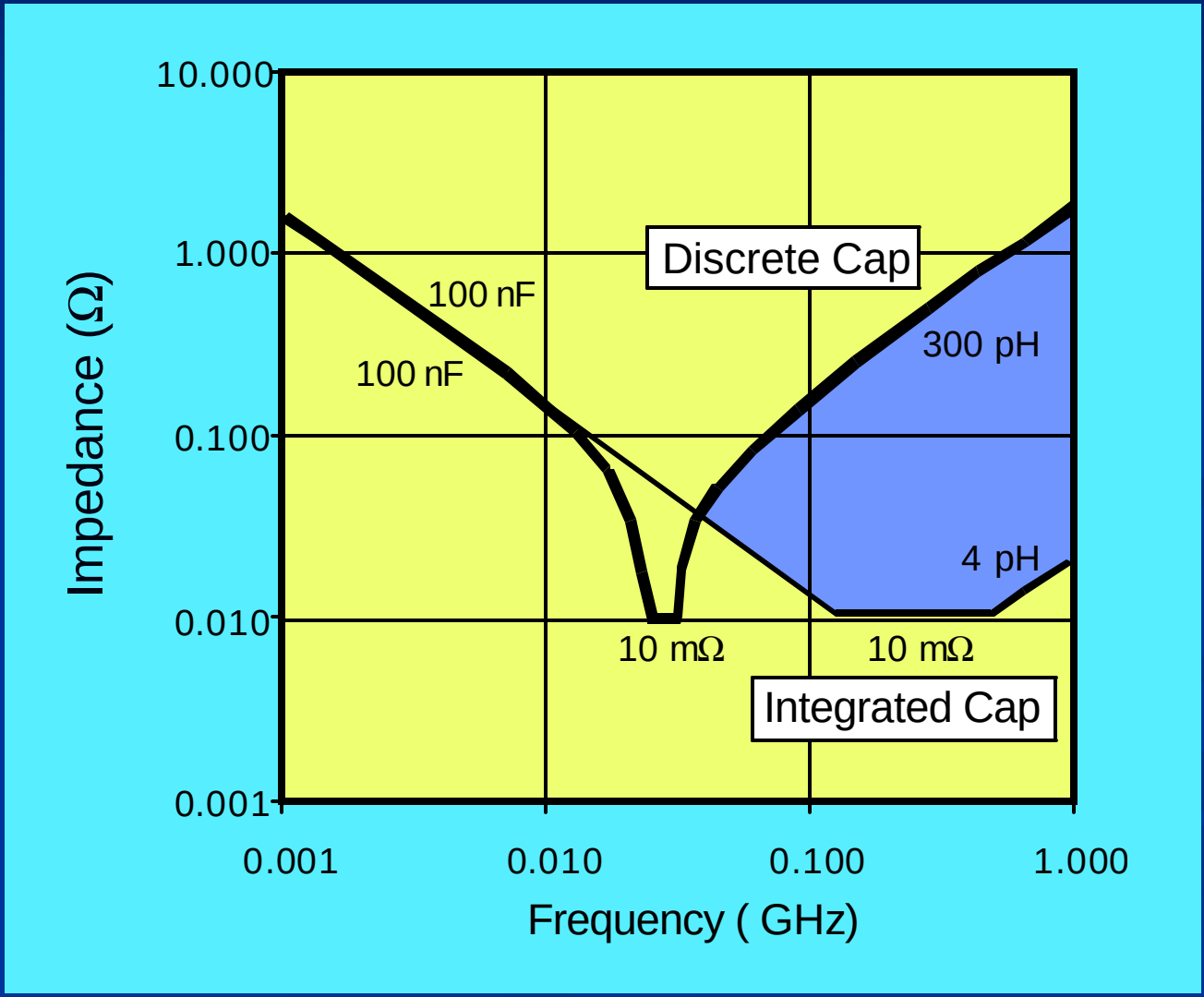
Embedded

Currents in opposite directions, fields cancel

parasitic L of planar, integrated caps w/parallel current:

L in pH/square = 1.26 (dielectric thickness in μm)

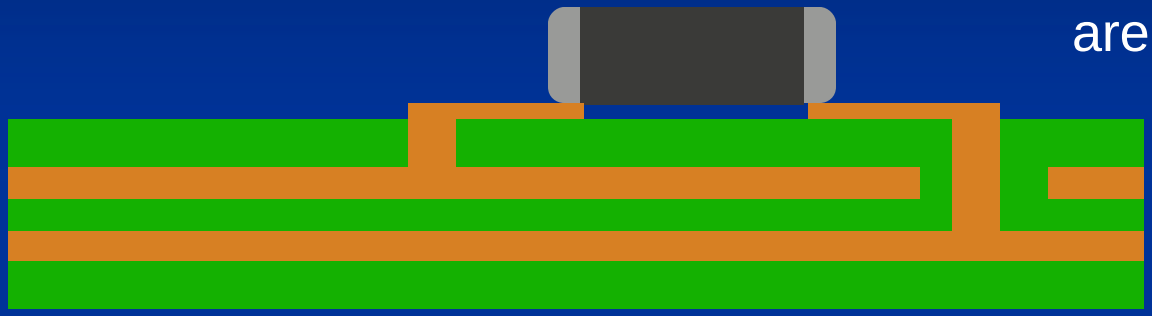
Parasitic Inductance in Integrated and Discrete Capacitors



Elimination of Inductive Connections

Surface Mount Cap Decoupling

Vias and Traces
are Inductive



Integrated Cap Decoupling

Integrated
Dielectric

How Much Inductance Is Where?

Just for comparison:

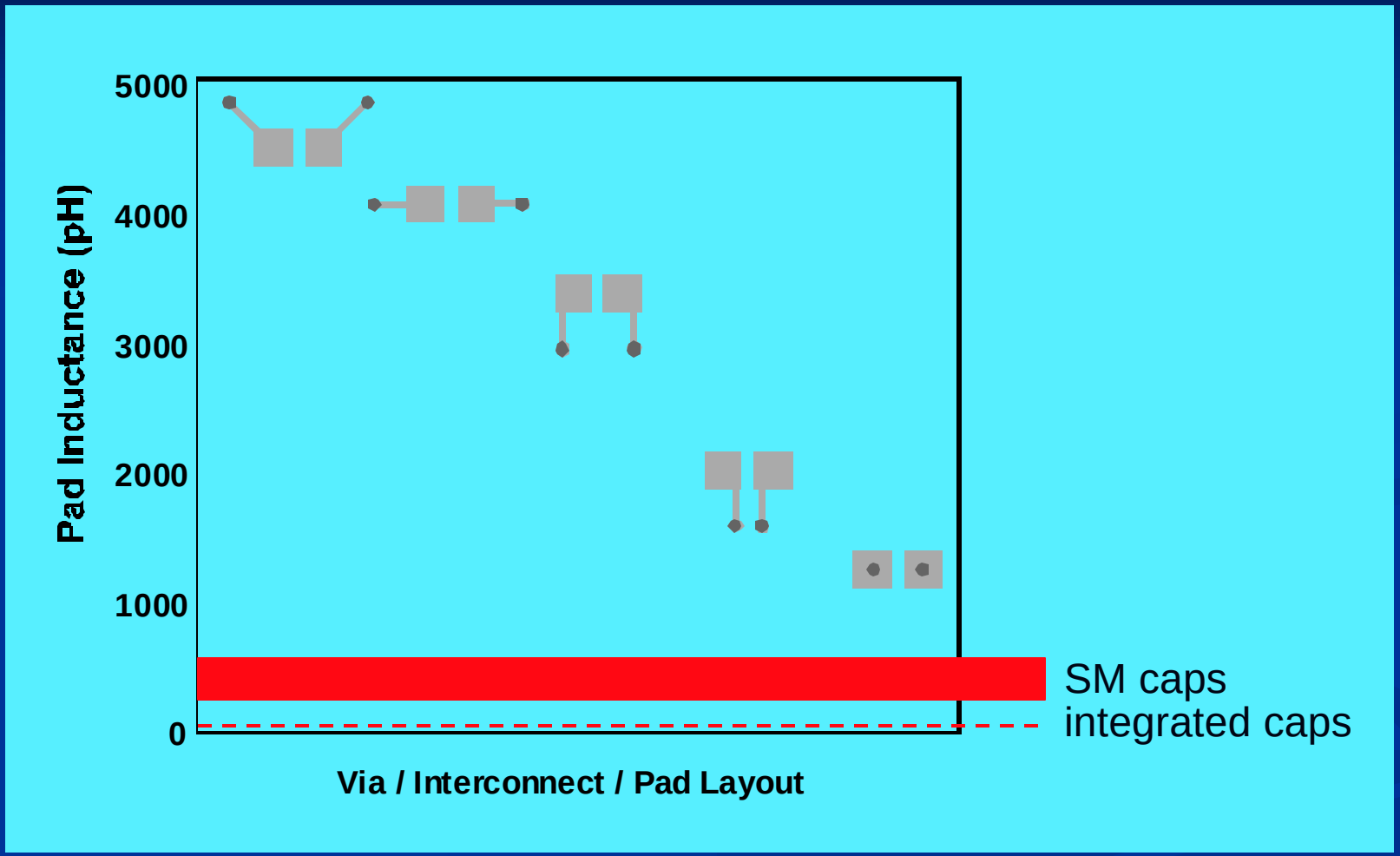
- 1 mm of 10 mil, 1/2 oz. Cu conductor: ~700 pH
- 1 mm dia circle of 10 mil conductor: ~3000 pH
- bond wire: 1000 - 5000 pH

10 mil diameter via, 30 mils long: ~300 pH
Solder bumps: ~10 - 100 pH
Pad/Trace/Via: 1000 - 5000 pH

SM Discrete Caps (not counting connects): 10's - 100's pH
Integrated parallel plate: <10 pH

Below some level of parasitic L, the cap doesn't matter anymore and the limiting factor becomes vias, pads and chip interconnect.

Inductance of Pad/Trace/Via Combinations



T. Roy, L. Smith "ESR and ESL of Ceramic Capacitor Applied to Decoupling Applications", IEEE Topical Meeting on Electrical Performance of Electrical Packaging, West Point, p. 213, Oct. 1998.

So there are two reasons that integrated capacitors have less parasitic inductance than surface mount:

1. **Opposed current directions provide field cancellation**

2. **Integrated caps can be placed in between the power and ground plane in the board, eliminating inductive vias and traces**

How Much Capacitance Do You Need?

Using surface mount discretes, there is usually much more than necessary because of the large number of caps placed in parallel to reduce parasitic inductance.

Since integrated capacitance is much lower in parasitic L, considerably less C is probably required.

How much less is very application-specific; it's very hard to generalize the answer to this.

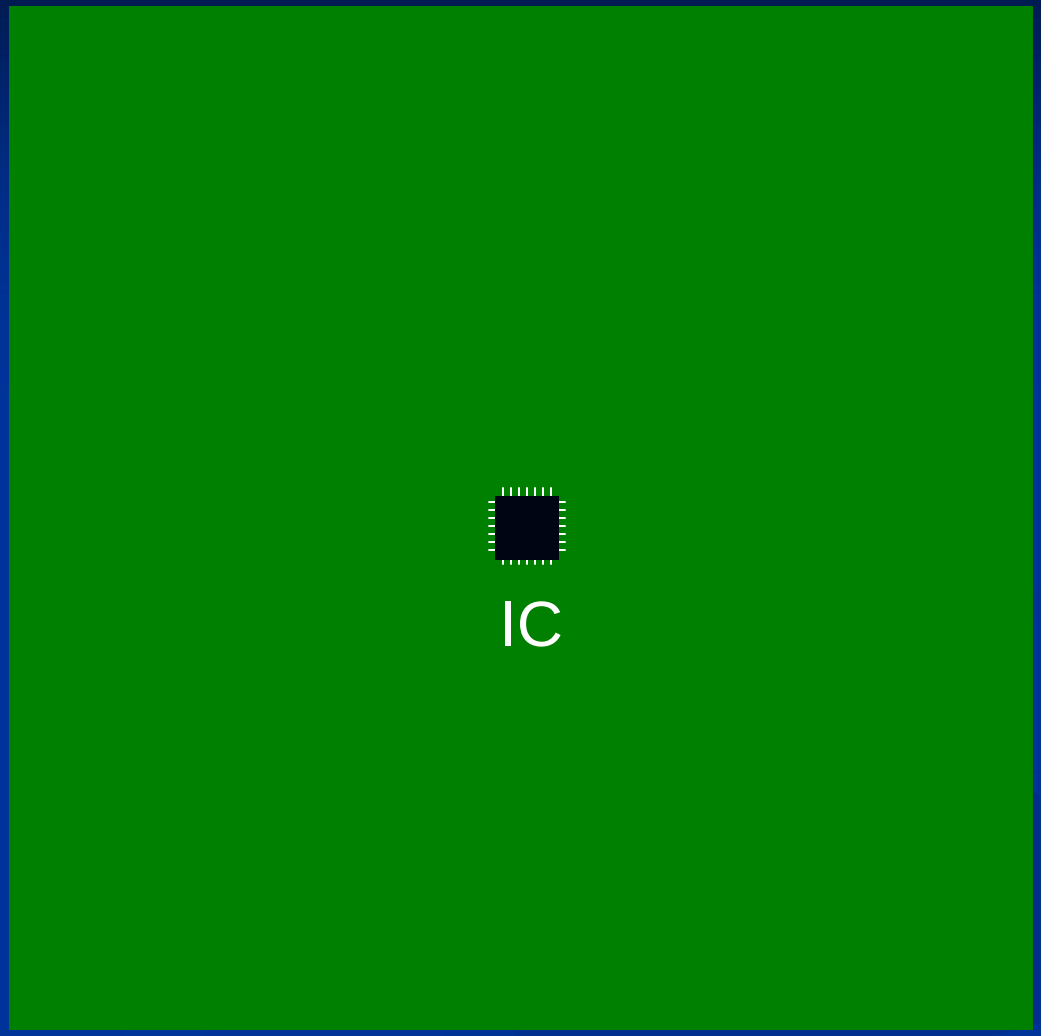
Decoupling Area

Imagine this scenario:

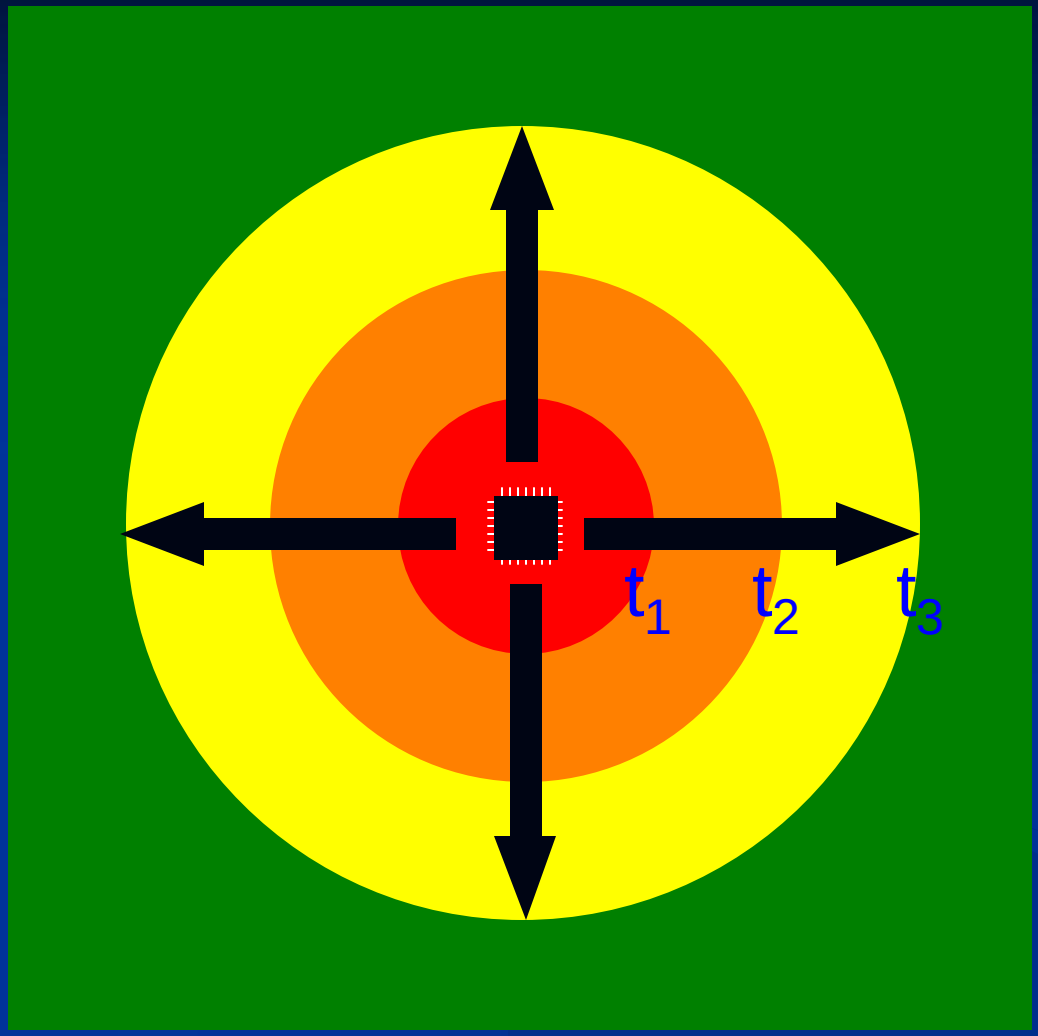
Large-area planar decoupling cap between two board layers, charged to 5 V

Chip in the center of the board

Starting at t = 0, it draws power from this extended cap



circuit board with embedded decoupling layer



end of clock cycle,
this is the “decoupling area”

How Much Charge Can The Chip Get?

The rate that the wave of discharging moves radially away from the vias is:

$$\text{velocity} = \frac{c}{\sqrt{k}}$$

in time t, the distance this travels radially away from the vias is:

$$\text{distance} = \frac{c}{\sqrt{k}}\, t$$

So, the area of capacitor discharged is:

$$\text{discharged area} = \pi(\text{distance})^2 = \pi \frac{c^2 t^2}{k}$$

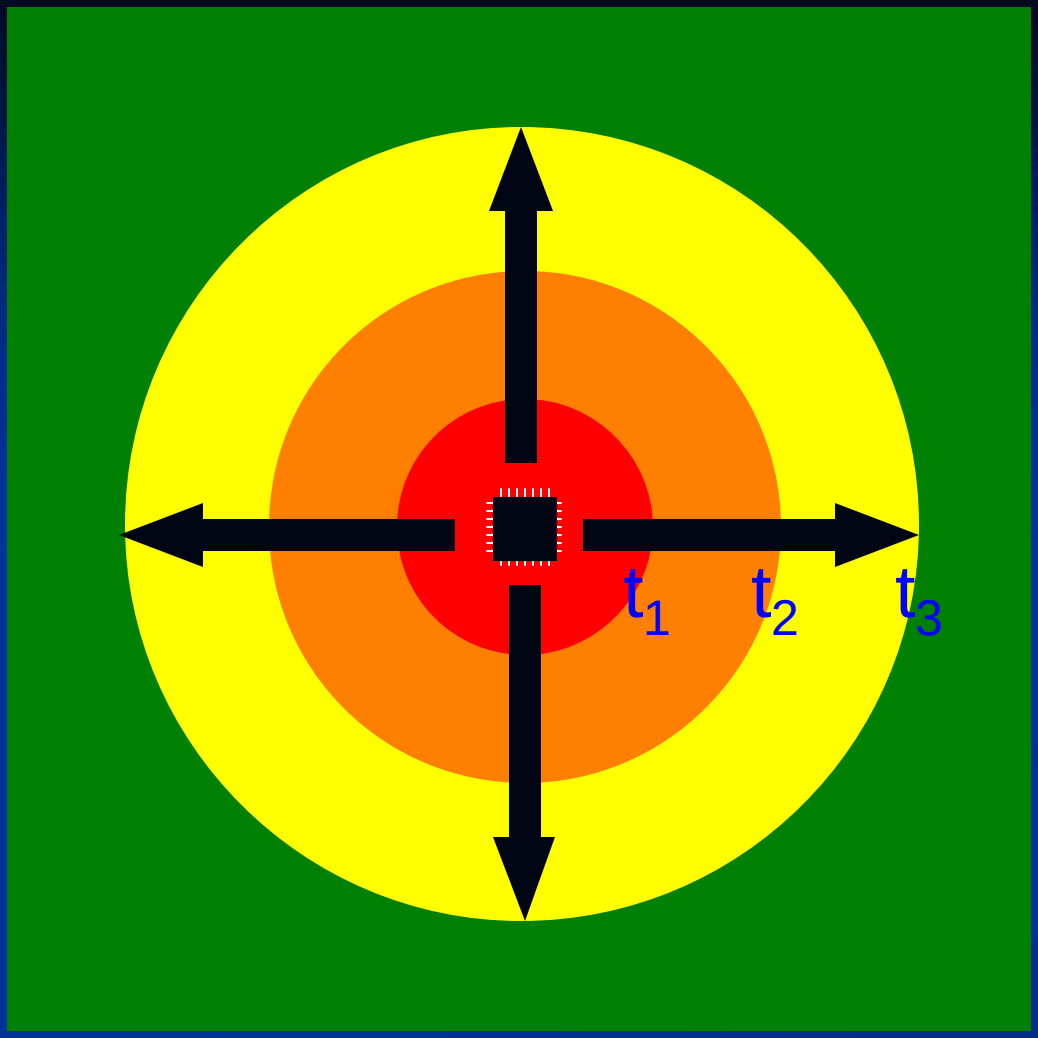
The capacitance in this area is:

$$\text{capacitance} = (\text{Area})\left(\varepsilon_o \frac{k}{h}\right) = \left(\pi \frac{c^2 t^2}{k}\right)\left(\varepsilon_o \frac{k}{h}\right)$$

$$= \pi \varepsilon_o \frac{c^2 t^2}{h}$$

no k left!

So k drops out of the eqn for the amount of charge that, in this idealized situation, can be drawn out of a power/ground plane in time t.



Higher k - slower propagation but more C/A

Lower k - faster propagation but less C/A

Do they really exactly offset???!!!

Let's Put In Some Numbers from Common Embeddable Dielectrics

	k	h (μm)	Distance in 1 ns (cm)	Area in 1 ns (cm^2)	Specific Capacitance (nF/cm^2)	Capacitance in This Area (nF)
FR4	4.6	50	14	616	0.0814	50
C-Ply	20	8	6.7	141	2.20	310
Ta_2O_5	23	0.2	6.3	125	101	12,600

Even if k doesn't matter to how much charge is available, the decoupling distance may run into other chips if you use low k materials

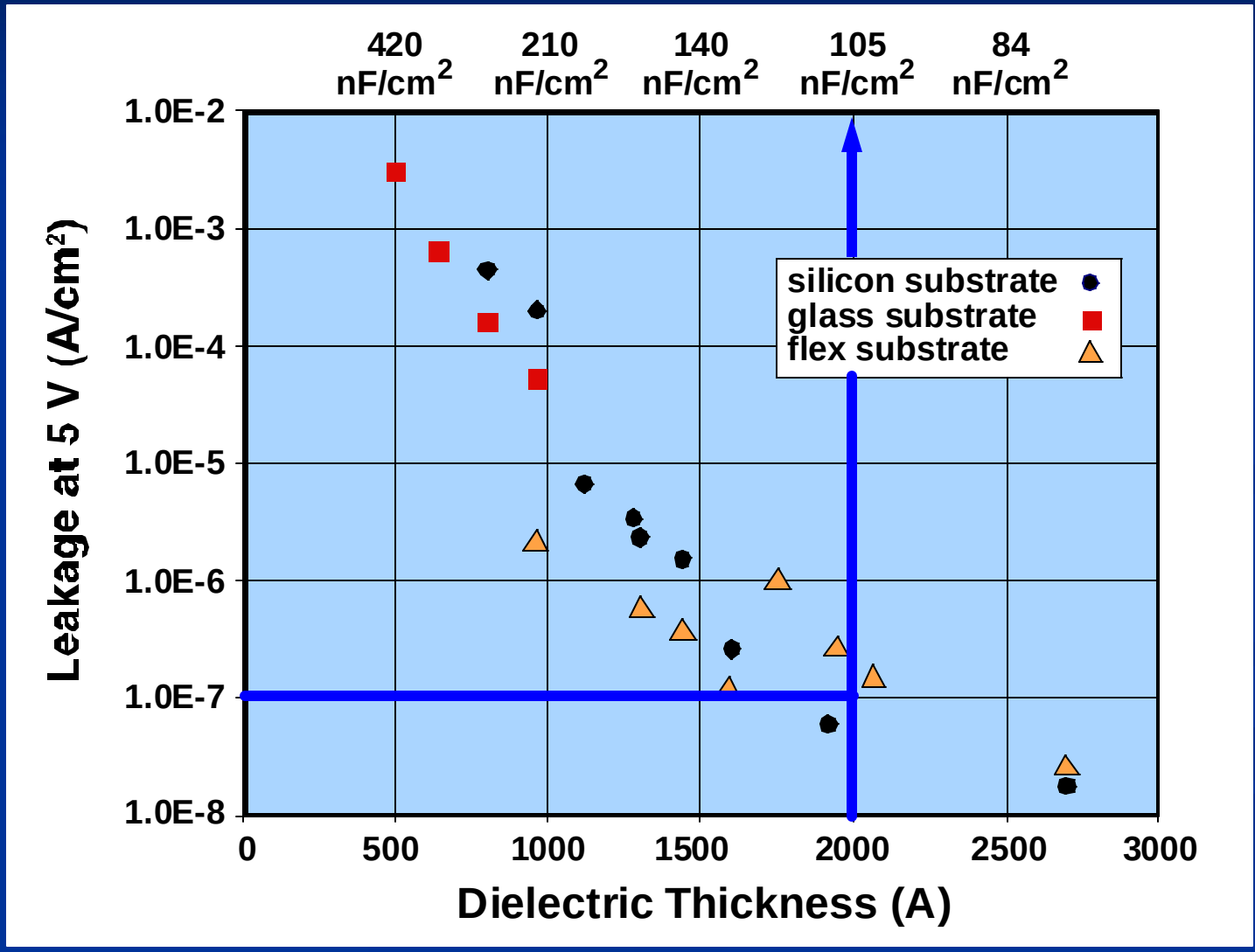
So After All That, Why Use Anodized Ta?

Very thin, so low parasitic inductance
< 5 pH for 1 cm^2

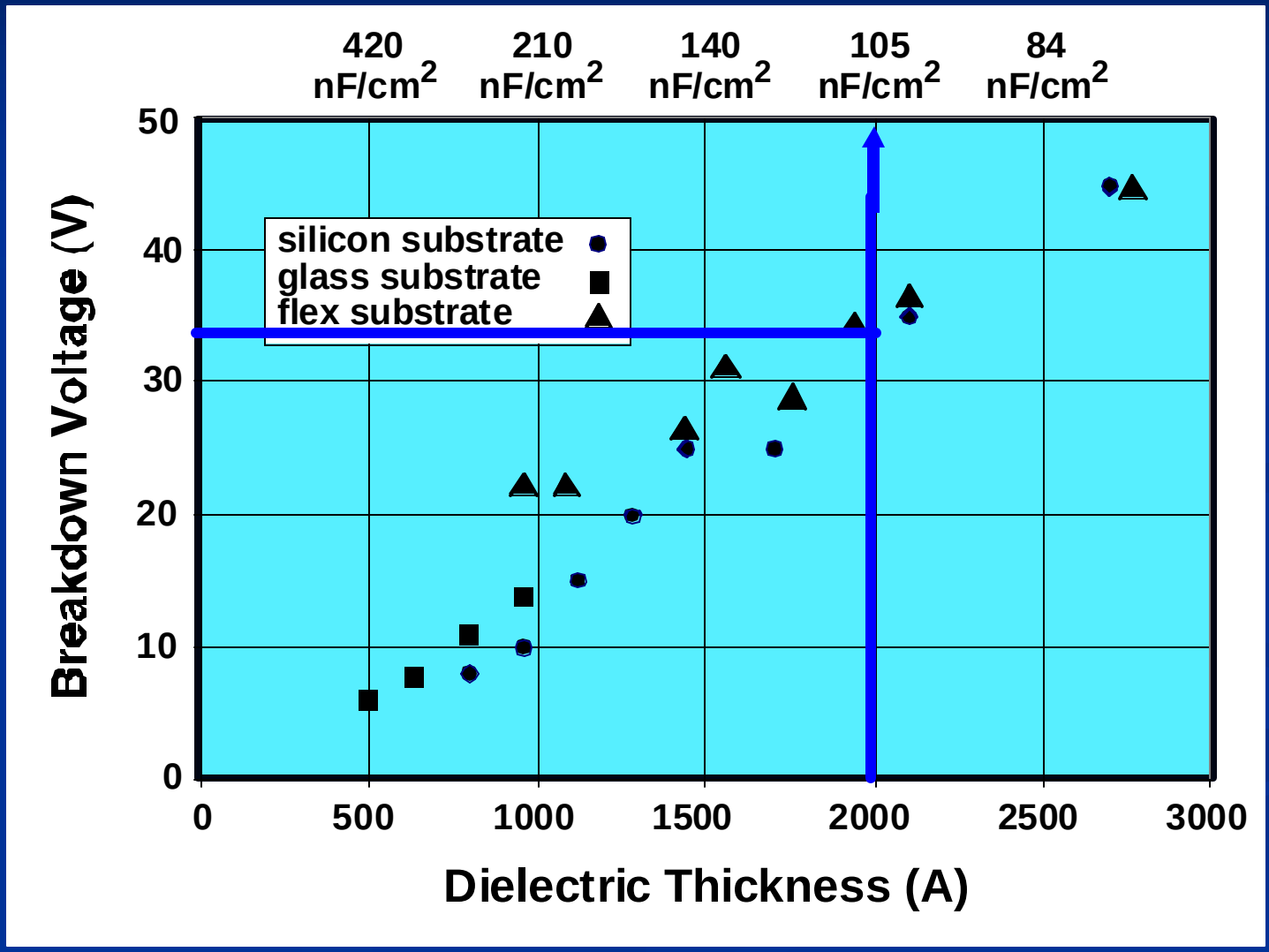
High k and thin so shorter decoupling distance

Proven technology in surface mount

Leakage Through Anodized Ta_2O_5 at 5 V
$<10^{-6}$ A/cm^2 at 5 V is an Often-Cited Specification



Breakdown Voltage of Ta_2O_5
Lower IC Operating Voltages Are In Everyone's Favor



Anodized Ta Embodied as a Decoupling Part

1 cm

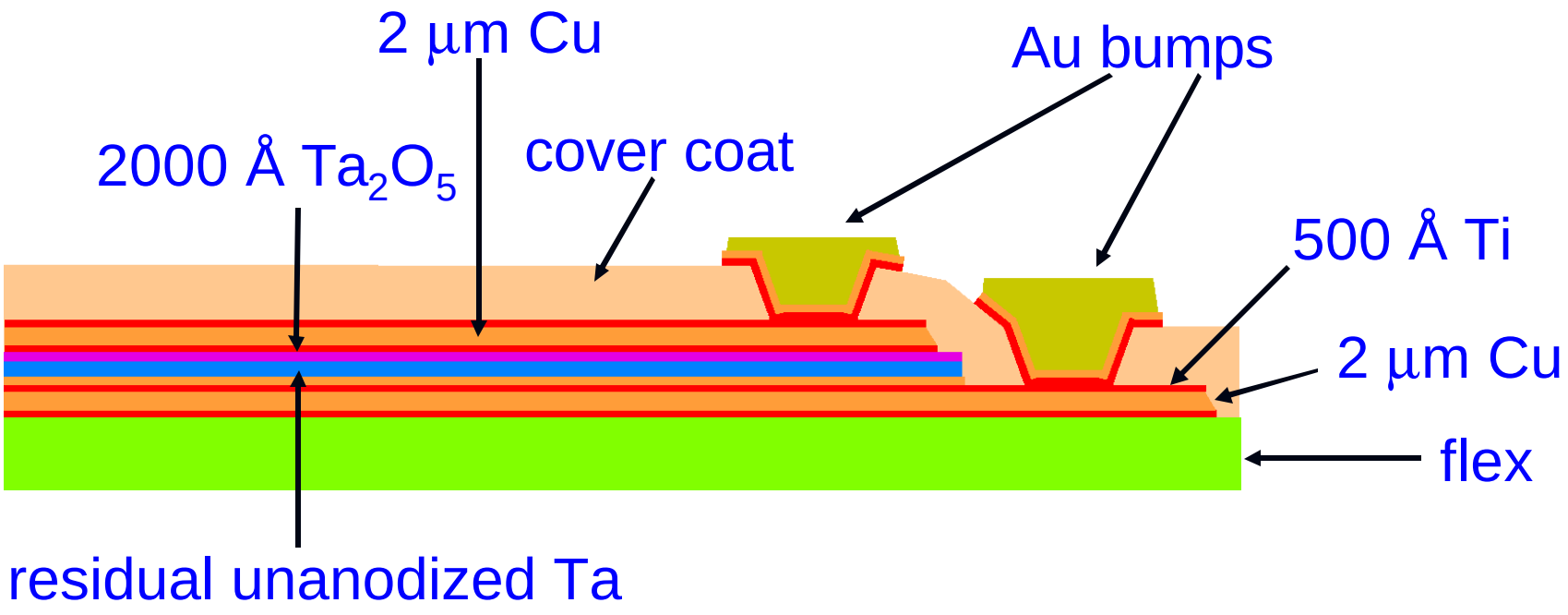
2000 Å TaO

110 nF

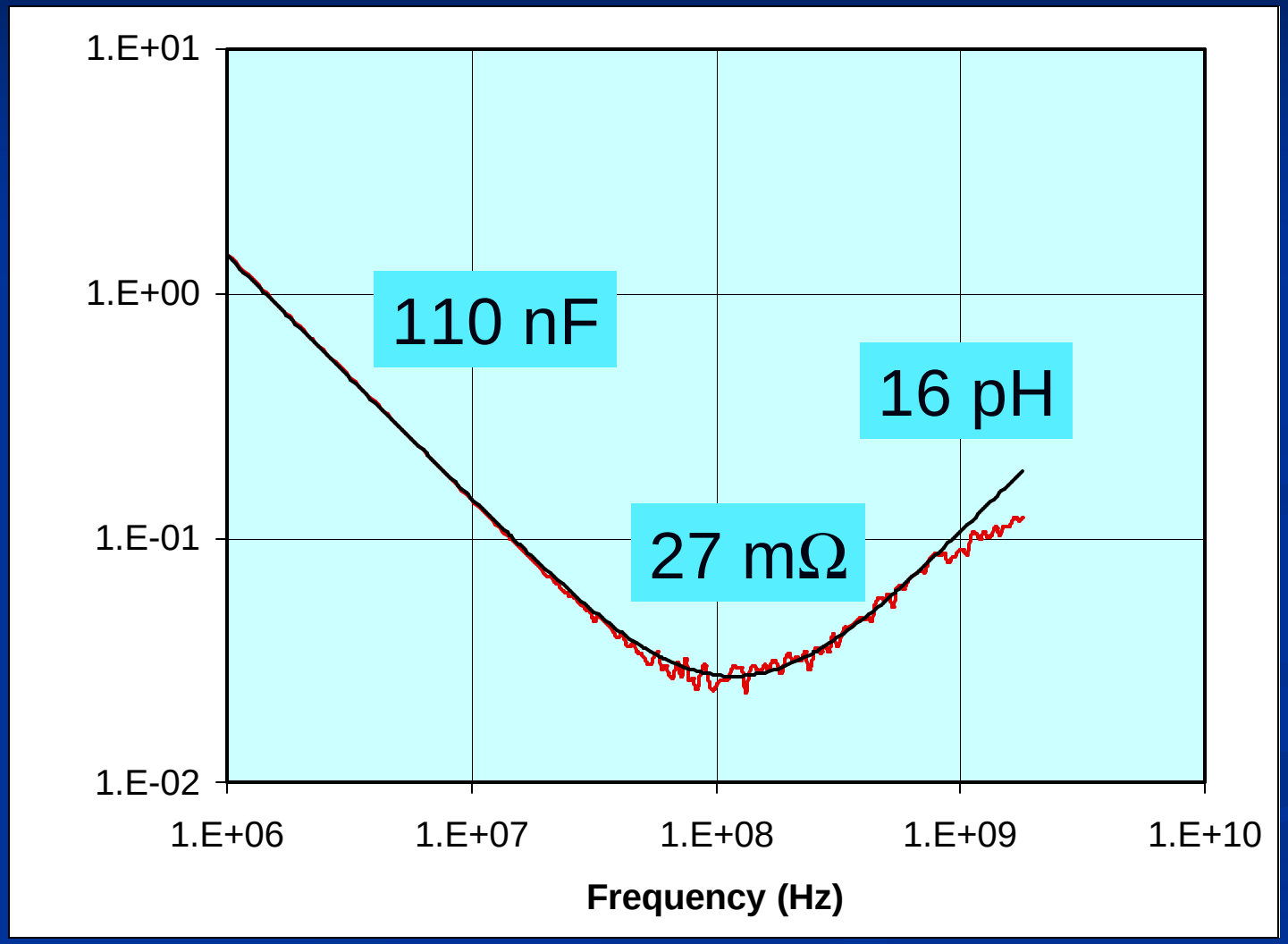
Multiple Alternating Contacts for Lowered Inductance

Mountable in a BGA

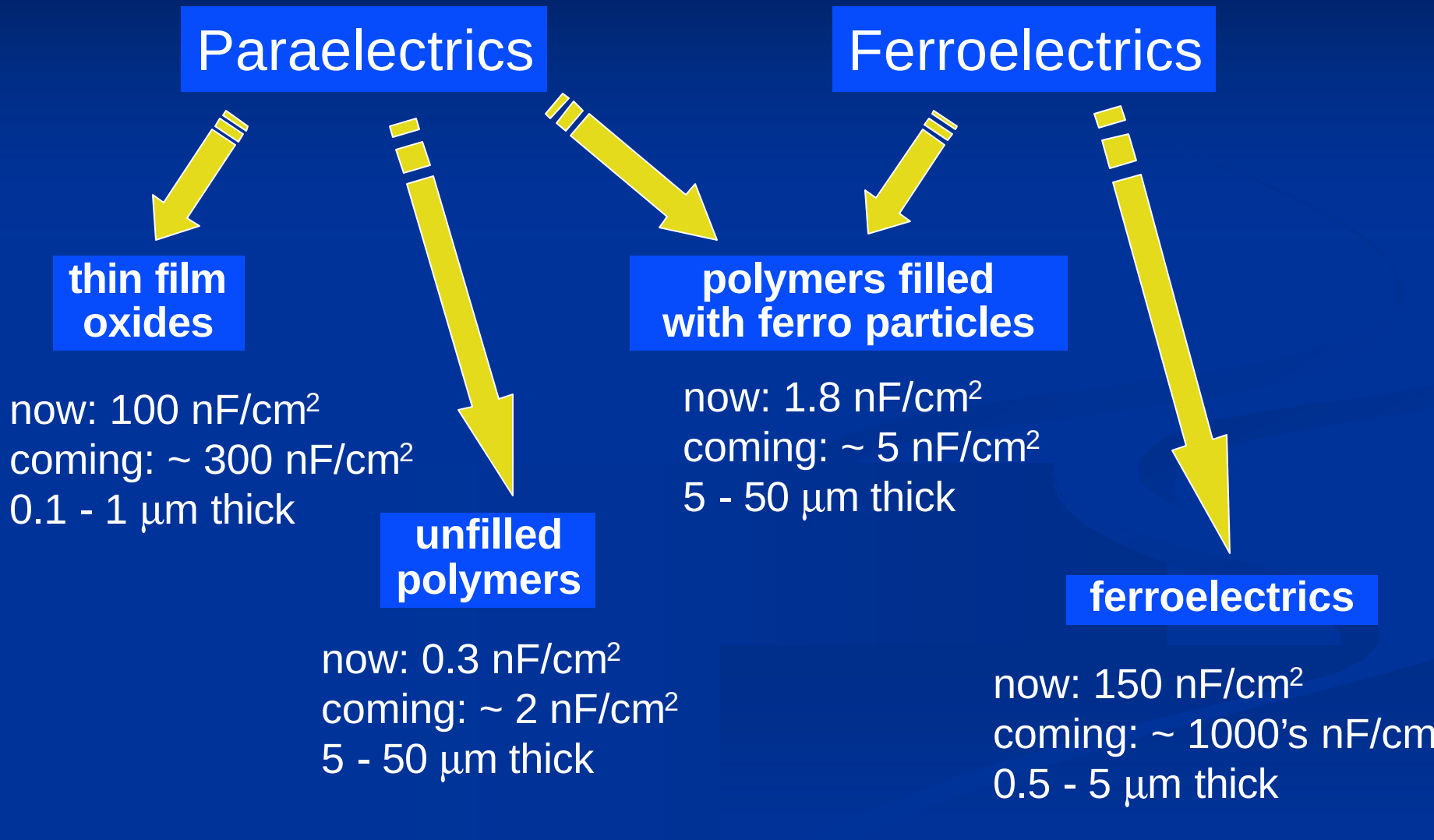
Structure is Buildup on Flex



Electrical Performance



Electrical Properties of Embeddable Dielectrics



Conclusions: Decoupling with Anodized Ta

There are two knobs to turn with caps: k and thickness

- importance of k is being debated, but it's fairly high with TaO
- very thin dielectric is beneficial to decreasing parasitic inductance

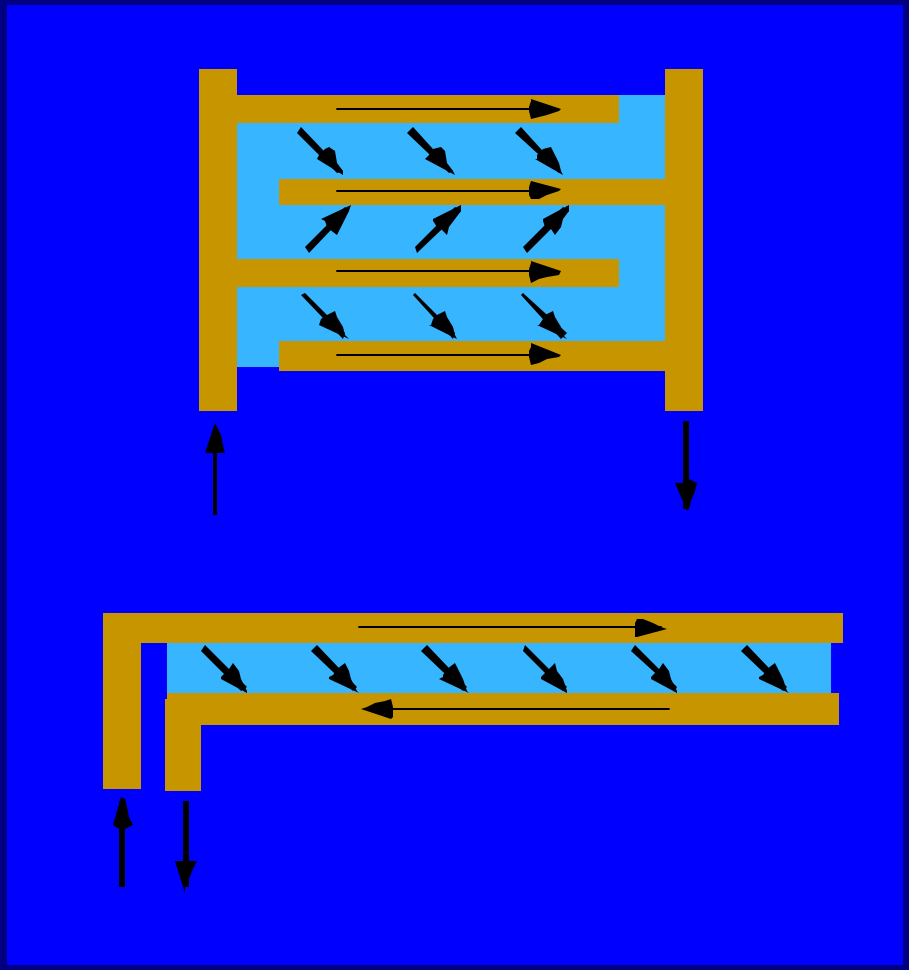
Optimal Ta_2O_5 thickness is around 2000 Å

- 110 nF/cm^2
- leakage < 1 μA/cm^2 @ 5V
- breakdown > 30 V
- < 1 pH/square

Example structure fabricated on flex

- multiple, alternating contacts for lowered inductance

Decoupling with Anodized Ta



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