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Designers Summit 04

Performance of Polymeric Ultra-thin Substrates for Use as Embedded Capacitors: Comparison of Unfilled and Filled Systems with Ferroelectric Particles

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We have previously published our work on developing thin substrates for use as embedded capacitor layers. Based on this work we have continued to characterize the performance and reliability of these materials.

We will discuss the experiences of PCB shops in processing the material and review the results of the various reliability studies. Also, additional test vehicles have been processed for testing at high frequencies.

Customers have requested even higher capacitance values. We continue to work on making thinner dielectrics, and thus raise capacitance, but it is believed that loading the polymer with high dielectric (Ferroelectric) particles will provide the best values for this type of capacitor. We will exam the effect of loading the polymer with High Dk particles and compare the positive and negative aspects of using filler.

The results of our internal and external testing (and a comparison to existing and developing capacitor materials) will help determine what benefit(s), if any, a high speed system would get by using a high Dk filler polymer substrate.

Introduction

The use of thin dielectric substrates to provide Embedded Capacitance has been driven by the need to improve electrical performance of Printed Circuit Boards. Current standard capacitive material used in the industry is mainly the 2mil dielectric thick material, mostly utilized for telecom and networking applications[1)]. For this particular high-end application of PCBs, embedded capacitor technology has been utilized to reduce the inductance between the chip and the power supply. This improves the electrical performance of the distributed capacitance, enhances signal integrity, and reduces impedance at high frequencies while dampening noise.

A number of papers have been published regarding development of materials for embedded capacitors and advantages of incorporating embedded capacitor in PWB. From the electrical performance standpoint, demand is increasing for thinner capacitor material, as low as 10 micron, as the signal frequency increases.[2]

The addition of high dielectric constant Ferroelectric particles, in order to increase capacitance density, will be investigated. Also, the fabrication of the thin film capacitor material (with and without particles) incorporating into PCBs and their electrical performance are described. A comparison of the electrical performance of the unfilled and filled systems will be made.

Investigations

Embedded capacitance materials are constructed from two metal layers (usually copper foils) and dielectric polymer film layer in between. In order to design the construction of the capacitance material, properties of the copper foil and dielectric layer will be the “keys” to determining the performance of the capacitance materials.

Investigation of the influences of copper foil, dielectric type and dielectric thickness has been conducted to design the construction of the thin capacitance material.

Copper Foil

As previously described[3] different types of copper foils were investigated for their influence on the performance of the capacitance material. What we wanted from the foil was not only good performance from the normal characteristics (peel strength, HTE, etc.) but also good capacitance value and insulation resistance. We repeated our procedure for the filled material.

Copper Selection Process
We examined two electro-deposited (ED) and one wrought (rolled) foil based on our previous work. Peel strength, capacitance of the substrate and High Potential (Hi-Pot) Voltage Testing (at 100 Volts DC) were compared. As mentioned in our previous paper[3] it was found that the higher the profile of the copper foil, the higher the peel strength as well as the capacitance values. Unfortunately, increasing the profile also reduced the yield at Hi-Pot testing.

Copper Foil Decision
When the balance of properties was examined, it was determined that for the filled capacitor material our special very low profile (VLP) foil was required.

Dielectric Resin /Ferroelectric Particles
One of the challenges for thin capacitive material is the physical property of the dielectric. The thin dielectric must be tough and flexible in order to withstand processing through PCB manufacturing process. Another challenge for thin dielectric is the insulation reliability, such as hi-pot test and electro-migration. Additionally, if any particles are to be introduced into the dielectric, it must be evenly dispersed.

Dielectric Selection Process
As indicated previously[3] we developed a proprietary, modified resin system, specifically designed for being a capacitive material. We decided to use this resin for filling with high Dk particles.

Addition of Ferroelectric Particles
In order to increase the capacitance density of the material we experimented with adding high Dk filler to the resin. We chose Barium Titinate ($BaTiO_3$) as the High Dk material. This material is a well know and available Ferroelectric material that can have Dk's over 2,000 after sintering.

In order to disperse the particles (average particle size of less than 1 micron) several agents and mixing methods were tried. Through experimentation a suitable dispersing agent and mix method was obtained. We were able to get over 60% (by weight) loading of particles.

Description of the thin Capacitance Material
Based on the investigations of copper foil, dielectric resin properties and Barium Titinate particles, suitable copper foil and resin type was selected to construct/manufacture 8, 12, 16 and 24 µm dielectric thickness capacitive material without particles and 16µm with Barium Titinate filled material. Characteristics of the developed capacitive materials are listed in Table 1.

Table 1 – Dielectric Material Characteristics

Properties	24 µm	16 µm	12 µm	8µm	16 µm $BaTiO_3$
Copper foil type	RTF	RTF	VLP	VLP	VLP
Dielectric type	B	B	B	B	B
Copper weight (oz)	1	1	1	1	1
Peel strength (kN/m)	>1.3	>1.3	>1.3	>1.3	>0.7
Dielectric thickness µm	24	16	12	8	16
Capacitance at 1GHz nF/cm^2	0.14	0.23	0.31	0.45	1.75
Dk at 1GHz	4.4	4.4	4.4	4.4	30
Df at 1GHz	0.015	0.015	0.015	0.016	0.019
Dielectric breakdown V	>500	>500	>500	>500	>100
Tg(DMA) Celsius	>200	>200	>200	>200	>200
Electrical migration*(hrs)	>1000	>1000	>1000	>1000	>1000
Solder float (288Cx5times)	Passed	Passed	Passed	Passed	Passed

*RH85%/85C/35V

Processing of the Capacitance Material
Ten different PCB fabrication facilities have processed the substrates without high Dk particles. The trials were conducted on thin film capacitance materials of 24, 16 and 12 μm dielectric thickness. Two of the fabricators have also processed the 8 μm and the 16 μm with particles as well. These trials were conducted to see the capability of processing the material with conventional manufacturing equipment as well as build vehicles for testing.

Pattern Formation
One of the major design criteria for the material was to be able to be processed through the standard inner layer process. The typical process consists of:
1. Chemical Pre-clean
2. Dry Film lamination
3. Image Expose
4. Develop, Etch and Strip (Dual sides)
5. Black oxide or Alternative

Due to the tough and flexible nature of the resin, the material without particles was processed without being damaged. This included not having the clearance holes "blow out" during etching or having the border detach from the circuit. This is not the case for many thin capacitor materials.

For the 16 μm material with particles, the process had to be modified due to the more brittle nature of the material. The following is an example of the process flow for this material:

1. Chemical Pre-clean
2. Dry Film lamination
3. Image Expose one side/Blanket Expose other side
4. Develop and Etch one side, Strip resist both sides
5. Black oxide or Alternative (one or both sides depending on equipment)
6. Laminate Prepreg and Copper to Imaged Side
7. Chemical Pre-clean
8. Dry Film lamination
9. Image Expose both sides
10. Develop, Etch and Strip both sides
11. Black Oxide or Alternative

Although, processing thin capacitance material can be challenging and may need modifications or adjustment to the process, the material was capable of processing through the conventional PCB manufacturing steps. This was proven at all ten fabrication facilities.

Hi-Pot (High Potential) Test
The patterned laminate was tested to Hi-Pot test. All unfilled panels passed the 500V test, including the 8 μm dielectric thickness material. The 16 μm material with high Dk particles, also had very high yields but was tested only to 100V, as the loading of the polymer greatly reduces the electric strength. The high yields at inner-layer test are due not only to the construction of the material, but by having any marginal material caught at the substrate manufacturer by pre-testing.

Lamination
Scaling is a very important parameter for multilayer lamination. Figure 1 shows the measured result of the movements of the distance between the holes during the process. As it can be seen, thin capacitance material's movement was equivalent to that of 50 μm (2mil) core material. This is most likely due to the fact that since most of the copper is retained, the dielectric thickness has little effect on the scaling. Hence, as a first trial the scaling factor for the thin capacitance material can be the same as is used for the 50 μm core material. This was verified at the three PCB facilities previously mentioned.

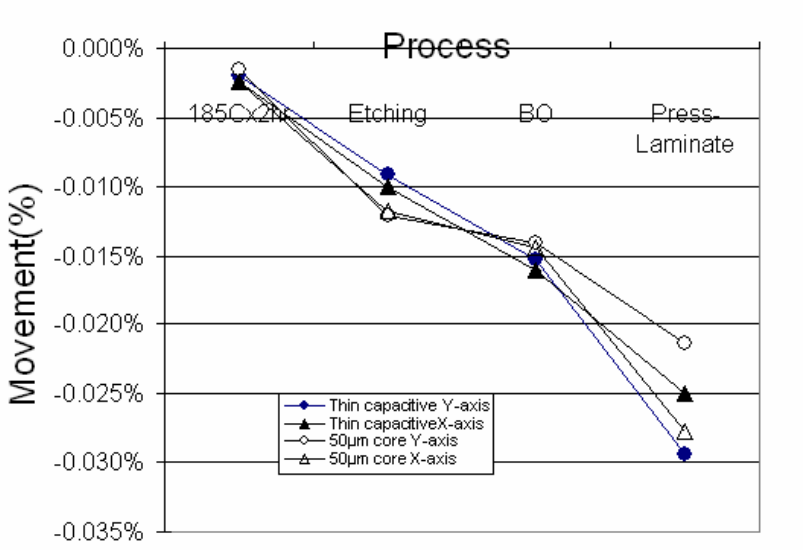

Figure 1 – Dimensional Stability during the Process

Through Hole and Micro-Via Plating Reliability

Figure 2-4 shows the cross-sections of the boards using thin capacitive material. Figure 2 is the cross-section of a PTH in a board using 12µm dielectric thickness capacitor material and Figure 3 is of a 24µm capacitor board connected with a micro-via. Because the material is non-woven, it is easily laser ablated and plated. Figure 4 is of a 24 layer board using the 12 micron material after 6x Solder shock at 288^0C. Good connection of the plated copper to the thin dielectric layers is observed. Also, all the cross-sections show good compatibility with the surrounding FR-4 laminates.

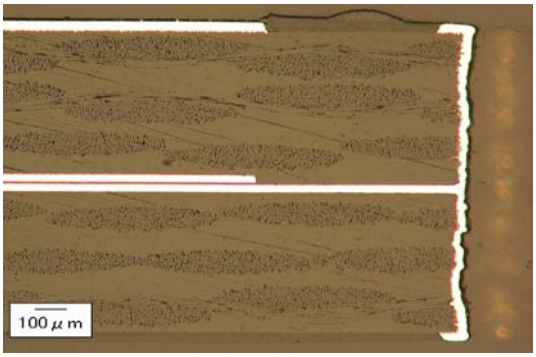

Figure 2 – Cross-Section of Board Using 12 µm Capacitance Layer

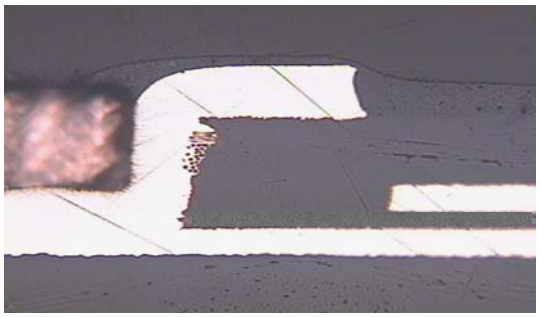

Figure 3 – Cross-section of Board Using 24 µm Capacitance Layer with Micro-Via

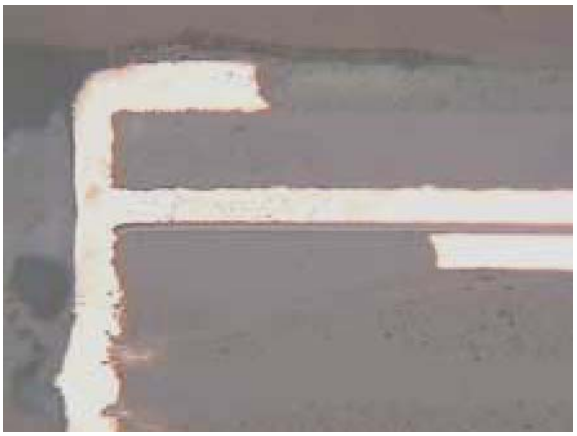

Figure 4 – Cross-Section of 24 Layer Board Using 12 μm Capacitance Layer after 6x Solder Shock

Electrical Performance of the Board Using Thin Capacitive Material

Many advantages on electrical performance, such as power distribution and Electro Magnetic Interference (EMI), can be expected by using thin capacitive material in PCBs.

Conducted emissions on the supply line for a microprocessor (MPU) running at 40MHz were measured by VDE method. No discrete decoupling capacitors were mounted on the four-layer board (See Figure 5). Comparison of conducted emissions between conventional standard 400μm laminate core and 12μm thin film capacitive core are shown In the Figure 6. Significant reduction of emissions in the frequency range of 150 to 550MHz, which is known as the difficult range to reduce by discrete capacitors were observed by the thin film capacitive core. Lower effective inductance and larger capacitance of the thin film core structure improves performance of supply decoupling for MCUs.

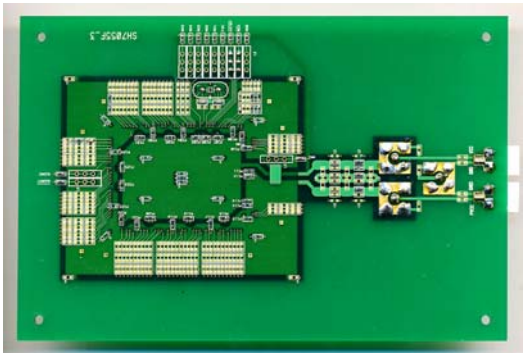

Figure 5 – Board Used for the Noise Current Measurement[4]

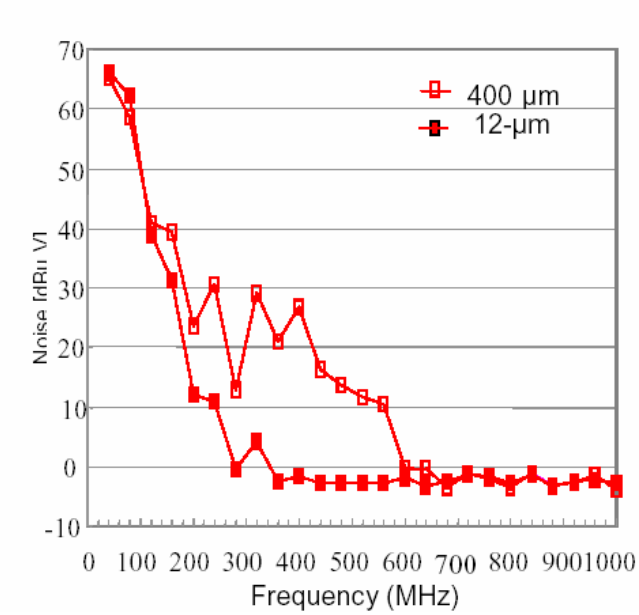

Figure 6 – Comparison of Noise Current with Standard Laminate Core and 12 µm Core[5]

The reduction in EMI is a good benefit of using these thin capacitor substrates, but the major benefit is in the reduction in impedance of the power planes. Figure 7 shows the test vehicle used to check the power plane impedance. Figure 8 shows the reduction in self-impedance of various capacitive layers. Figure 9 shows the transfer impedance change in capacitance at 1" distance. The distance from the chip and the shape of the planes will impact these numbers, but it is easily seen that the thinner the material the lower the impedance. This is a very important design consideration and shows the benefit of the embedded capacitor material.

Additionally, the 16 µm material with the high Dk particles reduced the crossover from capacitance driven impedance to inductance driven impedance from 100 to 50 MHz. It also further reduced the impedance at higher frequencies (at the time of writing of this article we had not yet secured permission from the company who tested the material to publish the detailed data. We hope to be able to present this at the conference).

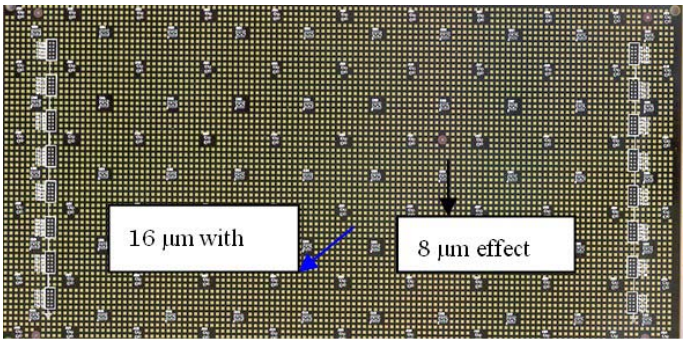

Figure 7- Test Vehicle for Measuring Power Plane Impedance

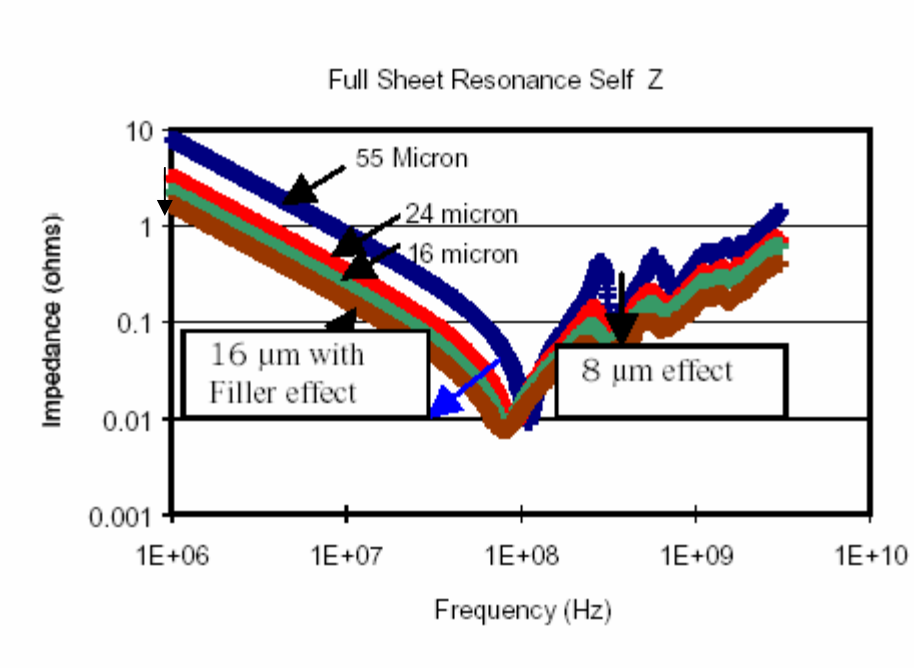

Figure 8- Self Impedance Results

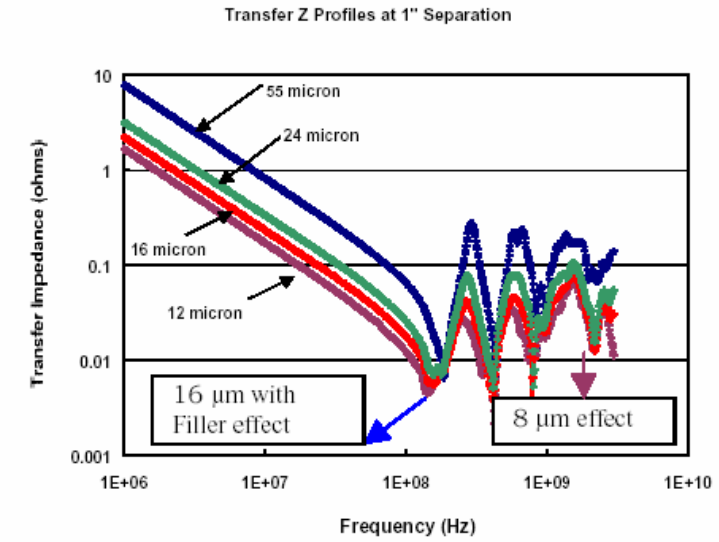

Figure 9- Transfer Impedance Results

Conclusion

Contributions and influences of copper foil and dielectric resin properties to construct a thin dielectric capacitive material have been investigated. Suitable copper foil type and dielectric resin was selected to construct thin film capacitive material.

The thin film capacitive materials 8, 12, 16 and 24 µm dielectric thickness, were capable of processing through the conventional PCB manufacturing steps. The 16 µm with particles required additional steps, but also processed through the inner layer process. This was shown at multiple PCB shop locations.

The electrical performance and capacitance values are improved over the traditional FR4 laminate substrates. The ability to withstand 500 volt Hi-Pot testing (even at 8µm) is significant, and has not been demonstrated by any other thin polymer capacitive substrate. For the particle-containing product the lower Hi-Pot testing will still insure reliable performance for many applications. A dramatic reduction in EMI and both self and transfer impedance will allow for better system performance especially at high speeds. In addition both filled and unfilled substrates demonstrated X7R TCC characteristics. These characteristics will also help to simplify the designer's tasks. Table 2 shows a comparison of the properties between the unfilled and filled (with High Dk particles) thin substrates.

Table 2 -Comparison of Unfilled and Filled Thin Substrates

Property	Unfilled Thin Substrates	Filled Substrates
Impedance Reduction/lower noise		+
Electric Strength/ High Potential Testing	+	
Ease of PCB Processing	+	
Cost of Substrate/Raw Board	+	
Cost of Assembled Board	?	?

The cost of the assembled board is based on the number of discrete capacitors that can be removed. Since the filled substrate provides a higher capacitance, it may allow more components to be removed and actually make for a less expensive assembly. This is very product specific and can not be generalized.

As the demand for a power distribution system with low impedance and control of EMI increases for hi-end computing boards with high signal frequency, the usage of thin film capacitive material in PCBs is expected to grow.

Acknowledgement
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We appreciate Atsushi Nakamura and his team of Hitachi LTD for providing data and suggestions.
We appreciate the manufacturing of the test vehicles for impedance testing by Howard Jones (formerly of Sanmina-SCI in Owego, NY).

Reference
1) An improved laminate for embedded capacitance application, Jeffrey Gotro and Jeffery Kamla, 1999 IPC proceedings
2) Embedded Passive Electrical Characterization Results, Istvan Novak, 2000 IPC proceedings
3) Next Generation Embedded Capacitance Material, T.Yamamoto, K.Yamazaki, F.Kuwako 2002 ECWC proceedings
4) Courtesy of HITACHI LTD.
5) Courtesy of HITACHI LTD.

Note: A version of this paper was first presented at the Materials Research Society Fall 2003 Conference in Boston, MA

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February 26, 2004

INTRODUCTION

- Review of Buried Capacitance
- Product Design
- Performance Characteristics
- PWB Manufacturing Process
- Impedance/Noise Measurements
- Comparison Summary
- Conclusion

Review

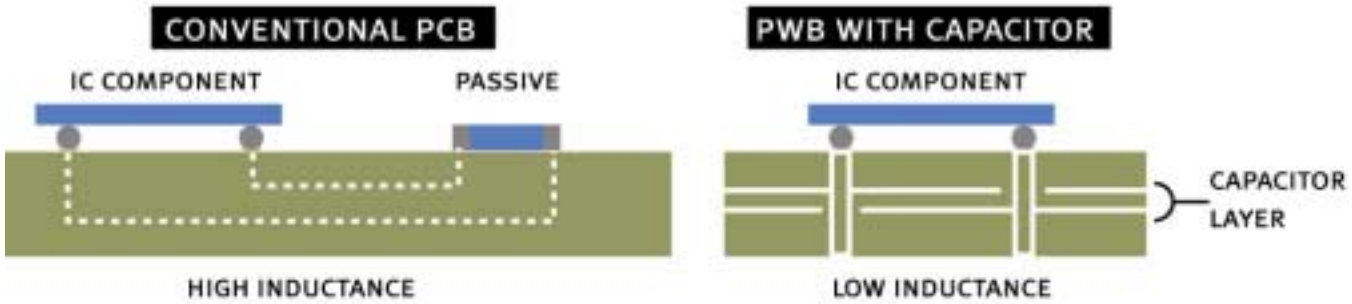
Current applications with Buried Capacitance

Hi-end computers

Network servers

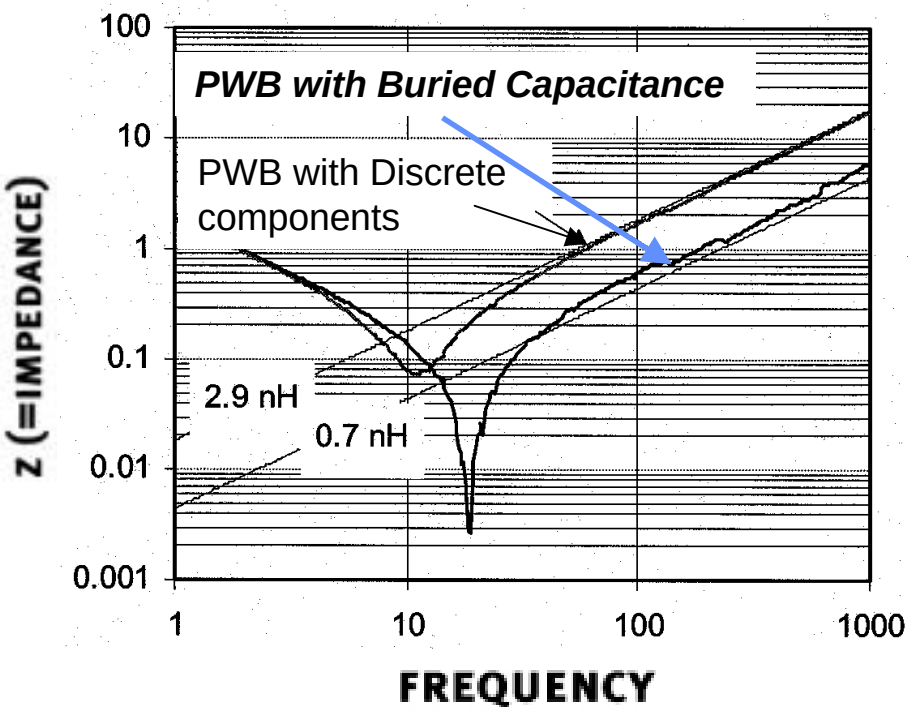
Network routers

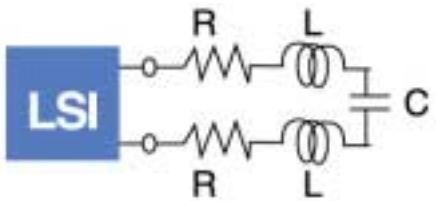
Demand for power distribution system with low impedance



Review

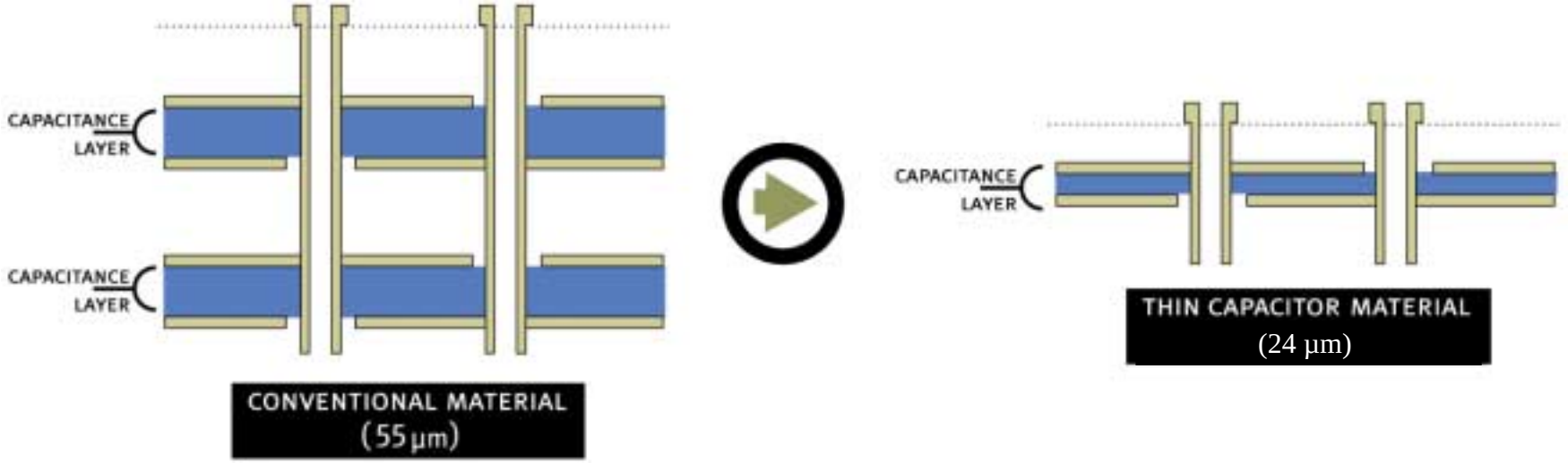
Lower Impedance compared to discrete components





Review

Demand for thin (<25micron) Buried Capacitance



Expectation by using Thin Capacitor Material

- Improvement in Electrical Performance
- Reduce System Cost
- Reduce Thickness of the Board
- Reduce Prototype Revisions

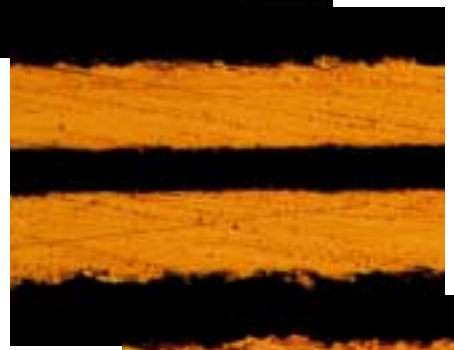
Product Design

Construction

12 µm

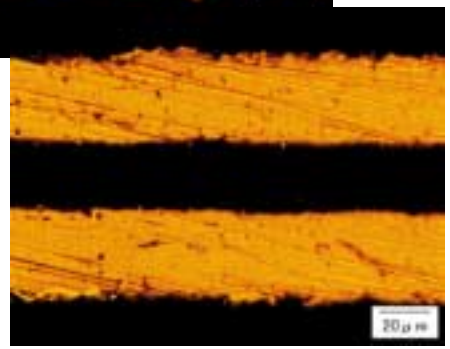
12 micron Polymer Dielectric

16 µm



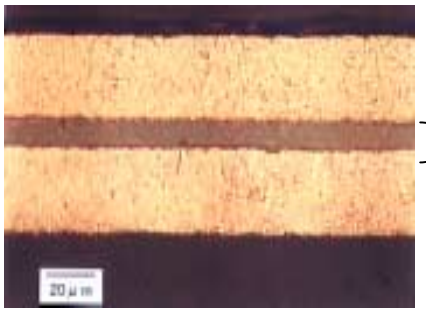
16 micron Polymer Dielectric

24 µm



24 micron Polymer Dielectric

16 µm



16 micron Polymer Dielectric ***with Hi-Dk Filler***

-Standard Copper thickness is 35 µm

Product Data

Electrical Properties

Characteristics	Condition	Unit	24µm	16µm	12µm	8µm	16µm-Filler
Capacitance	1GHz	nF/cm^2	0.14	0.23	0.31	0.45	1.75
Dk	1GHz	N/A	4.4	4.4	4.4	4.4	30.0
Df	1GHz	N/A	0.015	0.015	0.015	0.016	0.019
Dielectric Thickness	Nominal	Micro-Meter	24	16	12	8	16

Product Data

Physical Properties

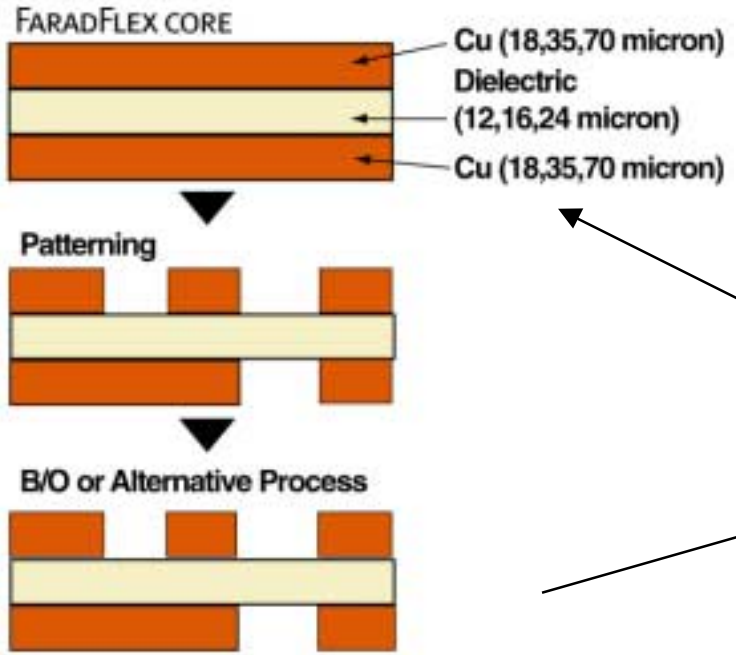
Characteristics	Condition	Unit	24µm	16µm	8&12µm	16µm-Filler
Tg	DMA	Celsius	200	200	200	200
Peel Strength	As received	lb/in	8.0	8.0	8.0	6.0
Young's Modules	JIS 2318	GPa	4.8	5.8	7.2	NA
Tensile Strength	JIS 2318	MPa	180	180	180	NA
CTE (x,y)	IPC TM650	PPM	23	23	28/23	TBD
Breakdown	1kV/sec	V	>5000	>4000	>4000	TBD
Insulation Reliability	85C/85%/35V	hr	>1000	>1000	>1000	>1000

NA- Not Applicable as Product is not self supporting

PWB Manufacturing Process

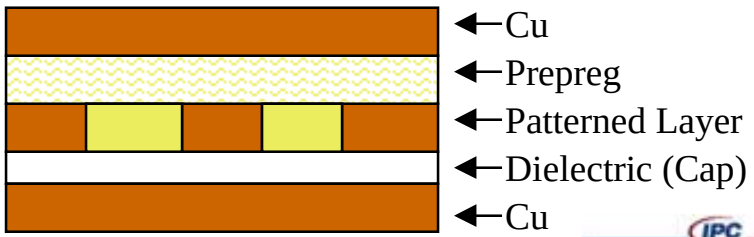
Thin Substrate without Particles

1. Pre-Clean
2. Dry Film lamination
3. Expose Image
4. Pattern etching (Both sides)
5. Black Oxide or Alternative



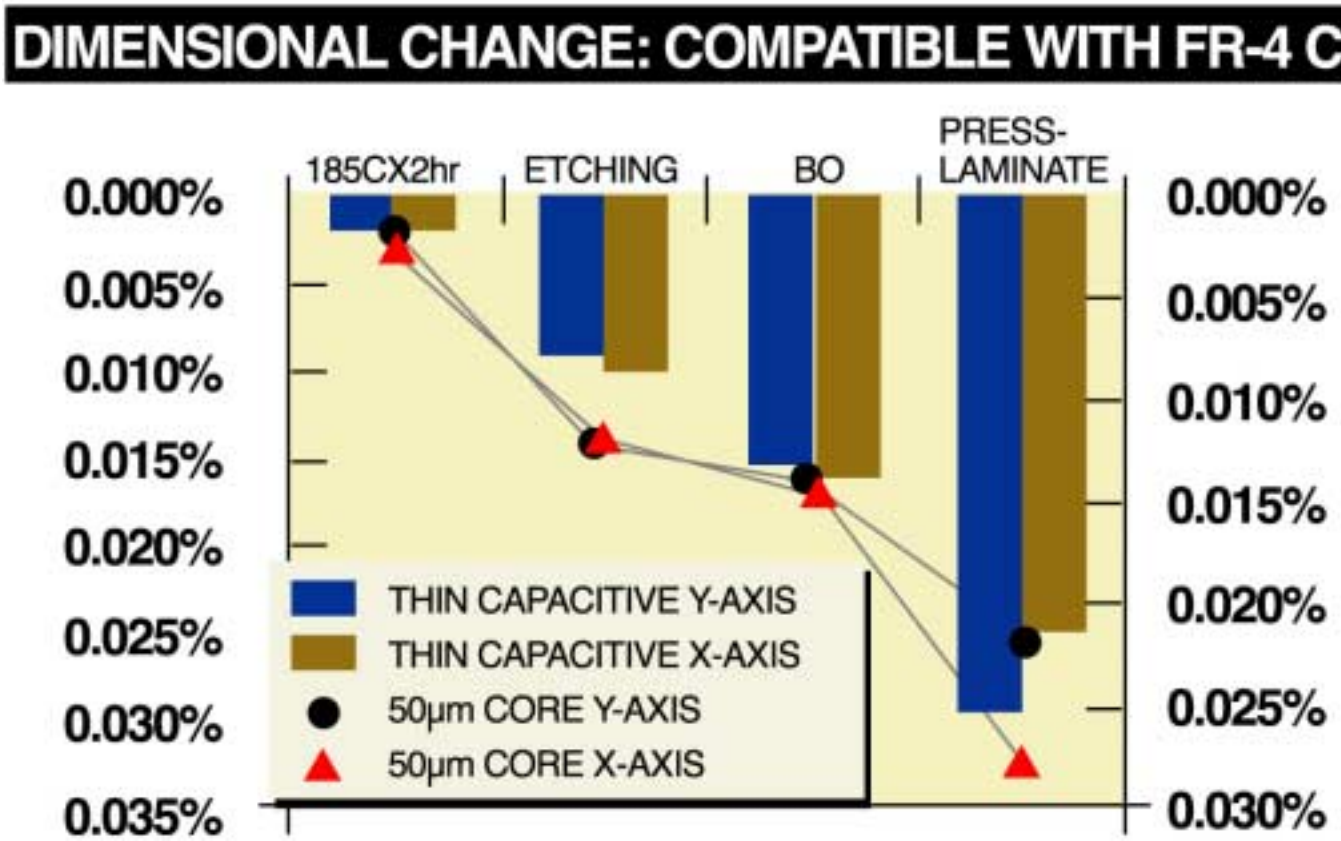
Thin Substrate with Particles

1. Pre-Clean
2. Dry Film lamination
3. Expose Image (Pattern/Blanket)
4. Pattern etching (One side)
5. Black Oxide or Alternative
6. Laminate Prepreg/Cu to Imaged Side
7. Pre-Clean
8. Dry Film Laminate
9. Expose Image (Both Sides)
10. Pattern Etching (Both Sides)
11. Black Oxide or Alternative



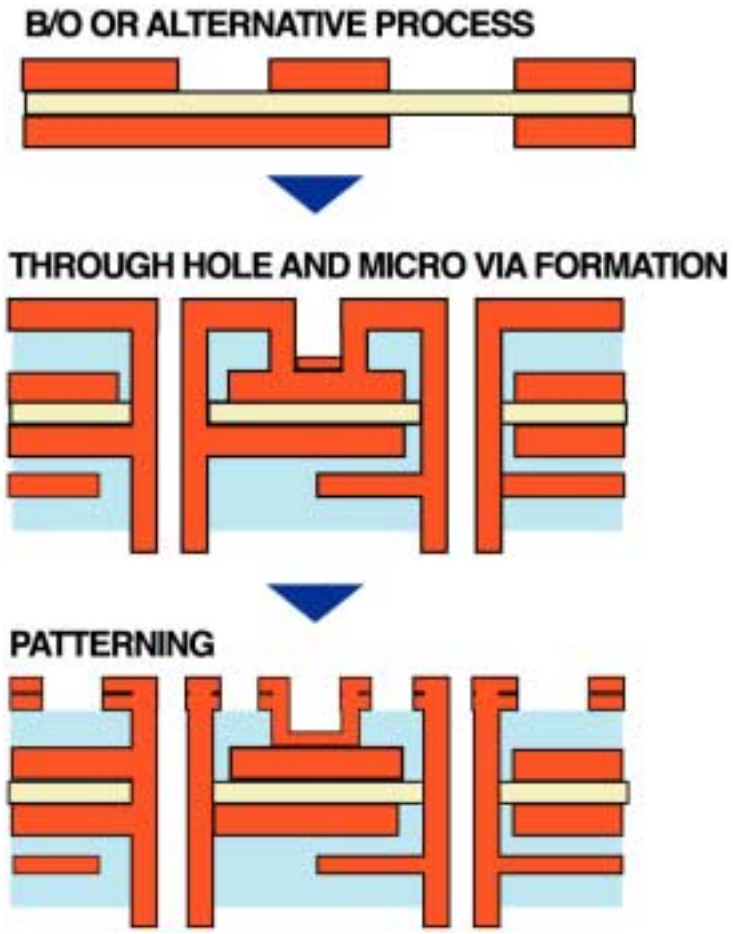
Subassembly

PWB Manufacturing Process

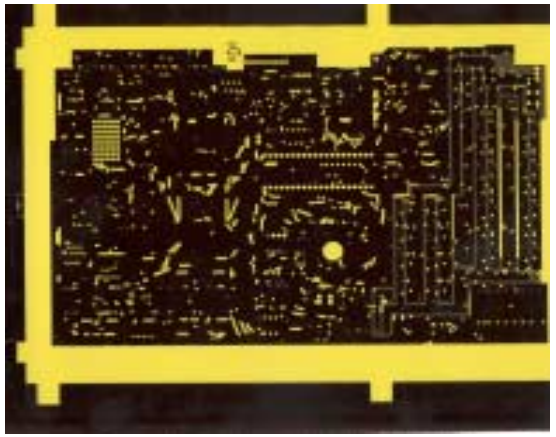


12 µm CAPACITOR

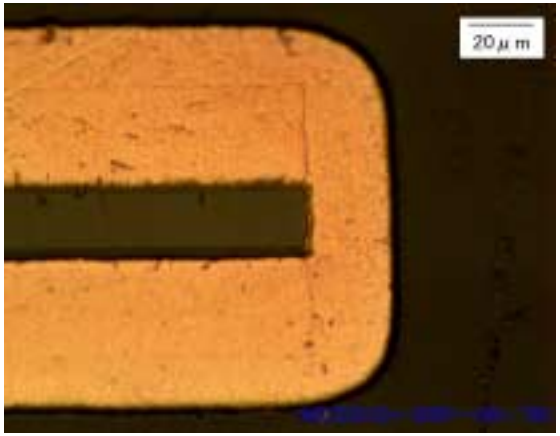
PWB Manufacturing Process



B/O treated panel



After processing drilling,desmear and plating



PWB Manufacturing Process

Summary of Unfilled Substrates

- Substrates Processed at 10 Major PCB Facilities
- Standard I/L Processing
- Results
    1. **No loss** due to jams
    2. **No "blow out"** of Clearance holes
    3. **No separation** from border pattern
    4. **99+ % Yield (due to material issues)** at Hi-Pot (500 Volts)
    5. Both Vertical Racked Black Oxide and Alternative Oxide used **successfully**
- PWBs available from ZBC™ Licensed Fabricators

ZBC™ - Is a trademark of HSCI

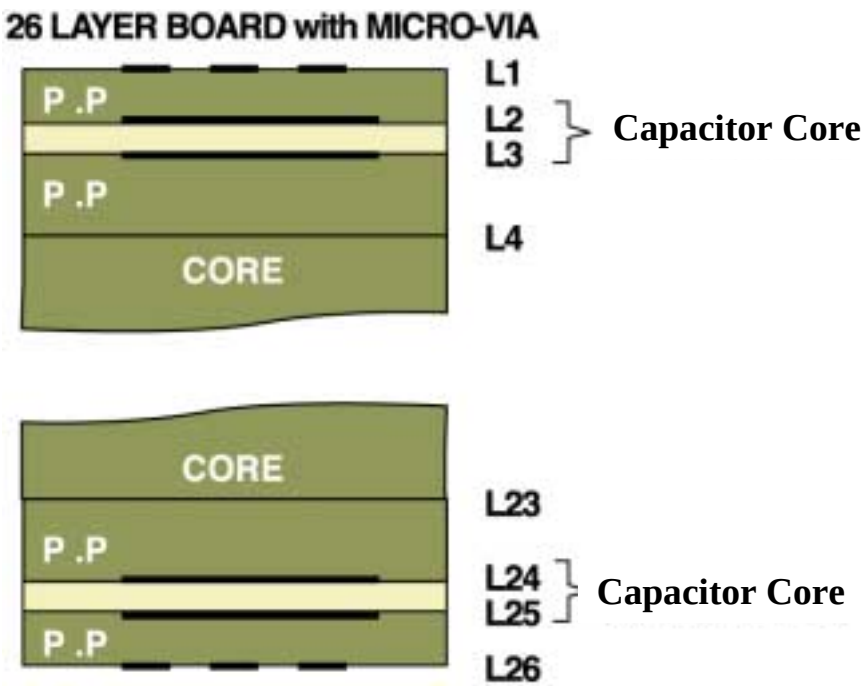
PWB Manufacturing Process

Summary of Filled Substrates

- Substrates Processed at 2 Major PCB Facilities
- Standard I/L Processing with additional steps
- Results
    1. **No loss** due to jams
    2. **No "blow out"** of Clearance holes
    3. **No separation** from border pattern(Cu to edges)
    4. **100 % Yield** at Hi-Pot (100 Volts) (limited quantity)
    5. Both Vertical Racked Black Oxide and Alternative Oxide used **successfully**
    6. **Registration between *buried* and outer core layers on subassembly critical**
- PWBs available from ZBC™ Licensed Fabricators

ZBC™ - Is a trademark of HSCI

Reliability Tests



Micro-via Plating

24 µm

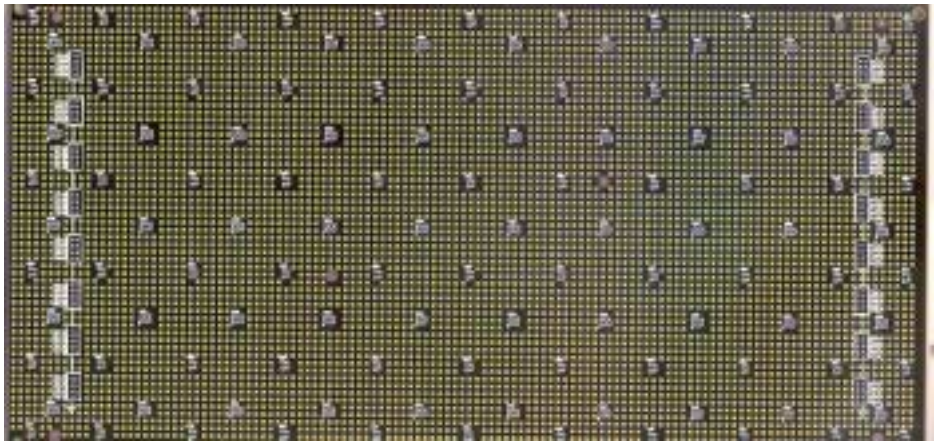
Thermal Solder Shock 288C x6

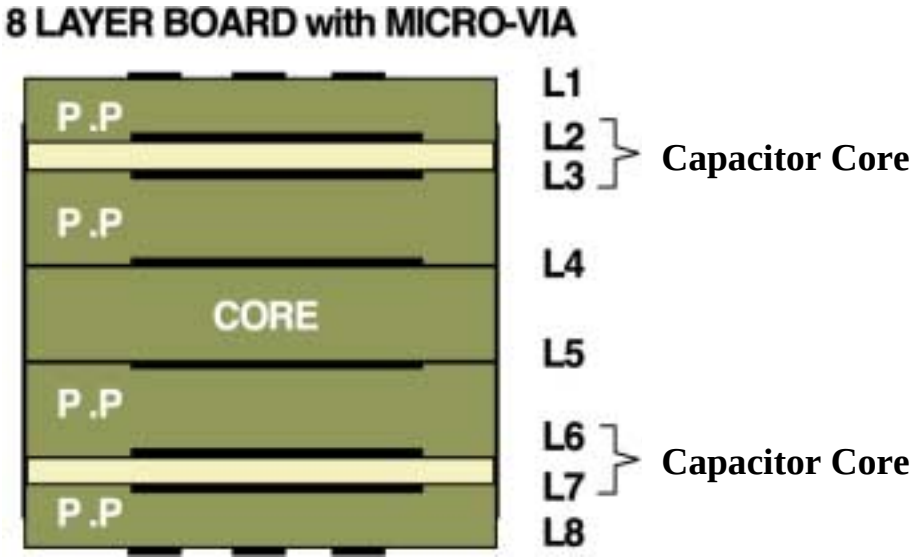
12 µm

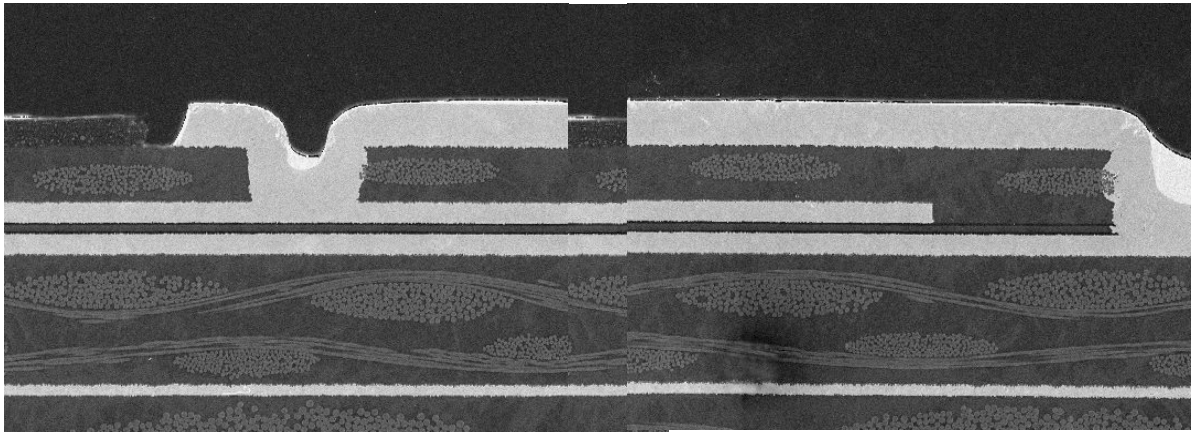
- Dielectric Withstanding Voltage : 500V Passed, No failure
- T-260 Time to Delamination : *12 µm*- 6.3min, *24 µm*- 5.2min
- Blind Via Plating Defects : No defects found
- Thermal Solder Shock (288°C)– 6x : No defects found
- Liquid-Liquid : *24 µm* 4.2%(500 cycle)
- IST Testing: Passed 500 Cycles

Impedance Test Vehicle

8 Layer Board



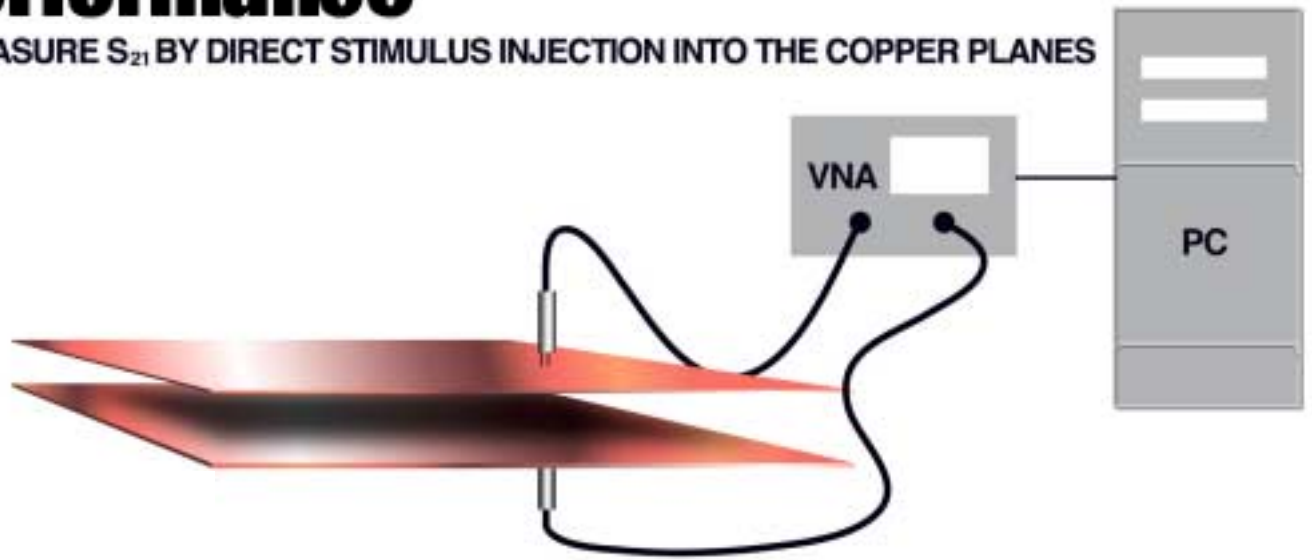




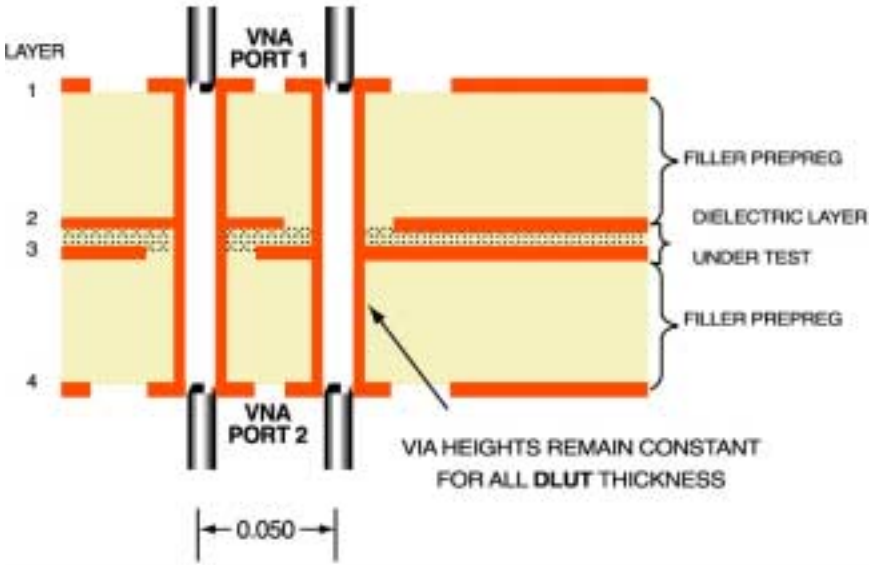
12 µm

PWB Electrical Performance

MEASURE S_{21} BY DIRECT STIMULUS INJECTION INTO THE COPPER PLANES

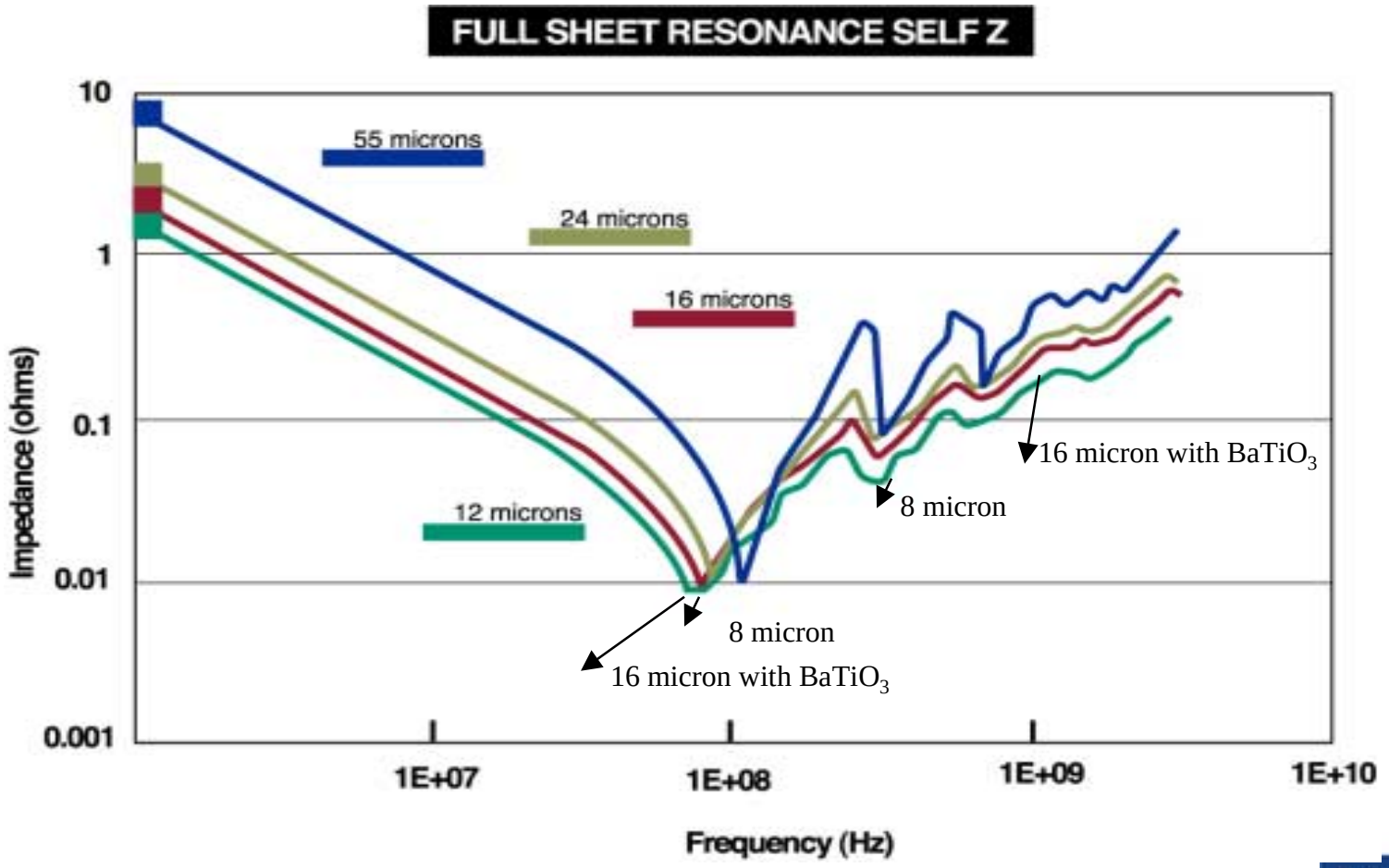


4 LAYER TEST BOARD CROSS SECTION VIEW



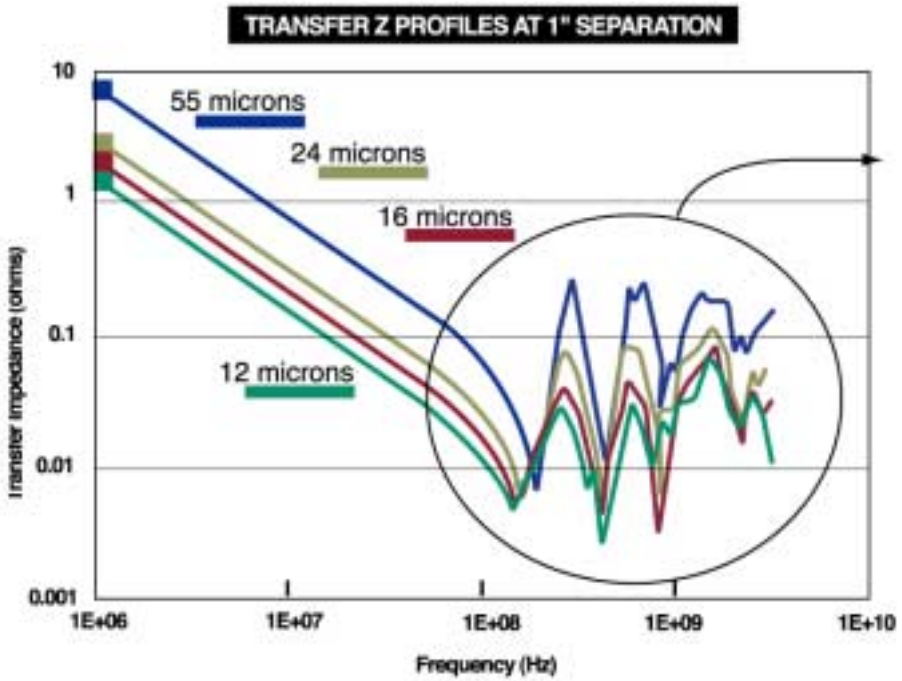
PWB Electrical Performance (Self Z)

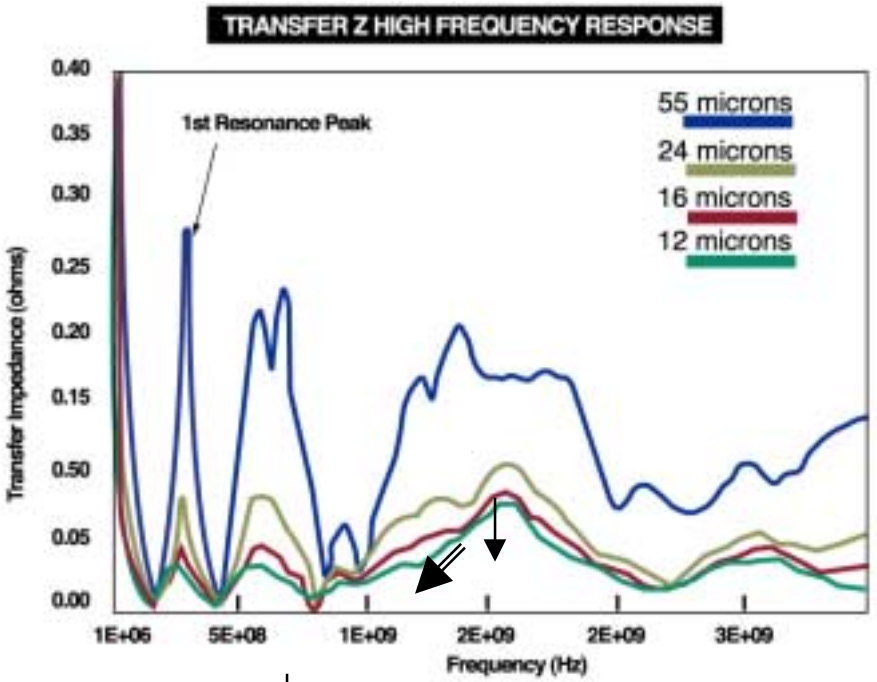
Significant Reduction on Impedance



PWB Electrical Performance (Transfer Z)

Significant Reduction on Impedance





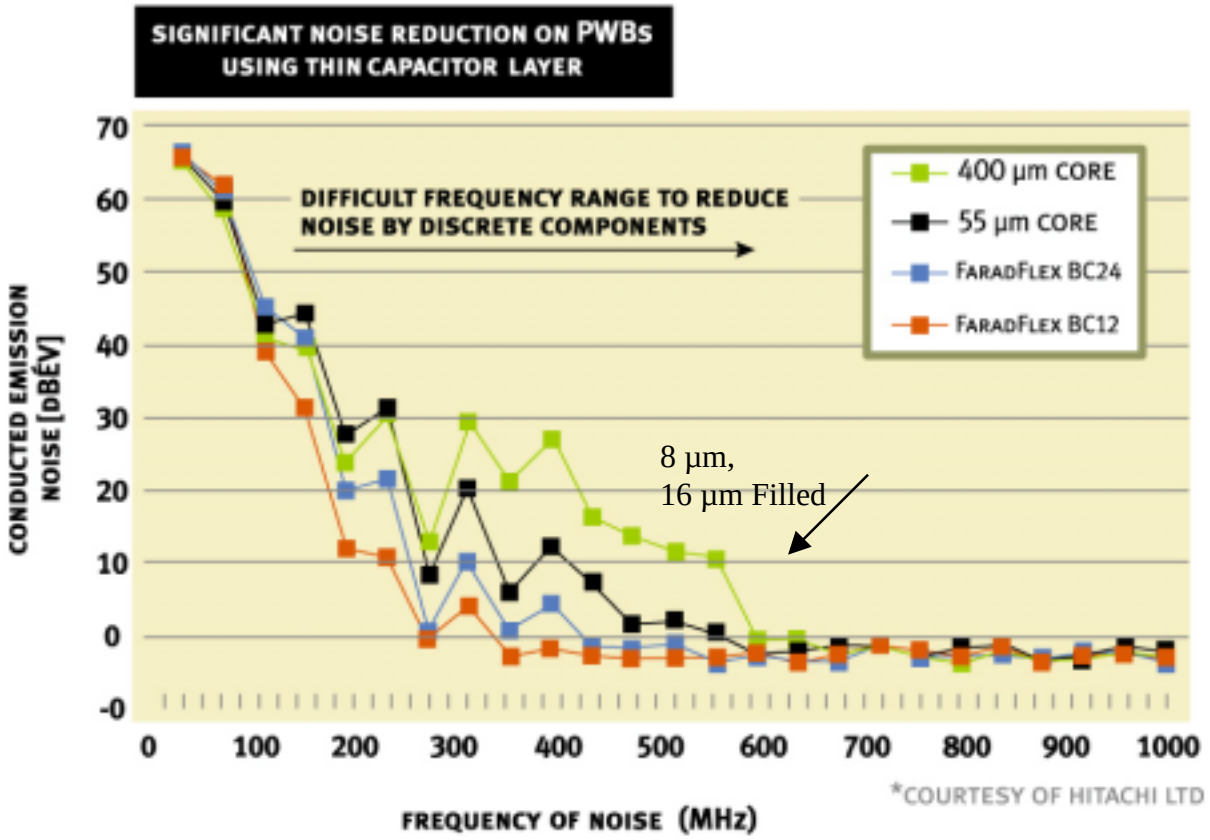
Data Coutesy of Sanmina-SCI Corp.

↓ 8 micron

↙ 16 micron with $BaTiO_3$

PWB Electrical Performance

Significant Reduction of EMI



Comparison Summary

Unfilled Substrates Versus Filled Substrates

Property	Unfilled Thin Substrates	Filled Substrates
Impedance Reduction/lower noise		+
Electric Strength/ High Potential Testing	+	
Ease of PCB Processing	+	
Cost of Substrate/Raw Board	+	
Cost of Assembled Board	?	?

Conclusion

- Thinner Power Distribution Planes are required for improved Impedance Performance at high frequency
- New Substrates have demonstrated *excellent* electrical performance and physical properties.
- They are *compatible* with PWB processing; a truly “drop in” material.
- Materials are commercially available from Licensed Fabricators
- The use of Embedded Capacitance can simplify PCB lay-out and reduce the number of prototypes required.
- The Technology can Improve System Price/Performance by
  - Reducing Discrete Caps
  - Reducing PWB size
  - Increasing Functionality
- Substrates Filled with Ferroelectric Particles have better performance, but result in higher cost PWBs
- Additional work is ongoing to
  - Improve PWB manufacturing process of filled substrates