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Embedded Passives in High Layer Count High Reliability Printed Wiring Boards

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Abstract
This paper will discuss the use of thin film buried resistors and thin core plane pairs in high layer count high reliability printed wiring boards used in single and double sided surface mount assemblies. Very high thermal stress durability is required for assembly and component repair/replacement. The high density multilayer and sequential built designs of 14-26 layers use a combination of buried vias, blind vias, thin cores, several layers of buried resistors and thin core plane pairs to meet controlled impedance and circuit performance. The design of the resistors for BGA pull down terminations and for in-circuit resistors contain various values and tolerances. Overall thermal performance of the board is critical to the product reliability requiring the buried resistors and thin core plane pairs to also survive extreme thermal exposure. Thermal stress testing, as required by the applicable standard, was extended to multiple times in order to determine product robustness for laminate defects, plating integrity and inner plane connection durability. In addition, Current Induced Thermal Cycling Testing can be performed for comparative analysis. Special test coupons can be designed that duplicate the actual conditions of the board and allow the buried resistor layer to be present in the microsection for evaluation during the required inspections. As with conventional printed wiring technology, failures do occur, but typically only after extreme thermal stress or rework. Failure analysis was performed to identify the cause. Pictorial views of the component density, resistor designs, layer stackup, and failure analysis activity are contained in the paper. This paper will show that embedded passive technology can be implemented with success for high density, high layer count and high reliability printed wiring boards.

Changing Component and Design Requirements
High reliability printed wiring board products are typically used in military, aerospace and medical applications. Historically, components, design principles and materials all were applied using a conservative approach using time tested methods and materials. As the need for increased density required the move from components attached by through hole soldering to surface mount assembly, the printed wiring board technology also required a shift to leading edge designs and materials. Ball Grid Array (BGA) components have especially driven the requirements for density. BGA pitch of 1.25 mm (50 mils) with typical 352 pins requires 5/4.5 mil lines and spaces for double channel circuit routing when using a .635 mm (25 mils) land. 1.0 mm (40 mils) and some perimeter array .8 mm (31 mils) pitch BGAs can be routed using conventional technology with 3 and 4 mil lines and spaces. Increasingly finer pitch will require High Density Interconnect (HDI) designs and fabrication methods.

Embedded Passive Utilization in Complex Designs
Embedded passive technology, consisting of buried resistor layers and embedded capacitance layers, has been used in leading edge designs typically in the commercial and industrial business environment. High layer count designs (greater than 12 layers) with high reliability requirements presented a new arena for the embedded passive application.

High speed processor designs most often employ several BGA components and can have double sided SMT mounting. Components on both sides of a complex design requires offset BGA mounting or sequentially built boards utilizing blind vias. Buried vias are also often required to hold the layer count down to meet thickness requirements either for connector or chassis mounting specifications. An example of an offset BGA placement on a multilayer board is shown in Figure 1. The top layer has the dogbone fanout from the attachment land to the via. The bottom layer has the same geometry for the part on the other side. Via pads are present on both sides for interconnection. Being these via pads are under BGAs, they are tented with solder mask to prevent entrapment of contaminants and to improve reworkability of the assemblies during BGA replacement. Figure 2 shows a typical internal circuit layer with the routing at the BGA overlap area. Standard multilayer construction should always be the first choice for incorporating embedded passive technology. It follows in line with producibility driven designs that utilize the lowest level of technology to meet the product requirements. When standard multilayer design technology can't be used, then blind via sequential build is an option. Figure 3 shows a blind via sequential build board that has a buried resistor layer. Buried resistors can be incorporated into this type construction but it should be noted that sequential build requires at least two lamination cycles and subjects the resistor layer(s) to additional thermal stress and high pressure.

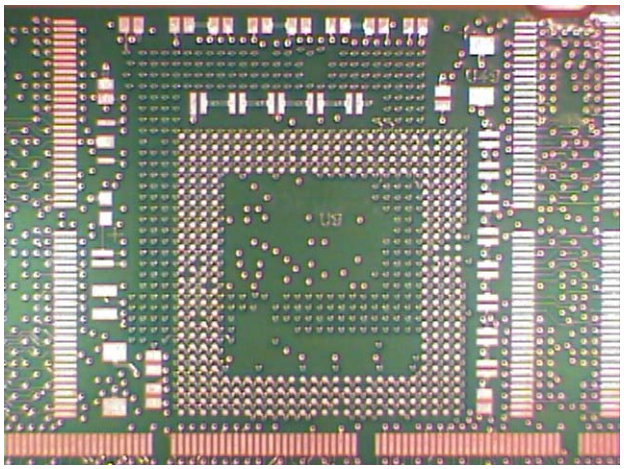


Figure 1 – Offset BGA Mounting on a Multilayer Board. 1.25 mm 352 pin BGA

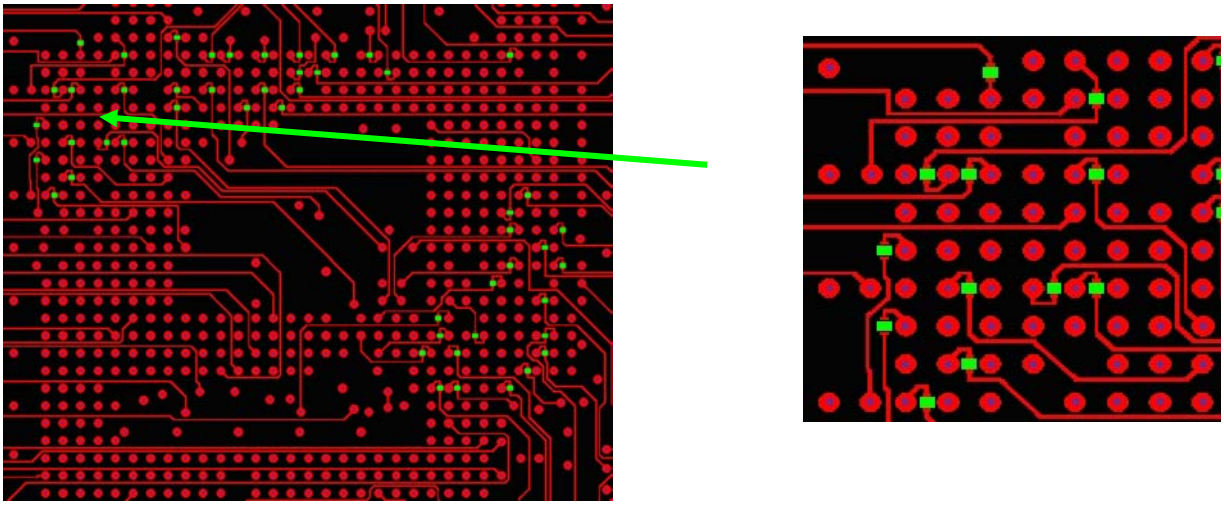


Figure 2 – Typical Internal Layer Routing for an Offset BGA Mounting , 1.25 mm 352 pin BGA – CAD Image

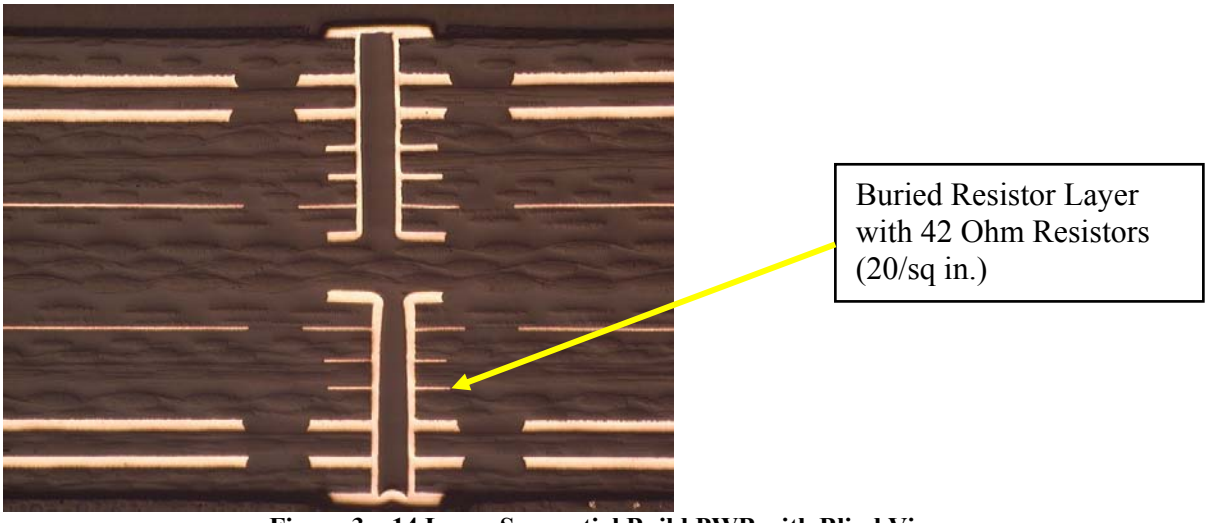


Figure 3 – 14 Layer Sequential Build PWB with Blind Vias

Buried resistors using thin film technology are designed into the circuitry and used as pullup, pulldown and termination resistors as well as in-circuit series or parallel resistors. Thin film materials of 25 ohms per square[1] have been used for resistors of typically 15 to 150 ohms. Typical tolerances are 15 to 25 percent. Designers always want a tighter tolerance and fabricators want a wider tolerance. A compromise must be made to meet both requirements. Designers must determine the actual range of values that can be allowed and the fabricator often will require process capability improvement to meet all

values and tolerances. Production designs have incorporated from 5 to 20 resistors per resistor circuit layer square inch. Buried resistors are typically on one to two internal layers of the board with only one per core recommended. Figure 4 shows a circuit layer with buried resistors that has a density of 20 resistors per resistor circuit layer square inch. Another method often used in high density printed wiring boards is the incorporation of buried vias. Although not recommended as a standard, buried resistors can be placed on blind via layers. Figure 5 is an example where buried vias on a circuit layer are combined with buried resistors. With this method, it is a fabricator's option, but most likely pattern button plating of the via will be used so the copper to be etched remains a known thickness and not affected by the plating.

The total number individual buried resistors produced in the last 5 years for the high reliability products is in excess of 2.5 million.

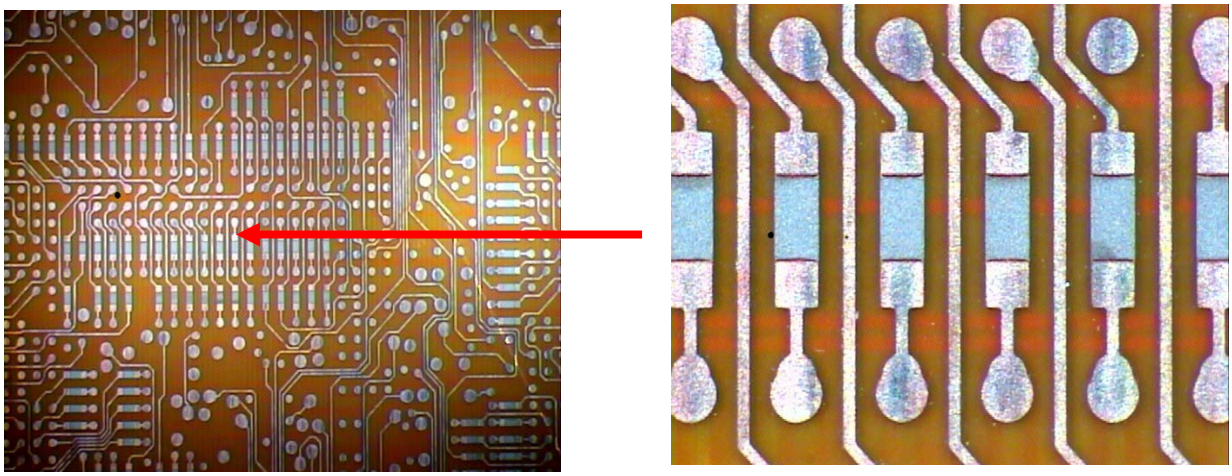


Figure 4 – 1.25 mm 352 Pin BGA Buried Resistor Internal Layer Routing

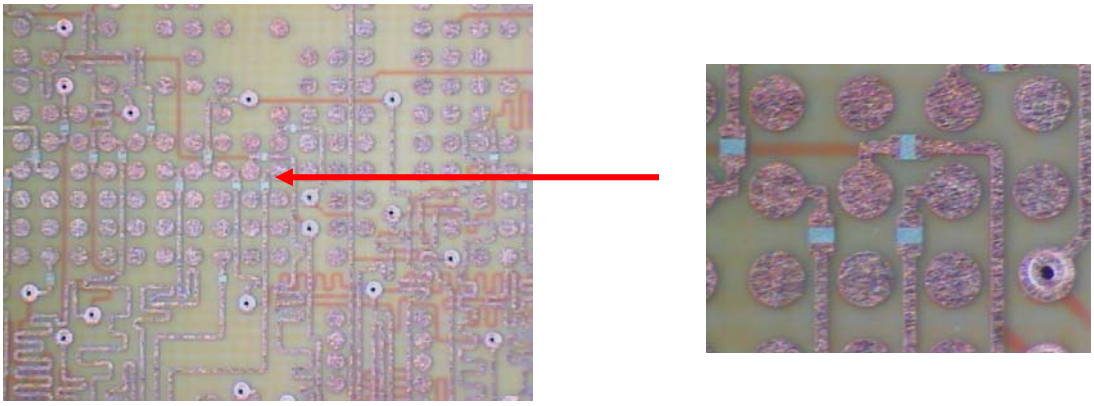


Figure 5 – Buried Resistors on a Buried Via Layer

Embedded capacitance can be designed into printed wiring boards by utilizing thin core plane pairs. This method may be able to be used to replace discrete surface decoupling capacitors as long as the capacitance value can be met. Some designs may not actually replace capacitors but can improve the performance of the circuitry. Thin core plane pairs can also be used to reduce overall thickness in high layer count designs. Dielectric spacing of .051 mm (.002 inches) with E-Glass resin systems of epoxy, polyimide or other blends is capable for thin core plane pairs.[2] cores are now available in other materials. Fabrication issues with thin core plane pairs are usually centered around handling, registration and the potential for dielectric breakdown resulting in power to ground shorting. To guard against potential power to ground shorts, a Hi-pot test per IPC-9252 should be incorporated into the fabrication process both at the layer stage and on the completed printed wiring board.

High Reliability Requirements

Assembly soldering of double sided component printed wiring boards subjects the board to 2X the thermal stress of a single sided assembly. A typical thermal profile of a high layer count double sided assembly is shown as Figure 6. Note that the time above 150 ºC is over four minutes. Time above 170 ºC is approximately one minute with a maximum temperature reached of 210 ºC. This cycle is applied two times to complete the assembly. This thermal stress requires the printed wiring board with the embedded passives to survive without delamination or other defect issues.

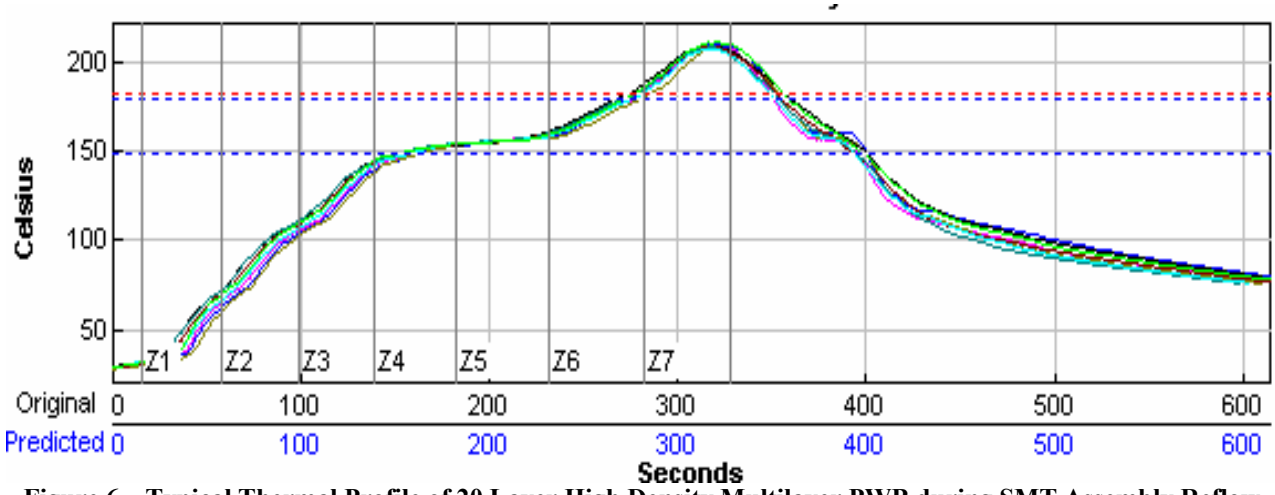


Figure 6 – Typical Thermal Profile of 20 Layer High Density Multilayer PWB during SMT Assembly Reflow

Additional thermal stress is applied to the printed wiring board during component repair/replacement. Many components, especially in military/aerospace products are Application Specific Integrated Circuits (ASIC) and thus are high cost components. The components on a printed wiring board most often are multiple times the cost of the board. When a component failure is detected, it is removed and replaced, often more than once. The component removal and replacement process must be characterized and controlled to prevent over heating the PWB and also to limit the number rework cycles that can be performed.

Thermal Damage Potentials

Thermal damage caused by extreme temperature excursions can be critical to embedded passive technology. The typical thermal damage such as barrel cracks, post or innerplane separation and delamination possible in conventional printed wiring boards, is potentially more susceptible in embedded passive technology. The fabricator must optimize the processes related to lamination bond strength both on conventional foils and the buried resistor thin film materials. Plated through hole processes for metallization and electrolytic copper plating must be capable to prevent innerlayer separation and barrel cracking from the multiple thermal stress cycles. Aspect ratio for high density boards can be 11:1.

A special coupon to detect delamination on the buried resistor layer can be incorporated for use during thermal stress of the B-coupon. This modified B-coupon should be designed with the actual line to pad spacing in the board and also contain the buried resistor material. During cross section analysis, the coupon can be evaluated for laminate defects at the closely spaced adjacent circuits and the buried resistor material.

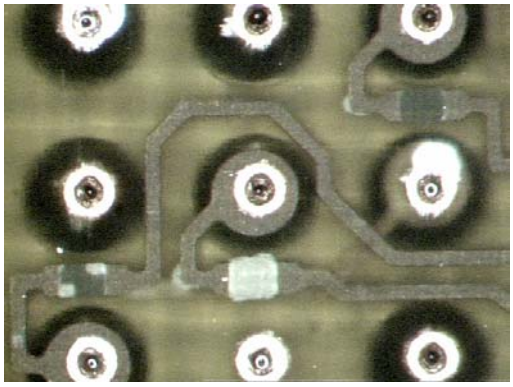
The standard thermal stress test is a 10 second one time 288 ºC (550 ºF) solder float per IPC-TM-650, Method 2.6.8. Multiple solder floats of 3 to 6X may be required to insure a more thermal resistant product. Minimal thermal damage should be attainable after multiple solder floats in a high reliability board. In order to meet the multiple thermal stress requirements, high Tg materials and those that are more thermally resistant may be required. Not all board designs react the same to thermal stress conditions. Tailoring of both materials and processes may be required.

Special testing for thermal resistance can be used. The DC Current Induced Thermal Cycling Stress Test per IPC-TM-650, Method 2.6.26 using special designed coupons and test equipment[3] can be used to simulate the extreme requirements placed on the board. Assembly reflow cycling preconditioning should be customized to the individual board and the rework cycles allowed for the product. Printed wiring board construction and materials may affect the results for the number of cycles obtainable from the testing so each product may need to be separately characterized for requirements in a production environment. Cycles of 300+ are attainable depending on the individual design. While not directly a test of the embedded passive variation, it can be used to identify pass or fail through the test cycles.

Failures and Failure Analysis

Failures on embedded resistors are generally either a change in resistance or a complete open circuit. Some resistance change can be expected after thermal stressing but it is minimal. In a specific test for assembly durability, data indicates that after a 6X assembly preconditioning thermal stress, the resistance change averaged 0.18% on 25 ohm/square thin film material.

Failures due to thermal stress can also result in complete open circuits. Failure analysis has shown that the resin bond to buried resistor material is somewhat less than to the copper foils used within the board. Thermal stress can cause local delamination and it typically results in an open circuit. Figure 7 shows an area of local delamination mostly over the buried resistor but also on nearby non-resistor areas. This indicates that the particular board was in total less thermally resistant and it is an opportunity for process and/or material improvements. Figure 8 and 9 show an open resistor found during failure analysis resulting from resin pull-away at the vertical conductor edge. These failures can be minimized within boards that are more thermally resistant. Specific designs may require different materials and process methods to survive in the environment of assembly, rework and field service.



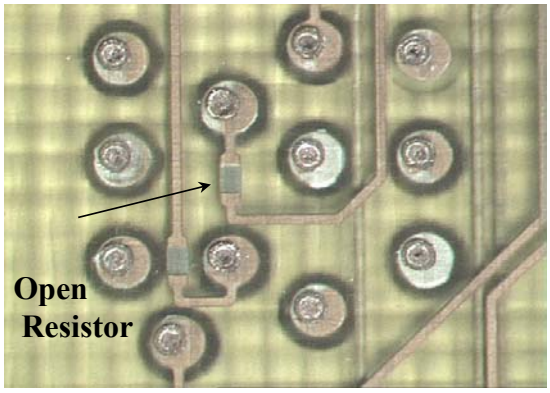


Figure 7 – Delamination Over Buried Resistors Figure 8 – Open Resistor

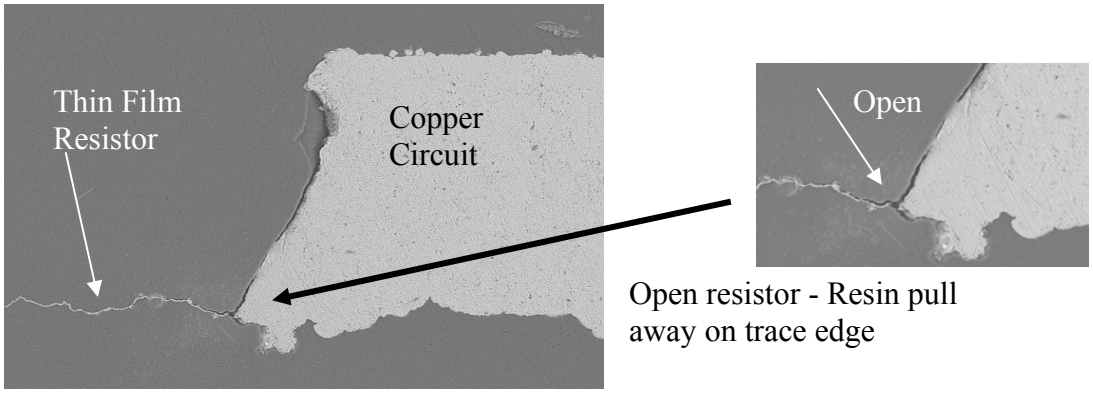


Figure 9 – Failure Analysis of Open Buried Resistor

Future Embedded Passive Technology

Many new embedded passive products for both buried resistors, buried capacitors and embedded capacitance have been introduced in the recent past. Limited data is available for their application in high reliability printed wiring board products. Opportunities exist to incorporate these new materials into future products. Increased electrical performance and the opportunity to increase package density are the benefits.

Conclusion

Embedded passives in high reliability printed wiring boards has been demonstrated to be capable in a production environment. Successful implementation requires careful design, material selection and process optimization. The selection of a printed wiring board supplier to meet these high reliability requirements is most important.

References

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Sanmina-SCI (HSCI BC™), Santa Clara, CA
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