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Design Considerations for Thin-Film Embedded Resistor and Capacitor Technologies

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Abstract
Embedded passives technologies can provide benefits of size, performance, cost, and reliability to high density, high-speed designs. A number of embedded passive technology solutions are available to the designer. Based on our experience with Shipley's thin-film, high-ohmic, InSite™ embedded resistor materials (500 and 1000 Ω/□), this paper provides some guidelines for selecting the appropriate embedded resistor technology and implementing it at a board fabricator. The design of embedded resistors, and the trade-offs between resistor size, tolerance, and capability of board fabrication processes, are analyzed in detail. This paper also discusses selection of the appropriate embedded capacitor technology and introduces some initial results on Shipley's thin-film, high-Dk, InSite embedded capacitor material (200 nF/cm^2). A simple cost analysis helps to screen which designs are appropriate candidates for embedded technology from a cost justification point of view.

Introduction
Designers of electronic circuits have always been challenged by trade-offs between performance, size, and cost. These trade-offs can be alleviated by monolithic integration of multiple devices in a common substrate, a practice that has long been exploited by semiconductor designers in the form of increasingly complex and lower cost integrated circuits (ICs). However, designers of printed circuit boards (PCBs) and IC packages have been slow to embrace and exploit the benefits of *integration*. The benefits of integrating passive components inside a board (embedded passive technology) are well known:

- Open up valuable real estate on the board surface resulting in increased functionality or reduced board size.
- Rout passive circuit elements with shorter, lower inductance interconnects which enable faster switching speeds and reduced EMI.
- Provide greater routing flexibility for high I/O count ICs by placement of passive elements on inner layers.
- Reduce parts count for assembly, with lower assembly and inventory costs.
- Improve board reliability with reduced number of solder joints.

The market penetration of embedded passives over the past few years has not lived up to earlier expectations. With some notable exceptions, OEM and EMS companies have taken a cautious approach to designing embedded passives into new products. However, as the global economic climate improves and barriers to market penetration are lowered (e.g. CAD tools), embedded passives technologies are expected to play a significant role in high-density and high-speed PCBs and IC packages.

Technology Selection
As is typical of technologies in the early phase of their life-cycle, designers are faced with a daunting list of alternative integrated passives technologies (see Figure 1) at various stages of development and commercialization.[1-3] Surface-mount (SMT) integrated passive components utilize the existing discrete component infrastructure but do not capture the full benefits of embedding components inside the board. For the latter approach, the choices include thin-film vs. thick-film resistor materials, paraelectric vs. ferroelectric capacitor materials, subtractive vs. additive fabrication processes, distributed vs. discrete capacitor structures, and innerlayer fabrication vs. pre-fabricated component placement approaches, as outlined in Figure 1.

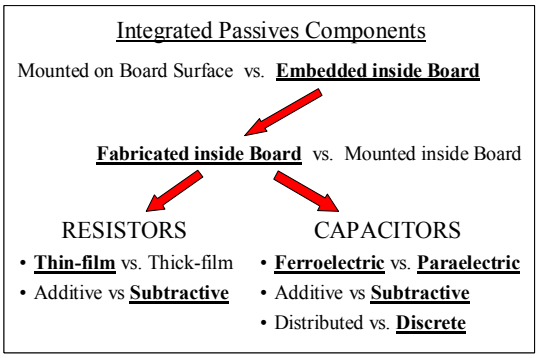


Figure 1 – Alternative Embedded Passives Technology Solutions

The choice of technology for a particular design need will be primarily driven by two factors:

- Satisfying design requirements of performance, size, total cost
- Ease of implementation – design, fabrication, test

The technology selection methodology typically begins with an analysis of the bill of materials (BOM) for the design. The number of embeddable resistors and capacitors is determined by the range of resistance and capacitance values and tolerances required by the design, with respect to the embedded technologies under consideration. It may not be possible nor even desirable to embed 100% of the SMT resistor and capacitor components regardless of the embedded technology used. Additional constraints such design flexibility for rapid changes to critical circuit elements will reduce the total number of embeddable components, as described by Savic et al.[4]

On the other hand, maximizing the number of embedded components improves the cost justification compared to total assembled cost of SMT components. This can be achieved by selecting technologies with sheet resistivity and capacitance density values that are centered in the distribution of resistance and capacitance values for a specific application. This methodology is illustrated in the following discussions on resistor and capacitor materials.

Resistor Material

The resistor material is a thin-film of doped-Platinum deposited on copper foil by atmospheric pressure, vapor deposition.[5, 6] The thin resistor films (<0.1μm thick) use small amounts of platinum and allow high values of sheet resistivity (ρ = 500 and 1000 Ω/□) to be economically produced.

$$R(\Omega) = \rho(\Omega/\square) \cdot L / W \qquad (1)$$

Depending on minimum dimensions and available board area, a wide range of resistance values between 50Ω and 100,000Ω can be fabricated by varying the length (L) to width (W) aspect ratio from 0.1 to 100 (see Eq. 1). This range of resistance values is represented by the red arrow in Figure 2 which illustrates resistance value distributions for typical designs in mobile phone, telecom, PC peripheral, automotive, and military/avionics market segments. Note that resistance value distributions can vary a lot between applications within a market segment, and hence will have to be analyzed on a case-by-case basis.

Resistor tolerances play an important role in embedded technology selection, especially between thin-film and thick-film technologies. Typical SMT resistors are specified at ±5% tolerance and this often becomes the default target for embedded resistors.

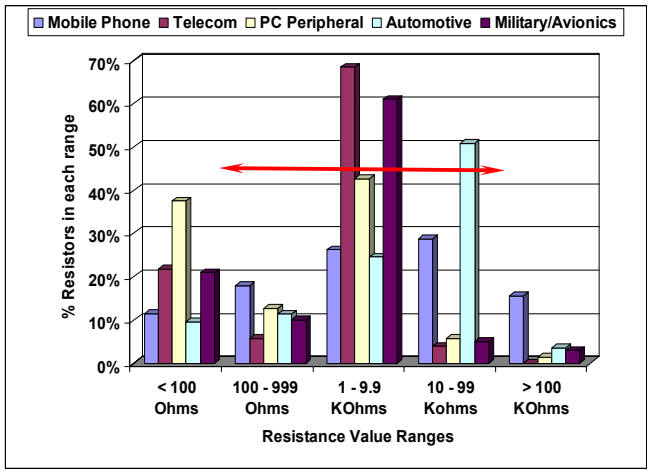


Figure 2 – Resistance Value Distributions for Examples of Applications in Various Industry Segments (Private Communications)

Resistor tolerance includes variations in material resistivity and physical dimensions of thickness, length, and width. This is discussed in detail in the section on resistor tolerance. To achieve the ±5% tolerance target consistently, embedded resistors require laser trimming[7, 8] which has implications on cost, throughput, and implementation.

With time-to-market pressures, there may not be sufficient time, tools, or expertise for designers to quantify the effect of resistor tolerances on overall performance. The designer is then required to make a judgment call on how much resistance variation can the design *really* tolerate. An experienced designer may allow ±10% to ±20% tolerance, depending on the function of the resistor in the circuit. In general, higher value, pull-up/down resistors (e.g. 1-10KΩ) have wider tolerance windows than termination resistors (e.g. 50Ω). The mix of resistance values and tolerances will generally determine which resistors get embedded and which are retained as SMT resistors.

The choice of embedded technology is also driven by ease of fabrication. Copper foil with a thin film of resistor material is first laminated with the resistor against the dielectric. This laminated core (Figure 3a) is supplied to the PCB fabricator. Resistors are fabricated by two-step etching process. The first step involves copper etching and removal of excess resistor material to define the width of resistors and conductor traces (Figure 3b). The second step involves copper etching over resistor areas to define the length of resistors (Figure 3c). These subtractive processes utilize standard chemistries, equipment, and processes familiar to PCB fabricators thus allowing them to leverage their existing capabilities. After electrical test, the known-good innerlayer core is laminated into a multilayer board (Figure 3d). After drill, desmear, plate, and solder mask, the board is electrically tested again to insure that the final resistance values in the board are within specified tolerances.
Figure 4 shows a cross-section image of the embedded resistor with copper pads on each side. The image also shows two different glass weaves of the glass-reinforced epoxy material used in the board construction.

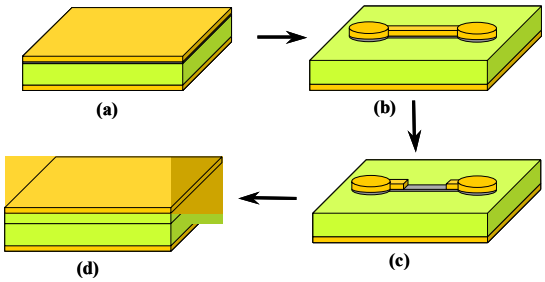


Figure 3 – Subtractive Circuitization Process for Embedded Resistors

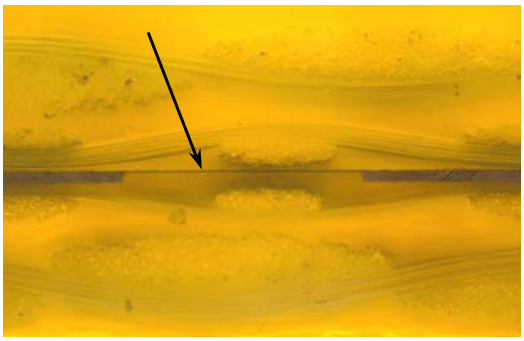


Figure 4 – Cross-Section Image of an Embedded Resistor (Indicated by Arrow)

Resistor Design

Equation 1 shows that resistance value (R) is determined by the L/W ratio but is independent of the absolute L and W dimensions. The actual dimensions are determined by the power dissipation and tolerance requirements as described below.

When current flows through a resistor, it generates heat ($=I^2R$) which causes a temperature rise in the resistor. This temperature is dependent upon how effectively the heat is dissipated through the board and to the ambient environment. The heat dissipation away from the resistor depends on the resistor size and board construction. Larger size resistors are able to dissipate more heat and so the power (P) or current (I) handling requirement of the resistor determines the minimum resistor dimensions.

$$I^2(\text{milliAmps}) \,.\, R(\Omega) = P(\text{milliWatts}) \qquad (2)$$

The current is specified by the circuit design while the maximum value of power dissipation is specified as a function of resistor size, as in Figure 5 for resistors.

Equations (1) and (2) together with the data in Figure 5 uniquely define the minimum resistor dimensions L and W.

Power dissipation depends on the specific board construction, e.g. a copper plane near the resistor enhances the heat spreading and gives higher power dissipation values. Power dissipation measurements are also dependent on the test conditions and failure criterion.[9] Fig 6 shows the I-V curve for a 1300Ω resistor. The current was slowly ramped up and the voltage measured. The slope of the linear portion of the curve in Figure 6 gives the resistance value. The slope (ie. resistance) changes beyond 125V and then the current abruptly falls to zero at failure. The cause of failure is thermal disintegration of the epoxy in the vicinity of the resistor. In this case, the failure criterion was taken as 90% of the Voltage at which the curve changed slope. This data feeds into Figure 6.

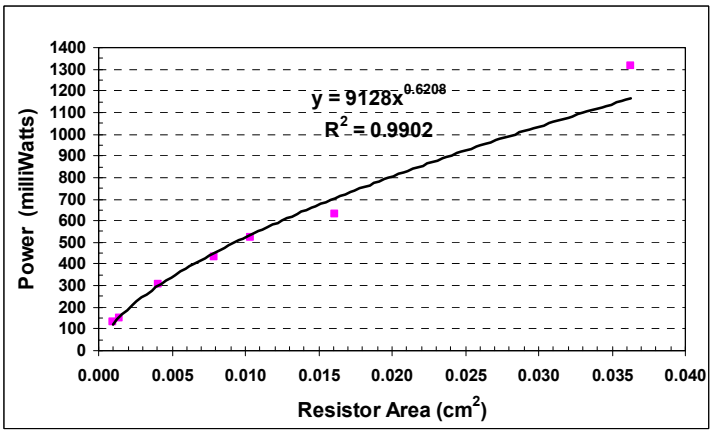


Figure 5 – Maximum Power Dissipation as a Function of Resistor Area for Resistor Material

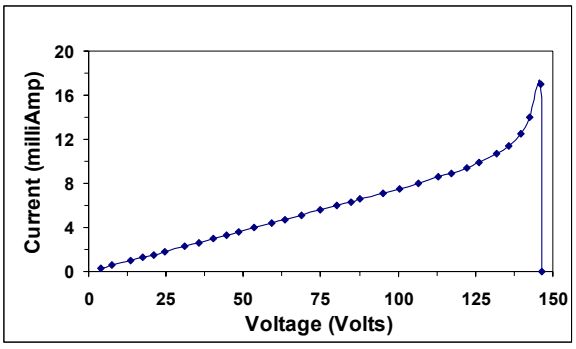


Figure 6 – I-V Curve of a 1300Ω Resistor in a 6-Layer Board with Copper Plane Adjacent to the Resistor Layer

According to the data in Figure 5, a resistor with high power handling specification of 1000mW will require relatively large resistor dimensions, e.g. L, W = 70mils for a square resistor. Accommodating such large resistor dimensions on an existing power or ground layer can be challenging. Thus, practical space constraints can limit the maximum resistor dimensions or the maximum resistance value, depending on the power handling requirements.

On the other hand, the data in Figure 5 shows that a resistor with low power handling specification of 100mW will require relatively small resistor dimensions, e.g. L, W = 10mils for a square resistor. For such small resistor dimensions, the design values of L and W are determined more by resistor tolerance (or uniformity) specifications, as described in the next section.

Resistor Tolerance

Resistance tolerance (or uniformity) data was obtained from thousands of resistors distributed over an 18"x24" board. Figure 7 shows sample resistance distribution of 500Ω/□ resistors in a multilayer board with 6σ uniformity < ±15%.

The data in Figure 7 is for a test artwork that includes a wide range of resistance values and dimensions. This particular board was fabricated at a relatively modest, prototype fabrication facility at Shipley. Tighter resistor distributions < ±10% have been obtained but the data in Figure 7 is meant as a lead-in to a discussion on how variations in the fabrication process can dramatically affect the achievable resistance uniformity, depending on the resistor dimensions. For example, an etch variability of 0.5mils, will account for 10% of tolerance budget for 5mils resistor dimension, 5% of tolerance budget for 10mils resistor dimension, and only 2.5% of tolerance budget for 20mils resistor dimension. The following discussion analyzes this effect in more detail.

Eq. 1 can be modified to:

$$\Delta R/R = \Delta\rho/\rho + \Delta L/L - \Delta W/W \qquad (3)$$

The overall resistance uniformity or tolerance (ΔR) is a combination of:

- Variations in material resistivity (Δρ) from the deposition and core lamination processes – this is controlled by material supply to the board fabricator
- Variations in resistor dimensions (ΔL, ΔW) from the etching processes – this is controlled by the board fabricator

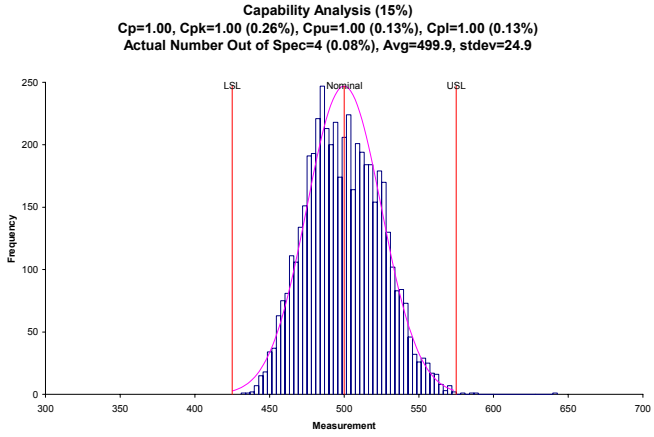


Figure 7 – Resistance Uniformity Data

Board fabricators add etch factors to the artwork based on the copper weight (1oz or 1/2oz) and their process capability. Etch factors make the resistor width larger and the resistor length smaller on the PCB artwork. Even with the etch factors, there are still etch variations from the center to the edge of a panel, and between panels. Again, these variations will represent a larger error for smaller size resistors.

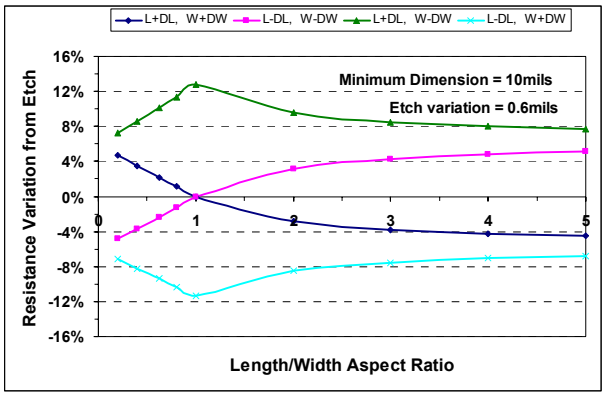
Figure 8 a-d illustrate the impact of etch variation on calculated resistance variation ΔR, as a function of aspect ratio. In each plot, the width is held constant at minimum dimension for aspect ratio >1 and the length is held constant at minimum dimension for aspect ratio <1. In each case, the maximum impact on resistance variation is for resistors with aspect ratio = 1 which has the minimum dimension of 10mils on both length and width.

Each figure shows four possible combinations of etch variations, ±ΔL and ±ΔW, as can be expected from board fabrication processes. When the etch variations are in the same direction, ie. both positive (dark blue curves) or both negative (pink curves, the impact on resistance variation is relatively smaller. In the special case of aspect ratio = 1, the two effects fortuitously cancel each other with no impact on resistance variation. When the etch variations are in opposite directions (green and light blue curves), the impact on resistance variation is relatively larger.

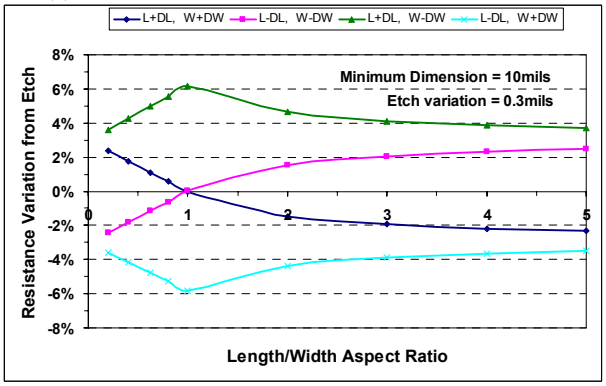
Figure 8a shows the impact of a ±0.6mils etch variation (as found at a typical board fabricator), for minimum resistor dimension of 10mils. Up to 8 – 12% variation in resistance values could be caused just by etch variations. This is in addition to variation in material resistivity.

Figure 8b shows the impact of a ±0.3mils etch variation (as found at a higher-end board fabricator). The maximum variation in resistance values is reduced to 4 – 6%. Figure 8 c and d show that the impact on resistance variation can be further reduced if the minimum dimension is increased to 20mils.

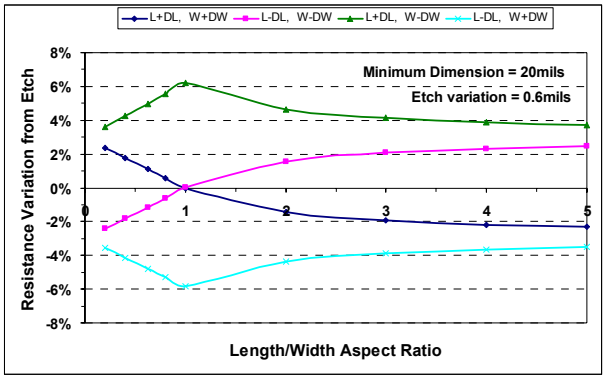
The material supplier specifies the tolerances on material resistivity ($\Delta\rho_s$) and this has to be added to etch tolerances from the board fabricator to get the total resistor tolerance. Designers need to understand the trade-offs between resistor size and tolerance, based on the process capability of the board fabricator. Successful implementation of embedded resistors requires a cohesive effort between the material supplier, board fabricator, and designer to achieve the desired performance.



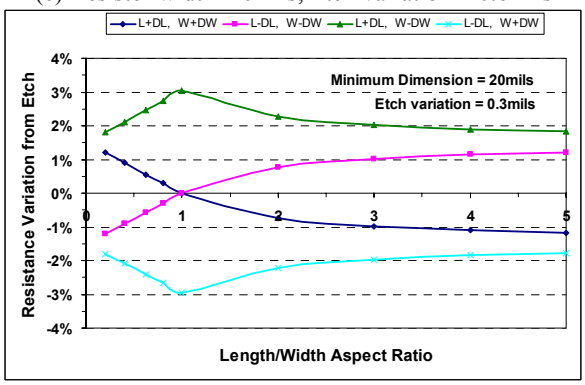
(a) Resistor width=10mils, Etch variation = 0.6mils



(b) Resistor width=10mils, Etch variation = 0.3mils



(c) Resistor width=20mils, Etch variation = 0.6mils



(d) Resistor width=20mils, Etch variation = 0.3mils

Figure 8 – Resistance Variation Resulting from Etch Variation, as a Function of Resistor Aspect Ratio for

Capacitor Material

The methodology described earlier for embedded resistors can also be applied to embedded capacitor selection. Two types of thin-film capacitor materials are in development: SiO_2 paraelectric material and ceramic ferroelectric material. In general, paraelectric materials have lower dielectric constants and are more stable with temperature, frequency, and voltage, whereas ferroelectric materials have higher dielectric constants and tend to vary with temperature, frequency, and voltage. Additional information on these dielectric materials have been presented by Ulrich and Schaper.[2]

The low inductance of thin-film dielectrics is well-suited for decoupling capacitors for low-impedance power supplied to high-speed digital circuits. It enables fast switching of required large currents at low supply voltages, and with reduced EMI. The combination of low dielectric thickness ($d < 1\mu m$) and high dielectric constant ($Dk > 100$) of the ceramic film results in high capacitance density around 1300 nF/inch^2 or 200 nF/cm^2 or 2000 pF/mm^2.

$$C/A(nF/cm^2) = 8.85 \times 10^{-5}(nF/cm).Dk / d(cm) \qquad (2)$$

For a given dielectric material, the total available capacitance depends on the total available board area. The high capacitance density allows fabrication of embedded decoupling capacitors in the range 100's pF to 100's nF, in a relatively small area. The lower limit is determined by etch tolerances while the upper limit is determined by available area. For example, in a module of size 0.5cm^2, a layer of high-Dk capacitor material can supply total 50nF capacitance, assuming 50% available area.

The high-Dk embedded capacitors will be implemented as discrete capacitors connected to specific devices in the IC. Figure 9 shows the schematic of an embedded discrete capacitor. In contrast, lower capacitance density materials are implemented as distributed or shared capacitive planes where multiple devices being switched simultaneously draw from the same charge reservoir.

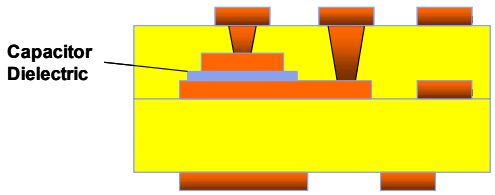


Figure 9 – Schematic of an Embedded Discrete Capacitor

Figure 10 illustrates the capacitance value distribution in a typical mobile phone design. The red arrow represents the range of embedded capacitance values achievable by the high-Dk capacitor material. Since the capacitance values cover a range of 6 decades (pF's to µF's) in many applications, it is likely that a couple of different embedded capacitor technologies will be utilized for different ranges.

As in the case of resistors, the importance of capacitor tolerances in embedded technology selection depends on the function of the capacitor in the circuit. Typical SMT capacitors used for decoupling have wide tolerance windows of ±10 to 20%. In many cases, decoupling capacitors can simply be specified as "greater than some minimum value". In contrast, lower value capacitors (<100pF) used for filtering or impedance matching require tighter tolerances (±5 to 10%). Capacitor tolerances include variations in dielectric constant in addition to physical dimensions of dielectric thickness, and metal length and width. Unlike resistors, embedded capacitors in boards cannot be easily trimmed and it would be challenging to meet tight tolerances in production.

The high-Dk embedded capacitor technology is still in the development phase but results so far have been very encouraging. Figure 11 shows high capacitance density values of 220 – 260 nF/cm^2 and low loss tangent of 0.010 – 0.015. The dielectric constant and loss tangent are stable over the ±5V bias range, adequate for low-voltage portable applications. Figure 12 shows leakage current <10^{-7} Amps/cm^2 up to breakdown around 45Volts. Again, this is adequate for low-voltage portable applications. Additional characterization of the dielectric properties as a function of frequency, temperature, and voltage are planned.

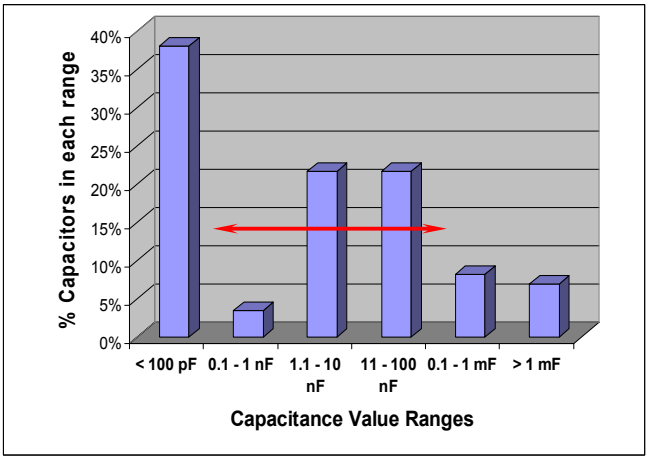


Figure 10 – Capacitance Value Distribution for a Mobile Phone Design (Private Communication)

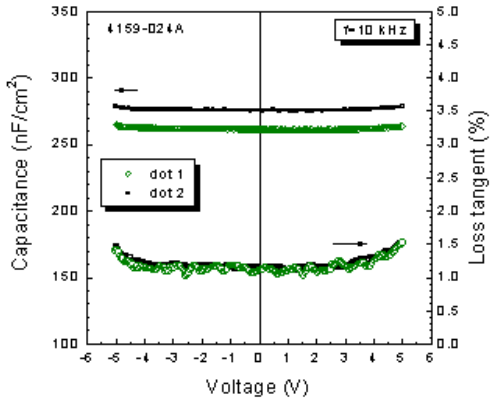


Figure 11 – Data of Capacitance Density and Loss Tangent as a Function of Bias Voltage for high-Dk Material.

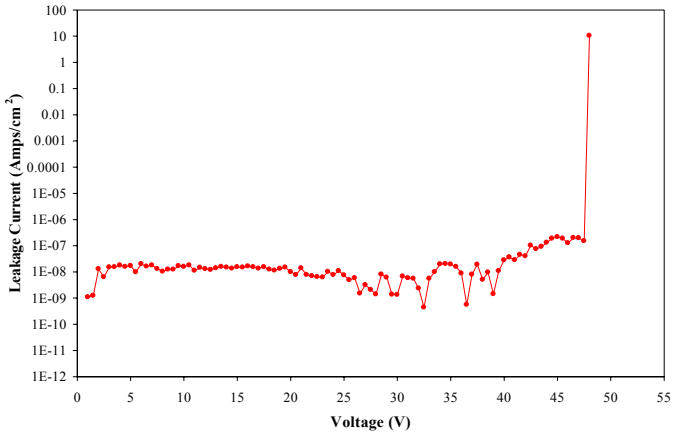


Figure 12 – Leakage Current and Breakdown Voltage Data for high-Dk Material

Total Cost Tradeoffs

The cost of embedded passive materials, process, test, and yield add to the final bare board cost. The cost per unit area of a board containing embedded passive components will always be higher than a board without embedded components. Since cost per unit area is a common metric in the procurement of boards from fabricators, this presents one of the most formidable barriers to market penetration of embedded passives. Many of the cost benefits of embedded passives are realized further up the value chain (e.g. assembly) and so a systems-level cost analysis is required to capture these benefits.

The following are some potential cost benefits of embedded technology:

1. Reduced SMT component cost
2. Reduced SMT assembly cost
3. Reduced parts count and inventory costs
4. More boards/panel with reduced board area
5. Reduced layer count from less routing
6. Improved assembly yield with fewer solder joints

Some cost benefits can be easily quantified (1-2) but many benefits are not easily quantifiable in a generic sense (3-6) and require cost modeling on a case-by-case basis to determine the cost effectiveness of embedded technology for that application. Many cost models for embedded passives have been reported in the literature with varying degrees of complexity.[10-12]

A very simple break-even cost analysis that has been around for a long time is shown in Figure 13. It is based on the number of embeddable components per unit area on a board and only considers the benefits of reduced component and assembly costs. In Figure 13, the cost of an assembled 0402 or 0603 discrete component is assumed to vary from 1.1 cents in higher volumes (>1M) as shown by the solid green line, to 2.5 cents in lower volumes (>10K) as shown by the solid red line. The horizontal dashed lines represent a range of incremental cost of embedded material, process, and test (not including trimming). The intersections of these lines represent the cost break-even points.

Depending on the assumptions used, the break-even component density is approximately 5 to 20 /inch2 or 1 to 3 /cm2. Note that it is important to make similar assumptions for SMT and embedded scenarios in order to insure a fair comparison. For example, the very low cost of assembled discrete components is only valid in very high volumes but new embedded technologies recently introduced in the market are often priced for low initial volumes. As the production volumes ramp up and economies of scale kick in, the price of these embedded technologies will come down (as in the case of manufacture and assembly of discrete SMT components). Decision-makers at the OEM/EMS level can work with material suppliers and board fabricators on forward pricing strategies for embedded passive technologies in order to overcome the cost barrier.

High-speed designs may utilize multiple SMT decoupling capacitors in parallel to get lower inductance and these could be replaced by a single low-inductance embedded capacitor. This scenario is represented by the dashed green and red lines in Figure 13 where 2 SMT components are replaced by one embedded component. This could significantly change the break-even analysis in favor of embedded capacitors to 0.3 to 1.8 /cm^2 component density.

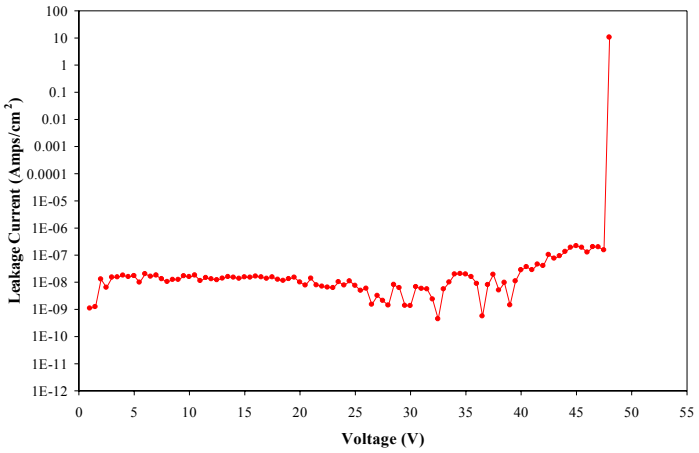


Figure 13 – Simple Break-Even Cost Analysis Based on Component Density

Summary
Designers are faced with a number of alternative embedded passive technologies at various stages of development and commercialization. The technology selection depends on performance, size, total cost, and implementation considerations.

Thin-film, high-ohmic, embedded resistor materials (500 and 1000 Ω/□) allow a wide range of resistor values to be embedded, across many applications. While it is easily implemented at a board fabricator, variations in the fabrication process can have a significant impact on the resistor tolerance, especially for smaller dimensions. Designers of embedded resistors need to understand these trade-offs between resistor size, tolerance, and capability of board fabrication processes.

Thin-film, high-Dk, embedded capacitor material (1300 nF/inch^2 or 200 nF/cm^2) enables the embedding of decoupling capacitors for power supply to high-speed circuits. Measured data shows loss tangent <0.02 and breakdown voltage >40V.

A simple cost analysis can help the initial screening of which designs are appropriate candidates for embedded passives technology based on the density of embeddable components.

Acknowledgement
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