Presented at IPC Printed Circuits Expo®
SMEMA Council APEX®
Designers Summit 04

Designing Embedded Resistors and Capacitors

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Abstract
Embedded passives, i.e., resistors and capacitors built right into the printed circuit board substrate, is a rapidly emerging and pivotal technology for the PCB industry preceded only by the plated thru hole in the 50s and microvias in the 80s.

This paper is a presentation of the design process for embedding discrete resistors and capacitors into circuit board substrates. Materials are available in a wide range of values and technologies. The paper includes a step-by-step process for designing resistors and capacitors with a variety of materials and embedded passive technologies.

Performance, miniaturization, and cost are the drivers. The average cell phone has 445 SMT passive components at a 25:1 ratio to ICs. Embedding many of these will improve performance, enable more functionality and reduce cost per function. Embedded passives are not limited to cell phones. Many other applications will benefit from improved performance. Several materials are commercially available today and many new materials are in development. The paper also includes a brief review of these materials.

Introduction
Electronic product development organizations vary in structure, size and resources. Requirements flow down from the market, the ultimate customer; thru the various channels of product development and eventually to the designer that has to create the data output that will convert schematics and parts lists into hardware. Although this paper is focused on the designer, the engineer should take heed since designing with embedded passives is different than what we have traditionally considered the normal flow. Typical design inputs are the schematic, parts list, critical placement, preliminary stack-up, impedance, board profile, mounting, materials, finishes, and thermal requirements. The designer's task is a systematic juggling act to integrate all of the requirements into a producible and functional PC board and assembly.

So what's different with embedded passives? First, you have to design the parts. Second you have to place them where you normally don't think of placing parts. That should be easy enough. Your CAD tool should be able to do that for you. Unfortunately, there is only one CAD tool on the market today (reference 17) that is close to being able to help you do that. The odds are very good that you don't have it, and don't have the luxury of time or budget to buy it let alone learn how to use it. CAD providers are slowly developing tools.

Design Flow
Figures 1 and 2 outline the design flow process for both embedded resistors and capacitors. Unique to both of these processes is that you are not selecting parts from a manufacturers catalog, using standard pad pattern features, placing the part on the top or bottom layer of the board, interconnecting them with your auto-routing tool, or creating the appropriate silk screen designation for the assembly. You are in fact designing discrete passive components that will be manufactured integral with the printed circuit board manufacturing process. You will design these parts to specific values and tolerances. However, beyond resistance and capacitance, their performance characteristics such as TCR, stability and drift, power dissipation, and environmental resistance are beyond your control. They are determined by the chosen material set and it's compatibility with the PCB process. Said another way, they are controlled by the material supplier and strongly influenced by the PCB manufacturer.

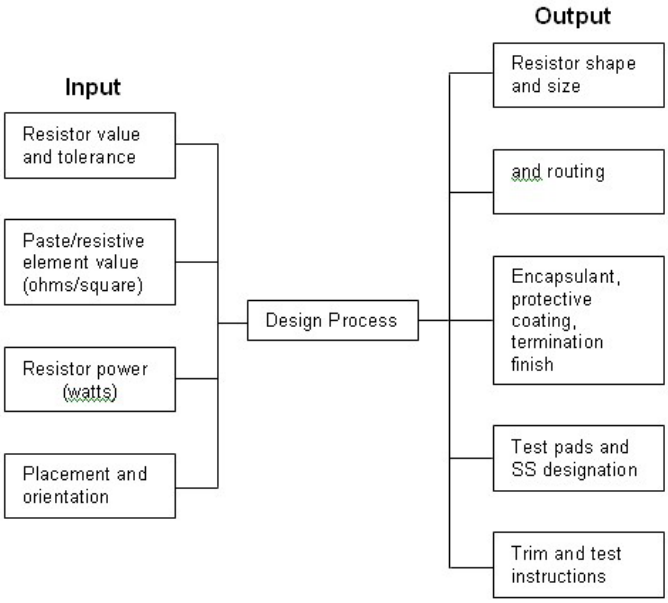

Figure 1 – Embedded Resistor Design Flow

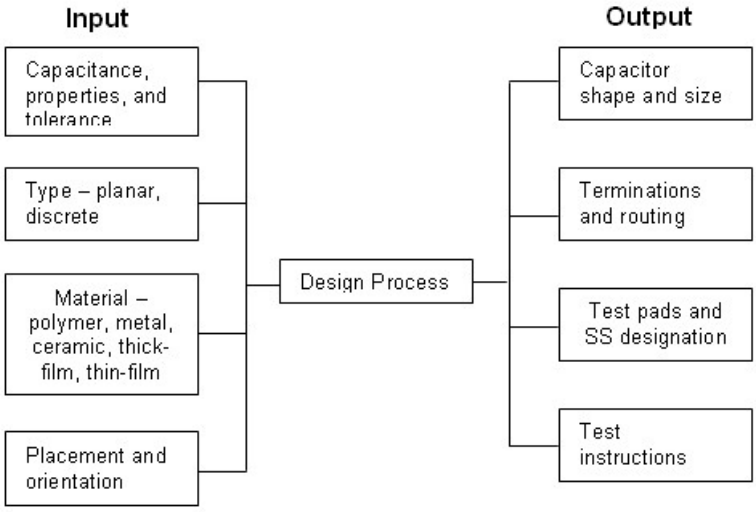

Figure 2 – Embedded Capacitor Design Flow

Decision Process

Figure 3 illustrates the major steps that project management and engineering must go through to decide whether or not, what and how to embed. Generally, selecting technology and parts is decided before the board design is started. Such is the case with embedding passives, however, since the board design process is not yet well established, it is extremely important that your engineer include you, the designer, in this decision process. This is to ensure that you will be able to achieve the desired result. However, for the purpose of this discussion, the materials have been selected by the project engineer. You will assume that he has studied the material characteristics, coordinated with you, and has made a sound choice to meet his project's needs.

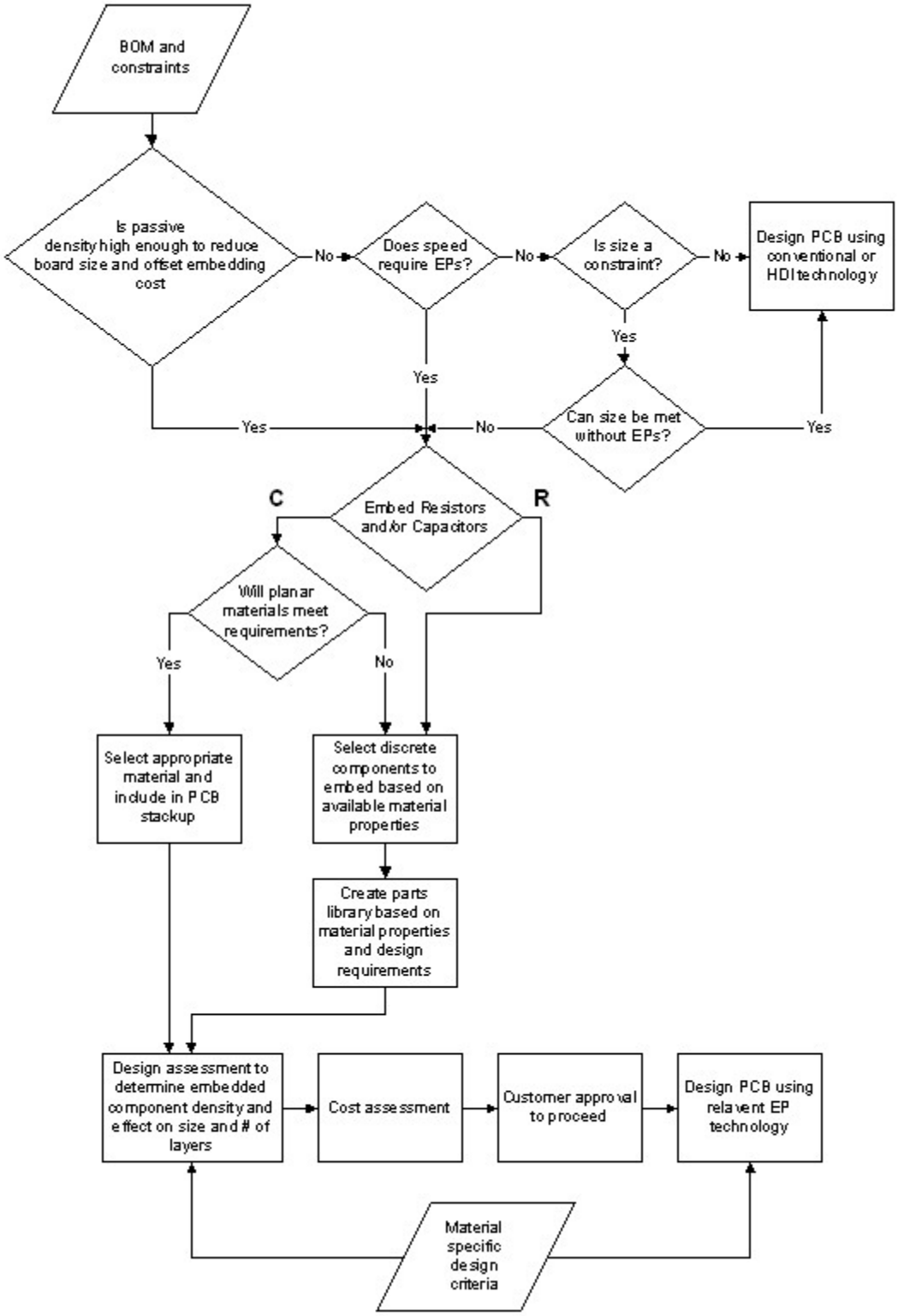

Figure 3 – The Design Decision[1]

Materials

Table 1 is a summary of the current resistor and capacitor materials reasonably available today. The ceramic thick-film materials are not quite commercialized as of this writing, but since they are so close to being commercial, I felt it was appropriate to include them.[2-5]

Table 1 – Passive Materials

Type	Description	Manufacturing process	Reference
Resistors	Polymer thick-film (PTF)	Screen print	(5), (6)
	Metal thin-film (MTF)	Etch	(7), (8), (9)
	Ceramic thick-film (CTF)	Screen print	(10)
Capacitors	Planar and low value discrete	Conventional layer etch	(11), (12), (13), (14), (15)
	Discrete ceramic thick-film (CTF)	Screen print	(16)

Design Tools

The major CAD providers all have embedded passive offerings to some degree. Some are based on modifications of existing hybrid design tools, others are tools developed specifically for embedding resistors and capacitors into circuit boards. All are in various states of usefulness. Unless you happen to be licensed for a tool that will do your job, you will have to go thru manual parts creation and manipulation of your CAD tool to place and route the parts.

Resistance

All resistor materials are provided with resistance values expressed in ohms per square.

$$R = pL/A$$

R is resistance in ohms, p is the resistivity of the material, L is the length and A is the cross sectional area (i.e., thickness times width).

When thickness is held constant then R is the same for any square area, hence the expression ohms/square. Resistance then can be varied by varying the aspect ratio of the area (L/W), as illustrated in Figure 4.

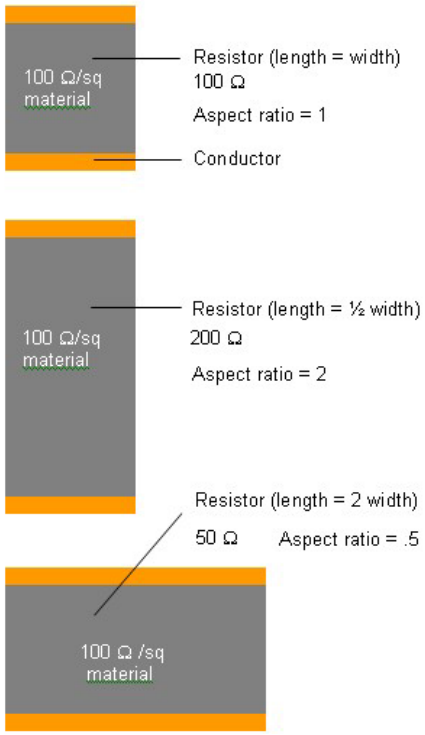

Figure 4 – Sheet Resistance Relationships

Resistors

Resistor terminations are the copper areas directly connected to the resistive material. For screen printed resistors, the termination must be designed larger than the resistor element to assure proper registration and manufacturability, see Figure 5. L and W for screen printed resistors should be 4 to 8 mils depending on the precision of the board manufacturers screening process. Some PTF screen printed resistors require that the copper be coated with an inert conductive barrier metal to prevent chemical reaction between the resistor material and the copper, see Figure 6. This feature should be 3 to 5 mils per side larger than the termination, depending on the precision of the board manufacturer. For CTF resistors, an encapsulant coating is required, see Figure 7. This image must be 5 to 7 mils per side larger than the resistor element. The design files must include these additional features for the manufacturer and the drawing must include the appropriate instructions.

For etched resistors, as shown in Figure 5, L will be zero, and W may be zero. See Figures 8, 9, and 10 for examples. A secondary etch pattern must be provided as shown in Figure 8. Length (L) is the calculated length of the resistor. Width (W) should be 3 to 4 mils. Be cautious with adjacent traces to prevent unintended removal of copper.

The resistor dimensions are determined by the ohms/square resistance of the selected material and the number of squares required to achieve the desired resistance. The use of serpentine patterns and the maximum aspect ratio should be within the limits established by the material manufacturer. Resistor values as manufactured will be in the range of +/- 25 to 40% for the screen printed materials and +/- 15 to 25% for the etched materials. These will vary depending on the board manufacturer and the precision and control of the processes. A variety of shapes can be used for resistors. Using a rectangular shape makes the resistance calculation with squares very easy.

Since terminations are formed by the conventional print and etch processes, spacing between resistors should be controlled by the copper spacing rules. Apply the same rules for via structures adjacent to resistors.

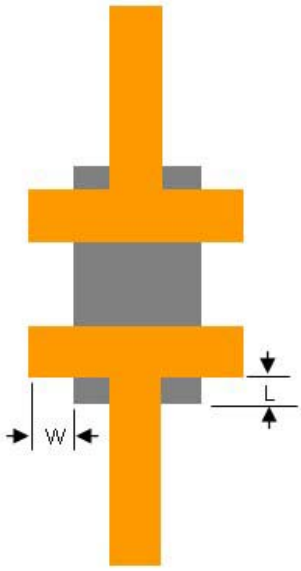

Figure 5 – Resistor Terminations

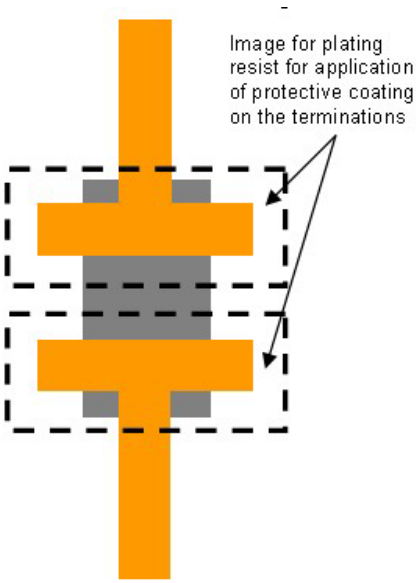

Figure 6 – Resistor Termination Coating

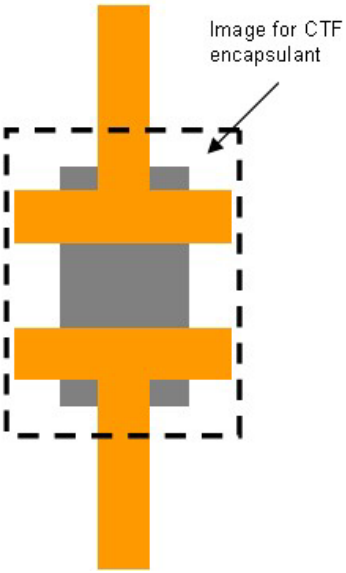

Figure 7 – CTF Resistor Encapsulant

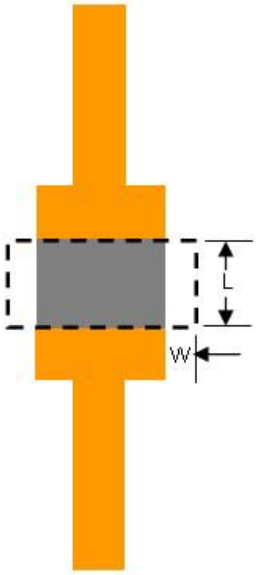

Figure 8 – Etched Resistor - T

Figure 9 – Etched Resistor – In Line

Figure 10 – Etched Resistor - Serpentine

Trimming

Where more precision is required, laser trimming must be used. Since resistors are "trimmed-up" to value, the design dimensional features must be based on approximately 30% lower value to allow for trimming. This means that the resistor element will be 30% wider than the nominal square calculation. Trimming can be a costly process. A systematic repetitive pattern of resistors and probe pads should be used where possible to minimize the number of probe cards required and the thru-put time. Probe pads should be proximal to the resistors. Because probe tip diameters are from 6 to 15 mils in diameter, probe pads must be a minimum10 to 20 mils larger. The larger the resistor, the more precisely it can be trimmed. Laser spot sizes are from 1 to 7 mils depending on the subject materials being trimmed.

Capacitance

Capacitance of a parallel plate capacitor is directly proportional to the plate area (A) and the dielectric constant (Dk) of the dielectric material and inversely proportional to the thickness (T) of the dielectric. When working in nF/in^2, a constant of 0.2247 must be used. I.e., C = (0.2247 X Dk X A)/T expressed in nF/in^2. Dks of planar materials range from 3.1 to 23 and thicknesses from 2.0 mils to 0.5 mils, giving a capacitance density range of approximately 0.5 to 8.6 nF/in^2.

The primary benefit of the ceramic material is it's high Dk, which enables a capacitance density of 560 nF/in^2. Given this property, it is possible to design discrete capacitors from approximately 60 pF to 100 nF.

Planar Capacitors

To the best of my knowledge as of this writing, none of the CAD tools calculate the effective capacitance area of opposing copper planes. Although this is not hard, the logic is sometimes elusive and the task is clearly laborious. The copper of one plane contributes as a plate of the capacitor only if it has copper facing it on the opposite plane. The smaller area of those plates determines the capacitance. To determine this requires a lot of arithmetic; measuring, calculating areas, counting and multiplying. The following formula is very detailed, since from previous discussions with designers, I have learned that it is important to explain it in such detail. If this is too much, please skip over it.

See Figure 11. From these, establish the following relationships:

A_{OT} = Overall area of the top plane

A_{OB} = Overall area of the bottom plane

A_{OS} = The smallest overall area of the plane (the lesser of A_{OT} or A_{OB})

A_{VAP} = The sum of the areas of all thru hole and via antipads (all holes and vias thru the planes will have a clearance (antipad) on at least one plane. The effect on capacitance is equivalent to 1X the clearance area for all holes and vias. This area should be subtracted from the A_{OS}.)

A_{CR} = Area of common rectangle top and bottom (i.e., same area, same location on both planes)

A_{URT} = Area of unique rectangle top (i.e., not common with the bottom plane)

A_{URB} = Area of unique rectangle bottom (i.e., not common with the top plane)

From these relationships, compute the area of the capacitor, A_C where:

$$A_C = A_{OS} - (A_{VAP} + A_{CR} + A_{URT} + A_{URB})$$

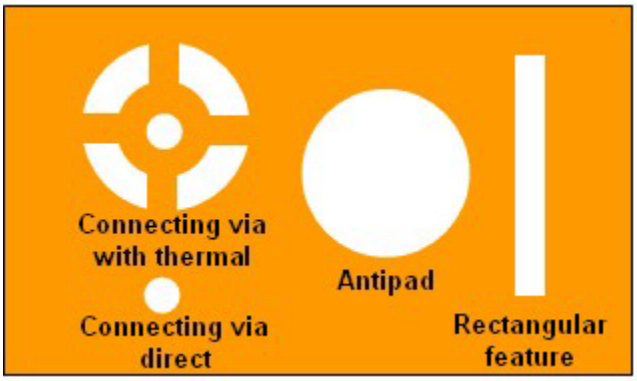

Figure 11 – Top and bottom "No Copper" Plane Features
(Overall area of top and bottom may be common or unique)

The capacitance for the planar capacitor is the product of the area A_C and the capacitance density of the material. The area units must be the same. For example, if the planar material has a capacitance density of 1.0 nF/in^2 and the calculated area (A_C) is 150 in^2 then the capacitance of the plane pair is 150 nF.

Discrete capacitors
Discrete capacitors may be created using planar materials. They may also be designed within a large planar capacitor.

Conclusions
Today we can design and manufacture resistors embedded within the PCB substrate. As new materials are being developed, the design process remains very manual, and manufacturers are learning more and more about these materials. Since standards and CAD tools are practically non-existent many questions still have to be answered, such as:

- What is the shape of the parts?
- What are the smallest feature sizes possible?
- What is the accuracy of a screened part?
- How many resistors can be placed on a layer?
- How to size for power requirements?
- When is trimming required?
- How to specify the trimming?
- How much should the pattern be oversized to allow for trimming?
- How does the embedded passive material affect the minimum dielectric thickness that can be used?
- What copper weights should be specified?
- What layers should the embedded passive parts be placed on?
- What termination pattern should be used?
- What is the size of the terminations?
- Are there conductor to passive part minimum spacing requirements?
- How are the required pastes to use specified?
- Does this process affect layer-to-layer registration?
- How do the part names relate to the BOM and schematic?
- How many planes can be tied together to increase capacitance?
- How much space is required between discrete capacitors?
- Can discrete capacitors share a common plate?
- What is the layer naming convention?
    - Resistor patterns
    - Capacitor patterns, dielectrics and conductors –
    - (single layer and multiple layers)
    - Encapsulant patterns (first and second)
    - Termination patterns
    - Copper termination layer and trim test points
- Which detail layers must be merged to provide tooling for the board manufacturer?

The list could go on and on. Time and the space available in this paper do not permit a complete set of design guidelines. These are being made available by PCB manufacturers and material suppliers as broadly and quickly as possible to assist designers in bridging the gap between now and when the CAD providers develop tools for creation of library parts, placement and routing.

References

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“Designing Embedded Resistors and Capacitors”

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Agenda

- Introduction
- Design Flow
- Decision Process
- Materials
- Design Tools
- Resistance
  - Resistors
- Capacitance
  - Planar capacitors
  - Discrete capacitors

Introduction

“Integrating passive components directly into the circuit board is a well-established idea but an immature practice”

Richard Ulrich

“Integrated Passive Component Technology” 2003

Pivotal PCB Events

- 50s PTH
- 80s Microvia
- Today EPs

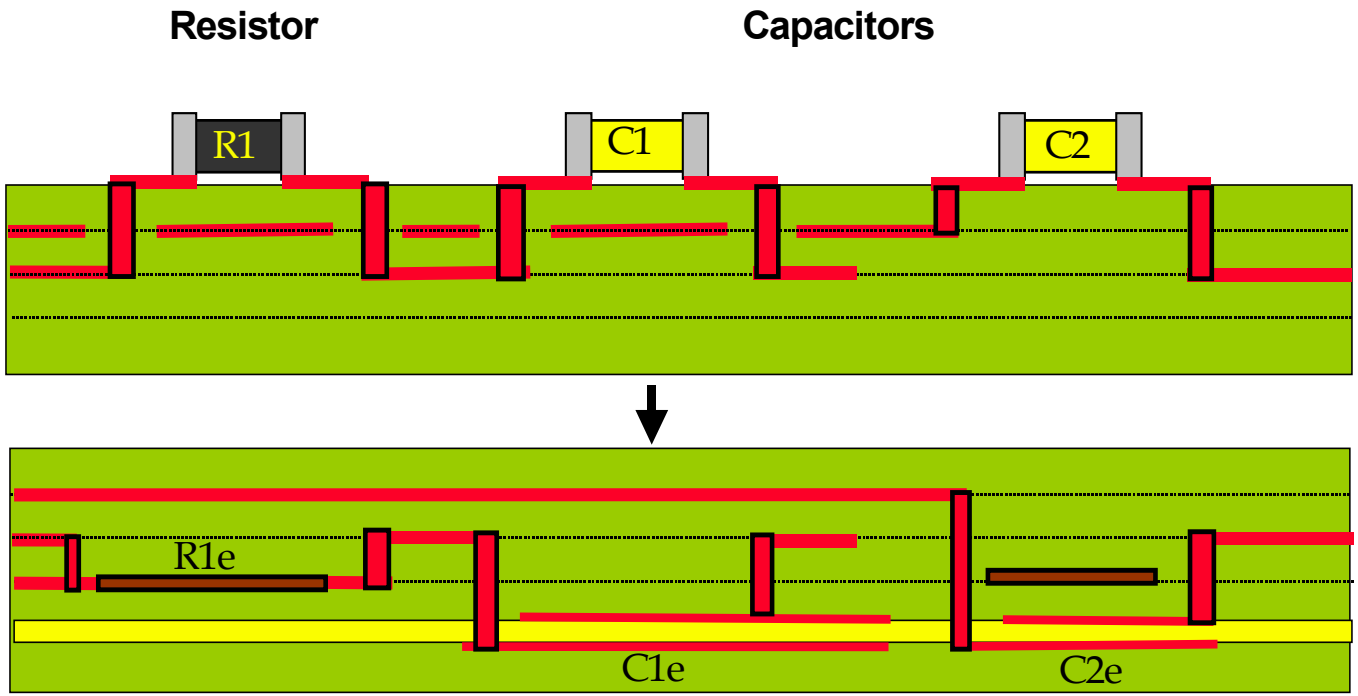
What are Passive Components?

- Resistors and capacitors (for this discussion)
- Provide/absorb energy
  - Maintain constant V or A
- Filter signals
- Control impedance
- Sense signals
- Delay or synchronize signals

Types of Passives

- Traditional Discrete Passive Components - SMT
- Passive Arrays
  - Multiple passive components, like function, shared substrate and package, mounted on a PCB
- Integrated Passives
  - Multiple passive components
  - May be embedded in the PCB substrate
  - May be on the surface of the PCB in a package
- Passives on the IC
- Embedded Passives
  - Passive components embedded in the PCB
  - May also be discrete components embedded in the PCB

Embedded Passives Singulated Construction

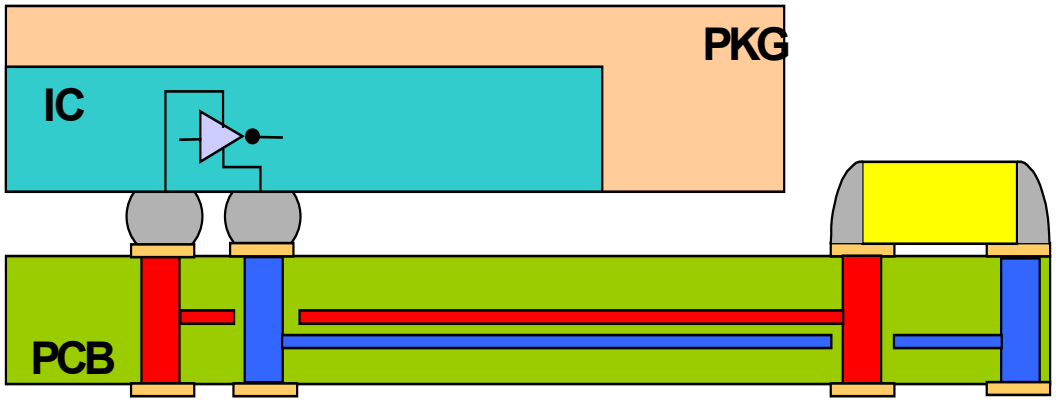


SMT passive components

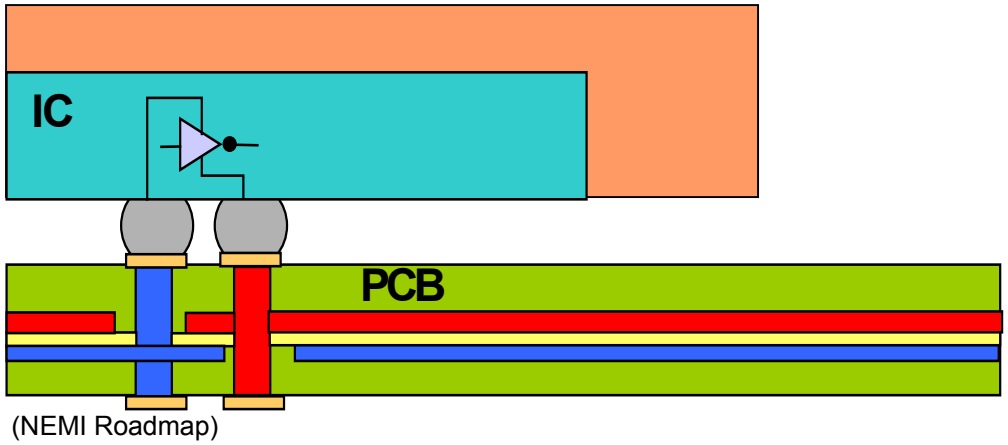
Embedded integral passives components

(NEMI Roadmap)

Embedded Capacitance – Planar Construction



Discrete SMT Decoupling



Embedded Planar Decoupling

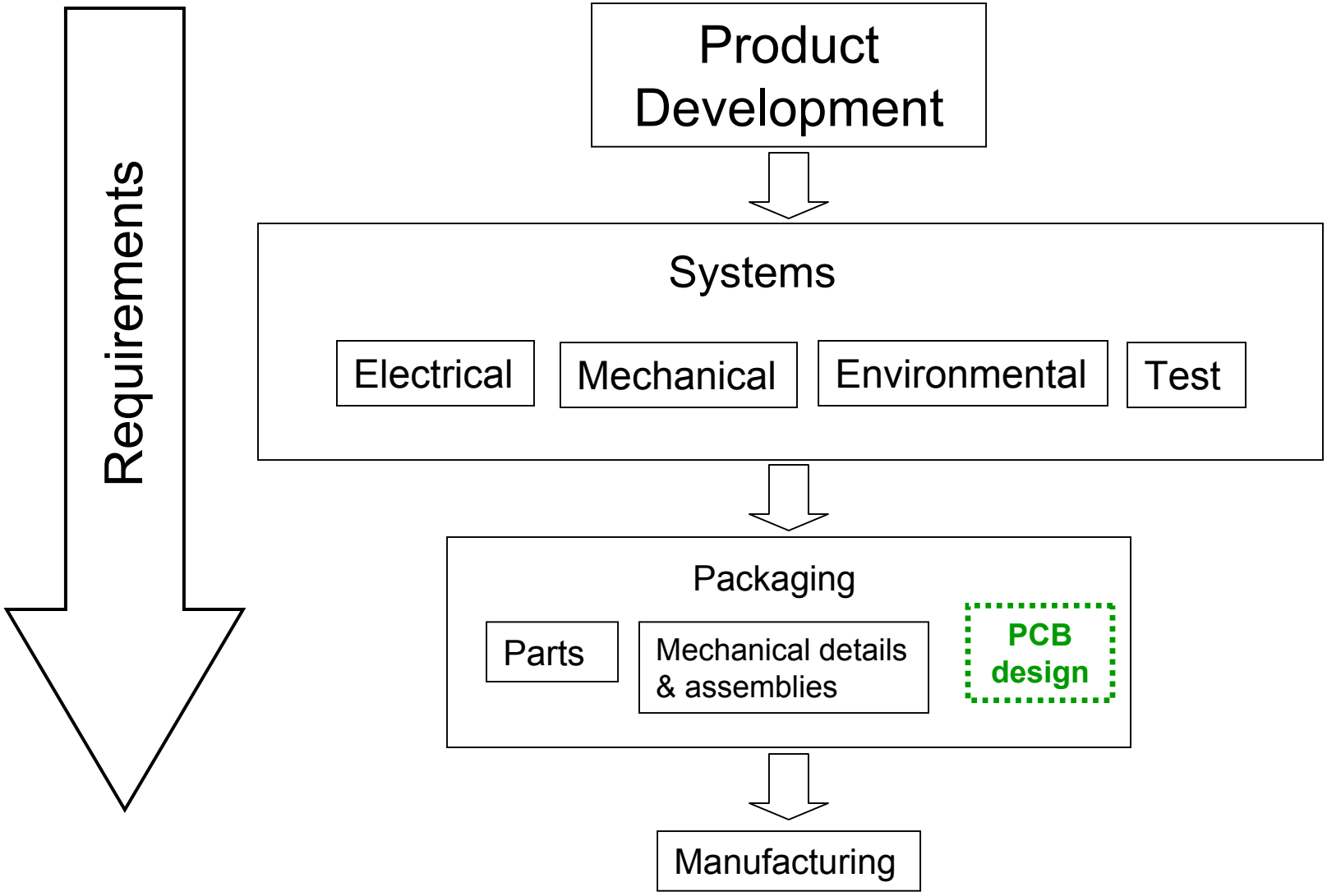
(NEMI Roadmap)

Product Development

Market

Requirements

Cost	Weight
Performance	Environment
Producibility	Life
Size	Regulatory


Requirements
Product Development
Systems
Electrical
Mechanical
Environmental
Test
Packaging
Parts
Mechanical details & assemblies
PCB design
Manufacturing

What's Different?

- Embedded passives are new materials
- Materials incorporated into the board during manufacture
- Part of the PCB structure or substrate
- Either internal or near surface of board
- Forms -
  - Laminate/foil
  - Paste/liquid
  - Plated
  - Thin-film metal

IPC Standards Activity – New Materials

- D-37A – Design (Kim Fjeldsted, ESI)
  - Initial stages, working on design guideline
- D-37B – Materials (Dave McGregor, DuPont)
  - IPC-4902 - Developed classification system, qualification and conformance test tables and slash sheet
- D-37C – Performance (Bob Greenlee, Merix)
  - Completed inputs for inclusion in IPC-6012, waiting completion of IPC-4902
- D-37D – Test (Jan Obrzut, NIST)
  - Current test methods not suitable, developing new test methods

New Materials

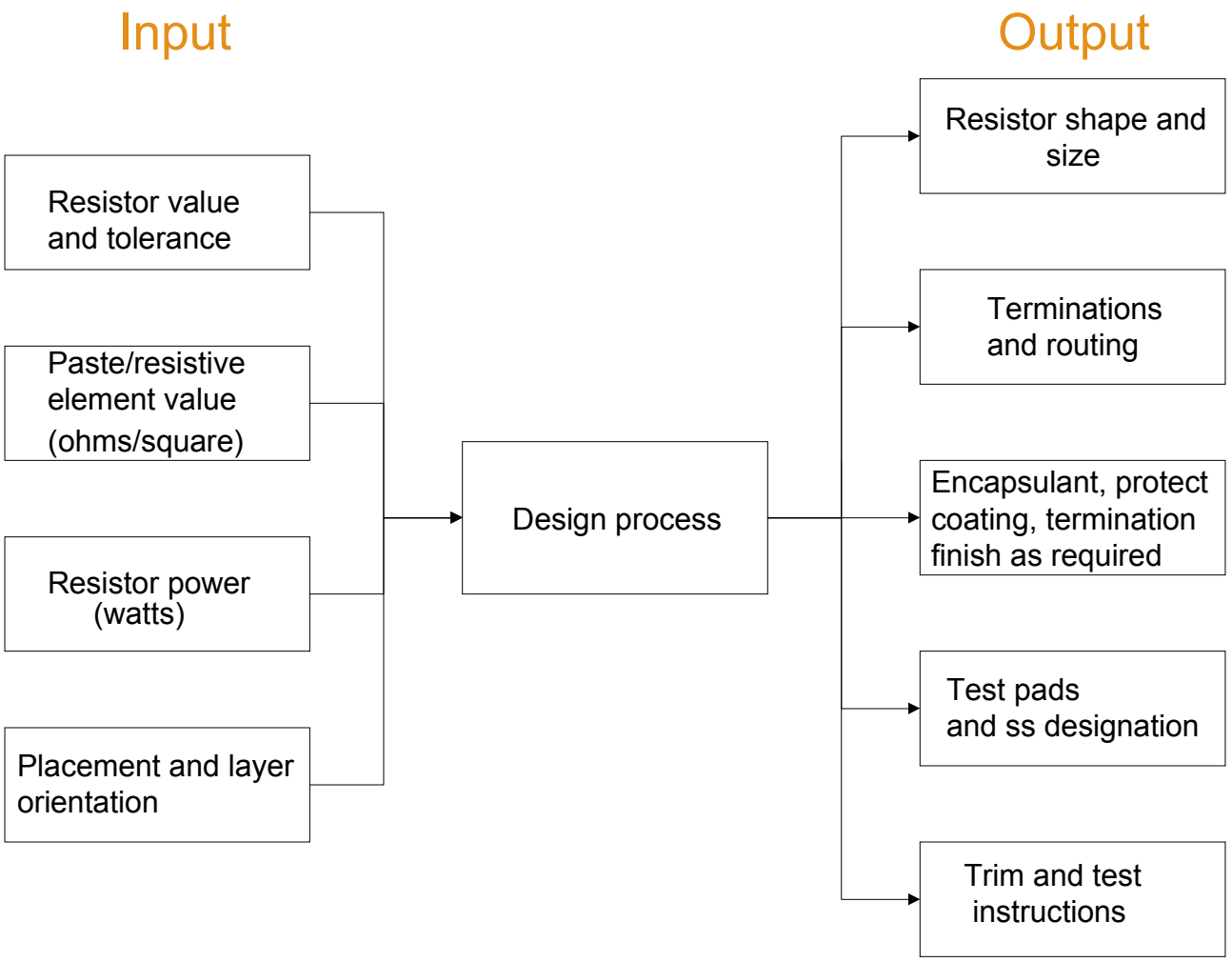
- New material introduction over the years
  - Screened mask to LPI
  - Low Tg FR-4 to 170 Tg FR-4
  - ED foil to TCE foil
  - Reflowed SnPb to HASL to ENIG
- Easy implementation by design activity
  - Change a drawing note here and there

Design What?

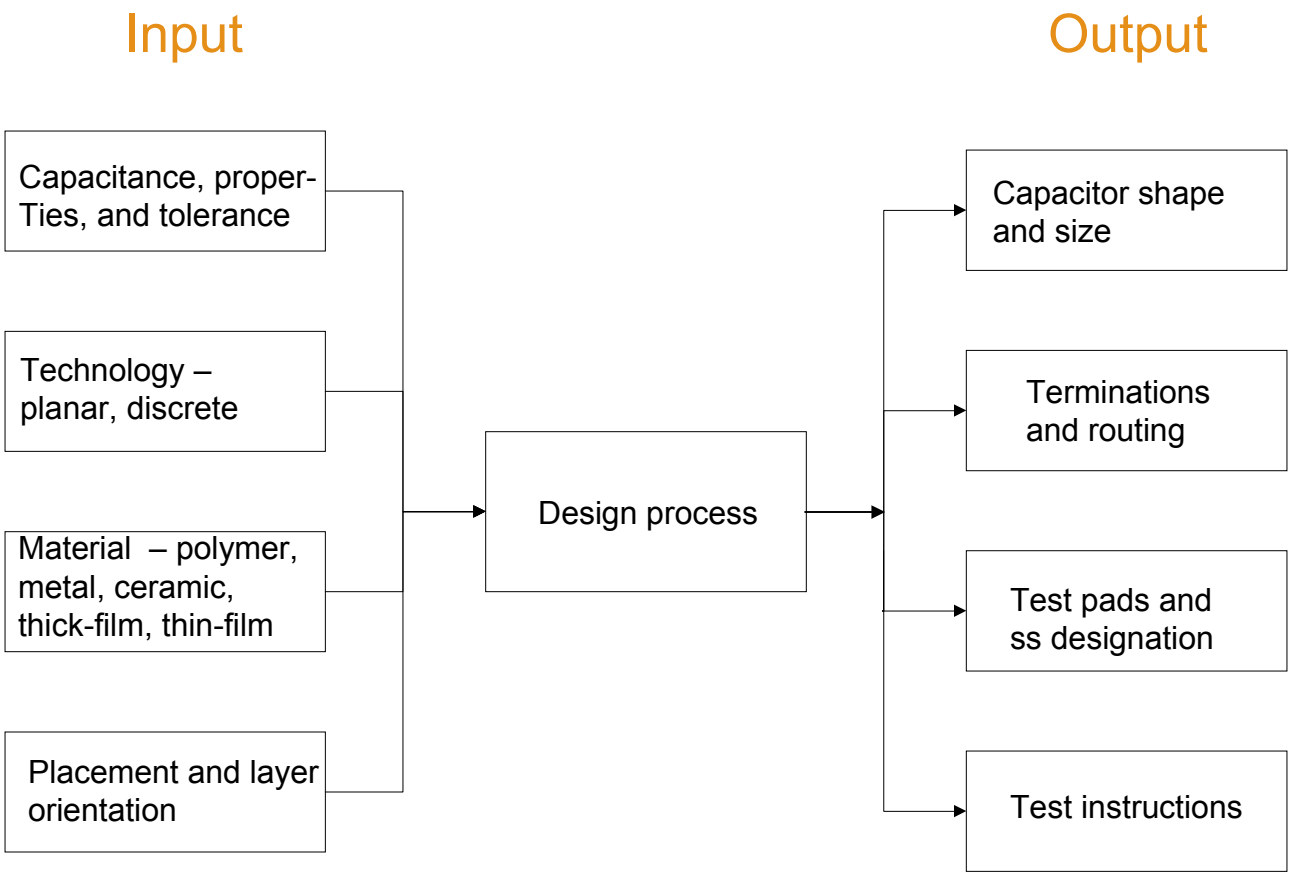
- Note title, “Designing Embedded Resistors and Capacitors”
- Not, “Designing with …….”
- Parts have to be designed
  - Manufacturing process affects the design
  - Libraries have to be created
- Parts have to be placed *(where you normally do not place parts)*

Design Flow

Embedded Resistor Design Flow



Embedded Capacitor Design Flow

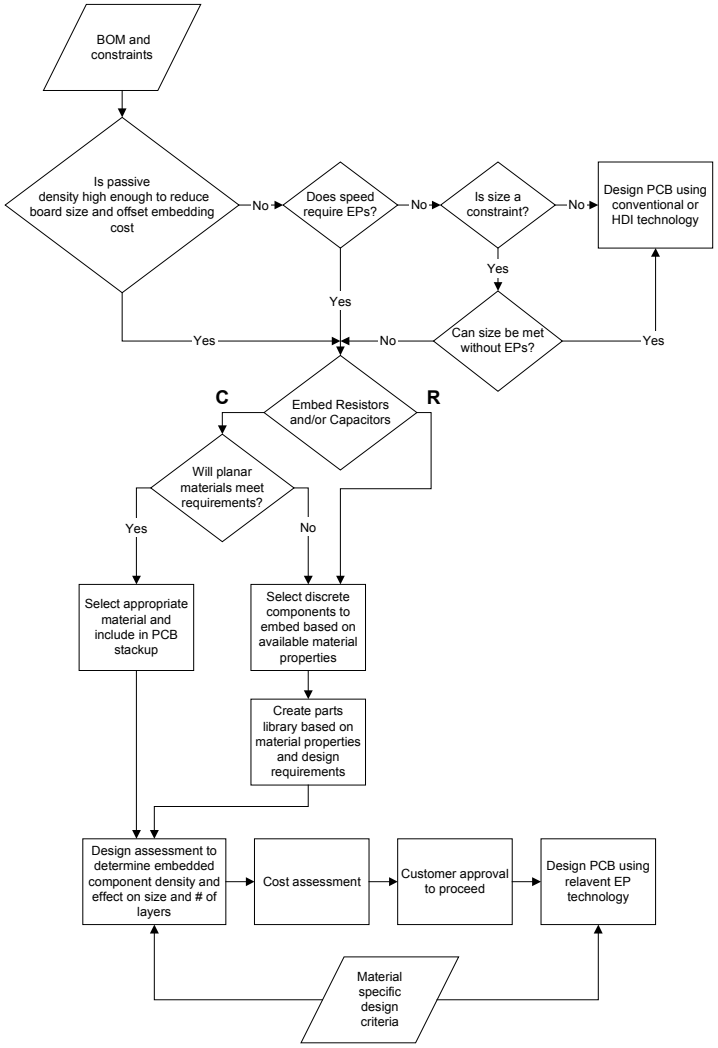


Design Flow

- No standard parts, pad patterns, placement rules
- Design discrete components
  - To be manufactured by the IMS (PCB shop)
  - From new and unique materials
- Design to values and tolerances are in your control
- Component characteristics are out of your control
  - TCR, TCC, Drift, Stability, Voltage breakdown, Power dissipation, environmental resistance
    - All a function of the chosen material
    - May be influenced by the manufacturing process
- Material selection is critical

Decision Process

Selection Process



The design decision

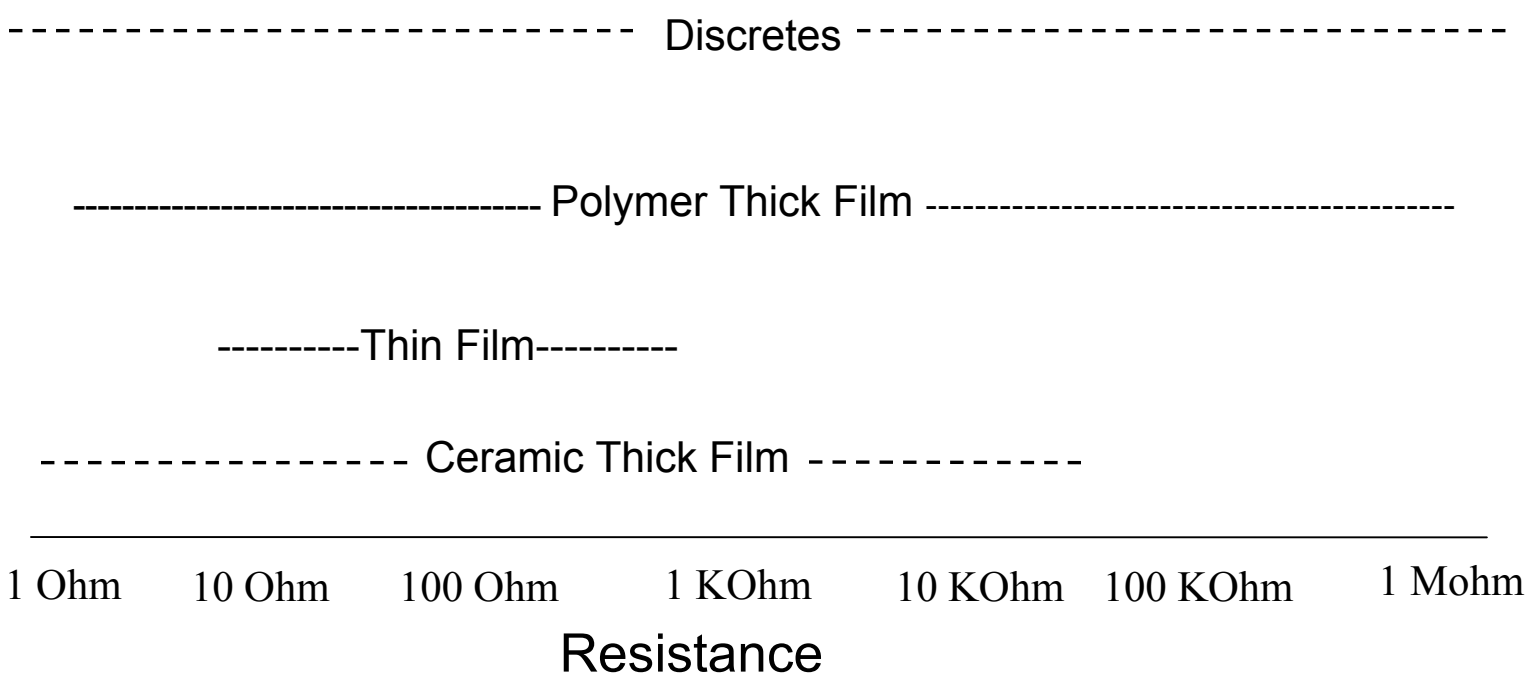
Selection

- Typically – parts selection decided before PCB design is started
- Will this be the case with EPs?
  - Engineer should include designer in decision process
  - Ensure that desired result is achievable

Materials

Materials for Embedding Resistors

Assumes aspect ratios of 1/8 to 8 squares



Resistor Requirements

(Tolerance; and Stability to Frequency, Voltage, Temperature and Time by Application)

Application	Tolerance	Stability
Digital	Low +/- 10%	2%
Analogue	High +/- 1%	2%

1 Ohm 10 Ohm 100 Ohm 1 KOhm 10 KOhm 100 KOhm 1 Mohm

Range of Resistance

Resistor Materials

PROCESS	TECHNOLOGY	MATERIAL SUPPLIER
Photoprint (Sheet resistor material)	Thin-film (NiCr)	Gould Electronics
	(Pt)	Rohm & Haas Electronic Materials
	(NiP)	Ohmega Industries
Screen or stencil print	Polymer thick-film (PTF)	Acheson Electronic Materials
		Asahi Chemical
		Electra
		Metech
		MIE

Resistor Materials – Under Development

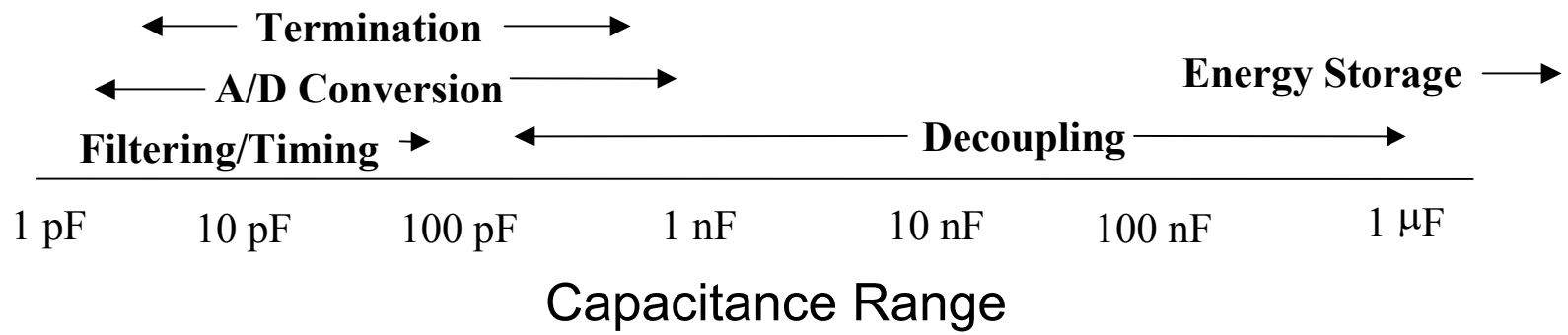
PROCESS	TECHNOLOGY	MATERIAL SUPPLIER
Plating	Thin-film (NiP)	MacDermid
Screen-print	PTF and CTF	DuPont
Inkjet	PTF	MicroFab Technologies

Capacitor Requirements

(Tolerance; and Stability to Frequency, Temperature and Time by Application)

Application	Tolerance	Stability
Filtering/Timing	Moderate	Moderate
A/D Conversion	Very high	Very High
Termination	Low	Low
Decoupling	Low	Low
Energy Storage	Low	Low

* chart from paper given at HDI conference, Denver, 2000, by Ulrich et al.



Capacitor Materials

PROCESS	TECHNOLOGY	MATERIAL SUPPLIER
Etched copper planes	FR-4/glass, copper clad laminate	Sanmina - SCI and Oak Mitsui
	Polyimide (unfilled and filled) copper clad laminate	DuPont
	Polyimide (unfilled) copper clad laminate	Gould
	Proprietary dielectric (filled) copper clad laminate	Matsushita Electric Works.
	Epoxy (filled) copper clad laminate	3-M
Photoimageable discrete	Photopolymer (filled)	Vantico/(Motorola)

Capacitor Materials – Under Development

PROCESS	TECHNOLOGY	MATERIAL SUPPLIER
Photoprint	Proprietary dielectric (filled) copper clad laminate	Hitachi Kasei
	Thin-film	MicroCoating
		Rohm & Haas Electronic Matls
Screen or stencil printed discrete	CTF (ceramic thick-film)	DuPont
	PTF – (polymer thick-film)	
Photoimageable discrete	Filled dielectric (sheet), Filled photoimageable sheet	Nippon Paint

Design Tools

Tools

- Software commercially available
  - Mentor Graphics (with DDE)
  - Zuken
  - Cadence
- Cadence and Mentor have major share of design tools in U.S.

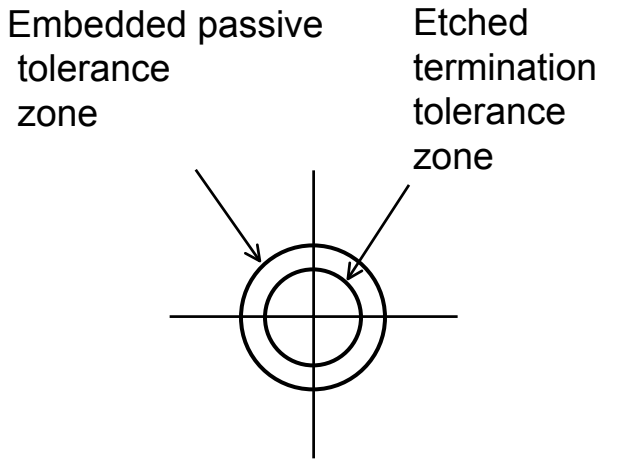
Manufacturing

PCB Manufacturing Process – Affects on Design

- Before going any further, BE CLEAR THAT:
- Regardless of the technology
- The embedded passive part design MUST allow for manufacturing registration tolerances

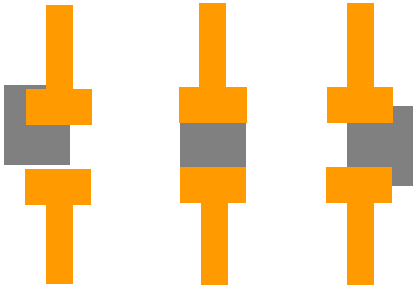
Registration Challenges

- Merging two image processes
- Whatever they are
- Design tolerances must match manufacturing capabilities

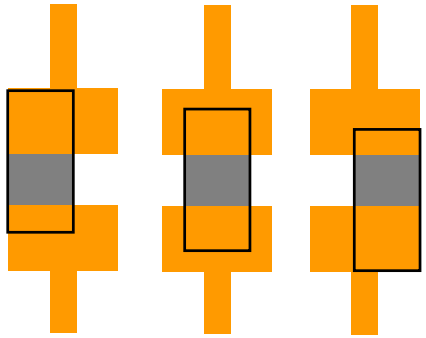


EP material and etched copper termination positional tolerance zones

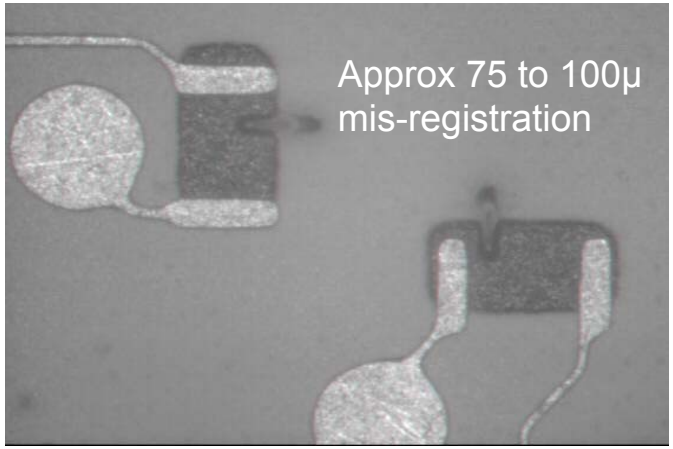
Registration Challenges



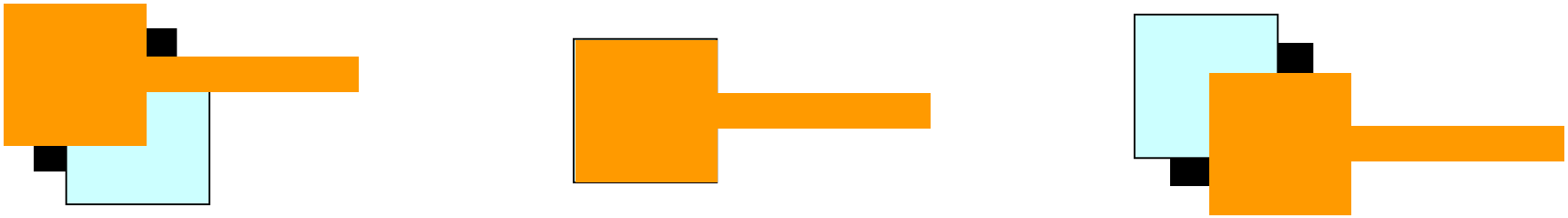
Improper termination design – insufficient allowance for manufacturing tolerance



Proper termination design – allowance for manufacturing tolerance

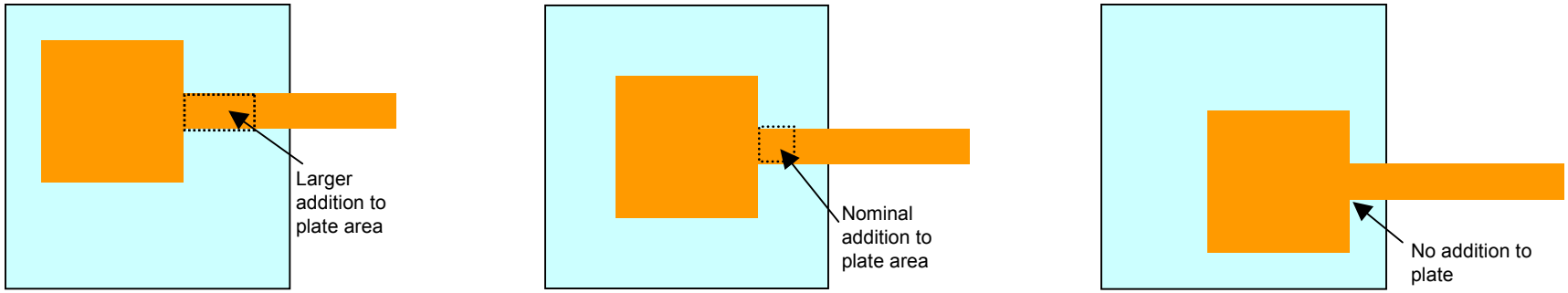


Capacitor Tolerances



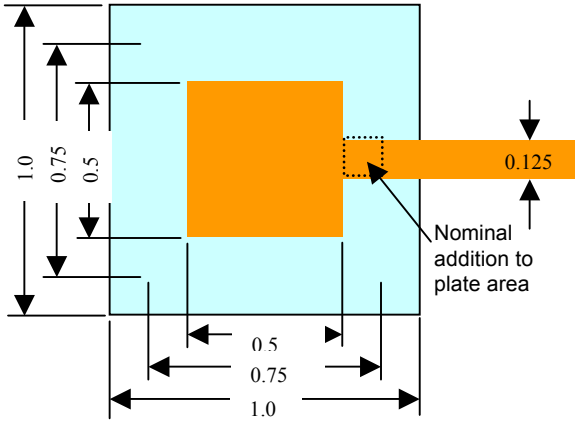
Worst case registration with improper print size

(results in failure)



Worst case registration with proper print size

Printed Capacitor Tolerances



Dimensioned with manufacturable tolerances

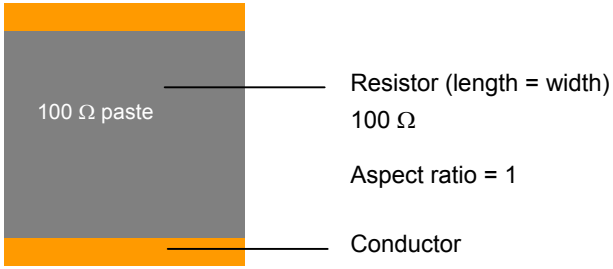
Feature	Tolerance (+/- %)
Dielectric thickness	10
Trace position	0.1
Etch	10
Total	20.1

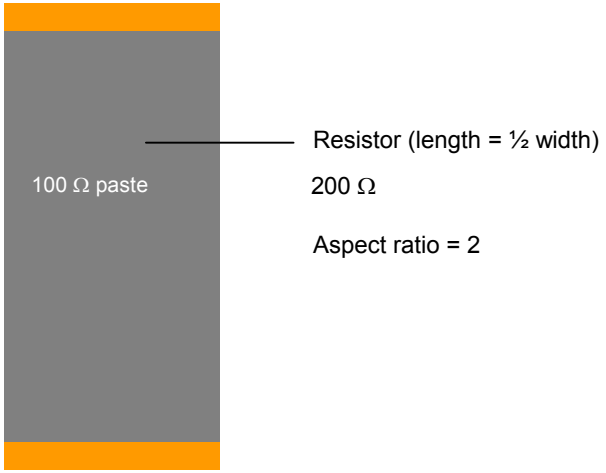
Resistance

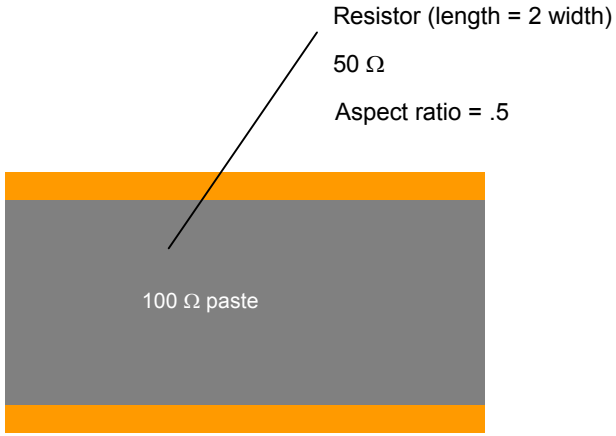
Resistance

- R = ρL/A
  - R = resistance in ohms
  - ρ = resistivity
    - resistivity (ρ) a material property
    - constant at a given temperature
    - expressed in resistance units (ohms) for area and length
    - I.e., the resistivity of copper is ρ = 7.09e-07 ohm in^2/in
  - L = length
  - A = area (cross sectional) (thickness X width)
- Sheet resistance
  - Where thickness is constant, R is constant for a square area
  - Expressed in Ω/sq
  - Resistance varied by varying the aspect ratio (L/W)

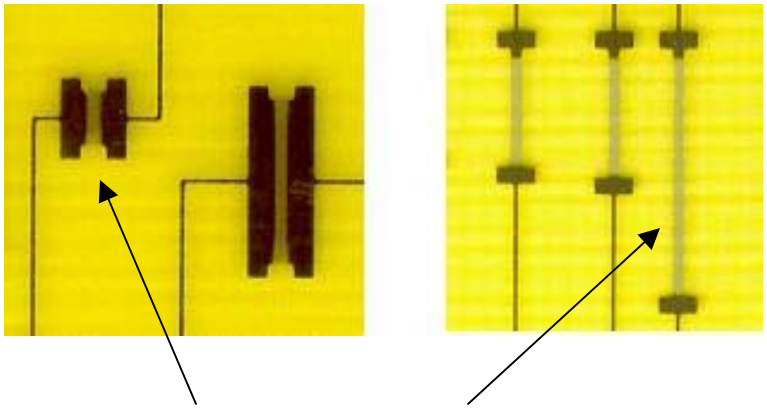
Aspect Ratio







Aspect Ratio



80 ohms to 20K ohms

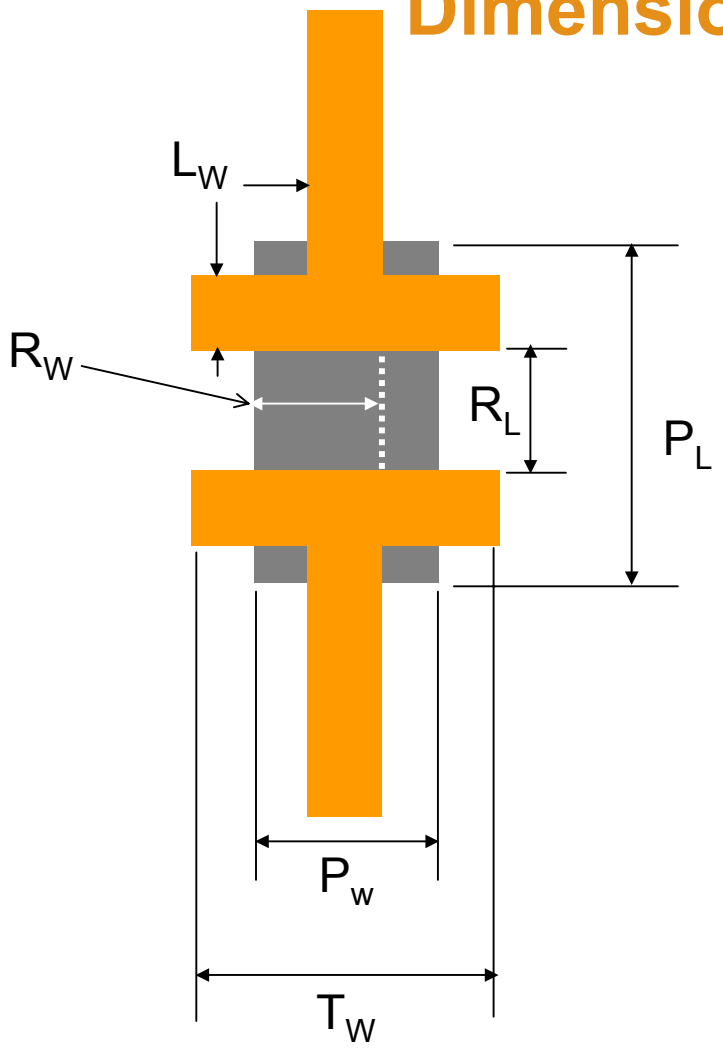
Achieved by varying aspect ratio from .08 to 20

Rohm and Haas Electronic Materials “InSite”

Designing Resistors

Printed Resistors and Terminations

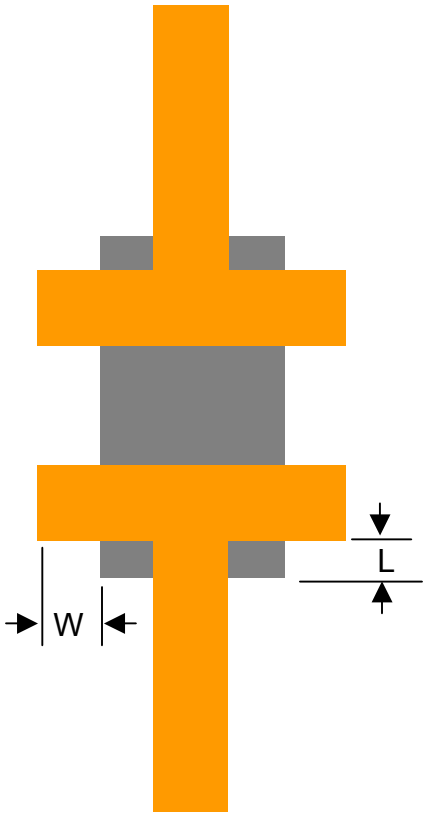
Dimension Guide



P_w – Print width
P_L – Print length
R_W – Resistor width
R_L – Resistor length
T_W – Termination width
L_W – Line width

Printed Resistors and Terminations

Critical Manufacturing Tolerance



	PTF Conventional	PTF Precision	Thin-film	CTF
L & W	+/- 200 µm	+/- 100 µm	+/- 0.0	+/- 125 µm

Etched Resistors

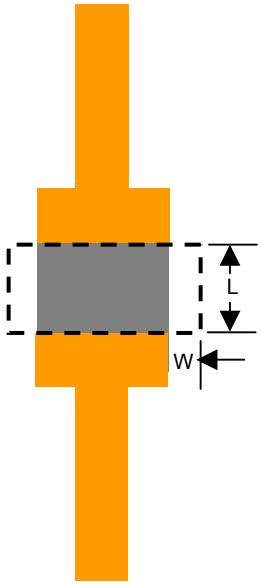


Figure 8
Etched resistor – T

Figure 9
Etched resistor – in line

Figure 10
Etched resistor – serpentine

Secondary Images Required

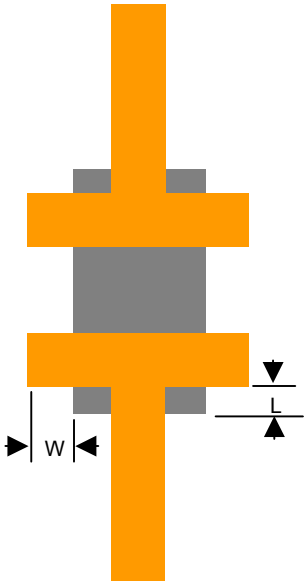


Figure 5
Resistor terminations

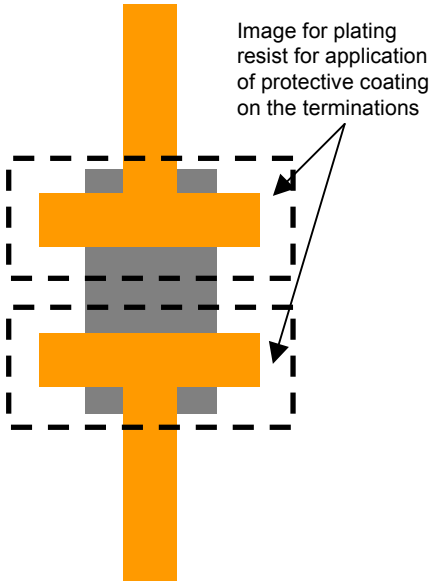


Figure 6
PTF Resistor termination coating

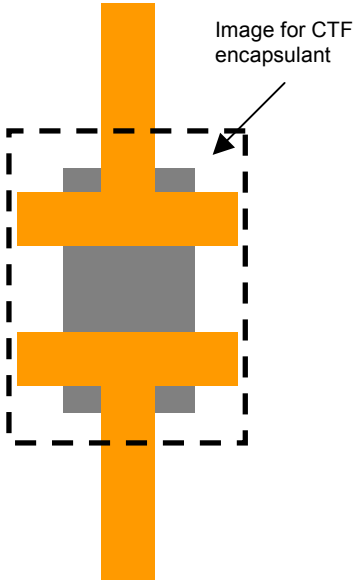
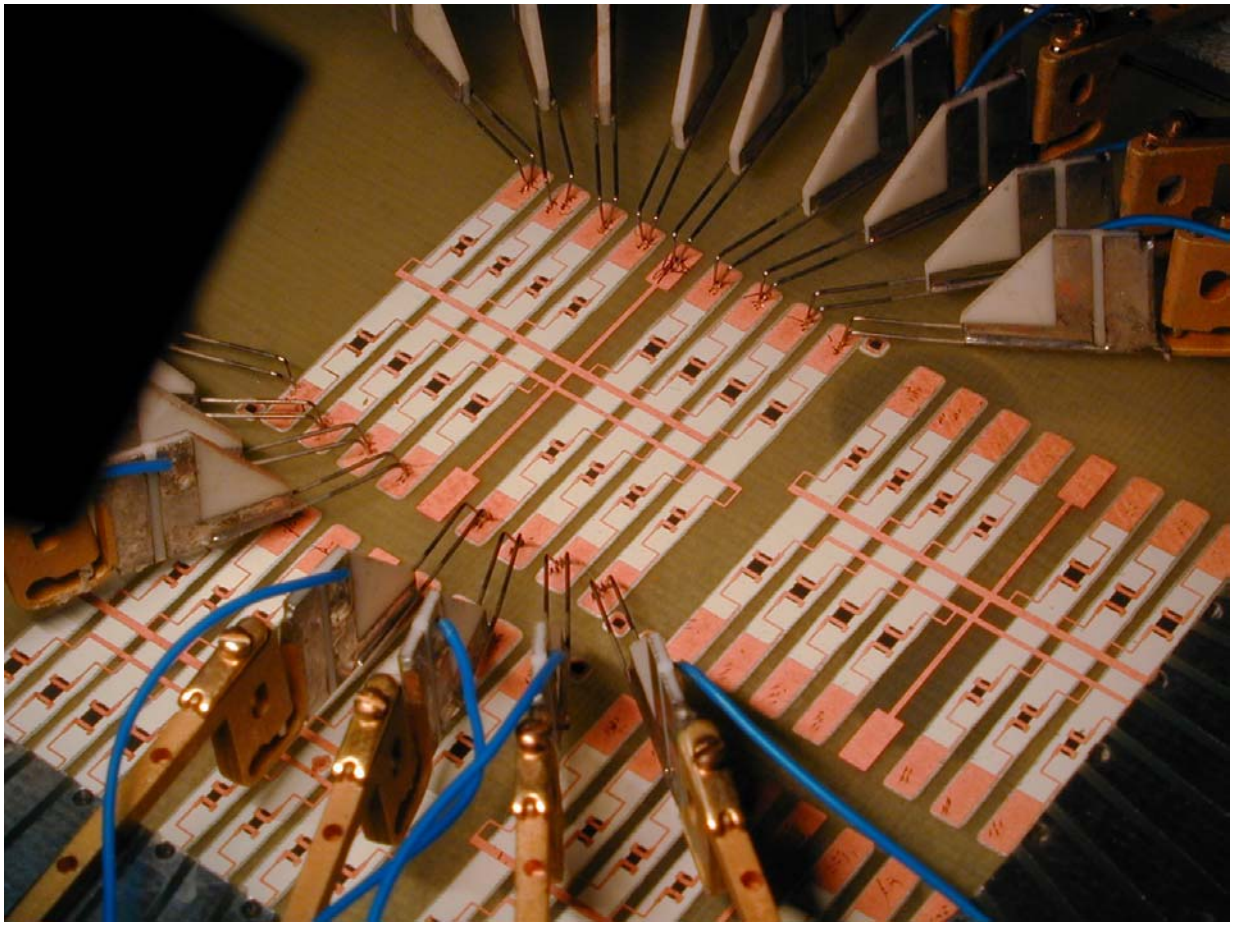


Figure 7
CTF Resistor encapsulant

Summary - General Resistor Guideline

- Determine min/max resistor feature sizes needed
- Recommend rectangular shape
- Aspect ratio < 8
- Smallest printed dimension >13mils (0.325mm)
- Printed length = resistor length + 2 X termination line width + 175μ
- See dimension guide for details
- Allow 125μ nearby copper feature as test/trim pad
- Determine optimum number of pastes or blends needed based on required resistors to embed, sizes, values and tolerances

Laser Trimmer Stage and Probe Card



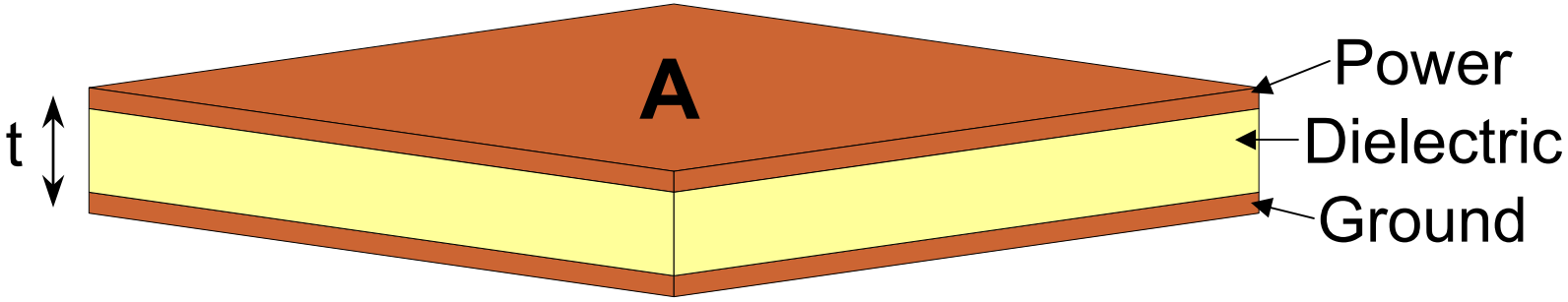
Laser Trim Guide Summary

- Board and panel layout
  - Systematic and repeated resistor and test pad pattern
- Test point pad size – 150μ minimum diameter
- Resistor size
  - Laser spot (75μ to 100μ)
  - Smaller resistors more difficult to trim
- Some resistor materials subject to thermal effects when trimming
  - Can affect power, TCR, and performance
  - Not observed on ceramic thick-films

Designing Capacitors

Capacitance

Parallel plates – separated by a dielectric



$$C = \frac{A * D_k * K}{t}$$

Where:

C = Capacitance (Farads)

A = Area of plates

D_k = Dielectric constant of material between plates

K = Constant

t = Thickness between plates

Capacitance Density

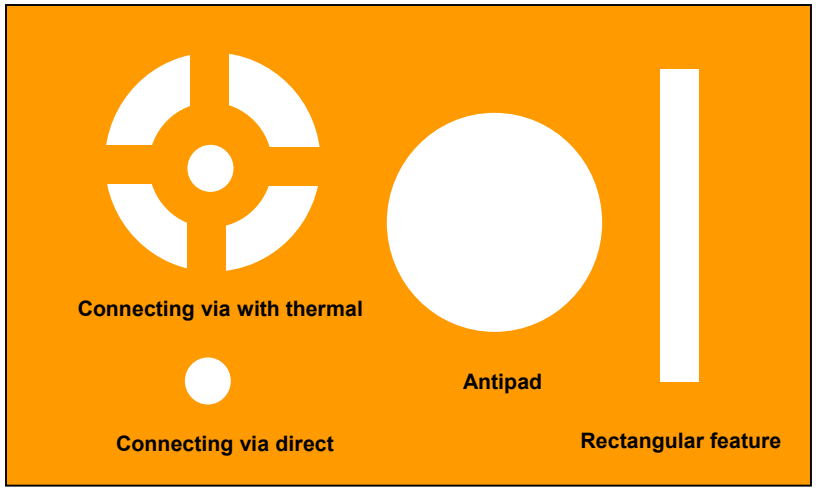
- Capacitance/unit area (C/A)
  - Expressed in $nF/in^2 = 0.2247D_k / t$ (where t is in mils)
  - Expressed in $nF/cm^2 = 0.885D_k / t$ (where t is in microns)

Capacitors

- Assumptions
  - Parallel plate, single layer capacitors
  - Dielectric thickness and Dk are constant for a given material
  - Sizing calculations are based on material supplier reported capacitance density
  - Termination and clearance based on PWB manufacturers registration guidelines
  - Capacitance tolerances based on material supplier reported capacitance density variance and PWB manufacturers etch tolerance

Capacitance of a Power and Ground Plane Layer Pair

P & G Plane Layer Pair



Top and bottom "no copper" plane features
(Overall area of top and bottom may be common or unique)

Plane Feature Relationships

- A_{OT} = Overall area of top plane
- A_{OB} = Overall area of bottom plane
- A_{OS} = Smallest overall area of planes
  - The lesser of A_{OT} or A_{OB}
- A_{VAP} = Sum of areas of thru holes and via antipads
  - All holes and vias thru the planes will have a clearance (antipad) on at least one plane.
  - The effect on capacitance is equivalent to 1X the clearance area for all holes and vias
  - This area should be substracted from A_{OS}

Plane Feature Relationships

- A_{CR} = Area of common rectangle top and bottom
  - Same area same location both planes
- A_{URT} = Area of unique rectangle top
  - Not common with bottom plane
- A_{URB} = Area of unique rectangle bottom
  - Not common with top plan

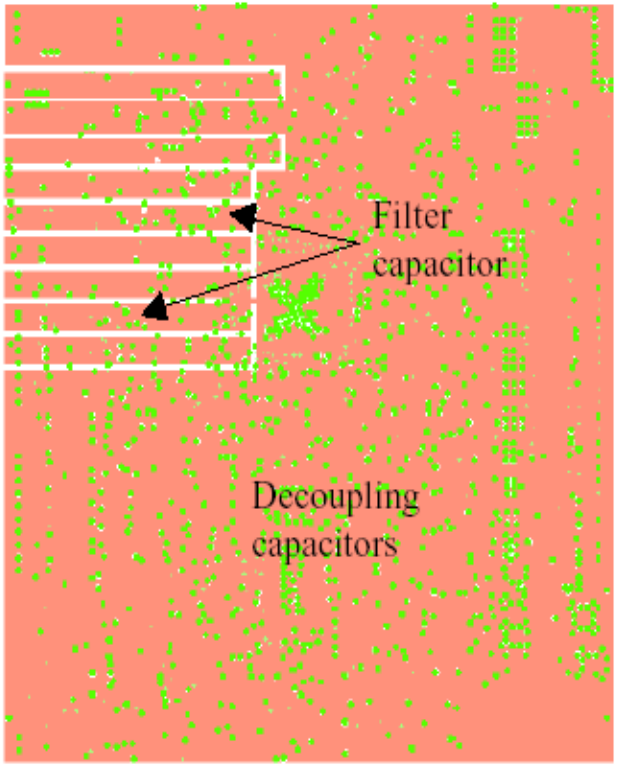
Plane Feature Relationships

- A_C = Area of capacitor
- $A_C = A_{OS} – (A_{VAP} + A_{CR} + A_{URT} + A_{URB})$

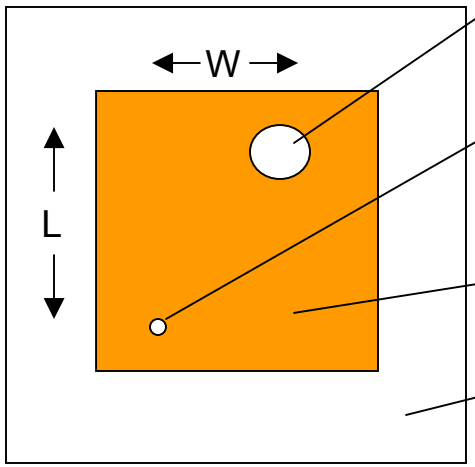
- C = Capacitance
- $C = A_C$ * Capacitance density
  - Be sure units are the same

Discrete Capacitors in Power/Ground Plane Pairs

Discrete Capacitors
(In P&G Plane)



Discrete Capacitor
(In P&G Planes)



Clearance = via drill + 0.016in (0.4mm)

A_L = area lost by clearance and via

Via drill

Coordinates of vias to be minimum of 0.5 X (drill dia + 0.020in [0.5mm]) from plate edge

Controlling plate (copper area = A_{CP})

0.043in (1.075mm) clearance all round separating capacitor from plane to avoid coupling

$LW = A_{CP} + A_L = A_S$

Controlling plate shown above. For the larger plate, via connection and clearance are opposite; and length and width dimensions are 0.006in (150μm) larger.

Discrete Capacitor
(In P&G Planes)

- Terms and relationships
  - C (required capacitance)
  - D (known capacitance density of selected material)
  - $C/D = A_{CP}$ (area of copper required in etched copper plate)
  - A_L (area lost by clearances and vias)
  - $A_S = A_{CP} + A_L$ (overall area of the smaller etched plate)
  - Coordinates of vias
    - Minimum of 0.5 X (drill dia + 0.020in [0.5mm]) from plate edge

Discrete Capacitor
(In P&G Planes)

- Discrete capacitors within a plane pair require:
  - Sufficient isolation from the plane - 0.040in (1mm) per side
  - Top and bottom plates designed such that normal process mis-registration will not affect the required capacitance
- Controlling capacitor plate - (smaller plate)
  - 0.003in (75µm) per side smaller than the opposite plate to assure that any mis-registration between the two plates will not change the required capacitance
- For simplicity, make the capacitor rectangular (however, it can be any shape, the math is the same)

Questions To Be Answered

(an abbreviated list)

Since standards and CAD tools are practically non-existent many questions still have to be answered, such as:

- What is the shape of the parts?
- What are the smallest feature sizes possible?
- What is the accuracy of a screened part?
- How many resistors can be placed on a layer?
- How to size for power requirements?
- When is trimming required?
- How to specify the trimming?
- How much should the pattern be oversized to allow for trimming?
- How does the embedded passive material affect the minimum dielectric thickness that can be used?
- What copper weights should be specified?
- What layers should the embedded passive parts be placed on?
- What termination pattern should be used?
- What is the size of the terminations?
- Are there conductor to passive part minimum spacing requirements?
- How are the required pastes to use specified?
- Does this process affect layer-to-layer registration?
- How do the part names relate to the BOM and schematic?
- How many planes can be tied together to increase capacitance?
- How much space is required between discrete capacitors?
- Can discrete capacitors share a common plate?
- What is the layer naming convention?
  - Resistor patterns
  - Capacitor patterns, dielectrics and conductors (single layer and multiple layers)
  - Encapsulant patterns (first and second)
  - Termination patterns
  - Copper termination layer and trim test points
- Which detail layers must be merged to provide tooling for the board manufacturer?
- On and on……

The Future

- Design tools
- Viable sources for PWBs
- Proven history

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Reference Material

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- HDI Simov Technologies - http://www.inboard.de
- AEPT Web Site: www.aept.ncms.org