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Reliability of High Density, High Layer Count, Multilayer Backplanes

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Abstract
This paper discusses the work and testing performed to obtain extreme high reliability performance from high layer count, large panel format multilayer printed wiring boards that are used for backplanes in surface mount technology applications. High density I/O surface mount connectors require fine lines, spacing and small vias. Couple this with a very large amount of connectors and with a Printed Circuit Board (PCB) of 330mm (13") by 990mm (39"), it results in very high layer count Printed Circuit Board (PCB) that can be thirty seven layers and with resulting thickness of approximately 5.3mm (0.210") having aspect ratios up to 11:1. Surface mount assembly on a double-sided board requires two reflows which thermally stress the product and have caused classic plated through hole failures (i.e. barrel fatigue) during initial assembly operations. Additionally rework of connectors is a requirement that applies additional stress and can cause more failures. This paper will show information on routing requirements that employ several layers of buried vias and thin 0.1mm (.004") cores and multiple ground power planes used for voltage and impedance control. Early failures caused by thermal exposure lead to an intensive development program to consider all aspects and variables in building a high reliability product. Material with varying Tg and Z-axis properties were included in the tests along with variables in lamination adhesion, etchback, and plating. A testing program was set up to include multiple thermal stress solder floats, a special plated through hole coupon for thermal cycle testing and then Current Induced Thermal Cycling preceded by multiple assembly simulation thermal exposures. Data accumulated will be reviewed with correlation made to the key items that produce the high reliability printed wiring board. Supplier and user cooperation was key to making the result a successful product that is now in small volume production. This knowledge can be useful to others who are considering high layer count large panel formats that required assembly reflow soldering as an alternative to compliant pin technology.

Technological Background
As technology progresses, systems become more and more complicated with greater demands for both throughput and interconnect requirements. One of electrical engineering's greatest challenges is system partitioning given the task at hand and the processing power available. Always striving for the latest and greatest, the electrical engineer is confined by physical considerations of how much interconnect is required between daughter card designs and how to dissipate the heat generated by the system components. As component density has increased, so has the capability and functionality of the daughter card designs. An ideal design minimizes the Input/Output (I/O) onto and off of the daughter card as interconnect is often a point of failure. A design team, which includes producibility, reliability, manufacturing, in addition to electrical and mechanical engineers, must help evaluate these system tradeoffs with high density connectors to optimize the interconnects required during system definition/partitioning. With the increased throughput and calculating capacity of daughter cards, comes the "opportunity" for large backplane designs that require high density interconnect which can increase daughter card communication capability. In efforts to eliminate large cable harnesses and "simplify" the interconnect between boxes, a design team can integrate multiple boxes into a common box and backplane; however, the backplane complexity can increase such that it bares the critical design load of the improvements in technology. The result is a backplane that is very challenging to both fabricate and assemble successfully.

Backplane Connectors and Assembly Processing
In the 1990s, there was a trend to make backplanes of a press fit configuration. Thick PCBs upwards of 10mm (.4") thick were relatively easy to fabricate with large pads, thick cores, large holes, and point-to-point routing. Press fit pin connectors offered no additional thermal excursions during assembly and depending on the PCB plating finish, the boards did not have to surpass their glass transition temperature (Tg) where the z-axis expansion rate can dramatically increase. Due to the broad pitch of the press fit connectors (when compared to surface mount connectors) and the high layer count PCBs available, routing of a signal was typically completed in point to point fashion within a single internal layer, and layer to layer interconnect was provided by the press fit hole so that vias typically were not required. Although press fit pin connectors are ideal for systems that do not require significant daughter card to daughter card interconnect, the press fit connector cannot offer the routing densities of Surface Mount Technology (SMT) connectors in most applications. Throughput of the press fit connector is limited due to the plated through hole size as well as the fixed location of the holes within the PCB.

The SMT connector on a 0.635mm (.025") pitch can be impedance matched for high-speed signal integrity. It can also be fanned out to vias with an aspect ratio of 11:1 to optimize routing. As the PCB increases in thickness, the drilled hole size for the via must be stepped up accordingly to maintain good plating characteristics; however, the via locations remain flexible

unlike the fixed hole of the press fit connector. In addition, the required via pad size was small enough to allow single channel routing of the PCB on a 12.7mm (.050") via. Every .25mm (.010") increase in spacing due to minimal pad sizes and flexible via location provided an additional single channel route as lines and spaces are .125/.125mm (.005"/.005") respectively. Thin cores of 0.13mm (.005") also assisted in keeping the overall PCB thickness to a minimum while maintaining 50 ohm matched impedance lines within an offset stripline construction. Buried vias on as many as six thin internal cores also helped optimize routability and minimized the final layer count and resultant via diameter and aspect ratio.

With the benefits of the SMT connector routing density also come the SMT assembly challenges. When utilizing SMT connectors, the PCB must be capable of withstanding the multiple thermal cycles of SMT assembly and rework in addition to any life cycle requirements. A solder reflow profile follows in Figure 1 below. The Tg of each material is indicated within the figure. Note the length of time that hardware is above the Tg for both /24 and the /29 materials.

Per Figure 1, the time above the Tg (170°C) for /24 is approximately 80 seconds or each SMT reflow or rework operation while the time above the Tg of 200°C for /29 is approximately 60 seconds.

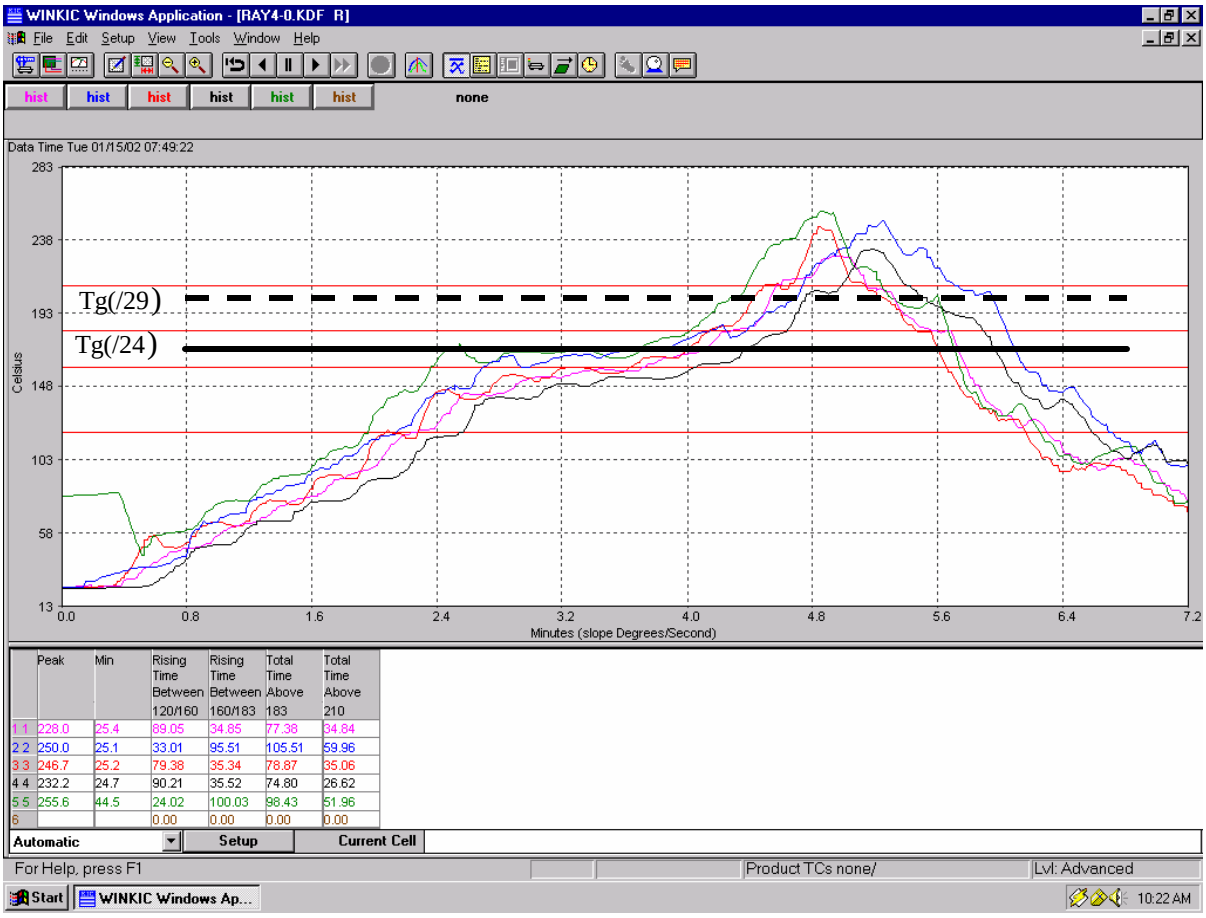

Figure 1 - Solder Reflow Profile

PCB Producibility
Producibility tradeoffs were carefully evaluated. Incorporating many leading edge design parameters into a single product can result in significantly decreased yields. Some of the design features have been previously mentioned and include:

- Layer counts up to thirty-seven (37) layers,
- Aspect ratios up to eleven to one (11:1),
- Lines and Spaces of .125mm/.125mm (.005"/.005"),
- SMT, Thru hole, and Press Fit Pin connectors within the same assembly design,
- Dielectric materials of thickness as thin as 0.10mm (.004"),
- Up to six buried via layers (cores),
- Impedance control on all signal layers (up to twenty three signal layers) with a ten percent (+/-10%) tolerance, and
- PCBs up to thirty-nine (39) inches in length.

With these increases in PCB complexity, there arises a greater opportunity for defects. By combining multiple technologies within the same construction, the final yield is geometrically reduced. For example, adding buried via layers, thin core materials, tight registration requirements (drill plus 0.36mm (.014")), large panel formats (42" panels), five mil lines and spaces, 11:1 aspect ratios, and an oversized panel can all be done individually within a PCB with great success, but throw all together, and the yield is reduced significantly. If each technology individually yields 90%, combining all seven in combination would yield only 47%. In addition, there might be many more defects that escape the standard inspection at the supplier. And, because of the lower yield and greater number of defects, the probability of escaping defects is increased. To help minimize the number of escaping defects, the Original Equipment Manufacturer (OEM) can set up an incoming inspection operation to screen out more defective product.

Damaging Thermal Excursions
After the lamination cycle of fabrication, the PCB is solder coated and fused in a hot oil bath for reflow prior to delivery. The thermal cycles experienced at assembly include SIDE A assembly reflow, SIDE B assembly reflow, as well as any required rework cycles of soldered components. Soldered component rework typically entails three thermal cycles to include the removal, sight dressing, and replacement of the soldered component. All assemblies are subjected to assembly reflow and many will undergo as many rework cycles as allowed by engineering. After assembly completion and functional test verification, the assembly may then undergo environmental screening before being released for life cycling in field operations. Life cycle requirements vary by product but may require up to twenty years of functionality and supportability.

Material selection for these products is important for both the reliability and cost. Moving with the industry "wave" toward best commercial practice, the polyimide materials were forgone for the improved line of high temperature epoxy resin systems. This material was also targeted to minimize cost. Early experience with the IPC 4101A/24 (henceforth /24) epoxy materials proved successful with the systems being robust enough to survive the reflow cycles of assembly and life cycle requirements during early stages of development where multiple component rework cycles were required. Even though the material meets a slash sheet configuration (/24), it does not mean that the slash sheet necessarily meets the products assembly and end item requirements. Also, the variation allowed between materials within a slash sheet may also border on the ability to meet product requirements. In addition, there may also be variation in the assembly and rework processing of the product. In summary, the slash sheet materials may survive initially assembly and five assembly reworks, but another build may survive only one rework after assembly.

Although there was early success with /24 product, barrel fatigue failures were identified midstream as product did not survive even initial assembly reflow. Although performance based Plated Through Hole (PTH) Reliability coupons had been incorporated into the fabrication panels, they were not used proactively for screening product until after such defects were detected.

It is always a good practice and sometimes even essential with some PCB materials to minimize the number of thermal excursions that the PCB sees in a lifetime to reduce the possibility of failure. The most critical and damaging thermal excursions may very well occur before the hardware ever leaves the assembly shop (i.e. when components are soldered and reflow temperatures are above the material's Tg for epoxy system). This will become even more challenging with the implementation of "lead free" soldering as processing (reflow) temperatures will be higher still and even further above the Tg of existing high temp epoxy materials. The epoxy resin system used and the respective Tg of the material plays a significant role in the PCB thermal cycling survival, but other factors also influence thermal cycling survival.

Industry Standard Structural Integrity Evaluation (B Coupon)
As a norm, the industry standard for structural integrity evaluation of the printed circuit board and fabrication panel has been the B Coupon segment per IPC-2221 (see Figure 2). The B coupon requires that a coupon be solder floated for ten seconds (i.e. a 1X float). This is required to thermally stress the coupon prior to microsectioning. The number of "floats" used to

thermally stress the coupon can also be negotiated by the procuring activity and fabrication house. Three float (3X) and six float (6X) specifications are becoming increasingly common for higher reliability product. An increase in the number of floats can cause defects that are subtle in single float specimen preparation to become more apparent and easier to identify; however, the coupons still require the review of an experienced operator for proper evaluation, and not all materials can consistently withstand the additional exposure. Anomalies identified under a microscope may be indicative of significant structural problems and need to be evaluated.

In addition to careful visual inspection, the microsection must be prepared properly as it is possible to smear the copper in the specimen such that it masks the structural defects to the extent that even the most experienced operator cannot find them. The B coupon review is often acceptable for product that will undergo very few reflow cycles or has a relatively benign working environment; however, for hardware which must be more robust in order to withstand extensive assembly processing and/or more rugged life cycle applications, the standard float test (even if increased from 1X to 6X) may not be sufficient.

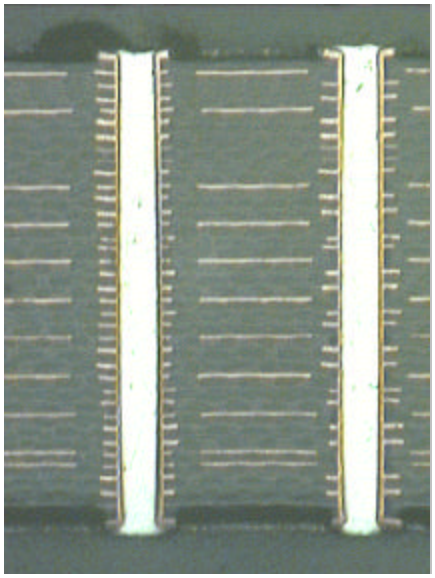

Figure 2 - B Coupon Microsection of Backplane

One limitation of the B coupon is its inability to simulate surface mount assembly processing and rework cycles with simple solder floats. Although the B coupon is exposed to high temperatures and large thermal gradients while on the molten solder, it does not see these high temperatures for extended periods of time. Most /24 materials are rated for less than four minutes at 260°C per T260 testing specifications. Although B coupons for this product (when fabricated with /24 materials) withstood up to six solder floats without any evidence defects, barrel failures were identified during initial surface mount assembly reflow and proved the B coupon evaluation to be a suspect performer for the /24 group for this 5.33mm (.210”) thick PCB design. In retrospect, after six solder floats, the specimen has seen a total of only sixty seconds of exposure to extreme temperature whereas each SMT reflow profile targets approximately eighty seconds of time above the solder reflow temperature which is also above the Tg of the /24 material.

In addition, when evaluating the B coupon, one must take into consideration that very few barrels are being reviewed as compared to the number of barrels in the PCB. In fact, the number of barrels reviewed is approximately .04 percent when compared to the number of barrels in the PCB for the product described in this paper. If any indication of a defect is identified, further investigation is well warranted.

Laminate Thermal Testing

T260 testing can be an indicator of the thermal robustness of a material and tests for the time required to separate materials while holding the test specimen at 260°C. The time to failure is then measured and recorded. The test results provide the thermoset points of the material and can help to determine whether or not the PCB materials were fully cured during lamination. The T260 also provides a relative measure the “robustness” of the material to handle extended exposure to high temperatures, specifically regarding assembly thermal exposure and reworkability. The /24 product is rated at less than four minutes and the /29 product is rated at thirty minutes. Extensive exposure of some /24 PCBs to two (2) SMT reflow cycles resulted in barrel failures even though the follow-up analysis showed the material to be fully cured. Although the assemblies are processed below 220°C during assembly as seen in Figure 1, as few as two reflows failed some /24 product. This was

contrary to the /24 product fabricated previously assembled, reworked, and delivered. The extended time over the Tg of the material can be detrimental to the resin system and classic barrel fatigue may result.

Performance Testing Alternatives

To increase the likelihood of identifying defects within a PCB prior to assembly, a test that increases the interconnect sample size as well as provides a test more indicative of the respective assembly, rework, and life cycling requirements is preferred. Such a test can be expensive prior to assembly and increase cycle time for PCB integrity verification, but the added process can also more than offset the cost if the effort is successful in screening suspect PCBs from assembly processing and field failures. Both the cost of the testing and the cycle time impact must be carefully evaluated and the trade study performed with respect to the cost and the risk of assembling suspect product. For many applications, performance testing may be cost prohibitive to implement.

A lower cost approach that can be described as passive yet somewhat proactive is to design a coupon to be used only if failures are identified in the future (i.e. use the coupon as a referee for the B coupon or as a fall-back for future screening of the PCB after assembly defects have been identified). The coupon must be designed and integrated into the fabrication panel for future testing.

To be included within the fabrication panel, the test coupon design must be delivered with the PCB database such that the supplier can incorporate it into the fabrication panel. It is preferred that the coupon be incorporated into the master database with the PCB, but it is not a requirement. The test vehicle (coupon) must be introduced to the panel during the Computer Aided Manufacturing (CAM) phase of fabrication. The coupon should be processed is if it is deliverable product by the manufacturer (i.e. unique markings, Automated Optical Inspection (AOI), etc.).

Regardless of whether the coupons are to be used proactively or passively, it is recommended that some testing be performed early in the program to establish a baseline for future comparison and evaluation. Determining the number of cycles to be used as a benchmark or threshold of acceptability can be the most challenging obstacle to successful performance coupon testing and implementation as fabrication materials, fabrication and assembly processes, as well as product life cycle need to be taken into consideration.

Test vehicle design is often dependent on the test method to be used. Two types of available performance testing coupons are described below. If in-house equipment is not available, contract testing is available for each.

Plated Through Hole Reliability Coupon Testing

One example of a performance test uses a coupon design that is typical for thermal cycling evaluation. The Plated Through Hole (PTH) reliability coupon tested per IPC-TM-650, Method 2.6.7.2 can be used with thermal shock chambers to simulate life cycle testing. Layer 1 of the coupon is depicted in Figure.

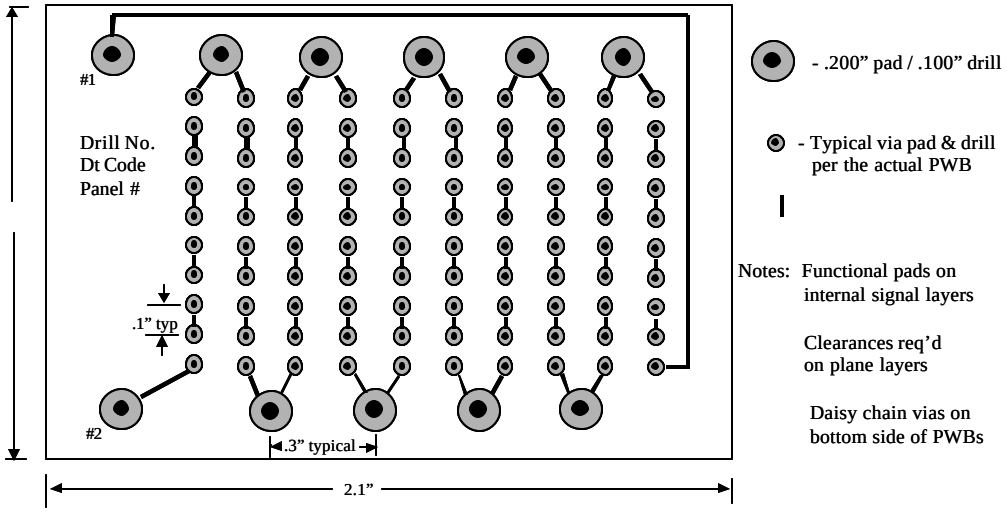

Figure 3 - Layer 1 of the PTH Coupon – 2.1" x 1.7" Typical

The coupon shown is designed to test for barrel fatigue using daisy chains on the top and bottom layer, but it can be modified to isolate circuits for post barrel interconnect failures as well. The coupon can be separated from the panel and subjected to assembly preconditioning (solder reflows) prior to beginning its thermal chamber testing with thermal cycles from –65°C to +125°C. Six preconditioning reflows can be used to simulate both initial assembly and rework. Four wire resistance measurements are then used in conjunction with data loggers to identify a failure (a 10% change in the resistance of the circuit). The resistance is monitored throughout the thermal cycle. After coupon failure, it can be removed from the oven and the defect can be pinpointed using an infrared viewer or a hot plate and a microohm meter.

Figure 4 shows a typical thermal cycle after preconditioning has been completed. The cycle includes the dwell and takes about thirty minutes to complete. The number of cycles defining failure is significant and often a point of discussion. It is dependent on the preconditioning specifications, the end item application, and the comfort level of quality engineering with this accelerated life test. Usually less than one hundred cycles is targeted to define the minimum threshold. The test is run as a batch operation and many wires must be soldered to the coupons so that monitoring remains continuous while the coupons are shuttled from hot to cold and cold to hot.

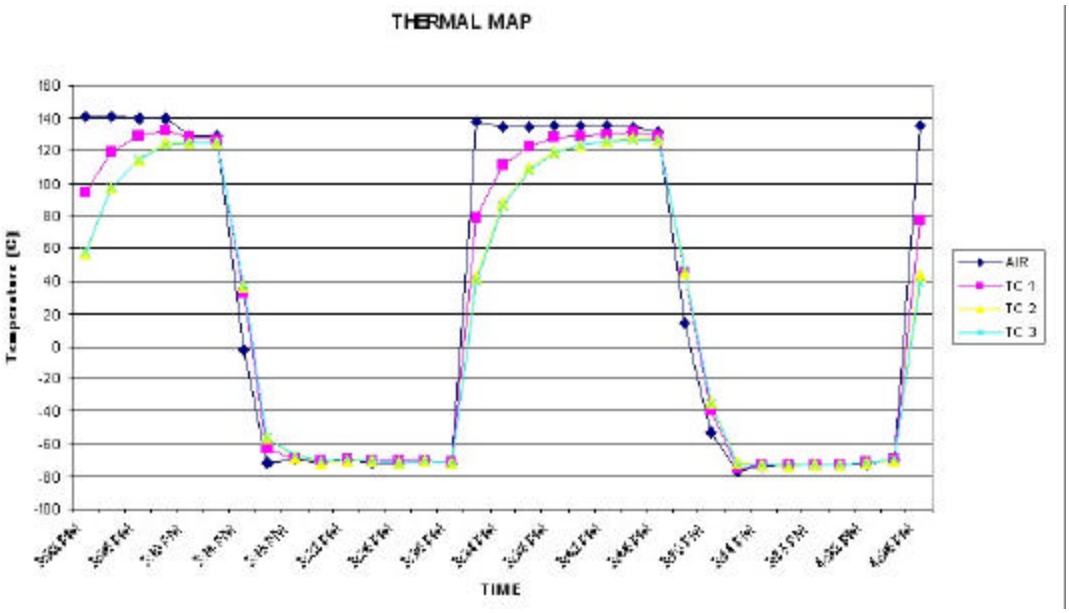

Figure 4 - PTH Thermal Cycle

DC Current Induced Thermal Cycling Stress Testing

Another example of a performance coupon is the DC Current Induced Thermal Cycling Stress Test per IPC-TM-650, Method 2.6.26 using custom designed coupons and test equipment.[1] Also referred to as the Interconnect Stress Test (IST), the IST test can also be used as an assembly and life cycle test in efforts to simulate the extreme requirements placed on the board. See sample design in Figure 5.

The coupon is designed to test for both the barrel fracture and for post interconnect failure. PCB Interconnect Solutions sells the unique test equipment and provides design services. The thermal cycles are approximately six minutes in length, and a single tester will test up to six coupons at a time. The tester also offers preconditioning cycles (220°C in this case) to simulate SMT reflow and rework. Also, the low temperature for this test is room temperature while the typical life cycle test is 150°C for the high. The use of higher temperatures to identify infant failures in a shorter cycle time is under evaluation.

A sample profile of an IST thermal cycle follows in Figure 6. The POWER circuit indicates the circuit that is used to heat up the coupon with DC current and that typically has larger holes (see Figure 5). The POWER circuit is also used to detect the post failures. The SENSE circuit uses the smaller holes on a PCB design evaluate the barrel integrity, as it is more of a concern in these holes with a higher aspect ratio.

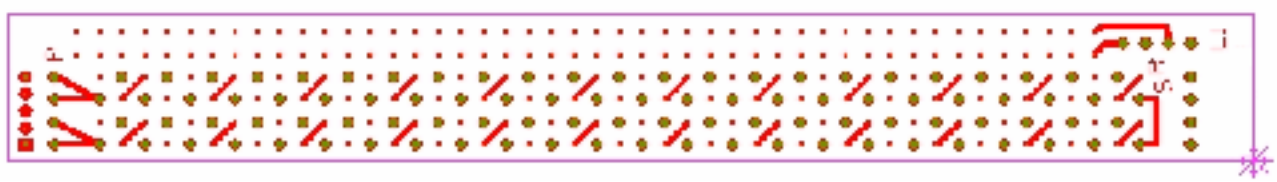

Figure 5 - Sample IST Test Coupon (5.5” x .75” Typical)

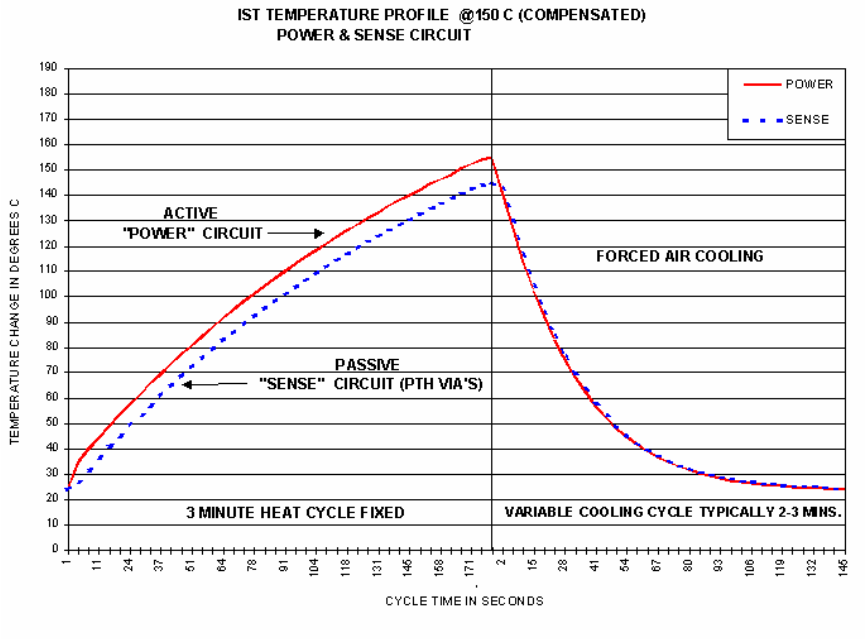

Figure 6 - IST Temperature Profile from Room Temperature to 150°C

The primary advantages of this test method are:

1) Assembly processing temperatures can be quickly incorporated into testing while on the tester,
2) The coupon and test are designed to test for post separation, and
3) Cycle time is minimized for the testing of six or fewer coupons. However, each tester can accommodate a maximum of six specimens; thus, the overall cycle time for large runs of coupons will be dependent on the specimen quantity, machine availability, and cycles defined to complete testing (different for different materials).

Why Use Performance Testing (/24 and /29 Material)?

Early in the program, /24 materials were used to fabricate the large backplanes and did not exhibit many failures even though assembly processing and rework was relatively harsh. B coupons were used as acceptance criteria. However, midstream, the /24 grade material proved borderline in its ability to consistently meet assembly processing and life cycle requirements as product exhibited barrel failures in many backplanes which had only completed the initial two assembly reflow cycles. The B coupons had been reviewed at 3X with no issues identified. B coupon retains were then subjected to 6X solder floats, but again no anomalies were found. The failed PCBs were also T260 tested and proved to be fully cured. Although the latter B coupon had been subjected to six of the ten second solder floats, it had only been exposed to the hot solder a total of sixty seconds. It appears that the extended time at temperature above the Tg of the material during assembly reflow significantly degraded the PCB while the 6X float specimen showed no signs of having a defect. Although a good indicator of structural integrity, the limited exposure (duration of only sixty seconds) of the B coupon to the heat source on this thick PCB for this run of product did not adequately simulate SMT assembly processing which had longer exposure times to above Tg temperatures.

When evaluating which performance test method to utilize in high reliability applications, time at temperature, maximum temperature, material, and the number of thermal cycles is important. Table 1 summarizes some aspects to be considered.

Table 1 - Cumulative "Time at Temperature" Evaluation for Assembly Processing and Testing After Assembly

	Assembly Metrics			Post Assembly Information	
Assembly or Test Description	**Assy & Rework Reflow Cycles OR IST Preconditioning Cycles**	**Time above Reflow Temperature (183°C) per Reflow (sec)**	**Cum Time above Reflow Temperature OR Time at Preconditioning**	**Life Cycle Req't After Preconditioning or Assy**	**Life Cycle Parameters**
Assy (2 in-line reflows + 2 thru hole connector replacements (each replacement = 3 reflows)	8	80	640	20 years?	various
B Coupon for Structural Integrity Evaluation (6x)	6	10	60	n/a	n/a
PTH Reliability	6	80	480	70 Cycles	-65°C to 125°C
IST	6	60	360	300 Cycles	25°C-150°C

The table shows both "Assembly Metrics" and "Post Assembly Information". The B coupon can quantify the "Assembly Metrics" portion; however, the assembly simulation may not accurately portray SMT processing. Also, the B coupon does not take into account any life cycle requirements, which performance tests attempt to simulate (see "Post Assembly Information" columns above).

Performance Testing Results (/29 Material)

After defects were identified after initial assembly reflow in /24 product, PTH coupons were used to determine that the /29 materials tested to be a bit more robust to assembly processing temperature and life cycle testing. When changing to the /29 material, IST coupons were added to the fabrication panel for testing evaluation and possibly PTH comparison. The benefit was to have a test for post barrel separation, which the design for the PTH coupon did not provide. A sample of test data from both the PTH and IST testing follows in Figure 7. This data pertains to only /29 material with a Tg of 200°C.

Both coupon types coexisted within the same fabrication panel. PTH coupons were located near the four corners of the panel, and the IST coupons along the long edge of the 1067mm (42") by 457mm (18") panel, but closer to the center. Only a few post interconnect failures were identified in the IST coupons as most were barrel fractures. The data above shows the results of the four PTH coupons and two IST coupons that were tested per panel. The minimum threshold for the PTH coupons after preconditioning was set at 70 cycles, testing was halted on the first eighteen sets of PTH coupons at 130 cycles as no failures were yet identified. For specimen #19 through #40, the PTH coupons continued to meet the minimum threshold but performance degraded. The IST test results also appear to track the success of the PTH coupons for this group as the life cycle results for the first eighteen met their respective minimum threshold, which was set at 300 cycles. Only one coupon failed to meet the minimum in this range of product. The IST results also show degradation in life cycle survival for panels #19 through #40.

From the graph, the IST coupons have both a greater nominal value as well as a greater standard deviation although the sample size for the IST is small at two per panel. All of the PTH failures were barrel fracture by design of the coupon, and most of the IST f failures failed at the barrel. If all four of the PTH coupons survived the barrel fracture minimum threshold of 70 cycles and the IST coupons failed for barrel fatigue below the 300-cycle minimum, the PCB was recommended for assembly. The PTH was picked as the "tie breaker" due to the fact that its preconditioning cycle is the same as that for the actual hardware (i.e. solder reflow through the oven) and because there is more history with the test. The temperature extremes of life cycling also better reflected product life cycle extremes while the IST tests of 25°C to 150°C came closer to the glass transition temperature of the material (i.e. 150°C in the DC test vs. 200°C Tg).

The PTH coupon has long been accepted as a high reliability military standard, but was not originally designed for post barrel interconnect testing. It is also a batch operation and used in this manner requires that expensive reflow operations to take place to precondition the coupons. The cycle time to precondition and functionally test the coupons with this method may be prohibitive, but test results are believed to provide good insight to structural integrity of the barrel. Non-recurring activity is required to precondition the samples for test and to set up the data loggers for thermal cycling. Cycle time can be prohibitive, but post barrel measurements can be introduced.

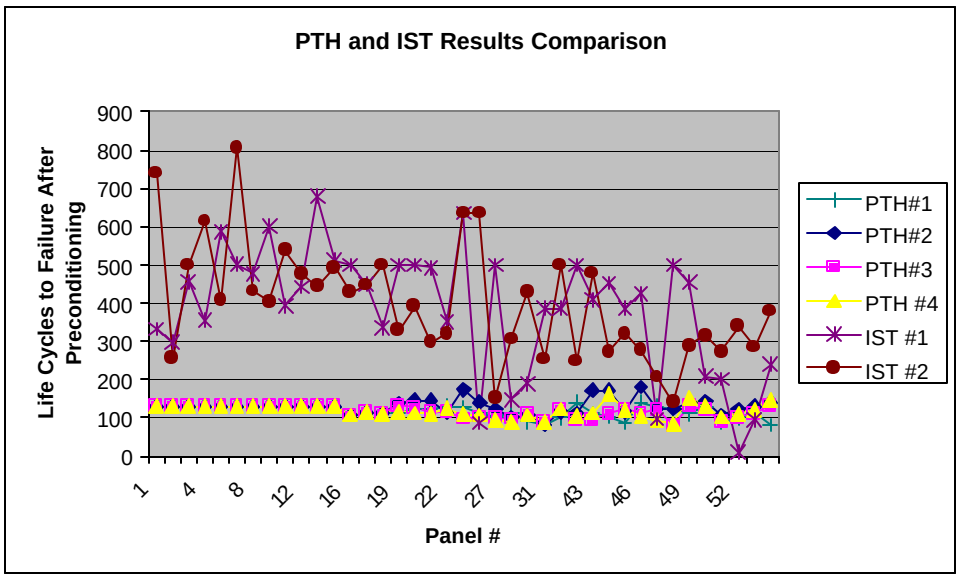

Figure 7 - Test Comparison

The IST coupon can be preconditioned on the test set which significantly reduces the cycle time as each precondition cycle only takes six minutes and follow on testing is performed on the same machine. The standard deviation was seen to be greater and a minimum threshold may be more difficult to define. One benefit is that if only samples are required, the tester can test six specimens at a time with little non-recurring effort.

Conclusion

Advances in mulitlayer technology have introduced more thermally robust epoxy resin systems with a higher Tg values. There are advantages and disadvantages to the higher Tg materials that need to be evaluated for each specific design. To insure structural integrity of the product through its life cycle for high reliability product in harsh assembly and rigorous environmental applications, one must assess many inputs, which include but are not limited to cost, assembly processing, rework processing, and life cycle requirements/environment.

Upon selection of a laminate material and the identification of assembly process requirements, performance based coupon testing and evaluation should be considered for high reliability product for the following reasons:

1) Good results insure that the PCB is suitable for release to assembly,
2) Performance based coupons can provide an objective number to assess the product,
3) Minimu m thresholds can be established per unit or per work order average for accept/reject criteria (although the number may be challenging to establish),
4) Testing (possibly samples) can be used to help detect improvement/degradation of product throughout fabrication lifetime,
5) Testing can be used to help differentiate and down select different materials for fabrication,
6) The number of interconnect tested is dramatically increased (from six in the B coupon to near one hundred),
7) B coupons when processed as specified may not adequately represent SMT assembly and rework processing (even at 6X),
8) B coupons can be improperly prepared (smeared copper masking defects), and
9) Skilled operators can overlook defects in B coupons.

Although a concrete number of life cycles for the performance test coupon may be difficult to assess and the variability of results needs to be managed, the performance test coupon can be used to identify infant failures and to provide measures of relative goodness between work orders.

Steps to determine whether a performance-based coupon is applicable follow:

1) Perform a trade study evaluating assembly thermal excursions, rework requirements, life cycle requirements, PCB cost, assembly cost, costs of failures at different levels,
2) Determine which type of performance test vehicle might best suite the application,
3) Design the coupon and provide it with the original database to the fabrication house,
4) Insure that the coupon is fabricated, marked, and processed exactly as the PCB is,
5) Determine whether the coupon will be used passively or proactively,

6) Determine if preconditioning is required,
7) Establish baseline performance for the test coupons,
8) Establish minimum thresholds for the test,
9) Sample product to insure product performance is maintained, and
10) Use the data to insure conforming product is assembled.

For high reliability product with challenging assembly and life cycle requirements (especially PCB failures and the assembly components are expensive), performance testing using coupons from the same panels as the PCB can provide a great deal of unbiased insight into fabrication quality where the B coupon may not.

Reference

1. PCB Interconnect Solutions, Inc., Ontario, Canada