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Via in Pad Study
Evaluating the Impact on Circuit Design, Board Layout, Manufacturing, Emissions Compliance and Product Reliability

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Driving Factors for the Use of Via in Pad Technology

Driving factors for the use of via in pad technology include the growing trend towards more dense and complex printed circuit board designs as well as the need to minimize parasitic capacitance and inductance on high speed digital circuits. These two driving factors are accompanied by the enhanced capability of printed circuit board suppliers to fabricate smaller via diameters without increased fabrication cost. In this study via in pad technology is referring to the use of standard vias, not microvia technology or blind via technology. Via diameters considered in this study include a range from 0.008" finished hole diameter up to a 0.012" finished hole diameter. Reduced via hole size enhances the use of via in pad technology, especially on smaller devices such as 0402 components. Via in pad technology creates increased printed circuit board (PCB) routing space on the outer layers, which aids in the routing of complex printed circuit board designs. Via in pad technology also reduces parasitic capacitance and inductance which are typically found in high speed digital circuits.[1] This is accomplished by eliminating the "stub trace" which is typically created by placing a second pad adjacent to the component pad just to have a land for the via to be drilled.

Evaluation Approach

Our approach for the evaluation of via in pad technology was to investigate the affect, be it negative or positive, on several critical areas within the new product development process. These areas included: Circuit Design, Board Layout, Manufacturing, Emissions Compliance and Product Reliability. All efforts were conducted with the understanding that raw PCB cost should not be increased in order to achieve the desired result. The above mentioned areas were placed in two subgroups and evaluated by separate means. Circuit Design and Emissions Compliance were grouped and evaluated by researching an abundance of existing technical information available while Board Layout, Manufacturing and Product Reliability were grouped and evaluated by developing and performing an in-house Design of Experiment.

Circuit Design and Emissions Compliance

Various sources were utilized to research prior work involving Circuit Design and Emissions Compliance in conjunction with Via in Pad Technology. The following trace inductance equation is used to calculate the amount of inductance associated with "trace stubs" traditionally used to tie a component pad to a via land.[2] (See Figure 1.)

$L = 0.005 \text{ Ln } (2\pi H/W)$ where L is in micro Henrys per inch
L = inductance
W = trace width
H = height above current return path

For example: The Inductance for a single component using a 0.015" long stub trace out to a traditional 0.020" via land with a 0.006" wide trace on an 4 layer PCB is as follows:

$L = 0.005 \text{ Ln } (2\pi\ 0.020" / 0.006") = 0.0152$ uH/inch
Total inductance for the component is 2L (two traces)
Total inductance for the PCB is determined by multiplying all the components on the PCB using this trace to via methodology by this single component inductance value.

Note: Assuming board thickness does not change, as board layer count increases inductance generally decreases due to the fact that the layers become closer together.

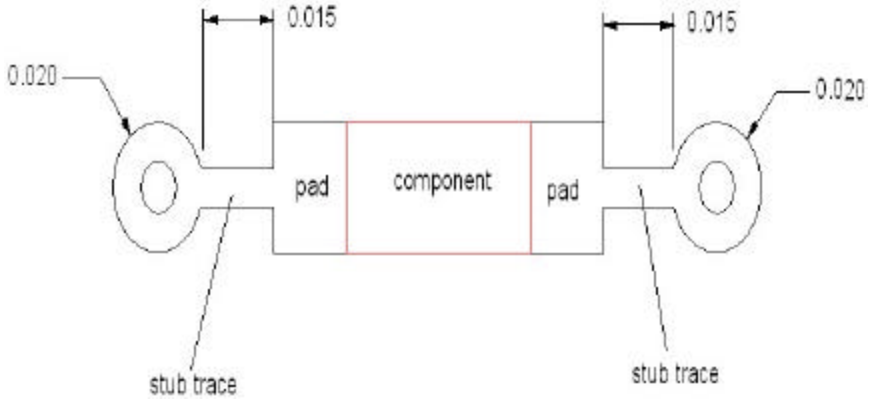


Figure 1 - Typical Trace to Pad Design for a Via Land

Board Layout, Manufacturing and Product Reliability

Significant enhancements can be seen with board layout by utilizing this technology due to the board surface that is made available for routing and component placement. Figure 2 details the real-estate savings that can be realized when using this technology.

In order to evaluate the affect of via in pad technology on Manufacturing and Product Reliability, a 3x3x3x2 factorial Design of Experiment was used. The following four factors were evaluated in this experiment: board finish, component size, via size and finally the affect of plugged versus unplugged vias. The board finishes that were used were standard Hot Air Solder Leveling (HASL), Silver Immersion and Gold Plating. Component sizes that were used were 0805, 0603 and 0402 packages. Via diameter sizes that were used were .012", .010" and .008" finished hole size. The last factor used was simply having an unplugged via verses a plugged via. Custom test boards were designed and used to conduct the experiment. The boards were designed to emulate the possible conditions that might be seen in manufacturing. A total of ten boards of each finish were evaluated. Each board had 180 component placements with two vias per placement. All possible combinations of factors were evaluated totaling 20 replications of each possible factor combination per board, times ten boards totaling 200 replications in all. The boards were built in random order to minimize any statistical noise that might occur in the data. Of the 10 boards of each finish that were built a smaller subset was examined for data collection. This examination consisted of a visual inspection of each solder joint with a pass or fail rating being assigned. All solder joints were inspected per IPC-A-610-C class 2. Failures were then totaled to create variable data that was then analyzed statistically.

For the purpose of this study the vias were located in the outer corner of the pads away from the component. This location was chosen so the via would be at the furthermost point from the component termination to minimize any affect on the solder joint. Also, because the lap joint provides a significant amount of strength for the joint, locating the via underneath the component would have weakened the joint. PCB thickness for this study was held constant at .062". The results and recommendations from this study apply for standard boards that measure .062" in thickness.

The affect of raw PCB cost was evaluated by polling existing PCB suppliers concerning their current capability with via in pad technology. Suppliers were specifically asked about the .012", .010" and .008" via hole diameters and their ability to achieve each and any associated cost that would be introduced.

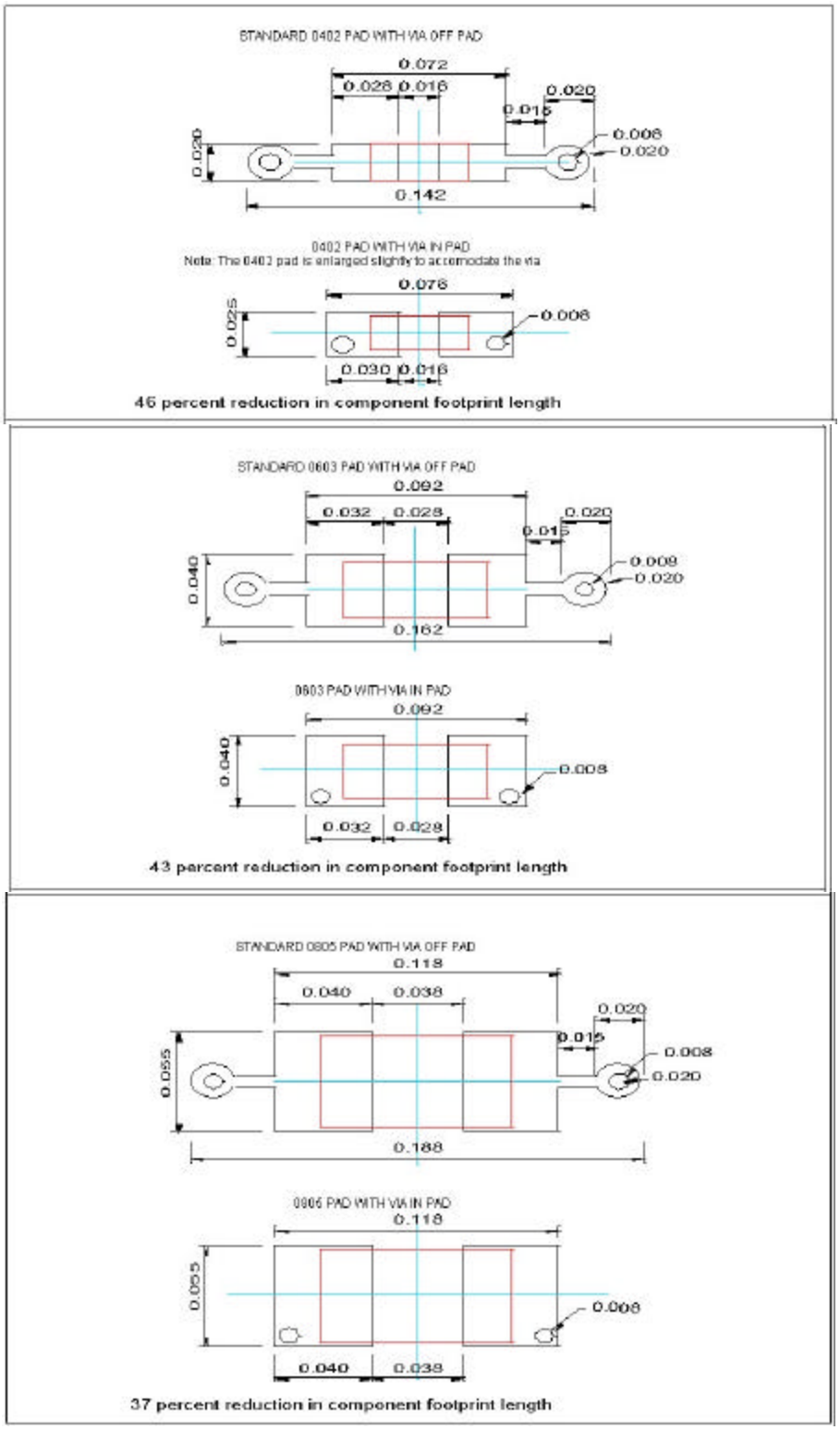
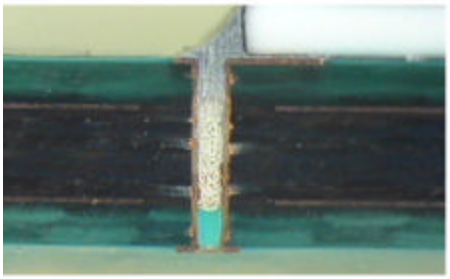


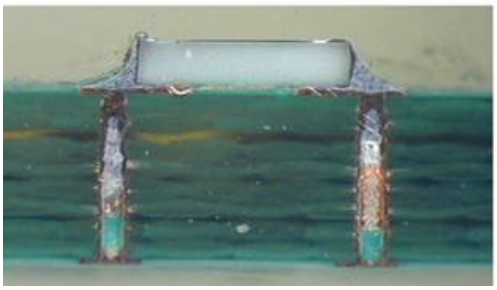
Figure 2 - Standard Pad Patterns used for 0402, 0603 and 0805 Devices Compared with Pad Patterns with Via In Pad Technology

Figures 3-6 show examples of the via in pad results from this study. Cross section examples in Figure 3 are of 0.008" diameter vias. Figures 4- 6 demonstrate the results of various board finishes with via in pad technology.

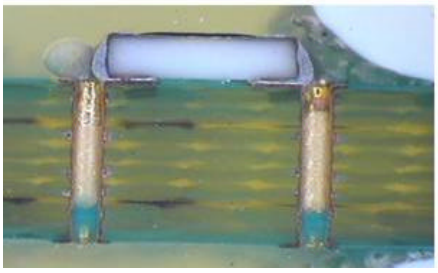
0805 package, .008" dia. via, HASL finish



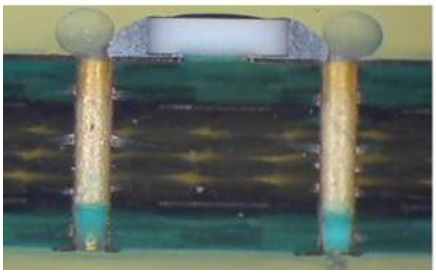
0603 package, .008" dia. via, HASL finish



0603 package, .008" dia. via, gold finish



0402 package, .008" dia. via, gold finish



0805 package, .008" dia. via, silver finish

0603 package, .008" dia. via, silver finish

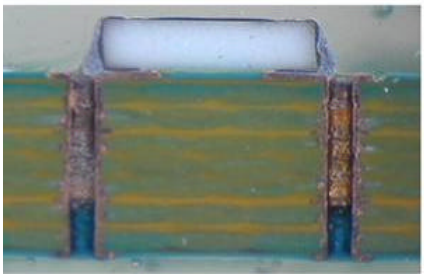


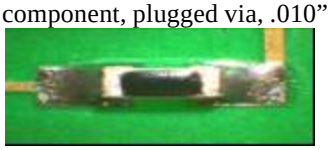
Figure 3 - Cross sections showing examples of .008" finished hole diameter plugged vias with various component packages and board finishes

0402 component, unplugged via, .012” via

0402 component, plugged via, .012” via

0402 component, unplugged via, .010” via

0402 component, plugged via, .010” via\

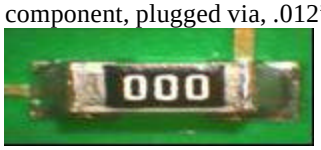


0402 component, unplugged via, .008” via

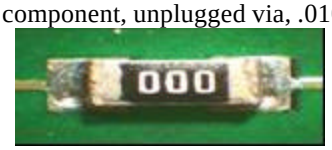
0402 component, plugged via, .008” via

0603 component, unplugged via, .012” via

0603 component, plugged via, .012” via

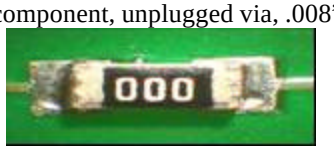


0603 component, unplugged via, .010” via



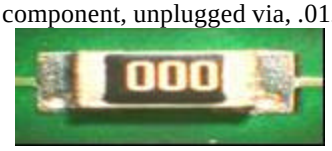
0603 component, plugged via, .010” via

0603component, unplugged via, .008” via

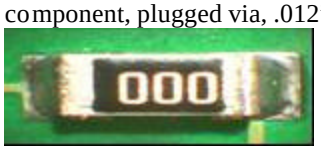


0603 component, plugged via, .008” via

0805 component, unplugged via, .012” via

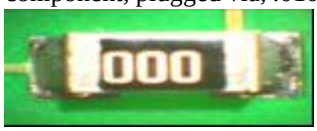


0805 component, plugged via, .012” via

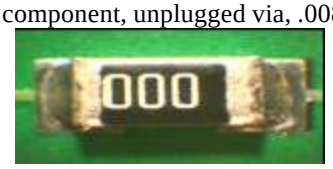


0805 component, unplugged via, .010” via

0805 component, plugged via, .010” via



0805 component, unplugged via, .008” via



0805 component, plugged via, .008” via

Figure 4 - Via in pad examples with HASL board finish

0402 component, unplugged via, .012” via

0402 component, plugged via, .012” via

0402 component, unplugged via, .010” via

0402 component, plugged via, .010” via

0402 component, unplugged via, .008” via

0402 component, plugged via, .008” via

0603 component, unplugged via, .012” via

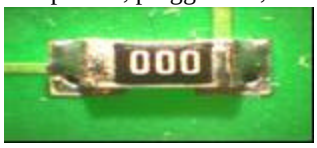
0603 component, plugged via, .012” via

0603 component, unplugged via, .010” via

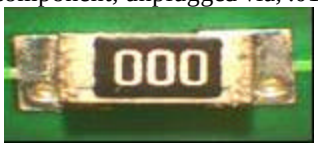
0603 component, plugged via, .010” via

0603 component, unplugged via, .008” via

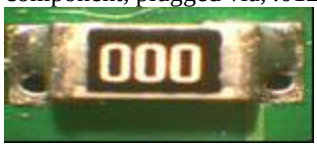
0603 component, plugged via, .008” via



0805 component, unplugged via, .012” via



0805 component, plugged via, .012” via



0805 component, unplugged via, .010” via

0805 component, plugged via, .010” via

0805 component, unplugged via, .008” via

0805 component, plugged via, .008” via

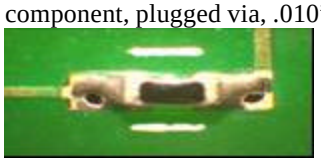
Figure 5 - Via in pad examples with Gold plated board finish

0402 component, unplugged via, .012” via

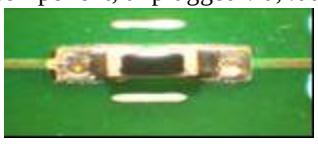
0402 component, plugged via, .012” via

0402 component, unplugged via, .010” via

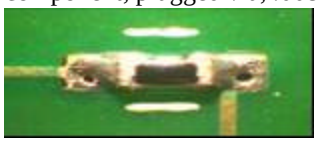
0402 component, plugged via, .010” via



0402 component, unplugged via, .008” via



0402 component, plugged via, .008” via

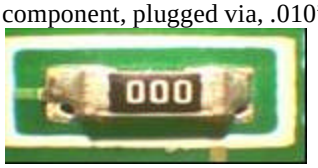


0603 component, unplugged via, .012” via

0603 component, plugged via, .012” via

0603 component, unplugged via, .010” via

0603 component, plugged via, .010” via



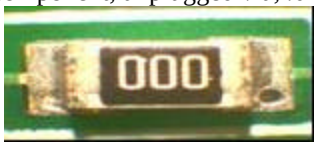
0603component, unplugged via, .008” via

0603 component, plugged via, .008” via

0805 component, unplugged via, .012” via

0805 component, plugged via, .012” via

0805 component, unplugged via, .010” via



0805 component, plugged via, .010” via

0805 component, unplugged via, .008” via

0805 component, plugged via, .008” via

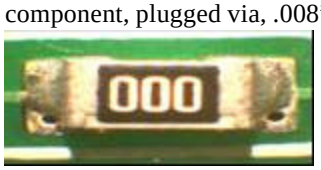


Figure 6 - Via in pad examples with Silver plated board finish

Conclusions

The literature concerning Circuit Design and Emissions Compliance in conjunction with Via in Pad Technology reviewed suggests that the use of this technology will reduce the parasitic capacitance and inductance typically found in high-speed digital circuits. This is accomplished by eliminating the "stub trace" and land which are normally present when a traditional via is utilized. [3] The Design of Experiment showed that the only significant factor for manufacturing was whether the vias were plugged regardless of board finish, component size, or via size. (See Table 1.)

Table 1 - Data from the 3x3x3x2 Factorial Design of Experiment Performed

Average defects by part size		
	Plugged	Unplugged
0402	0.1111	8.2778
0603	0.0000	13.0000
0805	0.0000	9.0000

Average defects by via size		
	Plugged	Unplugged
0.008"	0.0000	3.2222
0.010"	0.0000	12.3889
0.012"	0.1111	14.6667

Average defects by finish		
	Plugged	Unplugged
Gold	0.0000	7.3333
HASL	0.1111	14.1111
Silver	0.0000	8.8333

Average defects by plugged vs. unplugged
Plugged 0.0370
Unplugged 10.0926

It should be noted that the pad design utilized for 0402 components, during this experiment, was slightly oversized and is in the process of being reduced. Ideally, the pad should be reduced to enhance soldering 0402 devices without exceeding the threshold of pad area required to use via in pad technology. This balancing act of pad size designs can be best handled by simply creating two pad designs for each package size. One with via in pad technology and one standard pad for use without via in pad technology. In the case of 0402 components, these pad designs will actually differ slightly in physical size as detailed below (Figure 7-9). For the larger 0603 and 0805 packages this size differential is not necessary. One pad design would simply have the via in it while the other standard pad would not. Having two pad designs for each package will also afford the PCB designers the flexibility to use the pad design that best matches their needs. The dimensions for the 0402 pad that were used for this experiment are shown below along with two proposed new pad designs that can be utilized in the future when via in pad technology is implemented.

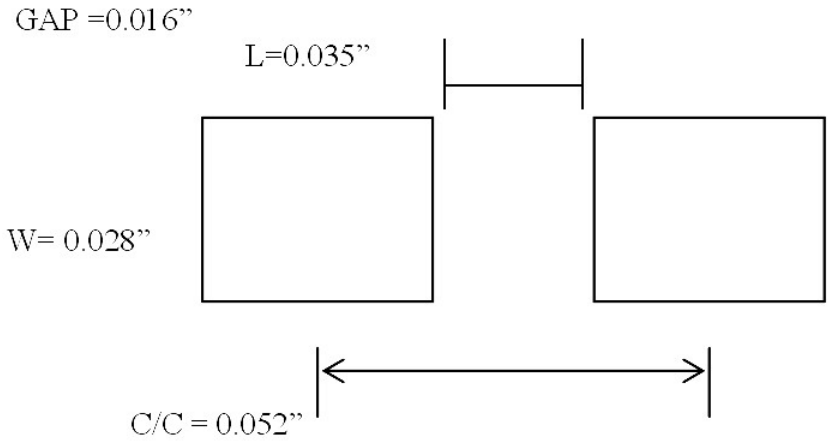


Figure 7 - 0402 Pad Design Used for the Experiment

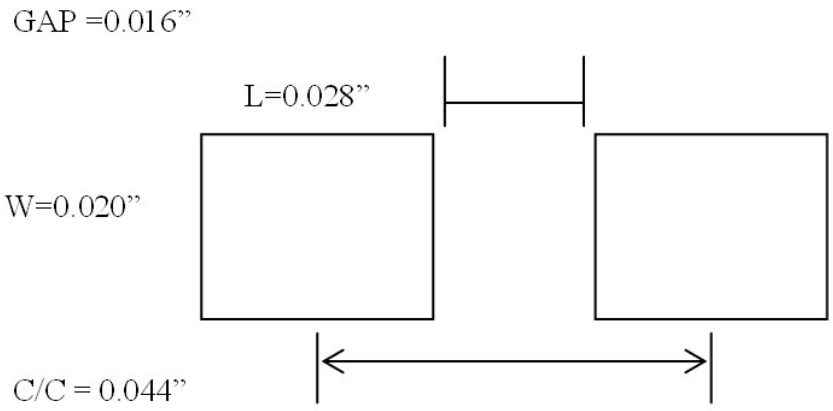


Figure 8 - Standard 0402 Pad Design for use in Non Via In Pad Technology Applications

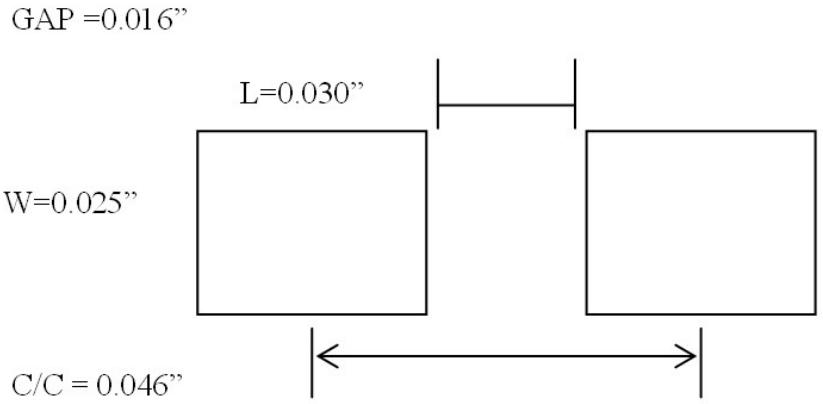


Figure 9 - Suggested 0402 Pad Design for Use in Via In Pad Technology Applications

Cross sections and visual images of the solder joints achieved when utilizing this technology indicated no reliability concerns. Requirements for IPC-A-610-C class 2 were satisfied.

An area that requires consideration is that of In-circuit Test (ICT) testability impact. As mentioned previously, a plugged via on the bottom side of the PCB will be a requirement in order for via in pad technology to be successful. However, this would create a problem if an ICT fixture was using a via for a test point. In this case, there would be potential that the test probe might not make contact if it hit residual plugging material on the vias land. The solution for this is that any via to be utilized for ICT access should not be a candidate for via in pad technology. Prior to ordering PCB’s, the ICT group would need to communicate with the board layout group detailing which points they would require to be left unmasked and accessible.

Training will be necessary for board level inspectors if this technology is implemented. This is simply due to the fact that the solder joints may appear different from a typical solder joint. A sunken area or even a small hole may be visible in the outer corner of the pad. This deviation from the typical appearance does not imply a bad solder joint. IPC-A-610 Rev. C can still easily be achieved even though the geometry of the joint may be different. For Class II products an acceptable solder joint for a chip component is defined as follows, “a properly wetted fillet is evident”. This is certainly achievable even though a depression or a hole may be visible in the outer corner of the pad.

Discussions with existing board suppliers indicate that PCB fabrication technology has developed to the point that achieving a via diameter size down to .008” is possible without incurring additional fabrication cost for the end user. However, it is notable that this diameter would be achieved by over drilling the hole and plating back down to the desired hole size. In other words, to achieve a .008” finished hole diameter via, a 0.014” diameter hole would actually be drilled and then the hole would be plated back to the specified size. Regardless of the means, this method should not affect the end result and should not present a problem. The one issue with the implementation of via in pad technology is that according to this study the vias will have to be plugged in order to insure success. This raises the question of potential additional cost by the board houses to perform this extra process. Research suggests that an approximate cost per PCB of 2 to 3 percent could be incurred for this additional process, depending on the specific arrangement with your PCB supplier. We found that we would incur no cost increase on 85 percent of our PCB’s purchased due to the specific arrangement we have with our primary PCB supplier. The remaining 15 percent could see the 2 to 3 percent cost increase. As PCB suppliers are added and removed from the AVL, this

area for potential added cost should be given consideration. This should apply to prototype PCB suppliers and production PCB suppliers alike.

Recommendations

Based on the findings detailed in this study, the following recommendations can be made. The use of via in pad technology can be used to reduce parasitic capacitance and inductance on high-speed digital circuits and can also be used where routing is restricted by dense, complex designs in order to free up valuable PCB surface real estate. As a minimum the following actions should be taken prior to the implementation of this technology:

- Process Engineering and PCB Layout groups need to develop pads for the use of this technology. As detailed previously, two 0402 pads should be developed due to the small size of the pads. As for 0603 and 0805 pads, their size will not need to change to accommodate this technology. For all three packages, 0402, 0603, and 0805, new pad designs will need to be developed for the CAD library. This will result in two sets of pads, one standard and one with via in pad technology.
- The ICT group and PCB layout group will need to work together closely in order to insure that no required test access points are candidates for via in pad technology. The via plugging required for use with via in pad technology could make the via inaccessible for a test contact point on the bottom side of the PCB.
- Manufacturing, Quality and Inspection groups, as well as any subcontractors used will need to be made aware of the intended use of this technology. Training in the use and inspection of this technology will be required in these areas.

References

1. "High Speed Digital Design, A Hand Book of Black Magic" by Howard Johnson and Martin Graham; Published in 1993 by Prentice Hall PTR, Upper Saddle River, NJ 07458
2. "Noise Reduction Techniques in Electronic Systems" Second Edition by Henry W. Ott; Published 1988 John Wiley & Sons, Inc. New York, New York
3. "High Speed Transmission Line Requirements: Impact on Performance, PCB Layout, Fabrication and Reliability" by Subhash Pochareddy, Lavanya Gopalakrishnan and Rajat Srivastava CircuiTree June 2003; Published in 2003 by Business News Publishing Co., Troy, Michigan 48084