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Solder Joint Reliability Qualification of Various Component Mounting Modification Configurations Using Thermal Cycle Testing

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Abstract
The selection and use of solder joint modification configurations for printed wiring assemblies has traditionally been a design specific activity. The implementation and use of a standardized set of solder joint modification configurations on an industry-wide basis would be cost effective and promote industry consistent modification practices. A set of 14 commonly used IPC Class 3 modification configurations were selected for investigation. Thermal cycle testing was chosen to evaluate the solder joint thermal cycle fatigue reliability of the configuration set. A total of 1,972 thermal cycles using a -55ºC to +125ºC recipe in accordance with the IPC-9701 guidelines were completed. Failure analysis and photo-documentation were conducted characterizing modification configuration solder joint geometries and wetting angles. The investigation results/recommendations were disseminated to the IPC-A-610 and IPC-7711/7722 specification committees for potential use.

Background
The design and fabrication of printed wiring assemblies is not an exact science. The interaction of circuit functions can not always be anticipated or modeled. Radio frequency (RF) and microwave electrical circuit designs can often produce undesirable electronic signal responses in segments of the electrical design. The need for having the methodology and procedures for modifying printed wiring board circuit traces, component pads, and plated thru holes is an essential skill in the production of electronic equipment. Additionally, possessing the ability to modify a printed wiring assembly can be a cost and/or schedule saver when a printed wiring board fabrication process results in a nonconforming condition. The nature of printed wiring assembly modification practices can be process of singular, product specific solutions. However, manufacturing processes which utilize consistent, reproducible procedures result in high yields and fewer defects. Finding and maintaining a balance between the product specific solution and a consistent/reproducible process is key for a high performance electronic manufacturer. Failure to maintain such a balance can result in product field failures and low manufacturing yield. Figure 1 illustrates a poor solder joint modification design. Two ceramic chip capacitor components were adhesively bonded to the printed wiring board surface. Attachment wires were soldered to one of the capacitor terminations and the other termination soldered to a component thus meeting an electrical functionality need. However, thermal mismatch of the ceramic capacitors, the printed wiring board, bonding adhesive and the attachment wires resulted in capacitor failure.

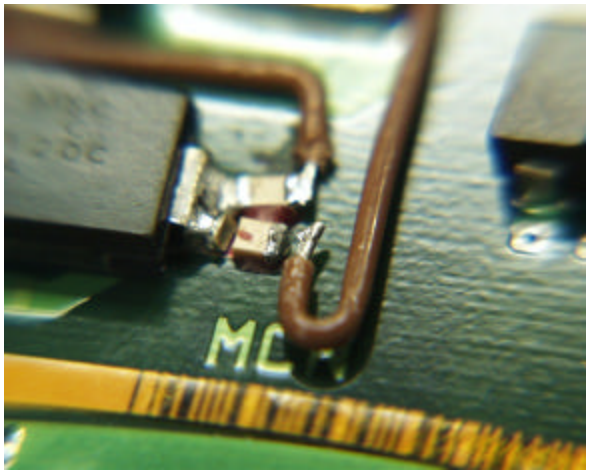


Figure 1 - Modification Design Failure

The use of a standardized set of solder joint modification configurations used on an industry-wide basis would be highly advantageous. The qualification of solder joint thermal cycle fatigue reliability of a standardized modification configuration set would be extremely useful in customer discussions.

Objectives

The objective of the investigation was to determine the solder joint thermal cycle fatigue reliability of a standardized solder joint modification configuration set. The investigation results and recommendations would be disseminated to the IPC-A-610 and IPC-7711/7722 specification committees for potential incorporation. The vibrational solder joint integrity aspects of the solder joint modification configurations were not addressed in the study because of product design and product use environment considerations. The vibrational solder joint integrity aspects are the responsibility of the product design team and should be addressed as a segment of product qualification.

Test Methodology

Test vehicle

Two board laminate materials were used in the investigation: 1) an FR4 laminate which was 0.060 inches thick; 2) a bismailimide triazine (BT) which was 0.031 inches thick. The construction of the test vehicles included two 1 ounce copper internal layers with a typical hot air solder leveled (HASL) surface finish. The FR4 laminate test vehicle was the laminate of primary interest. The BT laminate test vehicle was included in the investigation for comparison purposes. A series of various surface mount chip resister and chip capacitor pad geometries were selected. The component pad geometries were connected to plated thru holes configured to permit continuous electrical monitoring. Figure 2 illustrates the FR4 test vehicle.

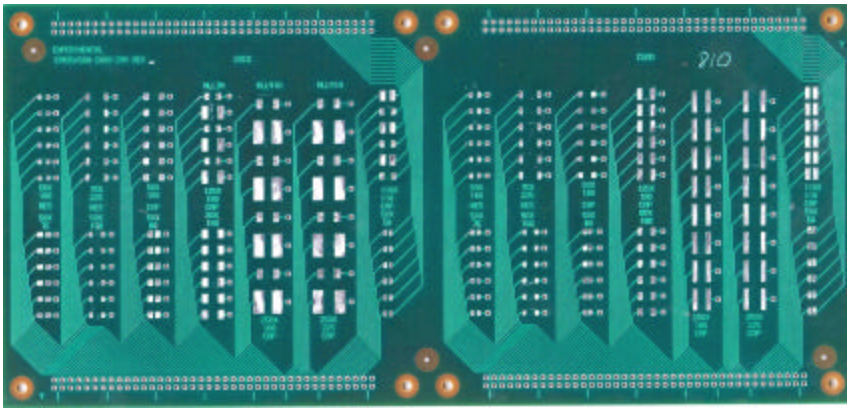


Figure 2 - FR4 Test Vehicle

Test components

A number of surface mount chip resistors and chip capacitors were used to construct the various modification configurations. Larger sized chip components were selected for the investigation as they represented a "worst case" scenario for test vehicle/component CTE mismatch stress. In addition to the chip resistors and chip capacitors, one metal film axial resistor commonly used in production was used for one modification configuration. Table 1 lists the different component types used in the investigation.

Table 1 - Investigation Components

Chip Capacitors	Chip Resistors	Axial Resistor
50 x 180	60 x 120	90 dia x 250 length
250 x 180	100 x 200	
250 x 180		
250 x 220		
Note: dimensions in mils		

Assembly

The expertise of an experienced rework operator was utilized to construct the 14 solder joint modification configurations. The modification configurations were chosen as they represented common IPC Class 3 modification constructions found on printed wiring assemblies. Figures 3-16 illustrate each of the modification configurations used in the investigation.

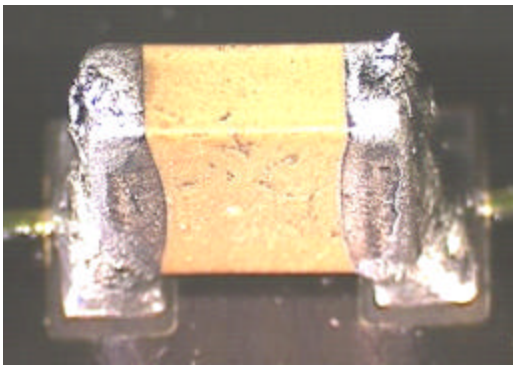


Figure 3 – Modivication A – 1812 Capacitor "Billboarded"

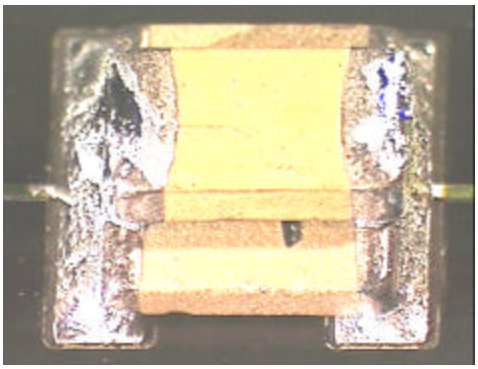


Figure 4 – Modification B – 1812/1825 Capacitor "Piggybacked"

Figure 5 – Modification C – Two 2010 Resistors "Piggybacked"

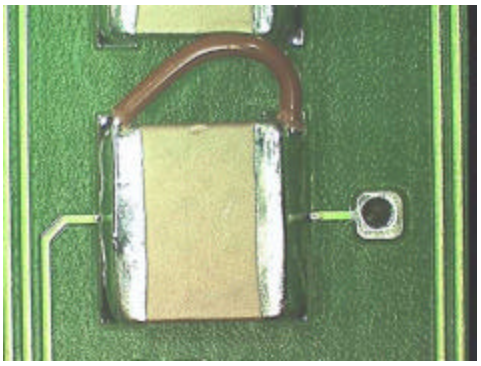


Figure 6 - Modification D - 2225 Capacitor With 2 Add Wires

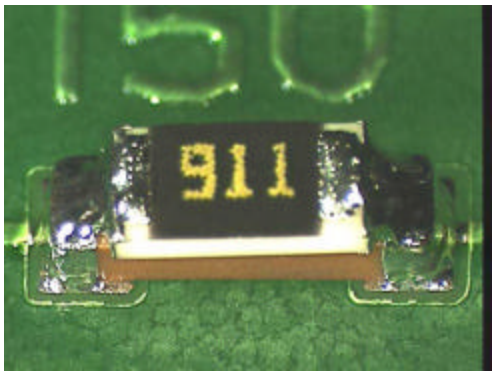


Figure 7 - Modification E - 1206 Resistor/1550 Capacitor "Piggybacked"

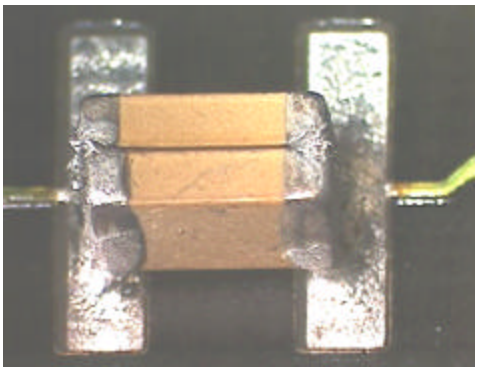


Figure 8 - Modification F - 1812/2225 Capacitors "Billboarded"

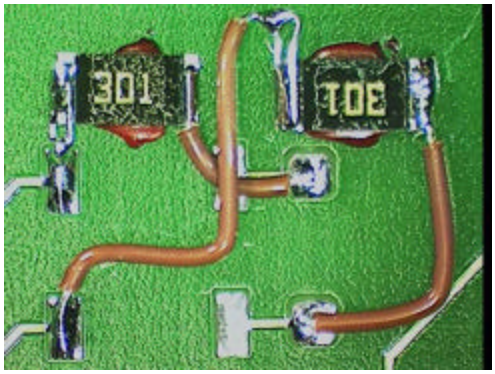


Figure 9 - Modification G - 2010 Resistor Adhesive Bonded On Laminate

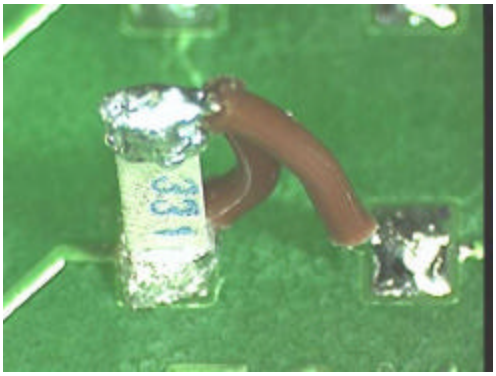


Figure 10 - Modification H - 1805 Capacitor "Tombstoned" With 2 Add Wires

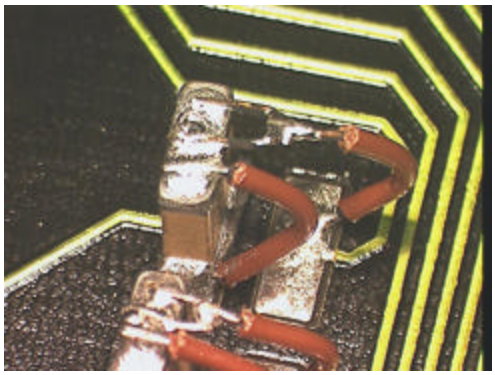


Figure 11 - Modification I - 1812 Capacitor "Tombstoned" With 3 Add Wires

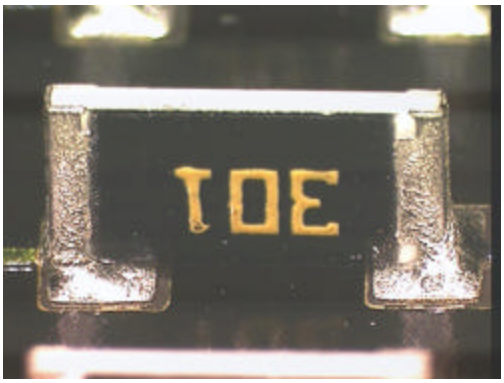


Figure 12 - Modification J - 2010 Resistor "Billboarded"

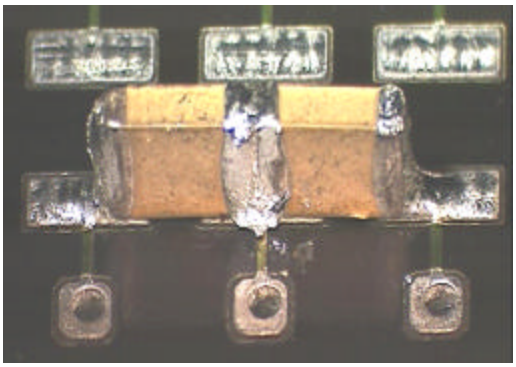


Figure13 - Modification K - Two 1812 Capacitors "In-Line Billboarded"

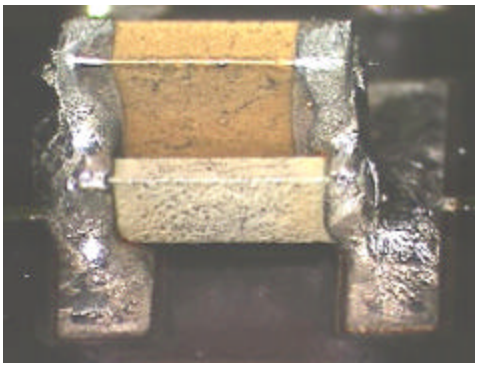


Figure 14 - Modification L 1805/1812 Capacitors "Shared Pad- Billboarded"

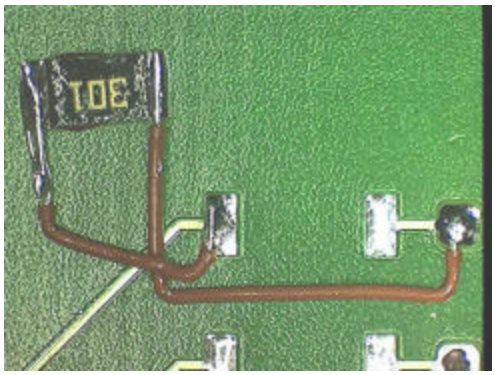


Figure 15 - Modification M - 2010 Resistor Adhesive Strip Bonded On Laminate

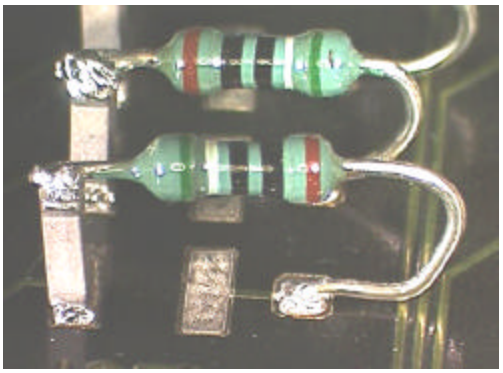


Figure 16 - Modification N - 1808 Capacitor "Billboarded"/Axial Resistor

A limited but statistically valid sample size was used for the investigation. Table 2 lists the sample population comprising each modification construction.

Table 2 - Modification Sample Populations

Modification Construction	Number of Test Samples	Test Vehicle ID Number
A	24	1 & 2
B	32	1 & 2
C	32	3 & 4
D	64	5 & 7
E	24	5 & 7
F	32	1 & 2
G1	12	1 & 2
G2	12	1 & 2
H	24	5 & 7
I	24	1 & 3
J	24	3 & 4
K	12	1 & 2 & 3
L	16	3 & 4
M	15	3 & 4
N	36	4 & 5 & 7

Two of the modification configurations, modification G and modification M, required the use of adhesive materials. These two modifications are used on printed wiring assemblies were the necessary pad geometries are either not available or not located in the region of the interest. Table 3 lists the adhesives used for the modifications.

Table 3 - Adhesives Used in the Modification Construction

Modification Construction	Adhesive Type	Cure Recipe
Modification G1	Epoxy	125ºC for 60 minutes
Modification G2	Epoxy	125ºC for 60 minutes
Modification M	Adhesive Strip (PWB)	N/A
	Epoxy (Component to Strip)	125ºC for 10 minutes

The assembly of the various modification constructions was done in conjunction with specific test vehicles which were each assigned an identification number. This practice was done to aid in the thermal cycle testing and failure analysis segments of the investigation. Table 4 lists the different test vehicle/modification construction combinations.

Table 4 - Test Vehicle/Modification Configuration Combinations

Test Vehicle ID Number	Modifications Used	Laminate Type
1	A, B, F, G I, K,	FR4
2	A, B, F, G, K,	FR4
3	C, I, J, K, L, M	FR4
4	C, J, L, M, N	FR4
5	D, E, H, N	FR4
6	Baseline	FR4
7	D, E, H, N	BT
8	Baseline	BT

Flux residues were removed from the test vehicles using manual and automated cleaning methods. Extreme care was exercised during the cleaning operations to insure that the modification configurations were not damaged.

Solder Joint Integrity Monitoring

Solder joint integrity was quantified by measuring the electrical continuity of all components throughout thermal cycle testing. Electrical continuity was monitored by an event detector. The event detector continuously monitored the electrical

resistance of each electrical channel, which in this case consisted of one component. A failure was recorded if the channel resistance exceeded 300 O for longer than 0.2 µsec in a 30-second period. The event detector recorded the total number of individual failures and the failure rate after first detection. A component was removed from the test vehicle for failure analysis if it read open/high resistance at room temperature and the failure rate was above 60%. Component failure was designated as the cycle at which it first recorded a failure by the event detector. The incorporation of chip capacitor components provided a monitoring complication. The lack of electrical resistance continuity of capacitors required a bypass wire be incorporated into modification configurations. The bypass wires were added to the modification configurations with negligible impact to the solder joints. Additionally, metallographic cross-sectional examinations were included in the failure analysis segment of the investigation to determine that a solder joint failure was not attributable to a bypass wire.

Thermal Cycle Conditioning

All modification configurations were tested using accelerated thermal cycling test procedures based on the IPC-9701 specification. The thermal cycle profile used ten minute minimum dwell times at -55°C and 125°C and a maximum ramp rate of 10°C/min between the two temperature extremes. The test vehicles were loaded into the thermal cycle chamber allowing for adequate air circulation. Thermal couples were attached to the test vehicles and several thermal cycles completed to insure that the test vehicles temperature variation was no greater than +/- 3ºC.

Test Results

A total of 1,972 thermal cycles were completed for the investigation. Table 5 lists the number of failures recorded for each modification construction in the investigation.

Table 5 - Thermal Cycle Testing Modification Failures

Modification Construction	Number of Failures	Average First Failure Cycle
A	1 of 24	1963
B	0 of 32	1972
C	4 of 32	1951
D	0 of 64	1972
E	24 of 24	1752
F	0 of 32	1972
G (1 & 2)	24 of 24	1752
H	0 of 24	1972
I	0 of 24	1972
J	24 of 24	1578
K	0 of 12	1972
L	0 of 16	1972
M	15 of 15	1649
N	36 of 36	1752

Discussion

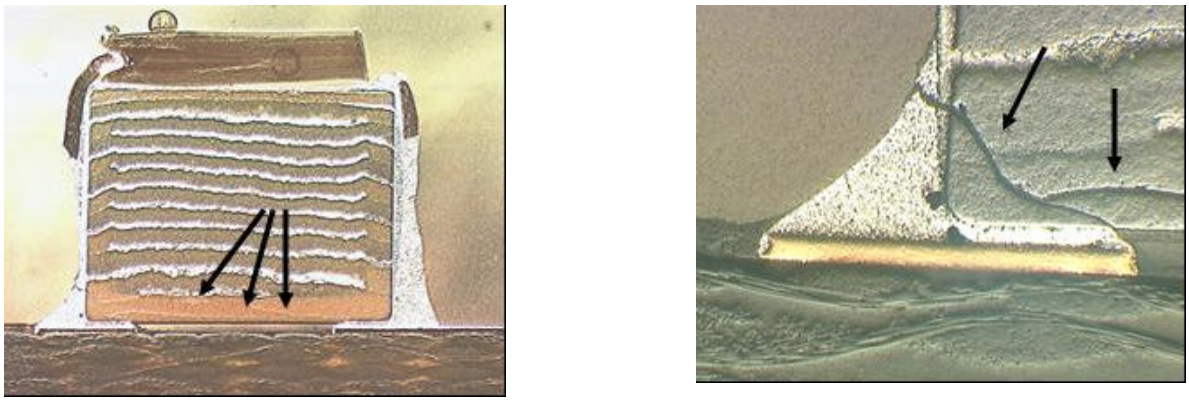
A detailed discussion of each modification construction test results is as follows:

Modification Constructions With No Failures

A number of the modification constructions completed the thermal cycle testing without registering a solder joint failure. These modification include Modification B “Piggybacked Capacitors”, Modification D “Capacitor with 2 Add Wires”, Modification F “Billboarded Capacitors”, Modification H “Tombstoned Capacitor with 2 Add Wires”, Modification I “Tombstoned Capacitor with 3 Add Wires”, Modification K “In-Line Billboarded Capacitors”, and Modification L “Shared Pad Billboarded Capacitors”. These modification configurations can be considered acceptable and should form the initial standardized modification configuration set.

Modification Construction A

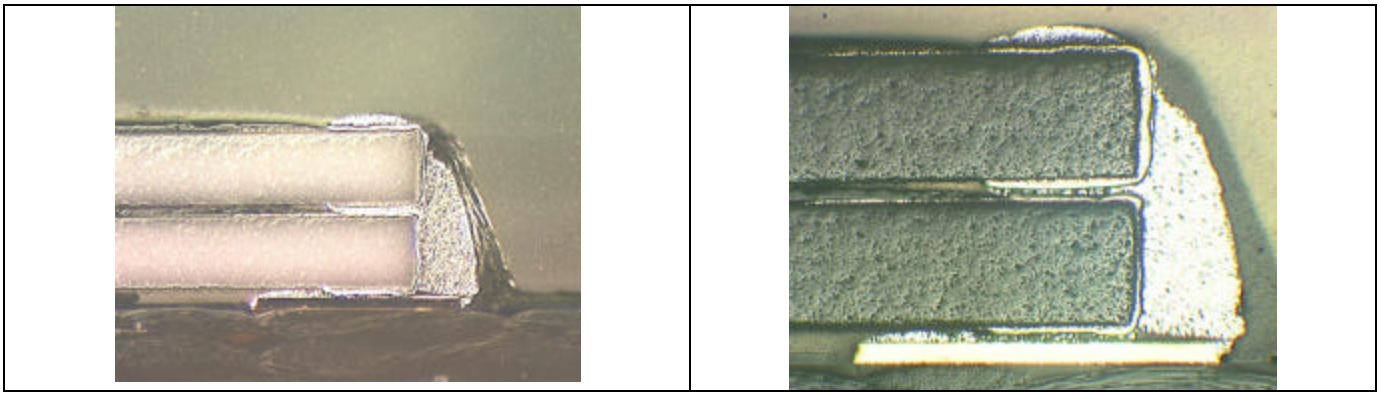
Modification construction A was the "Billboarded Capacitor" and registered one failure out of a population of 24 samples. The one failure occurred at thermal cycle 1963 – within 10 cycles of the total thermal cycles completed in the test. Examination of the failed sample after microsectioning shows a corner crack in the capacitor (see Figure 17). Possible crack sources could be either thermal shock due to improper soldering technique or mechanical damage due to handling issues.[1] None of the other Modification Construction A samples revealed any crack damage. The solder joint failure illustrates a potential problem with non-standard mounting of capacitors on printed wiring assemblies. Handling procedures need to be reviewed to insure that capacitors have a low risk of being damaged. The author's recommendation would be to include Modification construction A in the initial standardized modification configuration set.



Figures 17 - Modification A Capacitor Crack – Arrows Indicates Crack in Capacitor

Modification Construction C

Modification construction C was the "Piggybacked Resistors" and registered four failures out of a population of 34 samples. The four failures occurred at the following thermal cycle intervals: 1752, 1752, 1752, and 1972. Examination of the failed samples after microsectioning did not reveal any anomalies which would be a specific source cause of the solder joint failures (see Figure18). The thermal cycle failure intervals are relatively high demonstrating the modification construction had reasonable robustness. However, modification construction C should be limited for chip resistor components no larger than the 2010 geometry used in the investigation until further reliability studies are conducted.



Figures 18 - Modification C Microsectioning Views

Modification Construction E

Modification construction E was the "Piggybacked Resistor/Capacitor" combination and registered 100% failure of a population of 24 samples (12 samples on the FR4 test vehicle and 12 samples on the BT test vehicle). Examination of a number of the failed samples after microsectioning revealed the source cause of the solder joint failures. The resistor terminations did not overlap the capacitor terminations creating a solder bridge which did not withstand the CTE mismatch imposed by the thermal cycle conditioning (see Figure 19). Although the majority of the modification construction E solder joints failed at a relatively large thermal cycle interval – 1752 cycles – the failure mode illustrates the danger of creating a solder bridge. R.J. Klein Wassink previously documented the poor reliability of solder bridging/thickness.[2] The modification construction E failures demonstrate that overlapping component terminations must be required for "piggybacked" constructions. Modification construction E was recommended for inclusion in the initial standardized modification configuration set provided an overlapping component termination rule would be instituted.

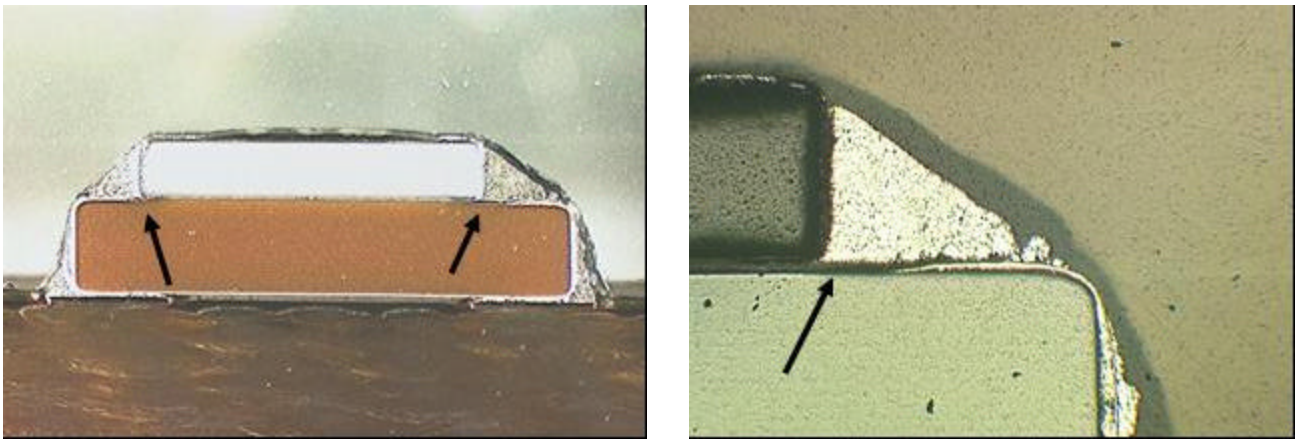


Figure 19 - Modification E Solder Bridge – Arrows Indicate Solder Bridge Between Components

Modification Construction G1 & G2

Modification construction G1 & G2 was the "Adhesive Bonded/Resistor" combination and registered 100% failure of a population of 24 samples. Examination of a number of the failed samples after microsectioning did not reveal any specific source cause of the solder joint failures (see Figure 20). However, the majority of the modification construction G1/G2 solder joints failed at a relatively larger thermal cycle interval – 1752 cycles. Implementation of better strain relief in the attachment wire would result in an increased solder joint thermal cycle fatigue life. Modification construction G1& G2 were recommended for inclusion in the initial standardized modification configuration set provided strain relief rules would be followed.

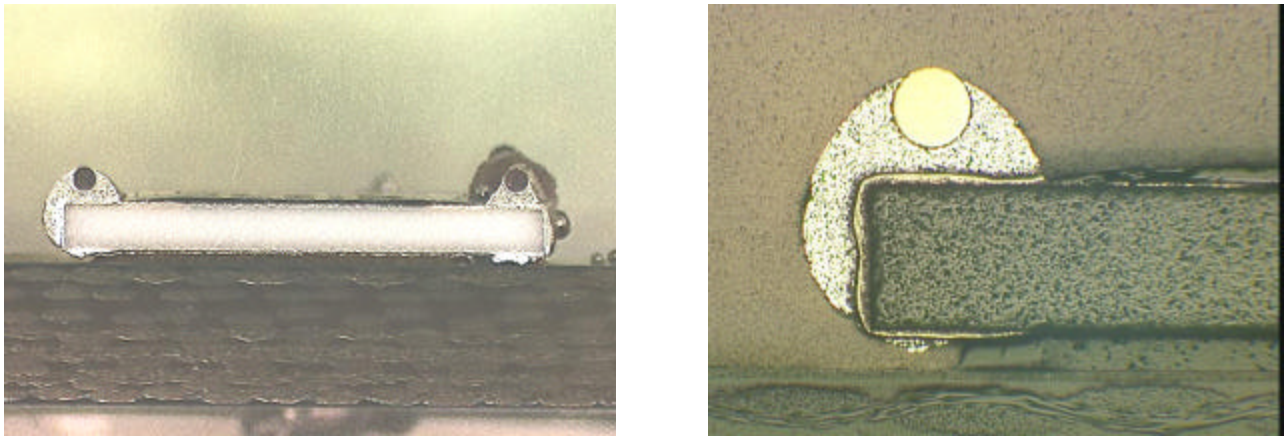
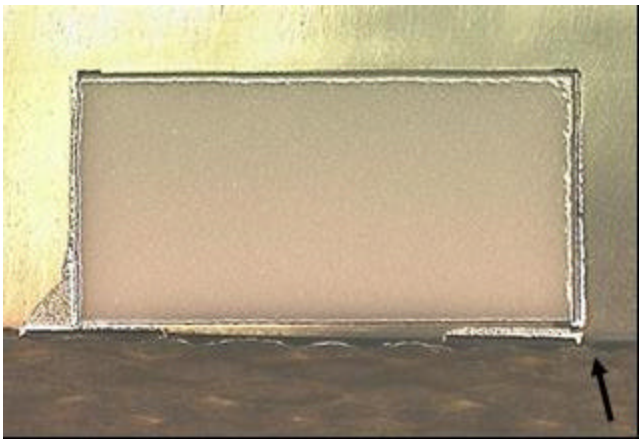


Figure 20 - Modification G1/G2 Microsectional View

Modification Construction J

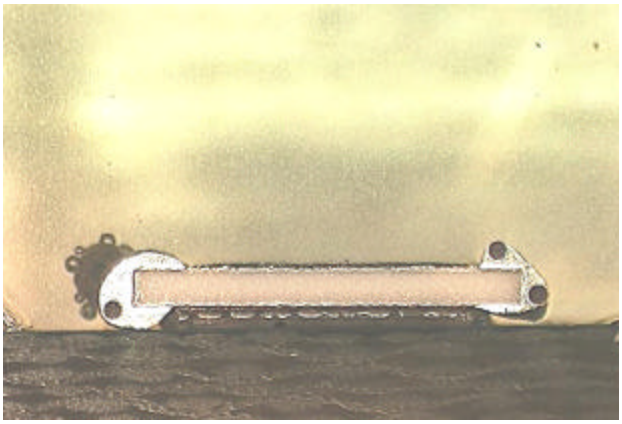
Modification construction J was the "Billboarded Resistor" and registered 100% failure of a population of 24 samples. Examination of a number of the failed samples after microsectioning revealed the source cause of the solder joint failures. Incorrect positioning of the resistor terminations in relation to the test vehicle pads resulted in minimal solder joint fillets for one of the two component terminations. Modification construction J minimal fillet solder joints failed much earlier than a standard solder joint fillet – J minimal fillet solder joint failures occurred in the 728-941 thermal cycle interval range in comparison to standard fillet solder joints failures occurring in the 1752-1972 thermal cycle interval range. The thermal cycle testing results demonstrated that proper component/pad dimensioning is required to meet thermal cycle fatigue reliability expectations. Figure 21 illustrates the solder joint fillet disparity. Modification construction J was recommended for inclusion in the initial standardized modification configuration set provided component/pad dimensioning rules would be followed.



**Figures 21 - Modification J Solder Fillet Disparity –
Arrow Illustrates Improper Component Termination/Component Pad Spacing**

Modification Construction M

Modification construction M was the "Adhesive Strip/Resistor" combination and registered 100% failure of a population of 15 samples. Examination of a number of the failed samples after microsectioning did not reveal any specific source cause of the solder joint failures (see Figure 22). Although the majority of the modification construction M solder joints failed at a relatively large thermal cycle interval – 1649 cycles – two interacting factors are know to have played a role in solder joint failures. The interaction of the attachment wire with minimal strain relief and the adhesive strip under the CTE mismatch conditions contributed to the formation and propagation of solder joint cracks. The implementation of better strain relief in the attachment wire and an improved adhesive strip attachment material would have increased the solder joint thermal cycle fatigue life. modification construction G, using adhesive attachment methodology, had better solder joint thermal cycle fatigue life than modification configuration M (1752 thermal cycles versus 1649 thermal cycles). The authors did not recommend modification construction M for inclusion in the initial standardized modification configuration set due to the improved thermal cycle solder joint fatigue of the adhesive attachment methodology.



Figures 22 - Modification M Microsectional View

Modification Construction N

Modification construction N was the "Billboarded Capacitor/Axial Resistor" combination and registered 100% failure of a population of 36 samples (24 samples on the FR4 test vehicle and 12 samples on the BT test vehicle). Examination of a number of the failed samples after microsectioning revealed the source cause of the solder joint failures. The lack of a strain relief loop on the axial resistor lead in contact with the capacitor termination resulted in a solder joint crack due to the CTE mismatch imposed by the thermal cycle conditioning (see Figure 23). Although the majority of the modification construction N solder joints failed at a relatively larger thermal cycle interval – 1752 cycles – the failure mode illustrates the danger of not having adequate strain relief of a component lead. Modification construction N was recommended for inclusion in the initial standardized modification configuration set provided strain relief rules would be followed.

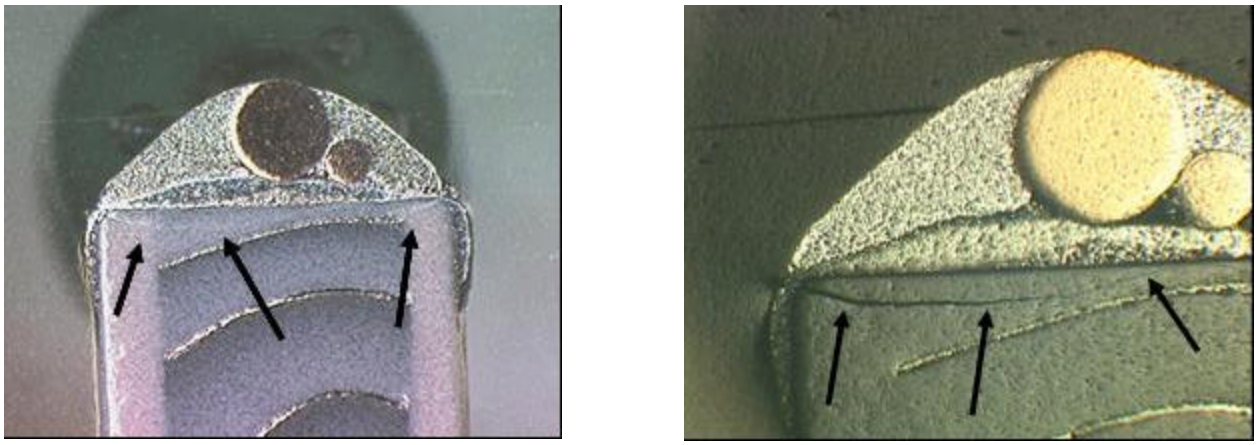


Figure 23 - Modification N Capacitor Crack - Arrows Indicate Crack in Capacitor

Standard Constructions

An initial review of the standard construction results were unanticipated – a 100% failure rate was recorded for the 1206 resistors on the 50 x150 pad field and 100% failure rate was recorded for the 2010 resistors on the 50 x 150 pad field. All other components on the standard test vehicles recorded no failures. However, examination of the failed component microsections revealed an obvious error in the DOE test plan. The 1206 and 2010 resistors are too large for the 50 x150 pad field resulting in minimal/poor solder joint fillets (see Figure 24). Despite the unacceptable component/pad dimensioning situation, the 1206/2010 solder joints failed at a relatively large thermal cycle interval – 1752 cycles – indicating the robustness of surface mount component solder joints. Hillman and Baker demonstrated a similar result for surface mount chip component overhang.[3] It should be noted that the inclusion of the FR4 and Bt test vehicles did not influence the failure issue.

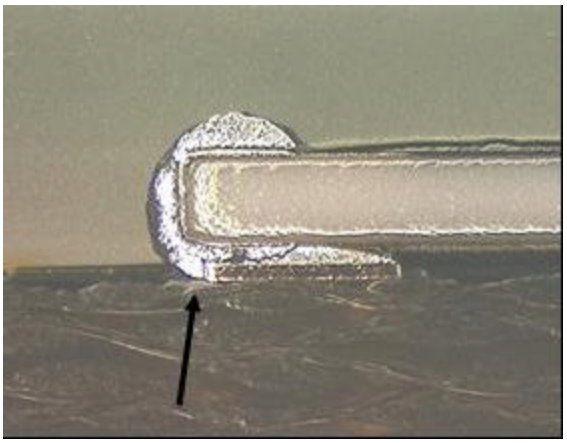


Figure 24 - Standard Construction Microsectional Views - Arrow Illustrates the Improper Component Termination/Component Pad Dimensioning

Workmanship Criteria For Modification Configurations

A set of workmanship criteria for the tested modification configurations was created for potential use by IPC specification committees. These workmanship criteria were intended to promote consistency and repeatability of solder joint formation. The following summaries/illustrations capture the critical wetting and geometry parameters as identified in the test results analysis.

Modification A and Modification J

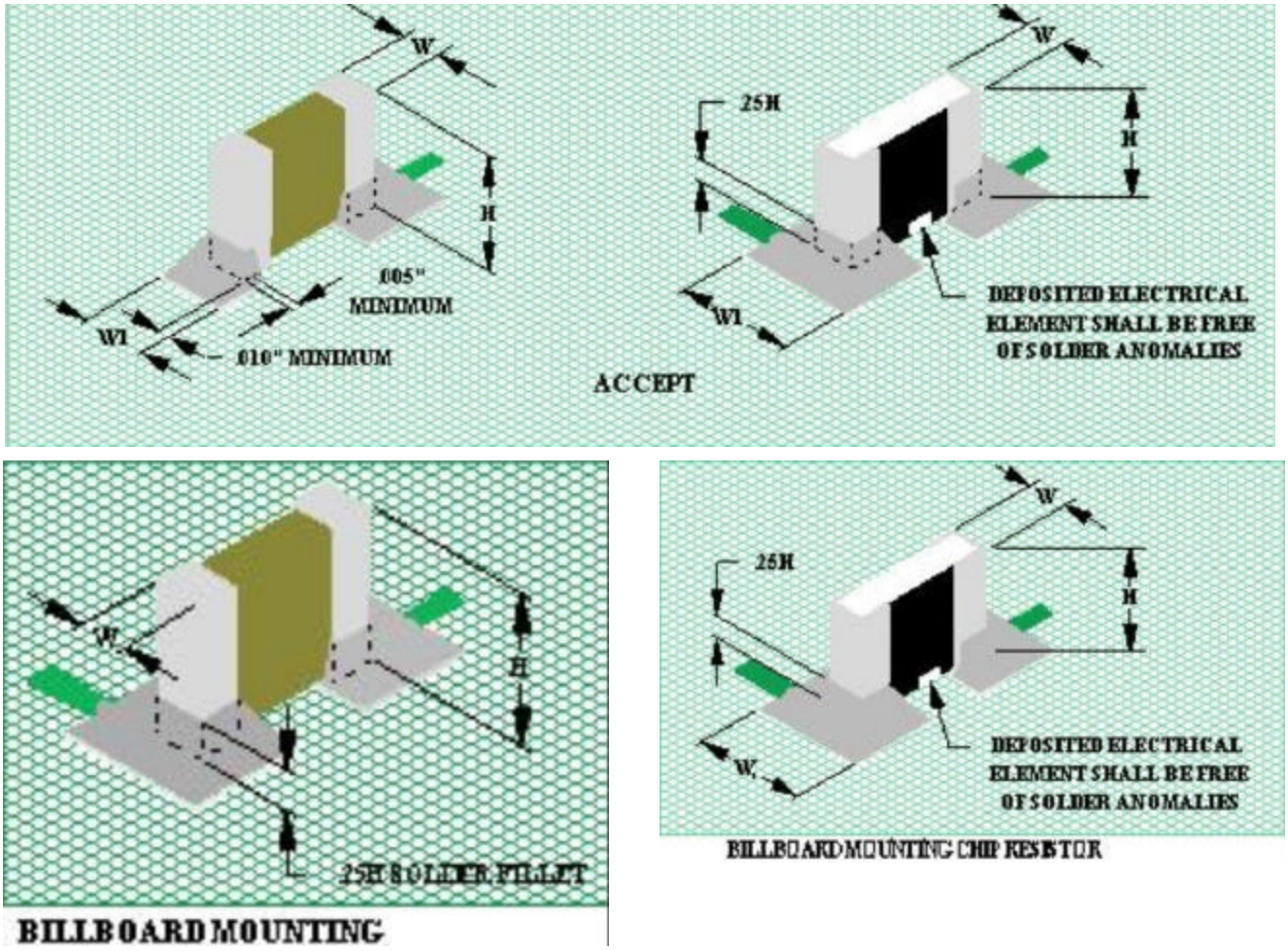


Figure 24 - Modification A and Modification J, - Acceptance Criteria Illustrations

Design Requirement

a) Component end metallization shall be on 3 sides minimum.
b) No end overhang.
c) The end metallization of the chip shall contact the pad .005" minimum both ends.
d) No side overhang.
e) The periphery of the pad shall extend .010"minimum beyond the end and both sides metallization of the component on both ends. **W1** shall be .020" greater then **W**.
f) **H** shall not exceed .250".
g) The height **H** may be greater than the width **W**.
h) Solder fillet shall be a minimum of **.25H** on all three metallized surfaces of the component on both ends.
i) The deposited electrical element of a resistor shall be free of solder and solder anomalies.

Modification F, Modification K and Modification L

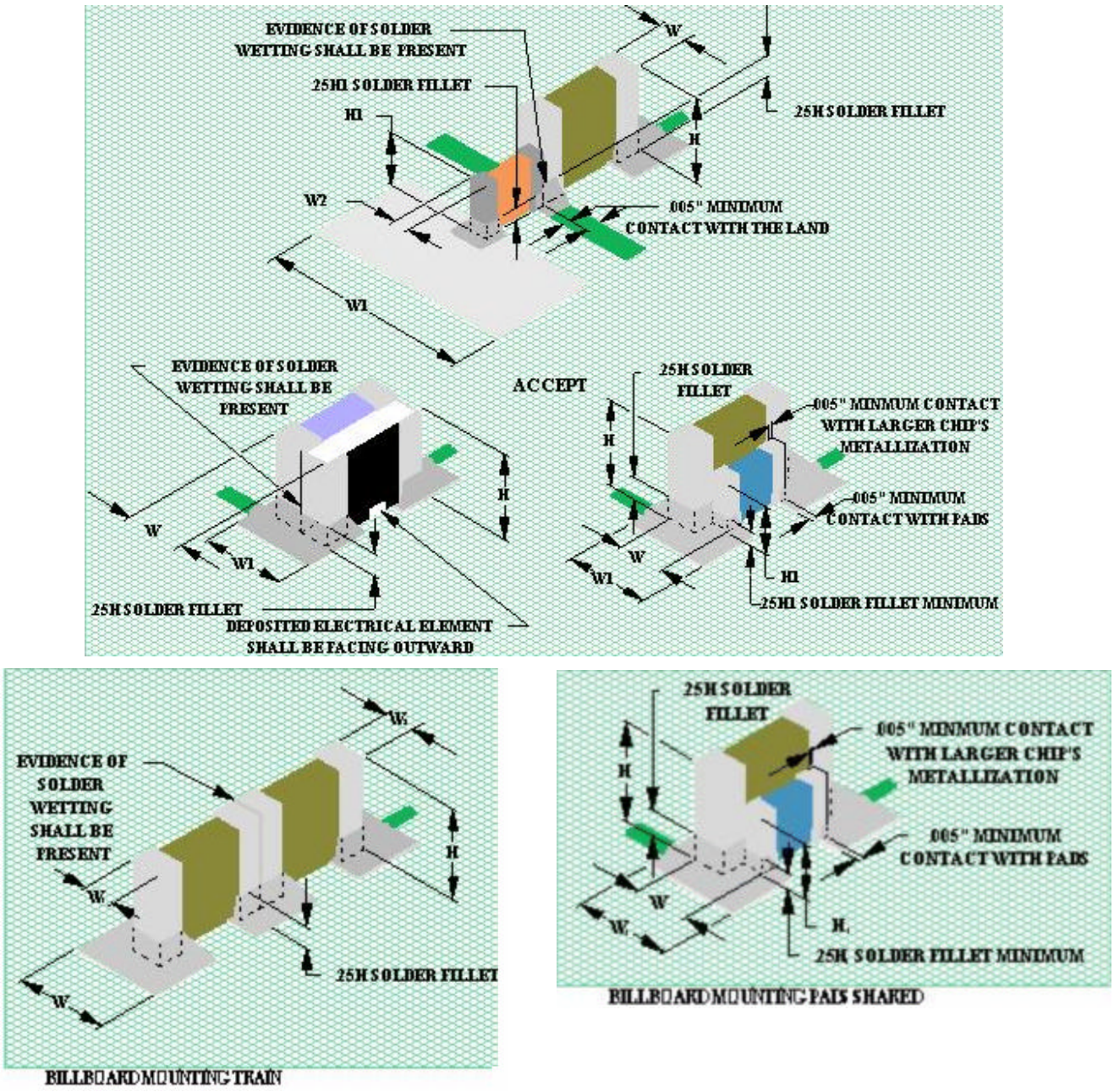
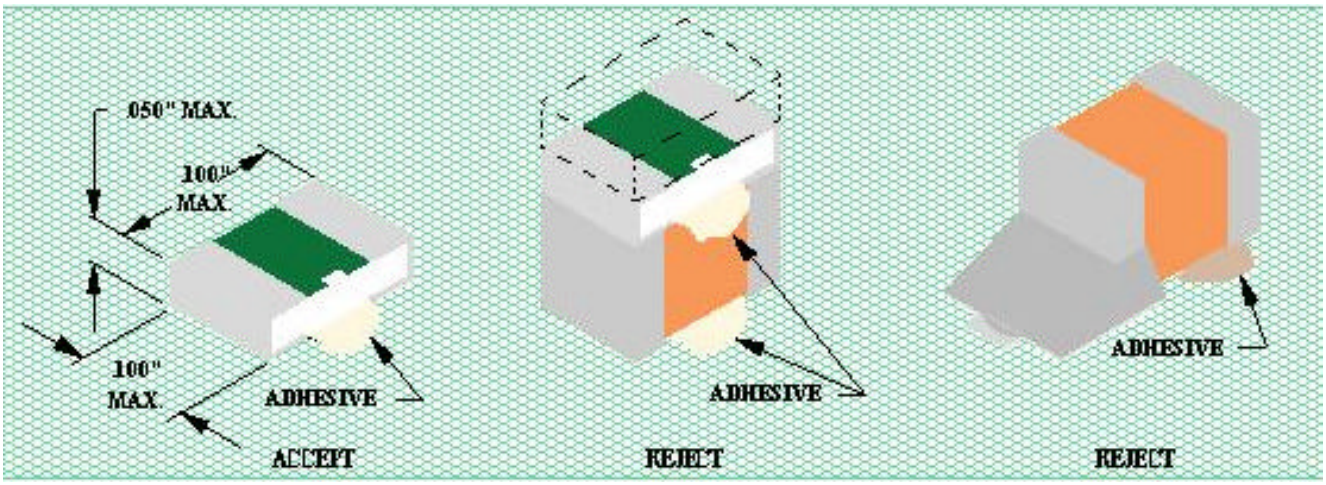


Figure 25 - Modification F, Modification K and Modification L - Acceptance Criteria Illustrations

Design Requirements

a) Component end metallization shall be on 3 sides minimum.
b) No end overhang.
c) The end metallization of the chip shall contact the pad/land .005" minimum both ends.
d) The side metallization of small chip shall overlap the larger chip's side metallization a minimum .005".
e) No side overhang.
f) The periphery of the pad shall extend .010"minimum beyond the end and both sides metallization of the component on both ends. **W1** shall be .020" greater then **W** or **W2**.
g) **H** shall not exceed .250" **H1** shall be equal to or less than **H.**
h) The height **H** may be greater than the width **W** or **W2**.
i) Solder fillets shall be a minimum of **.25H** and **.25H1** on the exposed periphery of chips metallization on both ends.
j) Solder wetting shall be evident between the two chips' side metallization.
k) Deposited electrical element shall be placed facing outward.

Modification G



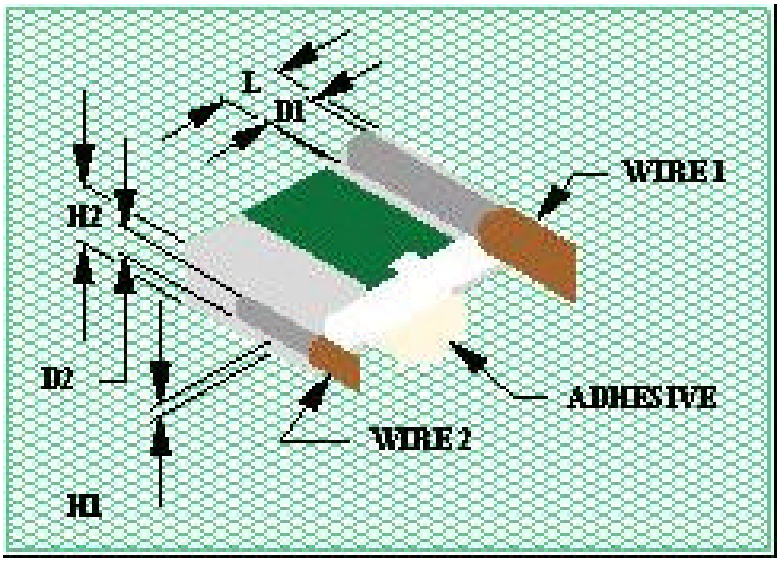
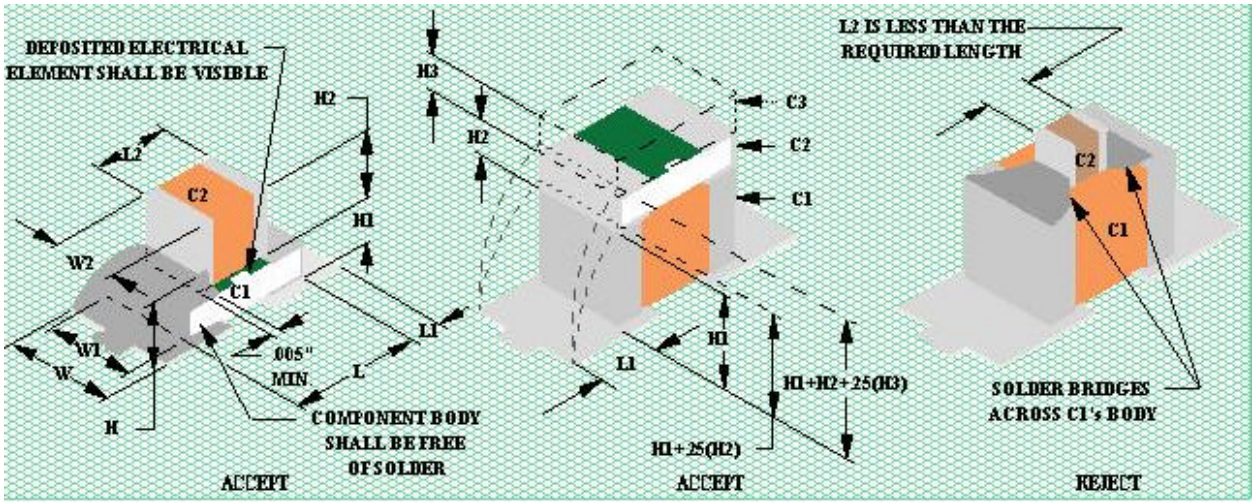


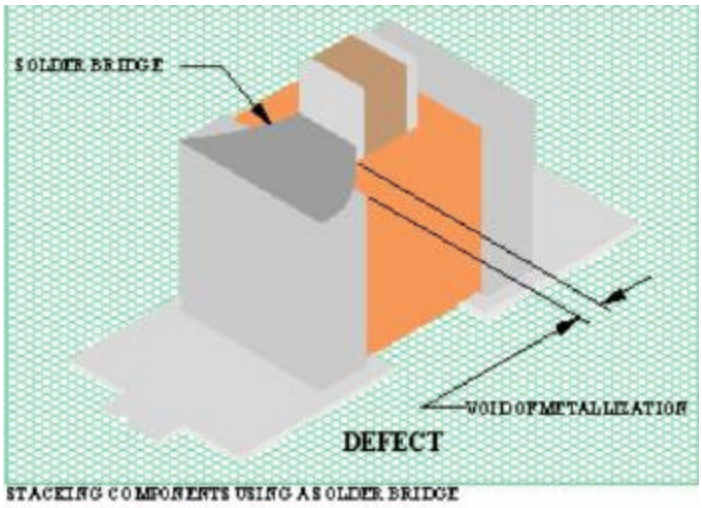
Figure 26 - Modification G - Acceptance Criteria Illustrations

Design Requirements

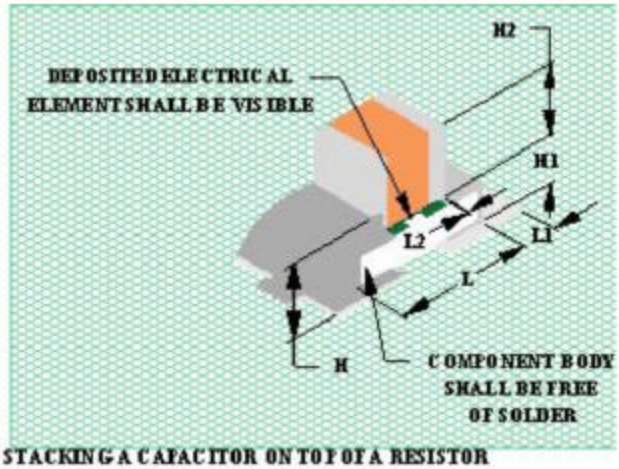
a) Adhesive selected shall withstand design requirements for product end use environment.
b) Stacking of other components on components bond to the board surface shall not be allowed.
c) **D1** shall be equal to or less than **L** and **D2** shall be equal to or less than **H2**.
d) There shall be not adhesive in the **H1** dimension and **H1** shall at minimum .25 percent of D2 **.25(D2)** to achieve proper solder fillet for the **Wire2**.
e) Leadless chip components greater than .050 inch thick x .100 inch wide x .200 inch long shall be tested using the program qualifications test parameters prior use on PWA that are manufacturing released.
f) If one end of the chip component is solder to a PWB feature the other end shall not be bonded to the board with adhesive.

Modification C, B and E

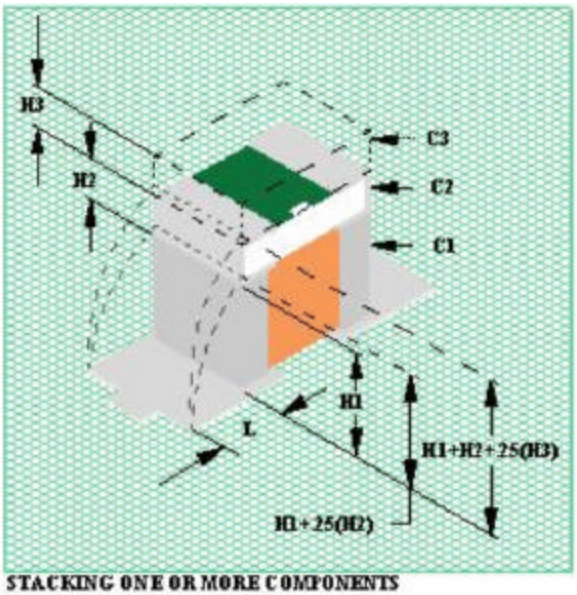




STACKING COMPONENTS USING A SOLDER BRIDGE



STACKING A CAPACITOR ON TOP OF A RESISTOR



STACKING ONE OR MORE COMPONENTS WITH THE SAME PACKAGE SIZE

Figure 27 - Modification C/B/E - Acceptance Criteria Illustrations

Design Requirements

a) No end overhang of top component.
b) No side overhang of top component.
c) Resistor shall be equal or greater than .125" in length **L**.
d) The unused portion of the pad shall be long enough to accommodate proper end solder fillet both ends **{L1 = H1 + H2(.25)}**
e) The top component's length **L2** shall be at a minimum .010" greater then the distance between the bottom component's top metallization and shall overlap the top metallization a minimum of. 005" both ends.
f) End solder fillets shall extend 25 percent of **H2**. **{H = H1 + H2(.25)}**
g) **W1** shall be less than **W** and **W2** shall be less than or equal to **W1**.
h) Solder fillet shall not encase the chip resistor's component body.
i) The deposited electrical element shall be visible for heat dissipation and to detect the presence of component damage.
j) A third component **C3** and additional components may be added as long as **C2** and **C1** are not resistors.
k) No end overhang for **C1** on pad.
l) No end overhang for **C2 & C3** on **C1**.
m) No side overhang for **C1** on pad.
n) No side overhang for **C2 & C3** on **C1**.
o) **L1** shall be long enough to accommodate **.25(H3)** solder fillet.
p) Evidence of solder wetting between **C1 & C2, C2 & C3,** and **C3 & etc**.
q) Stacking component by use of solder bridge shall not be allowed.

Modification H, I & N

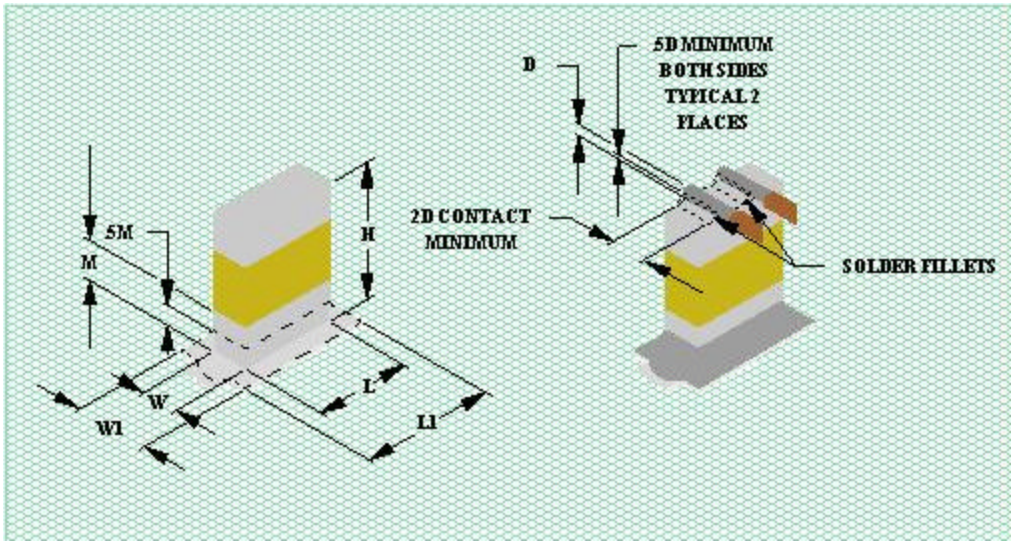


Figure 28 - Modification H/I/N - Acceptance Criteria Illustration

Design Requirements

a) No end overhang.
b) No side overhang.
c) The pad size shall larger enough to achieve proper solder fillets the pad's length **L1** at a minimum shall equal to the capacitor's length **L** plus the height of the chip's bottom, top and both sides metallization height **M**. **L1 = L + M**.
d) The pad size shall larger enough to achieve proper solder fillets the pad's width **W1** at a minimum shall equal to the capacitor's width **W** plus the height of the chip's bottom, top and both sides metallization height **M**. **W1 = W + M**.
e) Placement on pad to achieve solder fillet minimum of half the height of the chip's bottom, top and both sides metallization height **.5M**.
f) Component end metallization shall be on all 5 sides.
g) Distance off of pads limited be design requirements and pad geometry to achieve solder volume .
h) The wire shall have be 2 wire diameters **2D** contact in length with the end metallization of the capacitor.
i) The wire(s) shall be soldered having a half wire diameter **.5D** solder fillet extending sown both sides along the entire length at a minimum.
j) The wire shall not have any side or end overhang of the component's end metallization.
k) **H** shall not exceed .250"

Conclusions

Thermal cycle test results were used to evaluate and characterize 14 commonly used solder joint modification configurations. Thirteen of the fourteen modification configurations were recommended for potential inclusion in the IPC specifications.

Table 6 - Modification Configuration Recommendations

Modification Configuration	Restriction(s)
A	Use of Adequate Pad Size
B	Use of Adequate Pad Size
C	Maximum Resistor Size: 2010 & Use of Adequate Pad Size
D	Use of Adequate Pad Size
E	Use of Adequate Pad Size
F	Use of Adequate Pad Size
G1	Strain Relief Incorporated Into Add Wire
G2	Strain Relief Incorporated Into Add Wire
H	Strain Relief Incorporated Into Add Wire
I	Strain Relief Incorporated Into Add Wire
J	Use of Adequate Pad Size
K	Use of Adequate Pad Size
L	Use of Adequate Pad Size
M	Not Recommend For Industry Use
N	Strain Relief Incorporated Into Add Wire

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