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Design and Development of a High Performance Wirebond BGA Package

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Abstract
As the need for higher performance, higher I/O count packaging solutions at lower costs continues to grow, opportunities exist to support these applications with higher performance wire bonded packages, as an alternative to some of the more expensive FlipChip solutions.

This paper details the unique design layout and engineering development methodologies that were used to produce a family of organic wire bonded BGA packages. This family of packages utilizes a 'Stripline' cross-sectional structure in contrast to the more commonly used 'Microstrip' structure for electrical enhancement. This enhancement is combined with the package designed to support both 'Single ended' and 'Differential' I/O's as well as providing support for multiple I/O voltages. In supporting the need for increased power dissipation, built in heat spreaders as well as optimized thermal via and solderball layouts have been designed into the package.

The packages are able to support a high density of I/O's per unit area of the die, by combining an optimal layout of multiple rows of bonding pads on the die with a package layout that promotes the electrical enhancement features. Our modeling and characterization of this family of packages conclude it meets the high performance requirements needed of the next generation electronic packages.

Introduction
Over time, there has been a continuous need for increasing the number of I/O in a package for a given body size due to increasing bandwidth requirements in system architecture. The method of interconnect from the package to the circuit board has evolved from peripheral leaded packages to Pin Grid Arrays, and into Ball Grid arrays. Within Ball Grid arrays there has been evolution from 2 layer designs, to 4 layer designs, and higher layer counts. In order to support the higher I/O density of multiple pad rows and tighter pad pitches, a new package family had to be developed that could maximize the number of signal leads available for a given die size. Package bonding features had to be compatible with silicon that has multiple rows of die pads. We looked at different cavity configurations and the methods of interconnect within the substrate to fan out these I/O and connect them to the solder ball pads. Other features we wanted to incorporate into the package family included: split power planes, ability to use the I/O as single ended or as differential pairs, and tight impedance control. We needed to meet these objectives without significant increase in cost over current 4 layer Plastic Ball Grid Array.

New Package Family Design Features
Some of the design features for developing the new package family are listed below:

- Need for higher I/O density per unit area.
- Bonding features to be compatible with multiple Rows of Staggered Die Pads.
- Smaller die size per number of I/O.
- 55 Ohm single ended I/O Impedance.
- 100 Ohm Differential Pair I/O Impedance.
- Multiple I/O power splits.
- Generic package family.
- Finished substrate thickness 0.56mm thick.

A primary design constraint for this package was to provide bonding features compatible with our new Pads on I/O ™ silicon technology. With the Silicon pads placed directly on top of the I/O cells on the die and moving to multiple rows of pads, resulting in a reduced effective pad pitch of 27um, we were able to increase I/O density of the package by 1.29 times for a given die area.

Electrical Performance and Final Stack Up Selection.
Early in the development of this package family we worked on the relationships of I/O density, meeting the impedance requirements, and having a manufacturable package.

To determine the required cross-sectional dimensions that will meet electrical targets, quasi-static field solvers were used. After carefully considering various layer stack-up for specific applications, both the single-ended and differential routing

scheme were analyzed. Dielectric and metal thickness were varied and signal trace width and spacing were identified for each construction. These new values are echoed back to the substrate designs to gauge the impact on the I/O density. Iterations take place not only when the resulting trace widths and spaces degrades the I/O density, but, also when the identified values are beyond the volume capability of the target substrate vendors. In some cases, these values may result in quality concerns from the manufacturing group. We first looked at 4 layer constructions but found early on through modeling we could not meet the impedance requirements with the given I/O density requirements. The required trace widths and spaces in the 4 layer stack up were impractical.

Moving to a 6 layer stack up was key in meeting density requirements while maintaining the impedance control needed with this package. This is primarily because it provided the package a stripline configuration that allowed narrower widths and spaces for the same impedance targets. The I/O density increased about 10.6% for a given package body size when compared to our previous generation 4 layer package family. (See Figure 1.)

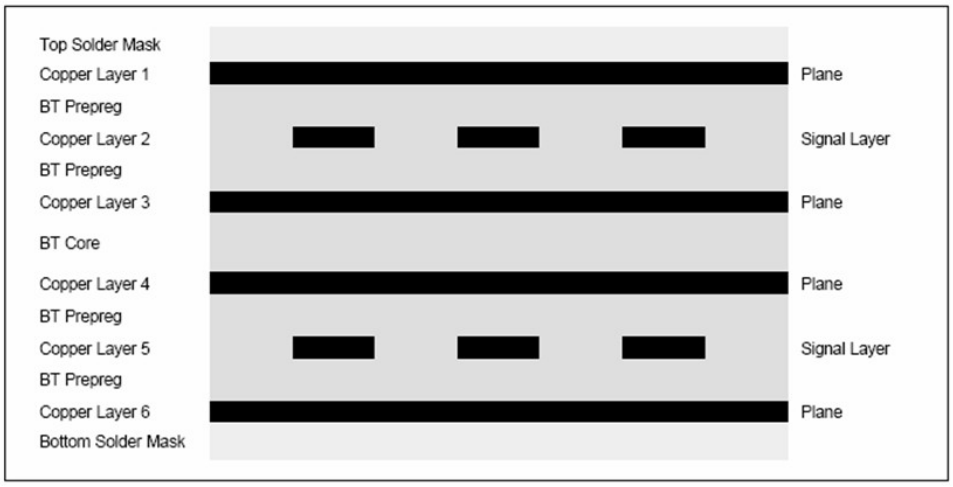

Figure 1 - Cross Section Stack-up

Silicon Interface / Cavity Layout

Our next challenge was to meet the silicon wire bonding interconnect density requirements. The silicon planned for this package family has multiple rows of die pads around the periphery of the die. See Figure 2.

Refer to Figure 3. The bond fingers are placed on the outer most tiers of the package for a couple of reasons. 1. A higher number of I/O can be achieved for a given bond finger pitch due to the longer bond finger layout arc. 2. The power and ground bonding wires are shorter as the power and ground rings are closer the die. This reduces inductance in the power and ground supplied to the die.

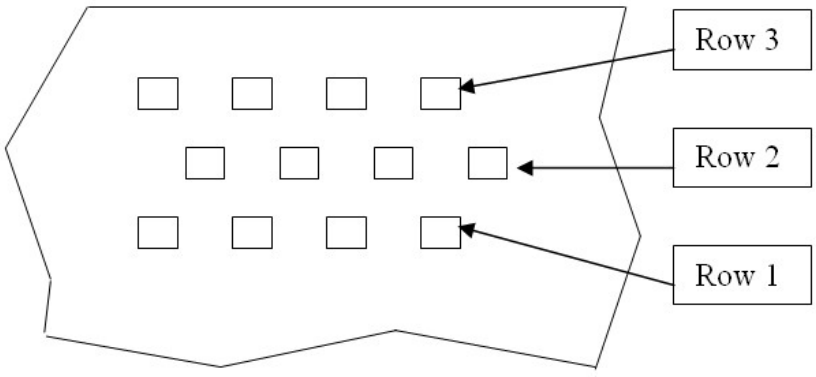

Figure 2 - Die Pad Layout

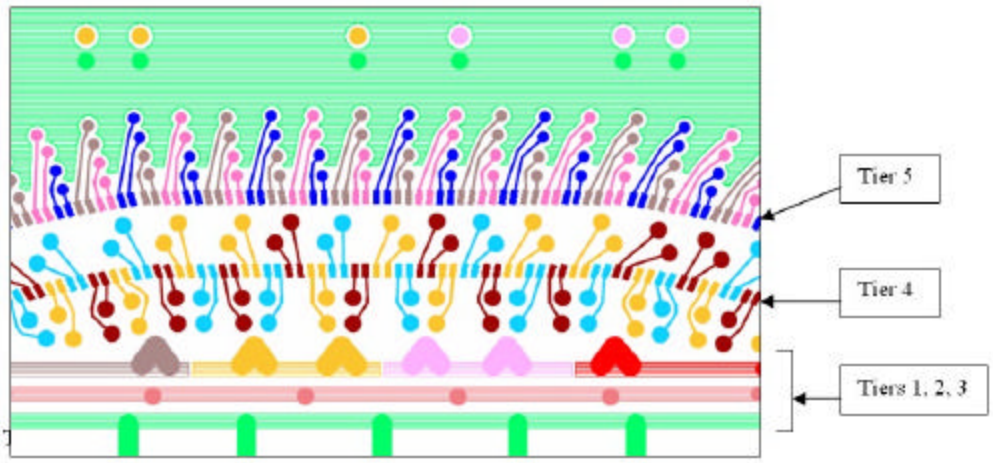

Figure 3 - Package Bonding Features

The wire bonding interconnect between the Die and Package are as follows:

- The outermost die pads connect to the power and ground rings of the package (Tiers 1, 2, and 3).
- The middle row(s) of die pads connect to the first row of Bond Fingers (Tier 4).
- The innermost die pads connect to the outer row of bond fingers (Tier 5).

Signal Routing in the Substrate

Refer to Figure 3. The Bond fingers in Tier 4 are connected to Through Hole Vias with short traces on Layer 1. The Through Hole vias provide connection to the signal routing layer on Layer 5. The bond fingers on Tier 5 are connected to blind laser vias using short traces on Layer 1. The blind vias are used for connection to the signal routing layer on Layer 2.

Layers 2, and 5 are the signal routing layers in this package family. The close proximity of the Ground Plane above and the Power Plane below the signal layers allow for finer trace width and space as compared to other package constructions. The routing was laid out to keep a fixed space between differential pair traces and to minimize differences in trace length. See Figure 4 for Layer 2 routing example. See Figure 5 for Layer 5 routing example.

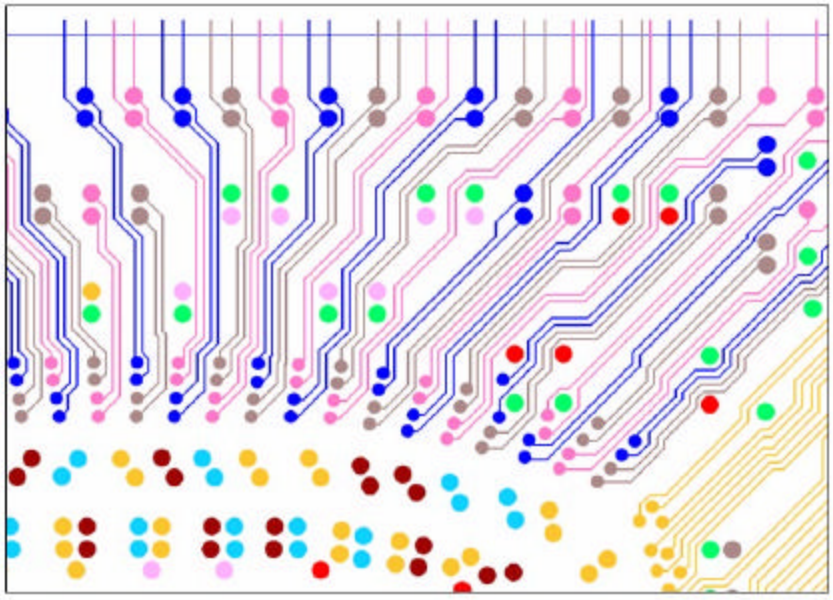

Figure 4, Layer 2 Routing Example

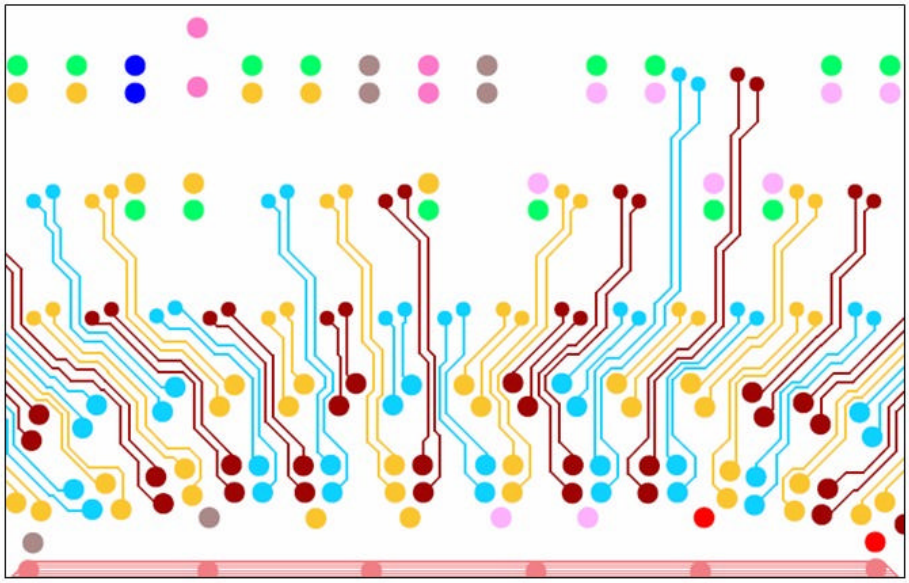

Figure 5 - Layer 5 Routing Example

Power Distribution

Another primary design feature of this new package family was to have many I/O power segments allowing use of multiple I/O voltages around the package. The power ball, ground ball, and plane split locations were optimized to provide 16 total I/O power splits for all package family members. See Figure 6 for an example of the power plane splits. These power plane splits are applied to both Layer 3 and Layer 6 in the package.

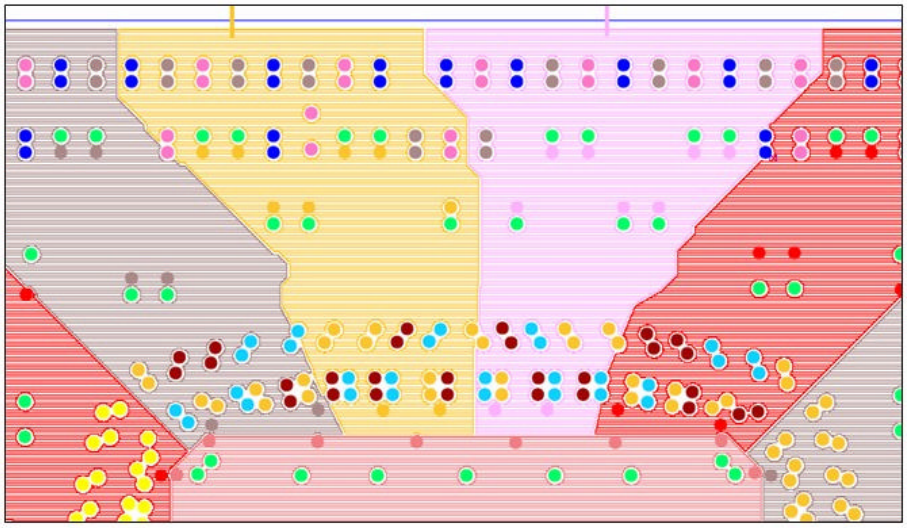

Figure 6 - Example of Power Plane Splits, Layer 3 and 6

Thermal Performance

In order to enhance the thermal performance of this package family, a stamped copper heat spreader is imbedded into the package during the mold encapsulation process. This heat spreader was designed to be compatible with the existing mold tooling. Refer to Figure 7 for the image of the Heat Spreader and Figure 8 for a finished package. Experimentation with different plating finishes and mold compounds were performed in order to maximize resistance to delamination. The final finishes selected were Black Oxide finish on the underside for adhesion to the mold compound and Matte Nickel finish on the top to be compatible with Laser Marking. An optional heat spreader configuration allows for grounding the heat spreader to the package.

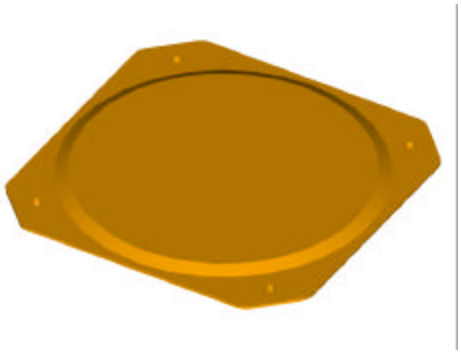

Figure 7 - Heat Spreader

Figure 8 - Finished Package

Figure 9 compares the thermal resistances of 40mm package with a 13.5mm die between the following packages at various air velocities.

- 4 Layer, 40mm PBGA without a Heat Spreader.
- 4 Layer, 40mm PBGA with a Heat Spreader.
- 6 Layer, 40mm PBGA with a Heat Spreader.

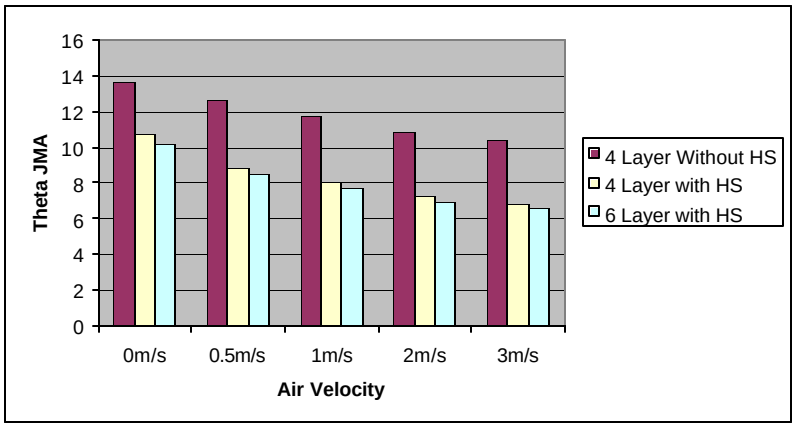

Figure 9 - Thermal Enhancement

Addition of the Heat Spreader to the package reduced Theta JMA from 21% to 34% with the higher reduction at the higher air velocities.

Verification of Actual Performance

When the design was locked we procured engineering units to perform assembly capability verification. Test sample units were built that allowed us to measure impedance. On 5 samples measured, we got an average single ended impedance of 53.76 Ohms. Our target impedance for this design was 55 Ohms.

Table 1 - Measured Single Ended Impedance

Sample #	Measured Impedance
1	54.500
2	53.347
3	53.294
4	53.708
5	53.994

Conclusions

LSI's 6 Layer EPBGA -HP met the target design parameters. We met the I/O density and die size requirements of multiple rows of staggered die pads. The package bonding features were laid out to maximize the available number of I/O without degrading the wire bonding manufacturability. This package family was designed with the capability of using the I/O as differential pairs or as single ended. The I/O signal traces, when used as single ended, have a measured impedance of 53.76 ohms. Our electrical modeling and refinement of the package stackup and trace width and space allowed us to hit very close to our desired target impedance values. Keeping the total thickness of the substrate at 0.56mm allows the use of existing mold tooling and singulation punches. Power distribution was setup to allow for 16 I/O power splits around the package. This offers great flexibility to the end users of this package as numerous I/O voltages can be used around the package. All of these features were designed into all members of the EPBGA -HP family. As an alternative to Flip Chip, these packages provide up to 1069 balls and 752 signals. For a package family listing refer to Table 2.

Table 2 - EPBGA-HP Package Family Lineup

Ball Count	Body Size	I/O Count
340	23	248
472	27	352
660	31	488
824	35	608
892	37.5	656
1069	40	752