

Lead Free Conversion Analysis for Multiple PWB/Component Materials and Finishes using Quality and Reliability Testing

Sammy Shina
University of Massachusetts
Lowell
Lowell, MA

Liz Harriman and Todd MacFadden
Massachusetts Toxics Use
Reduction Institute (TURI)
Lowell, MA

Donald Abbott
Texas Instruments
Attleboro, MA

Richard Anderson, Helena Pasquito
and George Wilkish
M-A/COM Tyco Electronics
Lowell, MA

Marie Kistler
Air Products and Chemicals, Inc.

David Pinsky
Raytheon Company
Lexington, MA

Mark Quealy
Schneider Electric
North Andover, MA

Karen Walters
Skyworks Inc.
Woburn, MA

Richard McCann and Al Grusby
Analog Devices
Wilmington, MA

Abstract

The world-wide movement to phase out lead from electronic products presents many challenges for companies throughout the electronics supply chain. The University of Massachusetts Lowell has brought together nine Massachusetts firms to collaborate on the manufacture and testing of lead-free printed wiring boards (PWBs). The results of the first set of experiments, published in 2001, showed that zero-defect soldering is achievable with lead-free materials. Following thermal cycling, the PWBs were visually inspected and the leads were pull tested for reliability analysis. They compared favorably to a baseline of lead soldered PWBs

A follow-on design of experiments was created in 2002 and a second set of test PWBs was made and tested in 2003. Several lead free solder pastes (3) based on Sn/Ag/Cu were used with a variety of surface finishes (5), component types (4) component finishes (2) and reflowed using either air or nitrogen. Visual inspection and pull testing has been completed and published in APEX, SMTI and IEEE conferences. This paper summarizes the effort and conclusions to date and discusses the methodology of the pull-testing phase after thermal cycling.

Key words

lead-free, design of experiments, PWB soldering; solder joint reliability, interchangeability of leaded and lead free components.

Background

The worldwide movement to phase out lead from electronic products presents challenges for companies throughout the electronics supply chain. Because lead had been integral to the integrity and reliability of electronic products, it is necessary to make changes carefully, and with the full participation of all parts of the product supply chain. The University of Massachusetts Lowell (UML) and the Massachusetts Toxics Use Reduction Institute (TURI) have brought together several key companies in the Commonwealth to form a research consortium to investigate lead-free manufacturing.

Drivers for Change

In January 2003, The European Union published Directives 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE) and 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment

(RoHS). These emerging directives have been the primary drivers for global movement toward lead-free electronics. The RoHS prohibits products that contain lead to be sold in the EU after July 2006, unless the use is specifically exempted.

The second major influence has been the movement of electronics manufacturers, particularly Japanese companies, toward so called “green products.” JEIDA, the Japanese Electronics Industries Association, developed a lead-free roadmap in 1998, and many firms have set targets for elimination of lead in their products, and have selected lead-free products already on the market.

In each case, suppliers must develop, test, and ensure performance of lead-free components and assemblies for manufacturers of electronic products. The short timeframe for these changes requires a coordinated effort of all firms in the electronics supply chain, from manufacturers of basic materials and components, to assemblers and OEMs.

The WEEE directive challenges electronics manufacturers to think in a fundamentally different way about their products and the materials they use, requiring both recycling at a product’s end of life, and inclusion of recycled materials in new products. This, together with the required development of new materials that don’t contain lead, cadmium, and other substances of concern, presents an opportunity for industry to design products that conserve resources and are safer for humans and the environment throughout their life cycle.

Massachusetts Lead-Free Consortium

The Massachusetts Toxics Use Reduction Act (TURA) program has a mission to assist companies in reducing or eliminating the use of toxic substances where possible, and in reducing the amount of toxic waste generated. TURA also has a goal “to sustain, safeguard and promote the competitive advantage of Massachusetts businesses, large and small, while advancing innovation in toxic use reduction and management.” These goals come together as we assist firms in meeting international materials restrictions on lead in electronic products.

TURI and UML provide training and information, and conduct research in innovative technologies to support Toxics use reduction. In 1999, as the movement toward lead-free emerged, TURI began supporting research at UMass Lowell to investigate the alternative lead-free solders.

The Massachusetts Lead-Free Research Consortium was formed in 2000, consisting of at least one representative of each part of the electronics supply chain. Members contribute time, materials, facilities, funding and expertise as they jointly develop and implement testing plans. Current consortium members are M/A-COM/Tyco Electronics, Texas Instruments, Raytheon Company, Schneider Electric, BTU International, Air Products and Chemicals, Analog Devices, UML and TURI.

In addition to supporting the consortium, TURI periodically brings together firms from the electronics supply chain to exchange information, to communicate the latest technical and regulatory developments, and to report on the consortium’s research program (for summaries of papers and presentations, see TURI’s web site: www.turi.org).

Experimental Design, Including Factor and Level Selection

A design of experiment matrix was selected by the consortium members based on their collective experience and the available resources and materials. The factors and levels selected were as follows:

1. PWB Finishes – Five Treatments– Solder Mask Over Bare Copper with Hot Air Solder Leveling (SMOBC/HASL), Matte Finish Tin (Sn) Electroplate, Immersion Silver (Ag), Organic Solder Preservative (OSP), and Electroless Nickel Immersion Gold (ENIG).
2. Reflow Atmospheres – Two Treatments – Air and Nitrogen. Nitrogen was supplied by Air Products and Chemicals and contained 50 ppm Oxygen for these experiments
3. Solder Pastes – Three Treatments – all with the same alloy composition – 95.5Sn-3.8 Ag-0.7Cu (NEMI recommended) from three different suppliers (A, B and C), all incorporating no-clean fluxes.
4. Component Lead Finishes – Four Treatments – matte Tin plating, Tin/Silver/Copper, Nickel/Palladium/Gold, and Nickel/Gold.
5. Sn-Pb eutectic solder PWB using the solder treatments as control PWBs.

Test Vehicles and experimental plans

The test vehicle was a 6” x 9” FR4 board, shown in the pull test fixture (Figure 1). A total of 100 PWBs were assembled and tested. The PWBs were divided as follows:

1. 60 PWBs consisting of 2 sets of 30 to harness the full factorial experiment of 5 finishes, 3 solder suppliers and 2 atmospheres ($5 \times 3 \times 2 = 30$). The full factorial experiment is shown in Table 1.
2. 10 PWBs, consisting of 2 sets of 5 PWBs soldered with a leaded solder from supplier B to act as baseline comparison to unleaded solder.

3. 8 PWBs, consisting of 2 sets of 4 to test out a more concentrated percentage of Nitrogen (50 ppm versus 5000 ppm oxygen)
4. 20 PWBs, consisting of 2 sets of 10 PWBs, to compare the results of leaded and unleaded components versus leaded and unleaded solders, using all 5 PWB finishes, air soldering environment and solder supplier B. This set was performed to demonstrate whether it is possible to exchange unleaded components with leaded components at will in all soldering environments.

Components

The control PWBs were built with devices that had a tin/lead component finish and the experimental test boards were assembled with parts that had lead-free finishes. The lead-free passive chips were tin-plated and the lead-free integrated circuit devices were plated, some with matte Tin plating, Tin/Silver/Copper, Nickel/Palladium/Gold, and Nickel/Gold. Components were donated from consortium companies.

Each PWB included:

1. *Standard SMT resistor and capacitor parts. (401 and 402 styles).*
2. *A set each of 0.030 and 0.014 vias*
3. *3 QFP 176 high-density interconnection (HDI) package one with daisy chain terminations,*
4. *2 BGA types, 35 and 45 mm*
5. *3 SOIC 20 packages, one with daisy chain terminations*
6. *3 special IC's used in wireless applications*

Table 1 - Lead Free Full Factorial Solder Test Plan

Experiment #	Surface Finish	Solder paste	Atmo - sphere
1	SMOBC/HASL	"A"	Air
2	SMOBC/HASL	"A"	Nitrogen
3	SMOBC/HASL	"B"	Air
4	SMOBC/HASL	"B"	Nitrogen
5	SMOBC/HASL	"C"	Air
6	SMOBC/HASL	"C"	Nitrogen
7	OSP	"A"	Air
8	OSP	"A"	Air
9	OSP	"B"	Nitrogen
10	OSP	"B"	Air
11	OSP	"C"	Nitrogen
12	OSP	"C"	Air
13	ENIG	"A"	Nitrogen
14	ENIG	"A"	Air
15	ENIG	"B"	Air
16	ENIG	"B"	Nitrogen
17	ENIG	"C"	Air
18	ENIG	"C"	Nitrogen
19	Matte Sn	"A"	Air
20	Matte Sn	"A"	Nitrogen
21	Matte Sn	"B"	Air
22	Matte Sn	"B"	Air
23	Matte Sn	"C"	Nitrogen
24	Matte Sn	"C"	Air
25	Imm. AG	"A"	Nitrogen
26	Imm. AG	"A"	Air
27	Imm. AG	"B"	Nitrogen
28	Imm. AG	"B"	Air
29	Imm. AG	"C"	Air
30	Imm. AG	"C"	Nitrogen

Experiment Layout

The test PWB was laid out at M/A-COM taking into account daisy chain resistance test capabilities in some of the parts and fabricated by Sanmina-SCI with the five different finishes. Pastes were obtained from three vendors and a reflow profile was developed based on the manufacturers' product data sheets. A reflow profile board was populated with parts and three K-probe thermocouples (TC) were attached to the surface. One TC was attached at the leading edge of the PWB, one at the lead attach area of a large QFP and one near the trailing edge. The thermocouples were connected to an industry standard data logger. The thermal readings were downloaded to the data collector software for comparison to the manufacturer recommended profiles. All three manufacturers recommended a 'ramp to spike' curve. Several runs were performed to ensure consistent performance. The reflow profile used for all three Pb-free solders is shown in Figure 2.

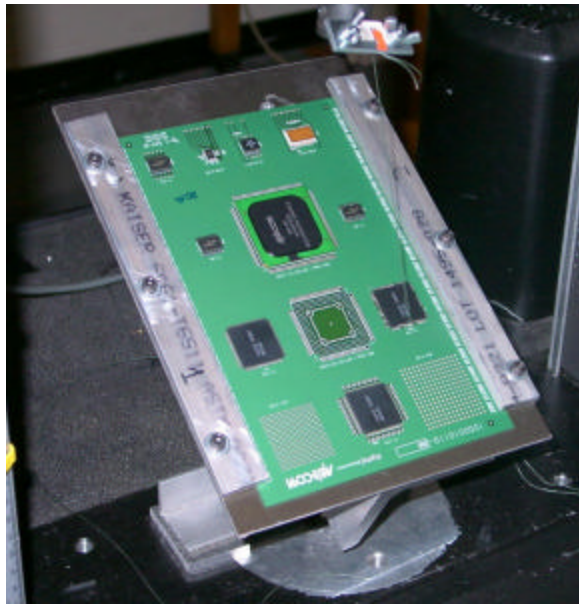


Figure 1 - Test Vehicle

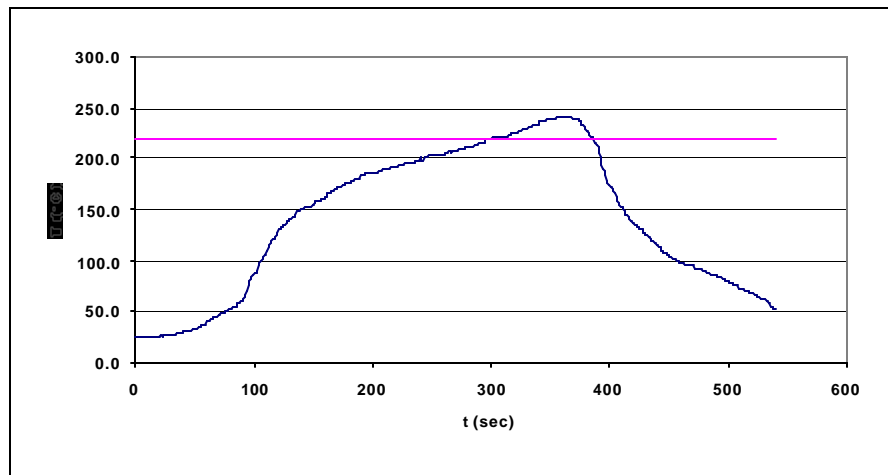


Figure 2 - Reflow Profile for SMT Board Assembly

Solder paste prints were made using a 0.006" thick stainless steel laser cut, electropolished stencil. Ten percent aperture reductions were used on the fine pitch devices. PWBs were assembled at Schneider Electric on their assembly line consisting of an MPM AP-25 screen printer, Siemens S20 and F5 placement equipment and a BTU Pyramax 98N Reflow Oven with Air and Nitrogen capability supplied by BTU International for this experiment. The Schneider plant maintains a Relative Humidity (RH) level between 35-40%.

After reflow, PWBs were packaged in ESD bags and taken to M/A-COM where two University of Massachusetts – Lowell senior students visually inspected the solder joints based on training by a certified IPC inspector / trainer. Inspection criteria were established as follows: Total Defects, Cold Solder joints, Non-wetting, Solder Balls, Dewetting, Bridging, Pinholes, Shiny Appearance, Smooth Appearance, and Flux Residue. X-ray radiography of the BGA solder joints was also performed. Initial inspection data has been tabulated and statistically analyzed by University of Massachusetts – Lowell and Air Products.

Visual Analysis Results

The major difficulties encountered in assembly were with stencil printing and placement system vision. In spite of using print parameters close to those in the application notes supplied for the three pastes, paste A had a tendency to adhere to the sides of the stencil openings. This resulted in scant prints on some of the fine pitch apertures. Paste B clogged the necessitating cleaning after every four or five prints. Paste C performed as expected with little difficulty. All three pastes exhibited good tack or component holding qualities during and after placement.

Visual Defects statistics

Eight main categories of common defects were selected and all boards were inspected. Those defects observed were photographed and recorded into a spreadsheet. The average analysis of all factors is shown in Figure 3. Statistical analyses were performed using Minintab and the following significant effects were determined (Table 2).

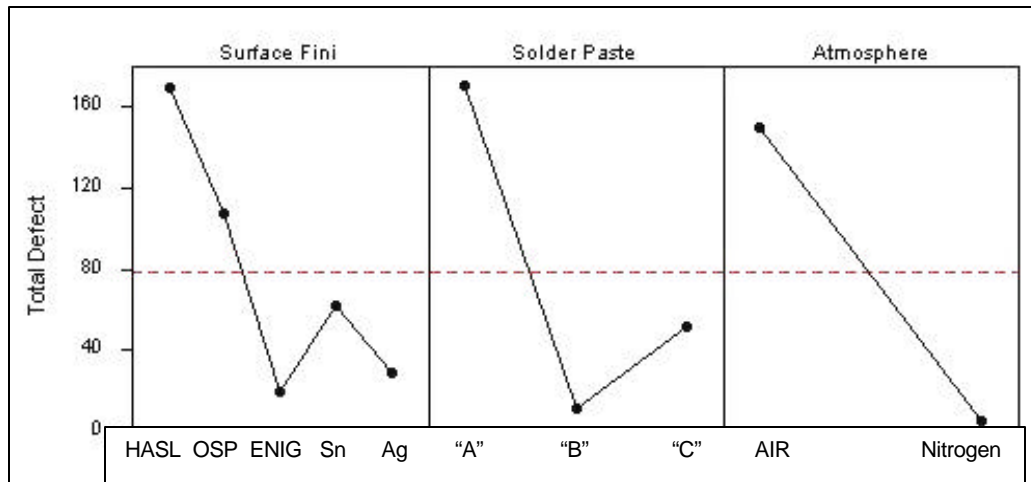


Figure 3 - Average Analysis Of Factor Levels Effecting Visual Defects

Table 2 - Statistical Analysis – Total Visual Defects

Source	DF	Sum of Squares Mean	Square	F Value	Pr > F
PWB Finish	4	44.7	11.2	7.33	0.0003
Solder	2	79	39.5	25.91	<.0001
Atmosphere	1	132.4	132.4	86.88	<.0001
Finish * Solder	8	16.04	2.00	1.32	0.2735
Finish*Atmosp.	4	15.3	3.8	2.51	0.0629
Solder *Atmosp.	2	54.3	27.2	17.83	<.0001
Finish * Solder *Atmosphere	8	21.8	2.7	1.79	0.1184
Total	59	409.20			

As seen above, the ANOVA (Analysis of Variance) is significant for the overall experiment and for the variables highlighted with probabilities (Pr) less than .05.

Further statistical analysis indicated the following conclusions:

1. The Board Finish level SMOBC/HASL significantly differs from all other finishes. No other finishes were found to be statistically different from one another at the 0.05 level.
2. All Pastes were found to differ significantly from all other pastes. B Pb-Free performed best
3. Nitrogen performed significantly better than Air
4. The A Pb-Free, Air combination was significantly worse than all other combinations. The C Pb-Free, Air combination was significantly worse than all other remaining combinations. The bottom four combinations B Pb-Free with Air, B Pb-Free with Nitrogen, A Pb-Free with Nitrogen and C Pb-Free with Nitrogen could not be told statistically apart from each other within the limitations of the current study.
5. Only in the case of solder paste B; it was shown that there is no significant difference between the use of Air or Nitrogen. However, this paste exhibited certain process issues relating to the cost of more frequently cleaning the stencil in the production process.
6. There was not enough data points to analyze the differences in defect data, if any, between the two levels of nitrogen in the experiment (50 ppm versus 5000 ppm oxygen)
7. There was not enough data to analyze the differences, if any, in visual defects between unleaded and leaded components using lead and unleaded solders from the same solder supplier.

Pull Test Analysis Results

The test methodology consisted of using an Instron pull test machine to pull the leads of an IC at different positions and record the maximum pull force. The pull tests were analyzed separately for each type of IC because of the differences of pad size and component finish. For the QFP (Nickel/Palladium/Gold) components leads, six (6) leads were pulled as follows (Figure 4), and for the SOIC 20 (Nickel/Palladium/Gold) and the SOIC 16 (Tin plate) component leads, four (4) leads were pulled (Figure 5).

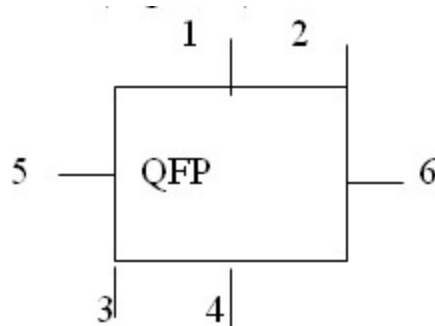


Figure 4 - Position of QFP Pulls

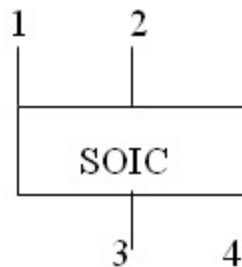


Figure 5 - SOIC Pulls

The process of pulling the leads was performed as follows:

1. The PCB is loaded at 45° to the Instron machine and is tied down with 6 screws on a specially designed hold down fixture
2. The leads adjacent the ones that were pulled were removed (clipped) to facilitate pulling of target leads
3. The leads that were pulled were tied with a wire loop right through the IC's leads. Music wire was used for QFP, and fishing line (#24lb test) was used for SOIC.
4. A new loop was made for each IC pulled
5. The pull rate was 1" per minute, noting down the peak pull force.
6. The fractures were inspected and the failure mode for each pull was noted.

Two (2) PWBs were unable to be pulled because of improper reflow in one case and severe bending in the other.

QFP-176 and SOIC-20 pull test results

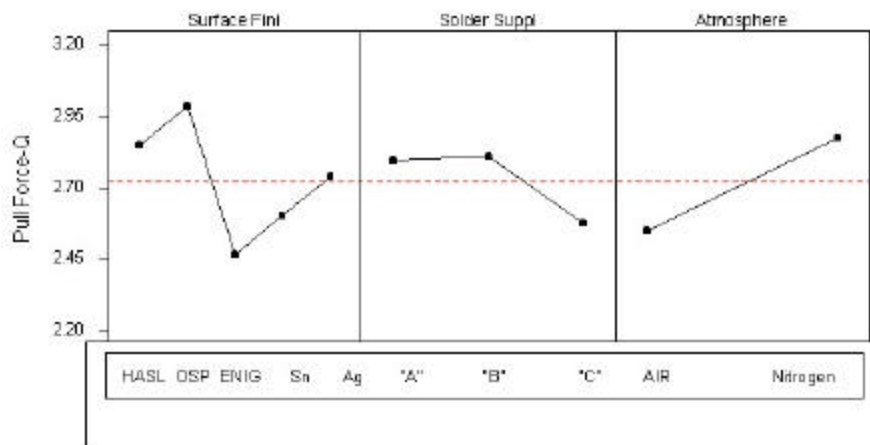
The leads of the QFP-176 and SOIC-20 devices that were pulled had a Nickel/Palladium/Gold finish. Six pulls were made for each of the 30 QFPs in the full factorial experiment shown in Table 1, for a total of 168 pulls (2 IC were not pulled because of problems in soldering). Four pulls were made for each of the 20 SOICs for a total of 112 pulls. The ANOVA analysis for QFP is shown in Table 3 and for the SOIC in Table 4. The QFP factor pulls averages are shown in Figure 6, and the individual level significance analysis for QFP are shown in Figures 7-9. The average SOIC factor pulls are shown in Figure 10, and the individual level significance analysis for SOIC are shown in Figures 11-13. The 3-way interaction for QFP and SOIC could not be calculated because of some of the missing pulls as explained earlier. For the level plots, the uneven limits are due to the 2 sets of PWBs that were unable to be pulled.

Table 3 - Statistical Analysis – QFP Pull Test (6 Pulls/IC)

Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Surface	4	5.36	1.34	5.0	0.001
Solder	2	1.7	0.85	3.17	0.045
Atmosphere	1	4.32	4.32	16.10	0.000
Surface* Solder	8	18.6	2.33	8.68	0.000
Surface*Atmosp	4	1.04	0.26	0.97	0.428
Solder *Atmosp.	2	3.0	1.5	5.57	0.005
Error	146	39.1	0.2681		
Total	167	73.7			

Table 4 - Statistical Analysis – SOIC Pull Test (4 Pulls/IC)

Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Surface	4	77.0	19.30	7.35	0.000
Solder	2	17.721	8.860	3.38	0.038
Atmosphere	1	1.758	1.758	0.67	0.415
Surface* Solder	8	14.258	1.782	0.68	0.707
Surface*Atmosp	4	28.720	7.180	2.74	0.033
Solder *Atmosp.	2	9.970	4.985	1.90	0.155
Error	90	235.6	2.618		
Total	111	392.804			

**Figure 6 – Pull Test Leadfree Average Analysis – QFP****Factorial experiment analysis for QFP and SOIC pulls**

Some of the conclusions that can be derived from this full factorial analysis from Tables 3-4 and Figures 6-12 are as follows:

1. Since all leads have a Nickel/Palladium/Gold finish, these conclusions are applicable to this case.
2. The pull force in the SOIC was significantly higher than QFP due to the large solder surface area in the IC pads.
3. The surface finish has a significant effect on the pull test of the leads. Of the five finishes (SMOBC, OSP, ENIG, Matted SN and Imm AG); the analysis showed that ENIG was significantly lower than the other finishes in both IC's pulled. Finish 2 (OSP) was significantly higher in QFP and Finish 1 (SMOBC/HASL) was significantly higher in SOIC.
4. The solder suppliers were not important in the pull tests for the two (2) IC types. Supplier B (Indium) was slightly higher in QFP-176 and significantly higher in SOIC-20.
5. Nitrogen was significantly higher than air reflow for QFP-176, not significant for SOIC 20
6. Some of the interactions were significant, more so in QFP than SOIC 20

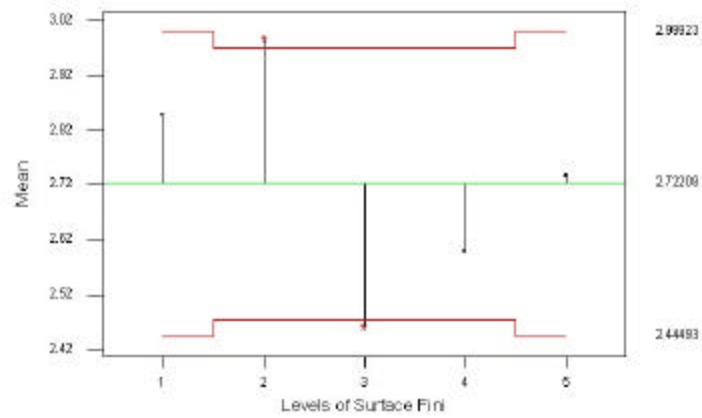


Figure 7 – Analysis of Averages for Surface finish – QFP

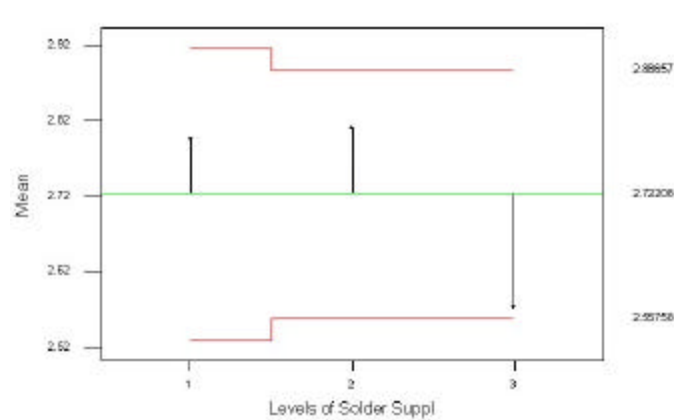


Figure 8 – Analysis of Average for Solder Suppliers – QFP

Figure 9 –

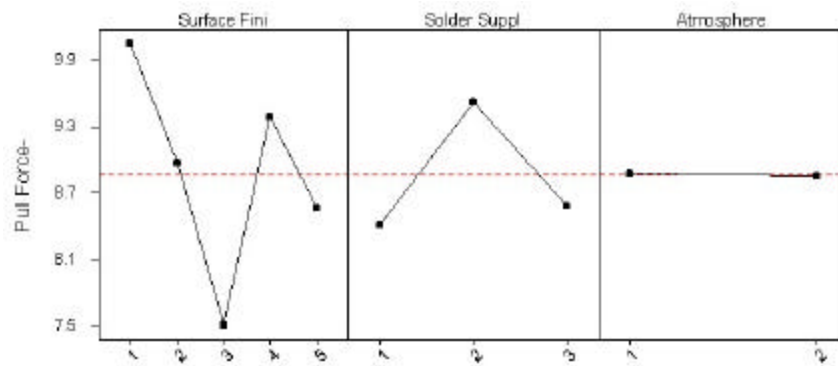


Figure 9 – Leadfree Average Analysis – SOIC 20

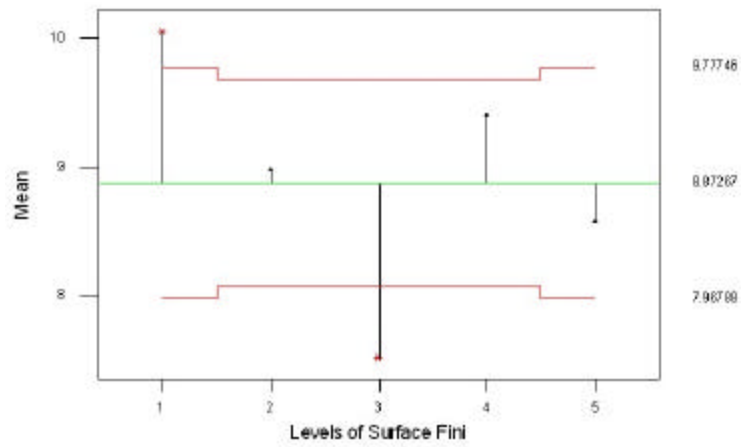


Figure 10 – One-way ANOM for Pull force by Surface Finish

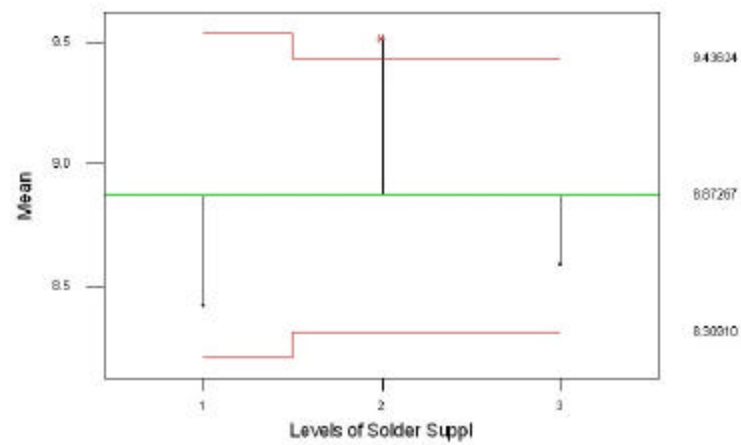


Figure 11 – Analysis of Averages for solder Suppliers – SOIC 20

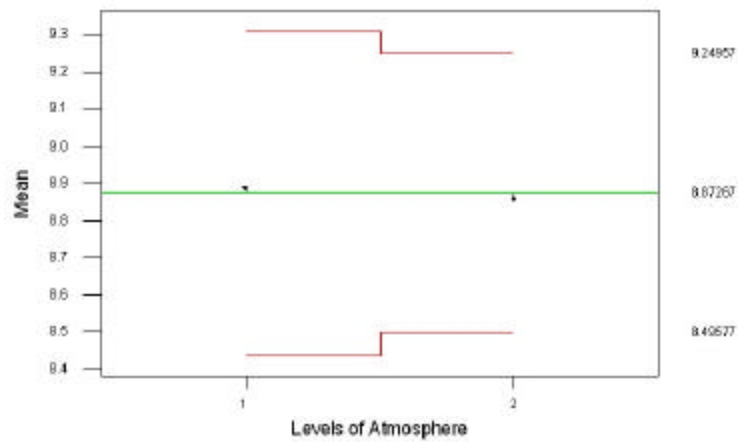


Figure 12 – Analysis of Averages for Atmosphere – SOIC 20

Comparison Of Unleaded Solder With Leaded Solder Baseline For Qfp-176 And Soic-20 With Nickel/Palladium/Gold Lead Finish

For each of the 5 surface finishes, a PWB was reflowed with the leaded solder from supplier B in air, which was used as the baseline for comparing pull tests. Figures 13 and 14 show the comparisons for QFP and SOIC respectively. All components used had Nickel/Palladium/Gold finish.

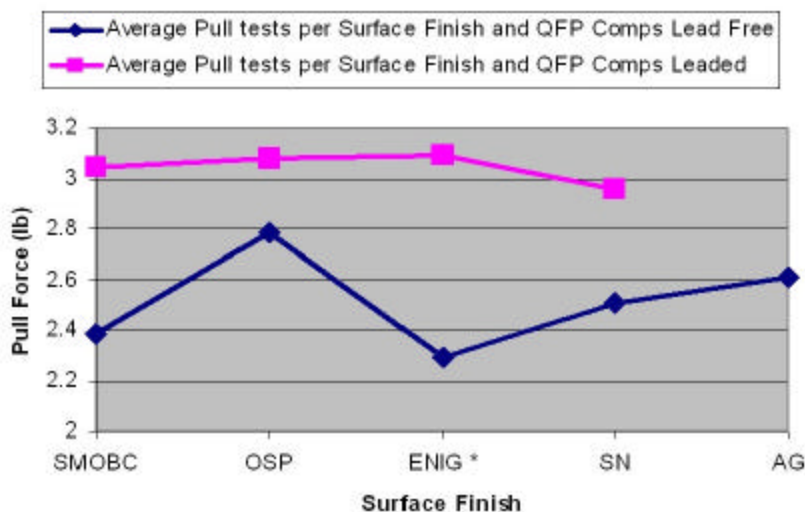


Figure 13 – Comparison for Unleaded vs. Leaded Solder and QFP Comps

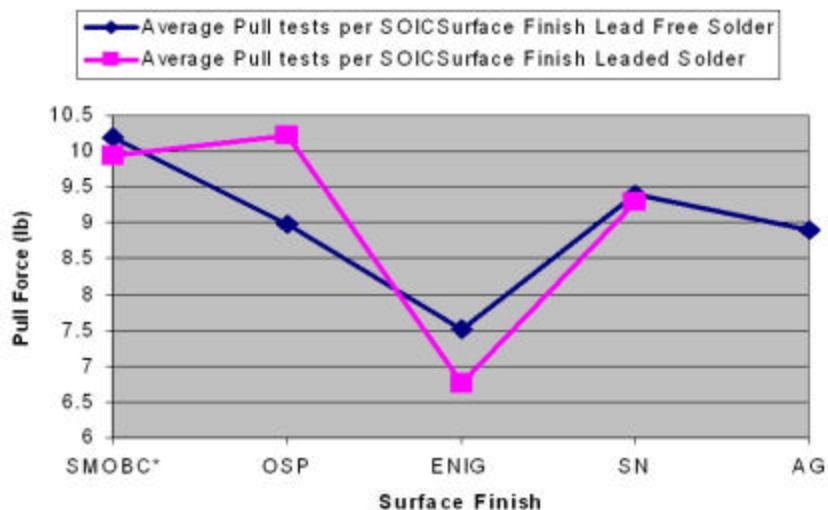


Figure 14 – Comparison of Unleaded and Leaded Solder per PWB Surface finish and SOIC Comps

Since nitrogen was significant in QFP-176, only air soldered PWBs from each finish (3 PWBs for each of 5 finish) were used in the comparison for QFP. For SOIC-20, all PWBs (6 PWBs for each of 5 finishes) were used in the comparison to the leaded solder baseline. The comparisons were made using a multiple-range test for means. Unfortunately the baseline PWB for Immersion Silver (AG) leaded solder was not available. The analysis had to be performed separately for QFP-176 and SOIC-20 because of higher pull force for SOIC.

For all B leaded solder Pastes used as baseline and air reflowed; the QFP-176 leads showed no significance due to PWB surface finish. The SOIC-20 leads showed that ENIG was the only significant (lower) pull force.

1. Unleaded and leaded pull tests showed no significant differences, if the same solder supplier (B) provided the solder paste, except for QFP ENIG and SOIC SMOBC. Otherwise the solder supplier proved to be a significant difference than the leaded baseline. This might indicate that other factors such as solder paste formulation might play a role in making a significant difference between leaded and unleaded solder, more in so in smaller footprint ICs such as QFP.
2. When comparing leaded solder supplier (B) with all 3 unleaded solder suppliers, some significant differences arise: These are shown in Table 5 for homogenous group in the same column. For Immersion Silver (AG), the comparison was not possible since the baseline data were not recorded because of manufacturing problems with the sample PWBs.

Table 5 - Multiple Range Tests – Homogenous Groups

Comparison of unleaded solders to lead baseline Nickel/Palladium/Gold Lead Finish			
QFP - SMOBC PWB Finish		SOIC 20 – SMOBC PWB Finish	
X	(C solder, pb free)	X	(B solder, leaded)
X	(B solder, leaded)	X	(C solder, pb free)
X	(B Solder, pb free)	X	(B solder, pb free)
QFP - OSP PWB Finish		SOIC 20 - OSP PWB Finish	
X	(A Solder, pb free)	X	(C solder, pb free)
XX	(C Solder, pb free)	XX	(A solder, pb free)
X	(B solder, leaded)	X	(B solder, pb Free)
X	(B solder, pb Free)	X	(B solder, leaded)
QFP - ENIG PWB Finish		SOIC 20 - ENIG PWB Finish	
X	(B Solder Lead free)	X	(B solder, leaded)
XX	XX (C Solder, pb free)	X	(B solder, pb free)
XX	XX (A Solder, pb free)	X	(C solder, pb free)
X	X (B Solder, leaded)	X	(A solder, pb free)
QFP - Matte SN PWB Finish		SOIC 20 - Matte SN PWB Finish	
X	(C Solder, pb free)	X	(B solder, leaded)
X	(A Solder, pb free)	X	(B solder, pb free)
X	(B Solder, leaded)	X	(C solder, pb free)
X	(B Solder, pb Free)	X	(A solder, pb free)
QFP - Imm Ag PWB Finish		SOIC 20 - Imm AG PWB Finish	
X	(B solder, pb free)	X	(B solder, pb free)
X	(C solder, pb free)	X	(C solder, pb free)

Table 5 is an expansion of Figures 14 and 15, since each point on these two figures represent an average of the three solder suppliers. It is an attempt to separate the data for each component type, solder supplier and PWB finish. It shows the pair-wise comparison of all samples in a statistical technique called Multiple Range Tests. This technique is a method to divide samples into groups which are homogenous to each other (not significant), but may be significantly different than other samples within the group. This is done by aligning the X's for each data point if they are in the same homogenous group.. For example, in the first grouping (QFP – SMOBC PWB Finish), B solder is not significant whether Lead free or leaded, but C solder is significantly different then the first two. In the QFP ENIG, there are 4 elements to be tested (A, B, C pb free; and B leaded) in 6 pair-wise tests ($6 = 3+2+1$). 3 paired tests showed no significance (A pb free X C pb free, A pb free X B leaded, B pb free X C pb free). The other 3 pairs were significantly different (A pb free X B pb free, B pb free X B leaded, C pb free X B leaded). This is shown in three columns of X's. All of the remaining data in Table 5 are grouped into a maximum of 2 homogenous sets.

Compatibility of Leaded/Unleaded Solders vs. Leaded/Unleaded Components

This test was performed for tin plated SOIC 16 components, to determine whether it was significant that leaded and/or unleaded solder and/or components with tin plating finish can be used for different types of PWB surface finish. This will enable component customers to achieve forward and backward compatibility as the industry transitions to lead free technology.

The results are shown in Table 6, for the 7 combinations of solders and component-finishes tested. There were no significant differences in the 21 ($6+5+4+3+2+1=21$) pair-wise comparisons made. The baseline set of leaded solder and leaded component-finishes, and the ultimate goal of unleaded solder and unleaded component-finishes was not fabricated.

Table 6 - Multiple Range tests – Homogenous Groups

Comparison of unleaded solders to lead baseline with leaded and unleaded tin plated lead finishes.	
X	(AG, B pb free solder, leaded comps)
X	(AG, B leaded Solder, pb free comp)
X	(SN, B leaded Solder, pb free Comps)
X	(SN, B pb free solder, leaded Comps)
X	(SMOBC, B pb free solder, leaded Comp)
X	(ENIG, B pb free solder, leaded Comps)
x	(OSP, B pb free solder, leaded Comps)

Conclusions to Date

This research has shown the effects of atmosphere, paste selection, and PWB surface finish on visual appearance defects and an initial reliability assessment of lead free soldering. While Nitrogen and paste “B” yielded the fewest visual defects and SMOBC – HASL was significantly worse as a surface finish, the assembly process was not optimized for any of the variable options. Further, throughput and cost can be significant issues that may override some of these results.

For pull testing, this research established several important conclusions:

- **The selection of materials and process affects the pull strength of the solder joints for the QFP and SOIC components tested, using components with Nickel/Palladium/Gold finish:**

The pull forces are dependant on the footprint of the components used Thus pull forces in the SOIC were significantly higher than QFP.

The PWB surface finish has a significant effect on the pull test of the leads. Of the five PWB finishes (SMOBC, OSP, ENIG, Matted SN and Imm AG), ENIG was significantly lower than the other finishes in both IC's pulled. OSP was significantly higher in QFP and SMOBC/HASL was significantly higher in SOIC.

The solder suppliers were not important in the pull tests for the two IC types. Supplier B was slightly higher in QFP and significantly higher in SOIC 20.

Nitrogen was significantly higher than air reflow for QFP, not significant for SOIC.

- **Comparison of unleaded solder pulls to leaded solder pulls in QFP and SOIC, using components with Nickel/Palladium/Gold finish.**

This comparison was difficult since the baseline leaded PWBs were made with a single process: that of being soldered in air with leaded solder from supplier B, and the silver surface finish baseline was not available. The data indicated that the difference is not significant in most cases when using the same solder supplier (B) for unleaded and leaded solders.

- **Interchangeability of leaded and unleaded components and solders in SOIC and tin plated components pull tests.**

This is an important issue for electronic component suppliers and customers, concerned about keeping a dual set of materials for different markets around the world as the technology transitions from leaded to lead free soldering. The data indicates that for the set of 7 conditions analyzed in Table 6, with 21 pair-wise tests, there is no significant difference in the pull test results. Note that the baseline condition of leaded solders and component-finishes, and the ultimate condition of lead free solders and component-finishes were not tested.

Future work will include thermal cycling and then pull testing to assess reliability.

Acknowledgments

The authors wish to acknowledge the following persons and organizations for their contributions to this effort:

- Richard McCann and Al Grusby of Analog Devices of Wilmington, MA. For their contributions to the consortium and providing of components.
- John Pessia – Tyco Electronics – M/A-COM for laying out the test PWB and sharing his excellent knowledge in creating a diverse test vehicle for the Pb-free project.
- University of Massachusetts Lowell students: Pat Retelle and Joey Pang for performing the visual tests under the guidance of Helena Pasquito. Pat also designed and built the pull test fixture. In addition, Ryan Jansen, for devising the pull test methodology and performing all of the pull tests
- Santos Alicea, Manufacturing Engineer, Dawn Gilbert and Tai Nguyen, Documentation and Programming, Schneider Electric for providing operational assistance to the consortium team.
- BTU International of North Billerica, MA for providing the reflow oven and Rob DiMatteo and Fred Dimock for technical support and discussions.
- Tom Bzik of the Statistical Science Group, Air Products, for statistical analysis and discussions.

References

1. Lead Free Electronics Workshop, hosted by Lucent technologies, Merrimack Valley Works, North Andover, MA, Tuesday April 13, 2000. Lecture by Dr. Sammy Shina, UMASS Lowell Faculty
2. TURI continuing education conference, “TURI in Massachusetts: the Next Generation” on Tuesday April 25th 2000, Session, C2, the Lead Free electronics, at the Best Western Royal Plaza and Trade Center, Marlborough, MA, by Dr. Sammy Shina, UMASS Lowell Faculty.
3. State of Massachusetts Legislative committee on education policy, UMASS President Bulger’s Office, May 4th, 2000, presented by Karen Walters of BTU, a member of the Umass Lowell Lead Free Consortium.

4. IMPAS New England, 27th annual symposium and exhibition, Tuesday May 9^h 2000, Holiday Inn Conference Center, Boxborough, MA, session F, Surface Mount Technology, presented by Hemant Belbase, Umass Lowell Graduate Student.
5. CEAM /Turi Colloquoy on University Research in Sustainable Technologies Program (URST) at UMass Lowell, June 2nd 2000, presented by Hemant Belbase, Umass Lowell Graduate Student.
6. 2nd Workshop on Lead-Free Electronics, Technical Issues and Challenges in the Transition To Lead-Free Technologies, Thursday, June 29, 2000, at BTU International North Billerica, Massachusetts, presented by Karen Walters of BTU.
7. Consortium authors, "Design Of Experiments For Lead Free Materials, Surface Finishes And Manufacturing Processes Of Printed Wiring Boards", published by the SMTA International Conference at Rosemount trade center, Chicago, IL, September 2000, presented by Karen Walters of BTU.
8. Consortium authors, "Design Of Experiments For Lead Free Materials, Surface Finishes And Manufacturing Processes Of Printed Wiring Boards", published by the Chinese Electronics Association Journal, in Chinese
9. Consortium authors, "Selecting Material and Process Parameters for Lead Free SMT Soldering Using Design of Experiments Techniques", Apex Conference, January 2001, San Diego, CA, presented by Karen Walters of BTU and David Pinsky of Raytheon, members of the Umass Lowell Lead Free Consortium
10. "Lead Free at UMASS Lowell", Workshop on Modeling and Data Needs for Lead-Free Solders, sponsored NEMI, NIST, NSF, and TMS, Thursday, February, 2001, New Orleans, LA, short summary by Dr. Shina
11. Consortium authors, Reliability Testing Techniques For Lead Free Soldering Of SMT Technology", ETRONIX Conference, Anaheim, CA, March 2001, presented by Don Abbott of TI and David Pinsky .of Raytheon Reliability Lab.
12. Above paper translated into Japanese Journal ANBE, SMT, Kanagawa, Japan, July 2001
13. Presentation by Karen Walters on the project research to the SMTA Georgia Chapter in Atlanta, Ga. April 19, 2001
14. Presentation by Karen Walters on the project research to the IMAPS Boston Chapter in Marlboro, MA May 8th, 2001
15. Consortium authors, "Process and Material Selection for zero defects and superior adhesion Lead Free SMT soldering", the SMTA International Conference, Chicago, IL. September 2001.
16. Consortium authors, "Lead Free UMASS Consortium", conference sponsored by the Strategic Envirotechnology Partnership (STEP), Boston MA , November 2nd, 2001, presented by Sammy Shina.
17. Book Chapter on Design of Experiments for Lead free soldering, ""Environment Friendly Electronics: Lead-Free Technology," J. Wang editor, published by Electrochemical Publications Ltd in November 2001
18. Mass Lead free Consortium Status Update; Annual New England IMAPS Symposium; IMAPS Chapter Symposium, May 2003;,Boxborough, MA, Presented By Dick Anderson of MA/Com.
19. Consortium authors; " Materials and Processes for Surface Mount Lead Free Soldering", proceedings of the APEX Conference, Anaheim, CA, March 2003, pp. 20-2-1/9, presented by George Wilkish and Helena Pasquito of MA/Com
20. Consortium authors, "Testing Results for Lead-Free PWB's by the Massachusetts Lead-Free Electronics Research Consortium"; 2003 IEEE International; Symposium on Electronics and the Environment (ISEE); Boston, MA, May 2003. Presentation By R. Anderson of MA/Com.
21. Shina et al; Consortium authors. "A Comparative Analysis of Lead Free Materials and Processes Using Design of Experiments Techniques", SMTI International, Chicago, IL, September 2003