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A Reliability Comparison of Different Lead-Free Alloys and Surface Finishes in SMT Assembly

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Abstract
As we inch towards the somewhat shifting deadlines towards lead (Pb) restriction in Japan and Europe, there is an increase seen in the amount of studies performed for electronics assemblies soldered with Pb-free alloys. This paper presents results of an ongoing formal Pb-free activity (planned in 2000 and begun in 2001) with which we have been involved. Most Pb-free studies involve test vehicle designs that are not typically representative of real-world printed circuit board assemblies. With surface mount and through-hole components, a large number of soldering defect opportunities, and a large-sized substrate (12”x10”, four-layers, 62mil thick, and a four-up design), our test vehicle is one that is more challenging to assemble. It is suggested that if this board can be assembled with Pb-free materials, then it goes a long way towards ensuring the successful implementation of a more environmentally friendly product.

Keywords: Pb-free, Reliability, Lead-Pull, Microstructure Analysis, Intermetallics

Introduction

In prior studies,[3,4] we have shown that this complex board can be assembled with commercially available Pb-free solder alloys and surface finishes. The Pb-free alloys studied in this work are the following: Sn/Ag, Sn/$Ag_{3.0}$/$Cu_{0.5}$, Sn/$Ag_{4.0}$/$Cu_{0.5}$, Sn/Ag/Cu/Bi, Sn/Ag/Cu/Sb, and Sn/Zn/Bi. The eutectic Sn-Pb is also incorporated in this experiment for control purposes. The surface finishes consist of the following: HASL (a Sn/Cu HASL is used for Pb-free alloys and a Pb-bearing HASL is used for the eutectic Sn/Pb alloy), ENIG, Immersion Sn, Immersion Ag, and OSP. This work discusses the reliability studies performed on those boards and discusses the results in terms of the interactions/effects between the solder materials and the surface finishes. The boards are subject to accelerated thermal testing, including Air-to-Air Thermal Cycling (AATC) and Liquid-to-Liquid Thermal Shock (LLTS). The reliability analyses on these tested boards include electrical resistance measurements, lead-pull tests, nail tests, cross-sectioning, and micrographs.

Test Plan

This research program involved various reliability tests. The primary concern was Degradation Analysis in the form of Accelerated Environmental Testing with an offline failure monitoring system (as an event detector was unavailable at the time of testing). Cross-sectioning of the failed components and lead-pull tests were also performed to confirm the failure results from Accelerated Environmental Testing. The test vehicle used in this study is shown in Figure 1. The circuit panel was cut into 6 separate test vehicles for subsequent tests.

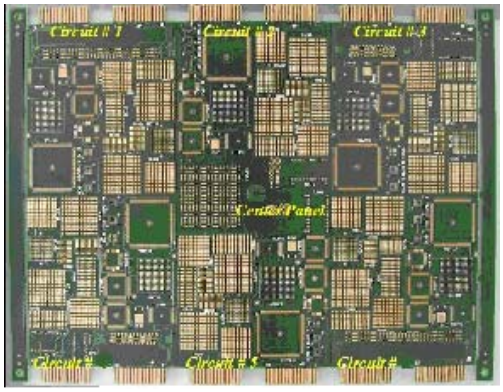

Figure 1 - Circuit Panel Used for Pb-free Assembly

This test vehicle has many different types of components each having varying electrical resistance values from 0.3 Ohm (BGAs) to 7 Ohms (QFP208)). These resistance values include the complete component circuit resistance.

A switching box ("Blue Box") was constructed to assist measurement of each component's electrical resistance. A Gage R&R study was performed to confirm the Blue Box's reproducibility, which was found to be acceptable.

A total of 360 circuit boards were allotted for this study. Out of 360, 240 were to be used for Air-to-Air Thermal Cycling treatment and the rest for Liquid-to-Liquid Thermal Shock treatment. Figure 2 shows a schematic for the AATC chamber test. JESD22-A104-B (condition B) standard was followed for this test.

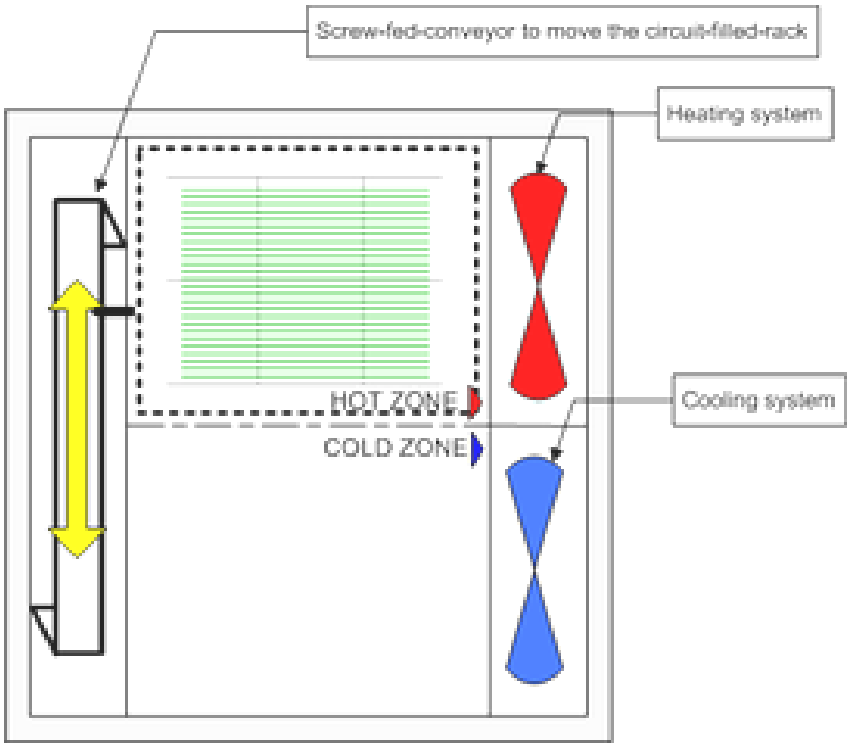

Figure 2 - Schematic of Air-to-Air Thermal Shock Chamber

As per the standards, the circuits were exposed from -55°C (T_{min}) to +125°C (T_{max}). The soak time (T_s) for the circuit is 10 minutes in both, cold and hot, chambers. For the LLTS shock chamber, JEDEC standard JESD22-A106-A (condition C) was followed, which requires the T_s to be 3 minutes. The cycle time, as based upon thermal loading, was 36.5 minutes for the Air-to-Air Thermal Cycling and 8 minutes for Liquid-to-Liquid Thermal Shock tests.

The condition of the electrical components was monitored by measuring electrical resistance at regular intervals (taken outside of the chambers) as mentioned in Table 1. Figure 3 is a schematic of the testing schedule and integral test-parameters, i.e., T_s, T_{min}, and T_{max}.

Table 1 - Accelerated Environmental Test Schedule

	Intervals	I	II	III	IV	V
# of Cycles	AATC	50	100	200	600	1008
	LLTS	30	60	120	300	-

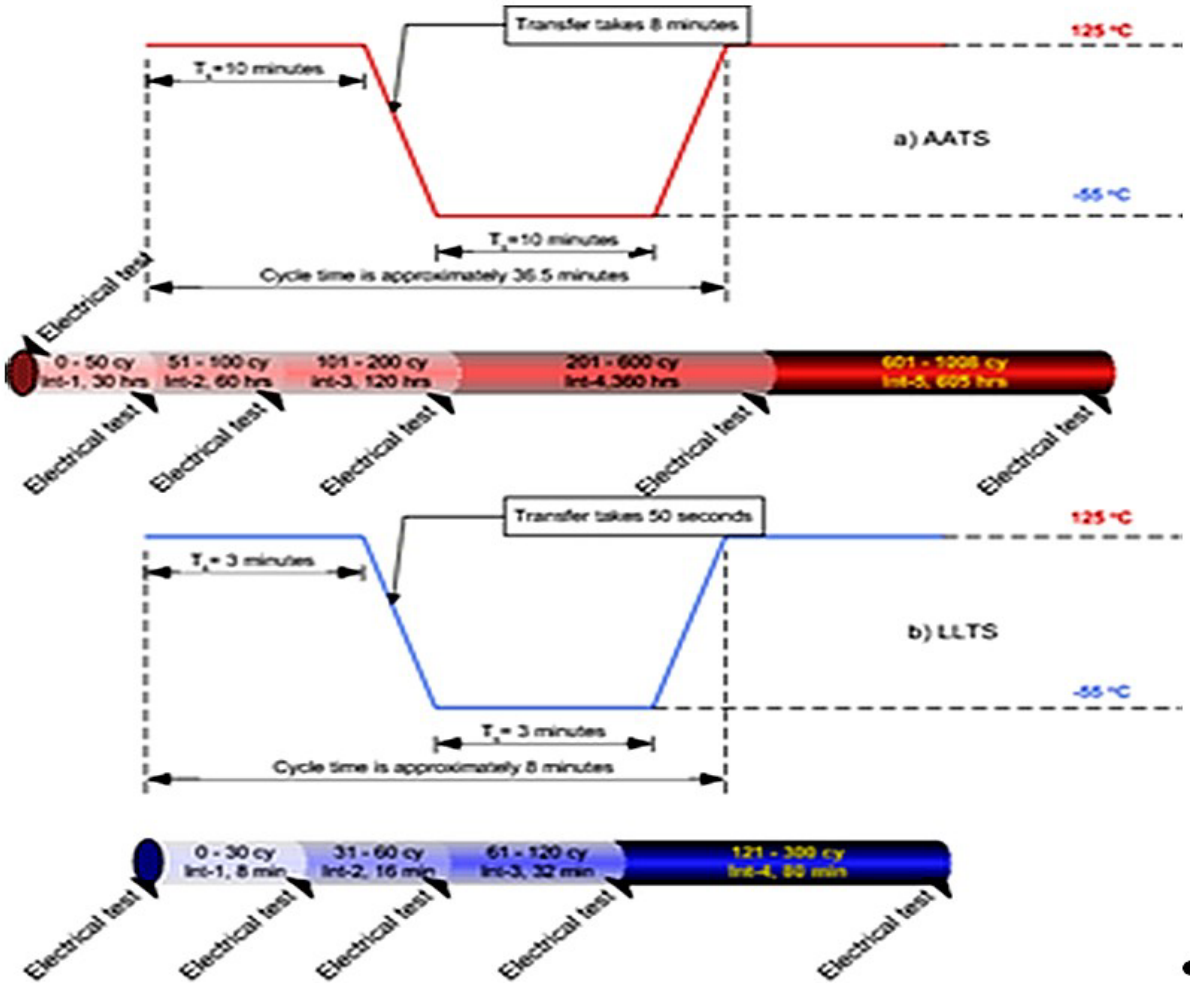

Figure 3 - Schematic Representation of Thermal Cycle Parameters for (a) AATC and (b) LLTS Chambers

A failure was said to have occurred when the resistance of a component-circuitry at any interval had increased by 10% of the initial resistance at the start of the thermal exposure. The choice was based on experience from research studies performed at the participating company's research lab. The basic idea was that if a component showed increase in resistance by 10% at room temperature then electrical continuity would indeed be "near-open" at extreme temperatures inside the shock chambers.

Upon identifying an electrical failure, the component was to be examined under a microscope for physical deterioration and increase in resistance across the component with remote probes just to confirm that it was really a failure.

The integrity of the solder joints was also tested by performing lead pull tests. Solder joints with gull wing leads of QFP208 were chosen for this test. The experimental set-up is shown in Figure 4. Several Pb-free paste/board-surface finish combinations mentioned in Table 2 were tested for the lead-pull tests. A total of 30 leads were pulled for each testing parameter condition with the pull speed of 0.05 inch/min and the data was statistically analyzed. The tested joints were longitudinally oriented with respect to the direction of the squeegee motion during stencil printing to keep variation in solder mass as minimal as possible.

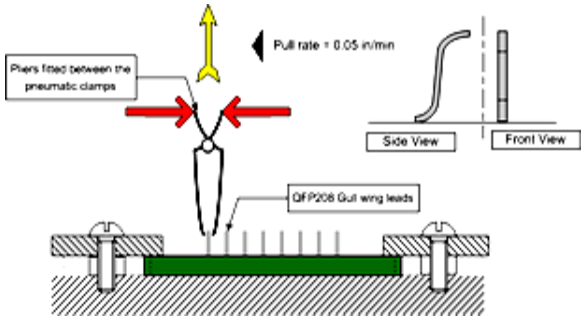

Figure 4 - Lead-pull Experimental Set-up

Table 2 - Lead-Pull Test Matrix

Paste	Board Surface Finish			
Sn-Pb	ENiG	OSP	FST	Alpha-Level
SAC305				
Sn-Ag				
SAC-Bi				
SZB				
SAC305-Stressed				

The next step was to identify failure modes by preparing epoxy cross-sections of the failed components and performing their visual inspections under high magnification microscopes. Visual inspection and increase in resistance with remote probes narrowed down the failure site. However, in the cases of μBGAs and QFPs that have solder joints in hard-to-reach areas, these components required more investigative efforts while grinding the cross-sections.

Observations and Results

During the environmental test monitoring, several important observations were made. Given the 10% resistance increase criterion, for small resistance components, mathematically a slight deterioration of the solder joint will result in a failure. On the other hand, for high resistance components, such as QFP208s and ¼ Watt Resistors, these would require a considerable amount of increase in resistance for them to be qualified as failures. This implies that even the slightest increase due to bad connection, worn edge connector or lower tare value could give rise to a false failure reading. This phenomenon is explained in Table 3. *(Tare value is an internal resistance of the blue box that is zeroed out before the start of each set of readings. This is achieved by shorting pins in the edge connectors with metal plates and proper switch positions that will bring the resistance value in a "ball park" of the predetermined internal resistance.)* Since this tare value did not always remain constant, it affected subsequent readings by the difference in the earlier tare and the tare value at a reading in question. Tare values of all the readings taken were not tracked and, hence, it was difficult to attribute the failure to the difference in tare at the time of failure analysis.

The following statement has been taken from the co-author's research work: [2] "It is important to bear in mind that each circuit is composed of several parts or legs, and each of these has a resistance, which sum up to the overall resistance of the daisy-chained circuit." To illustrate this, two circuits have been broken down into their constituent legs below (see Table 3).

From Table 3, it is evident that the QFP208 component would have to suffer a resistance increase of 10.74% to fail, whereas the 0402-H array would have to increase by 17.34% to fail (assuming the trace resistances stay the same). It is even worse for the PLCC28 circuit, which demands up to a 125% increase (by performing similar calculations as in Table 3 for PLCC28) for the component alone to show a 10% increase over the entire circuit.

Based on the pattern in resistance increase, the following two types of failures were classified.

- Transient Failures
- Terminal Failures

Table 3 - Breakdown of two SMT circuits on Pb-free board

	QFP208	**0402H**
Circuit Element	Ω	Ω
Card edge to via-1	0.010	0.000
Trace from via-1 to via-2	0.142	0.440
Component or array	6.060	1.130
Ground trace to card edge	0.300	0.390
Total resistance	6.510	1.960
Δ required to fail (10% criterion)	0.651	0.196
Required %increase in the resistance across a component alone to reflect 10% increase across the circuit containing that component	**(0.651/6.06) X 100** = 10.74	**(0.196/1.13)** X 100 = 17.34

Transient Failures are the ones that showed an increase in resistance by more than 10% (approx. 10~20%), however, upon additional exposure, the increase disappeared and the component's electrical continuity was "normal". These types of failures were analyzed for electrical continuity with remote probes to confirm the resistance change and, for almost all such cases, resistance increase was found to be in the operating range.

Terminal Failures are the ones that showed either discontinuity in the electric circuit or very high increase in the resistance that did not go back to the normal operating range. These types of failures were more suitable for failure mode identification and analysis by preparing cross-sections. However, during the failure-confirmation stage, certain components having a very high percent resistance change were identified to be "normal".

Table 4 shows the number of failures recorded for all the testing conditions, along with the total possible number of opportunities for a failure to occur. These failures include *Terminal Failures* as well as *Transient Failures*. However, since transient failures did not provide any failure mode information, it was deemed necessary to exclude transient failure data from the study. Hence, Table 5 represents a dependable distribution of the confirmed "open" failures.

Table 5 not only shows the "open" failures but also shows the number of R1206 failures that contributes to the total. Earlier it was thought that R1206, being a larger component, thus having larger solder mass, would provide greater strength. However, that was not the case as R1206 contributed to about 60% of the total failures. This could be due to higher extent of CTE mismatch or possible Pb-contamination arising from Pb-coated R1206s. The supplier's data sheets showed that the R1206 resistors were coated with Pb; however, it was not confirmed by metallurgical tests.

Compared to R1206, the other components recorded a fewer number of "open" failures, which is evident from Figure 5. A closer look at Figure 5 reveals that no R1206 failure were recorded for Sn-Pb solder alloy, whereas a significant number of failures occurred for all the rest of the solder alloys and R1206 combination. This fact supports the assumption of probable Pb-contamination from the possible Pb-coated R1206 components. There is a greater possibility that data of "open" including failures for R1206 is biased. Therefore, if R1206s are excluded from the dataset, then it provides a fair basis for comparison of the testing conditions and that is what has been done in Table 5.

The overall result has been plotted in the graph shown in Figure 6. With a maximum number of failures being 3 for several paste/board-finish conditions, the performance of these conditions could not be statistically evaluated with strong confidence. However, for the length of the thermal shock treatment that the Pb-free surface mount solder joints were tested, it can be concluded that Pb-free solders performed as good as the eutectic Sn-Pb solder.

Table 4 - Total Failure Out of Possible Opportunities

Alloy/Board Finish	Failure	Opportunities
Sn-Pb/ HASL	4	970
Sn-Pb/ ENIG	2	1164
Sn-Pb/ Alpha	11	1164
Sn-Pb/ FST	1	1164
Sn-Pb/ OSP	1	1164
Sn-Ag/ HASL	2	1164
Sn-Ag/ ENIG	6	1164
Sn-Ag/ Alpha	8	1164
Sn-Ag/ FST	4	1164
Sn-Ag/ OSP	6	1164
SAC305/ HASL	2	1164
SAC305/ ENIG	13	1164
SAC305/ Alpha	12	1164
SAC305/ FST	4	1164
SAC305/ OSP	11	1164
SAC405/ HASL	1	1164
SAC405/ ENIG	4	1164
SAC405/ Alpha	3	1164
SAC405/ FST	10	1164
SAC405/ OSP	4	1164
SACB/ HASL	2	1164
SACB/ ENIG	5	1164
SACB/ Alpha	13	1164
SACB/ FST	5	1164
SACB/ OSP	13	1164
SZB/ HASL	5	1164
SZB/ ENIG	3	1164
SZB/ Alpha	N/A	N/A
SZB/ FST	1	1164
SZB/ OSP	12	1164
SZB/ Sn-Pb HASL	0	1164

Table 5 - Actual Number of Failures and Only R1206 Failures

Finish / Paste	Sn-Pb	Sn-Ag	SAC 305	SAC 405	SAC B	SZB	Total
HASL	**0** -	**2** -	**0** 2	**0** 1	**2** -	**1** -	**5** 3
ENIG	**1** -	**1** 5	**0** 6	**0** 4	**3** 1	**1** -	**6** 16
OSP	**1** -	**0** 2	**3** 2	**2** 2	**0** 2	**1** 1	**7** 9
FST	**1** -	**1** 3	**3** -	**2** 3	**0** 2	**0** 1	**7** 9
Alpha	**0** -	**2** 2	**1** 2	**1** 2	**0** -	**N/A** N/A	**4** 6
Total	**3** -	**18** 12	**19** 12	**17** 12	**10** 5	**5** 2	**72** 43
w/o R1206	3	6	7	5	5	3	29

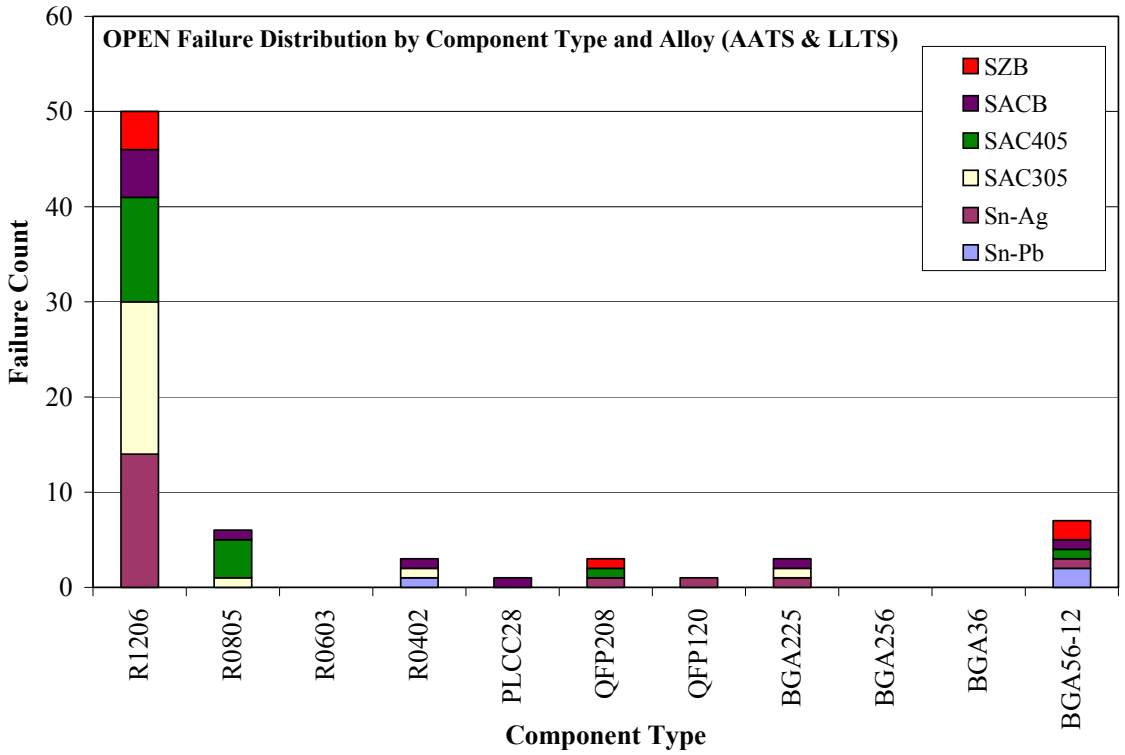

Figure 5 - Failure Distribution by Component Type and Alloy

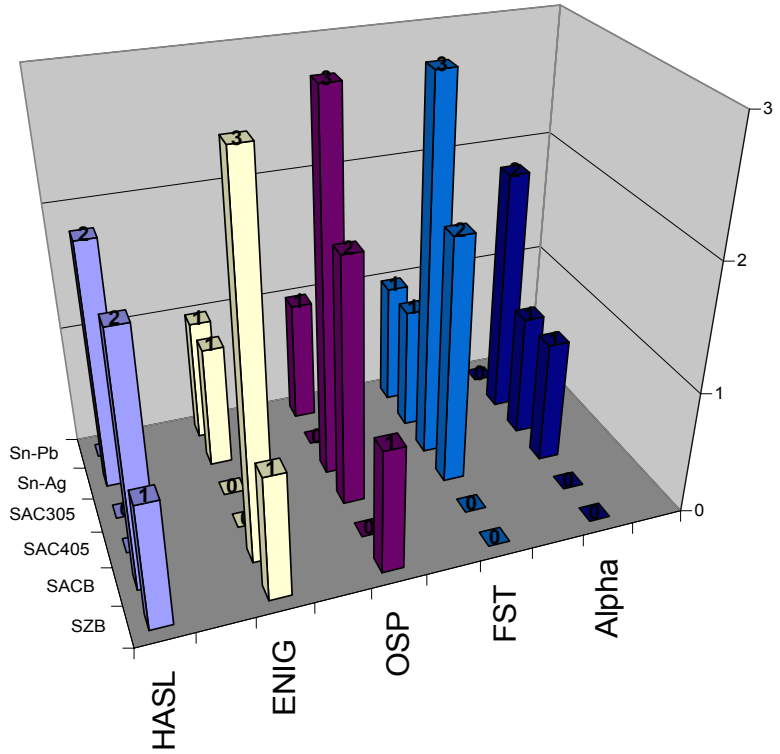

Figure 6 - Overall Failure Distribution

Results of the lead-pull testing performed to test solder joint strength are now discussed. Figure 7 shows the box plot of the results obtained from the Lead-pull tests performed for test matrix shown in Table 2. The box-and-whisker plot in Figure 7 shows the standard deviation associated with the dataset and the direct comparison among the tensile strength for each condition. Solder joint strength for Pb-free alloys are comparable to that of the eutectic Sn-Pb alloy. Certain Pb-free alloys

have even showed higher mean values, however, it is very difficult to say that a particular combination performed better than the other. From Figure 8, the confidence intervals for most of the conditions overlap, which shows that there is no significant difference in the obtained results.

Figures 9 through 11 show the distribution for the thermally stressed conditions of the SAC305 solder joints and the board surface finishes of OSP, I-Ag and FST. Thermal exposure weakened the solder joints due to increase in brittle intermetallic layer thickness and, therefore, the decrease in solder joint strength is observed. However, it is still comparable to the joints with no thermal exposure and, therefore, does not raise any alarms.

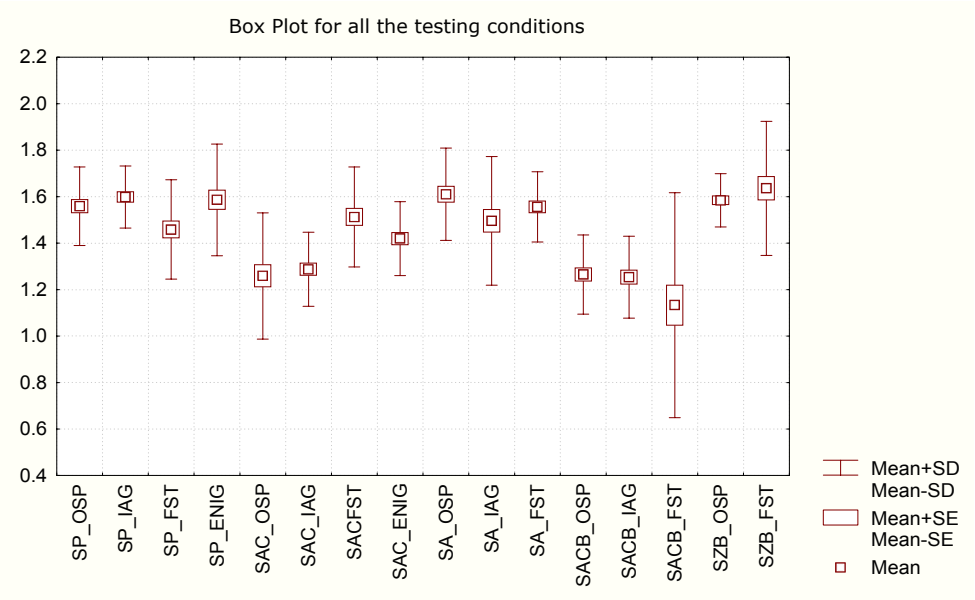

Figure 7 - Box Plot of Joint Strength Obtained from Lead-pull Tests

One-way ANOVA: Load at Failure versus Alloy/Finish Combination

```
Analysis of Variance for Load at
Source     DF        SS        MS        F        P
Alloy/Fi   15    9.0857    0.6057    14.99    0.000
Error     464   18.7444    0.0404
Total     479   27.8301

                                        Individual 95% CIs For Mean
                                        Based on Pooled StDev
Level      |  N      Mean     StDev  --+---------+---------+---------+----
SAC305/A      30    1.2877    0.1595     (----*----)
SAC305/E      30    1.4193    0.1594               (----*---)
SAC305/F      30    1.5127    0.2153                     (----*----)
SAC305/0      30    1.2587    0.2715   (----*----)
SACB/Alp      30    1.2533    0.1763   (----*---)
SACB/FST      30    1.3073    0.1737      (----*----)
SACB/OSP      30    1.2650    0.1705    (---*----)
Sn-Ag/Al      30    1.4960    0.2768                (----*----)
Sn-Ag/FS      30    1.5560    0.1509                    (----*----)
Sn-Ag/OS      30    1.6103    0.1989                        (---*----)
Sn-Pb/Al      30    1.5983    0.1335                       (----*---)
Sn-Pb/EN      30    1.5863    0.2402                       (----*----)
Sn-Pb/FS      30    1.4587    0.2137              (----*----)
Sn-Pb/OS      30    1.5587    0.1689                    (----*----)
SZB/FST       30    1.6357    0.2887                         (----*----)
SZB/OSP       30    1.5840    0.1147                       (----*---)
                                        --+---------+---------+---------+----
Pooled StDev =    0.2010                1.20      1.35      1.50      1.65
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Figure 8 - One-way ANOVA for Lead Pull Test for the Thermally Stressed Gull-wing Leads

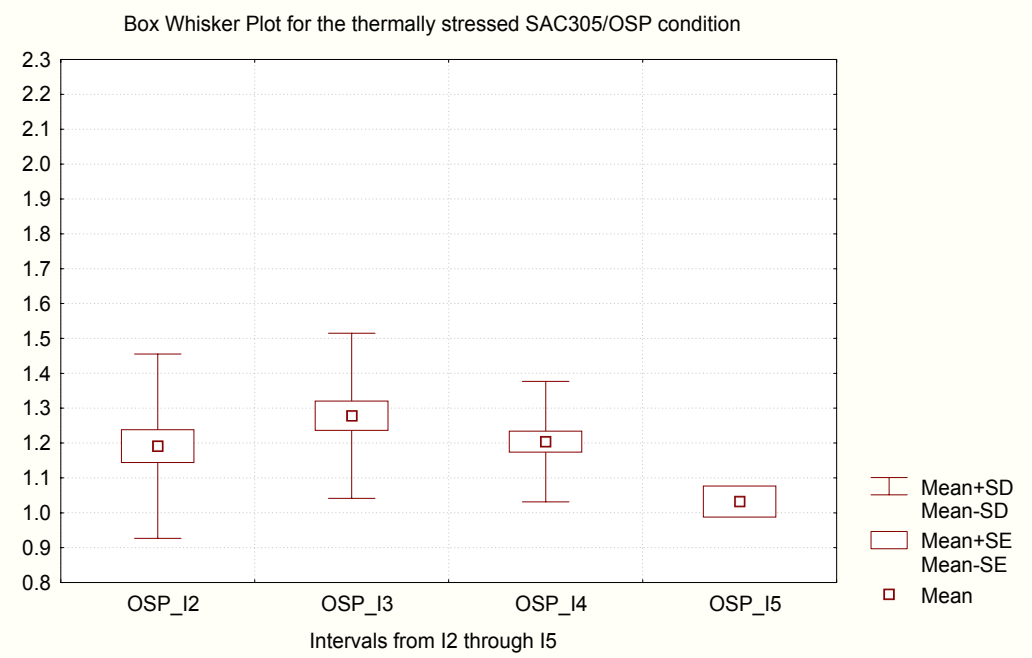

Figure 9 - Box-and-whisker Plot for Solder Joint Strength of SAC305/OSP Testing Condition

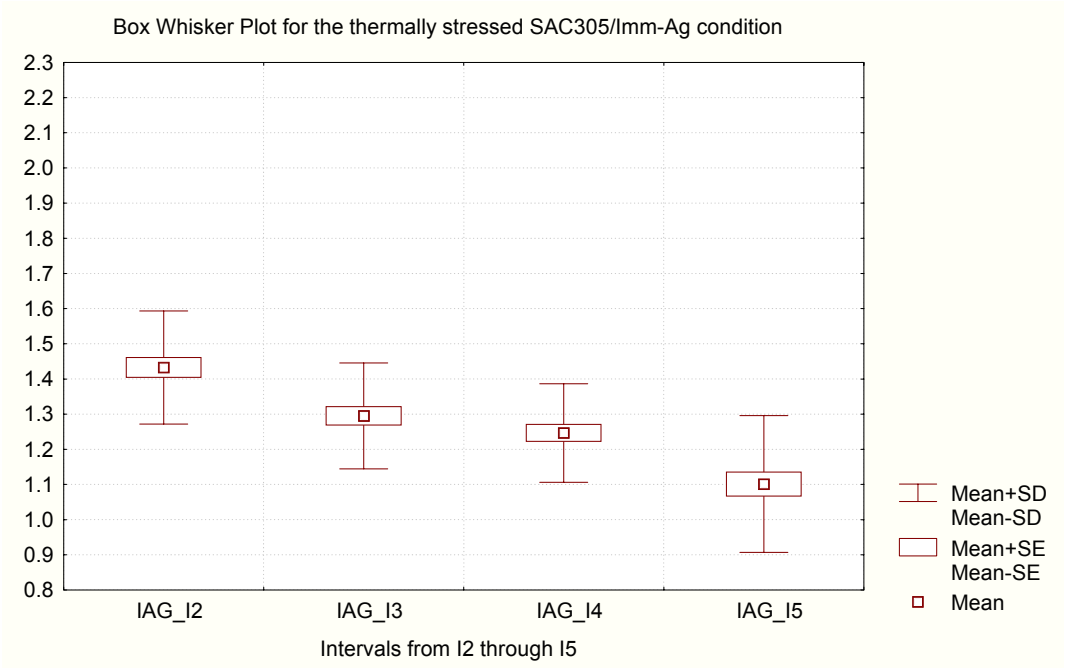

Figure 10 - Box-and-whisker Plot for Solder Joint Strength of SAC305/I-Ag Testing Condition

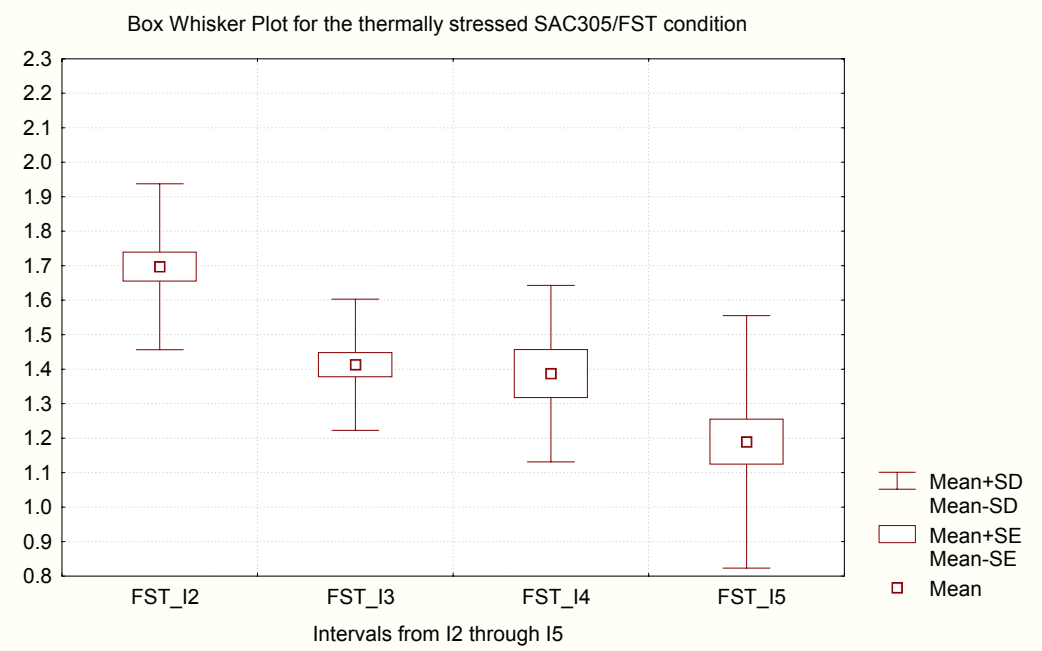

Figure 11 - Box-and-whisker Plot for Solder Joint Strength of SAC305/FST Testing Condition

Figure 12 shows results of a One-way ANOVA study for the thermally stressed gull-wing joints. SAC305/FST combination joints, right after the 2nd interval, stands out to have the maximum strength.

The following images in Figure 13 show the solder joint sites that were pull-tested. The top two images show pulled QFP208 joints that were thermally stressed up to 1008 cycles. All the failures for the thermally stressed components have occurred at the lead-solder interface, whereas baseline SZB conditions showed failures near both the solder-pad and the lead-solder interfaces.

The SZB/FST condition showed enormous voiding in the pulled joints. This voiding can be seen in the bottom two images of Figure 13. The top-left image belongs to the SAC305/OSP condition and the top-right image belongs to the Sn-Pb/OSP condition. Both of these images show voiding. SAC305/OSP showed less tensile strength than Sn-Pb/OSP, which could be because of voiding present in the solder joints of SAC305/OSP conditioned boards, whereas tensile strength remained unaffected for Sn-Pb/OSP.

One-way ANOVA: Max. Load at Failure versus Thermally Stressed Condition

```
Analysis of Variance for Max. Loa
Source     DF        SS        MS        F        P
Thermall   11    9.8016    0.8911    21.10    0.000
Error     327   13.8085    0.0422
Total     338   23.6101

                                    Individual 95% CIs For Mean
                                    Based on Pooled StDev
Level       N      Mean     StDev  --+---------+---------+---------+----
SAC3/A-2   30    1.4327    0.1607                  (--*--)
SAC3/A-3   30    1.2950    0.1505              (--*--)
SAC3/A-4   30    1.2463    0.1400           (--*--)
SAC3/A-5   30    1.1013    0.1944     (--*--)
SAC3/F-2   30    1.6970    0.2405                                (--*--)
SAC3/F-3   27    1.4130    0.1904                   (---*--)
SAC3/F-4   13    1.3873    0.2559                (---*----)
SAC3/F-5   29    1.2469    0.1889           (--*--)
SAC3/O-2   30    1.1910    0.2643        (--*--)
SAC3/O-3   30    1.2783    0.2368           (--*--)
SAC3/O-4   30    1.2040    0.1726        (--*--)
SAC3/O-5   30    1.0323    0.2503  (--*--)
                                    --+---------+---------+---------+----
Pooled StDev =    0.2055            1.00      1.25      1.50      1.75
```

Figure 12 - One-way ANOVA for Lead Pull Test for the Stressed Gull-wing Leads

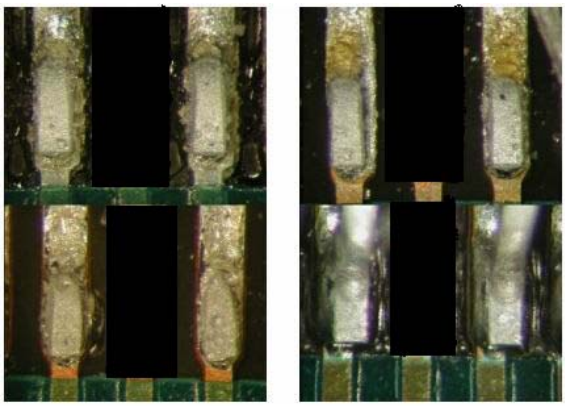

Figure 13 - Condition of Solder Joints at the Sites of the Pulled Leads

Some conditions demonstrated pad lifting during the lead-pull testing. Some of the prevalent conditions to show this phenomenon are SAC305/I-Ag, SAC305/FST, Sn-Pb/OSP, Sn-Pb/I-Ag and Sn-Pb/FST. Whether the pad-lifting phenomenon suggests better solder-joints is yet to be determined.

As some material is left at a very high temperature, the microstructure of that material becomes coarsened and the fatigue strength reduces. When the temperature is suddenly changed from a higher temperature to a lower temperature, the thermal stresses are induced in them. A site having higher concentrations of these thermal stresses shows initial signs of cracking and ultimately fails with a fractured joint. A typical thermal cycling loading that occurs during the accelerated environmental testing is as shown in Figure 14.[1] The schematic shows a typical loading pattern that causes fatigue and the solder joint deformation process.

Figure 15 is a cross-sectional view of a SZB alloy with OSP board surface finish BGA36 solder joint that has seen 300 thermal cycles in the LLTS chamber. The image on the right hand side is that of a magnified right corner of the same joint shown inside the red rectangle. With an increase in the number of thermal cycles, grains start to grow in all directions. As the growth occurs throughout the solder-mass, neighboring grain boundaries merge into each other and become longer. If the same joint would have been exposed to more cycles (say, an additional 300 cycles), it could have failed with a probable partial crack running parallel to the red arrows. We rarely see a crack propagating through the bulk of a spherical solder joint, the reason being that a crack initiates in the maximum stressed portion of a joint. The bulk of a solder has uniformly distributed stress, however, increased regional stresses are seen near sharp edges, corners or different-material interfaces. In addition to these inherent properties of a joint, a solder joint is already under stress right after it is reflowed due to mismatch in thermal coefficient, which is exacerbated by the thermal shock treatment near the solder-component interface.

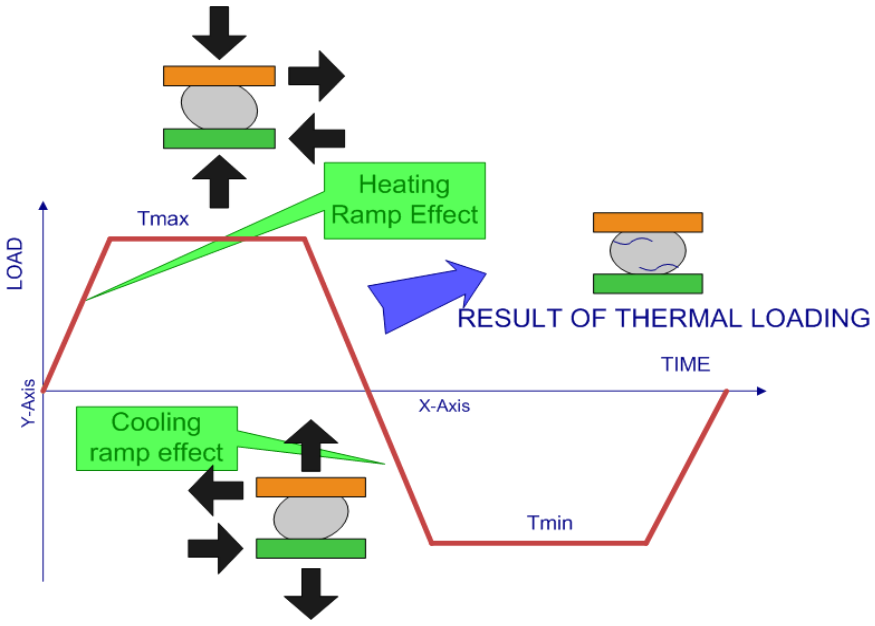

Figure 14 - Thermal Loading Pattern (Source: Ref. 1)

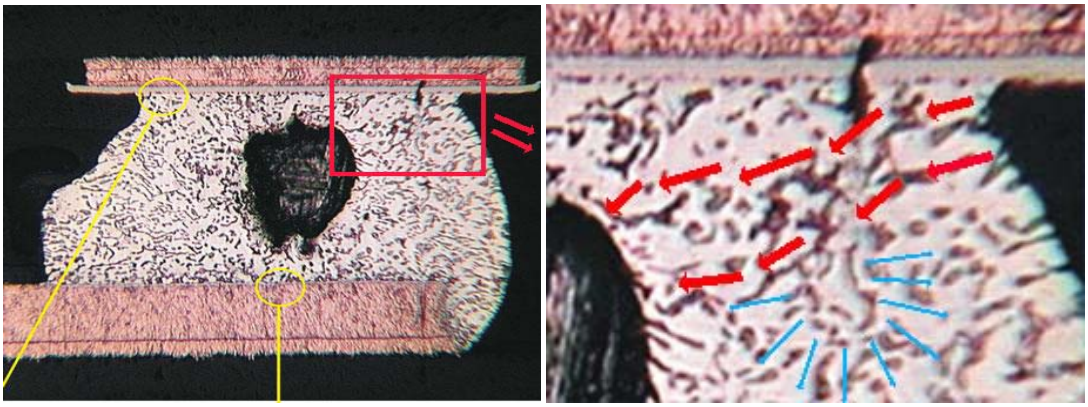

Figure 15 - Result of Increasing Grain Boundaries

Cracks and failed solder joints were prominent in the "open" failures cases of chip resistors and the PBGA225s. Whereas PLCC28 and QFP208, that were classified either as "open" or transient failures, hardly showed any presence of cracks. The following images of chip resistors and BGAs with cracked solder joints reveal areas that are prone to cracking.

In Figure 16, the first two images are that of the same component. The arrows show the direction of loading during thermal exposure. The top-right image shows a box where a crack initiates due to combined effects of thermal loading, thermal coefficient mismatch and highly stressed material transition area.

The chemistry of the solder alloy used seems to have a peculiar effect on the failure mode. The images in Figure 17 are those of failed chip resistors soldered with the Sn-Ag alloy. All of these solder joints have been exposed for 1008 cycles. Only solder joints of Sn-Ag and SZB alloys have showed the above type of failure mode in which the crack propagated through the solder bulk. This could be due to two possible reasons.

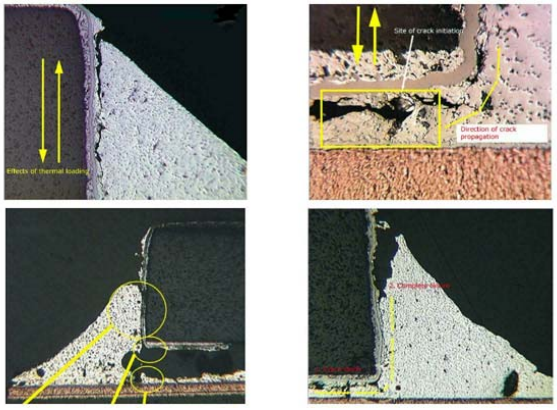

Figure 16 - Cracks found in R1206 Chips

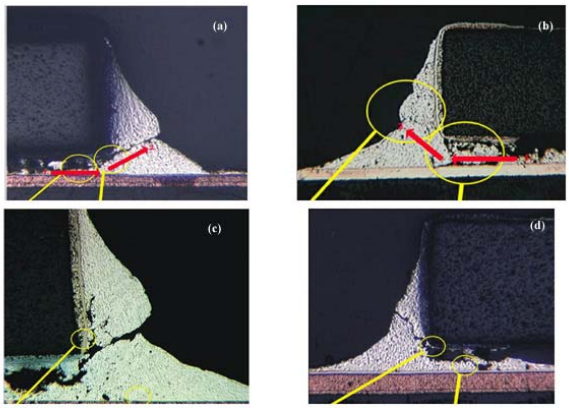

Figure 17 - Failures in Sn-Ag R1206 Solder Joints

Such failure, in one scenario, could be due to weakening of joints as a result of Sn-migration in the solder joints at the higher temperatures during the thermal exposures. In the other scenario, the location of the Pb-rich phase would guide the crack through the solder bulk. It is more likely for the low melting point Pb-rich phase to solidify near the bottom corner of the chip or in a layer by the vertical chip termination face. This needs to be verified with the help of a Scanning Electron Microscope (SEM) having Energy Dispersive X-ray Spectroscopy (EDX) feature.

PBGA225s and BGA256s are the other types of components that have revealed cracked joints upon the thermal shock treatment. The guiding factors of the failure mechanism for BGAs are the same as those for the discrete components. Almost all the failures that we have noticed in this study showed crack initiation from the solder/component interface. This is likely due to the interface having minimum cross-sectional area (parallel to the plane of the substrate) and thus offering the least resistance to the induced thermal stress. This is one of the main reasons as to why it does not fail at the solder/substrate interface. Also, another probable reason could be that the package thickness is less than the board thickness and warps more at higher temperature, which induces greater stresses at the solder/component interface.

The coarsened grains can be easily seen in the magnified images of Figure 18. The figure validates the difference in cross-sectional area at the solder/component and solder/substrate interfaces. Even though solder bumps on the components before reflow are spherical, they get modified into the shape seen here under the package's own weight when solder is in the liquidous state at the time of the reflow process.

Figure 19 reveals a huge void present in the center of the solder joint. However, it did not seem to affect the performance of the joint during an earlier part of the shock treatment as it failed only during the last interval of the exposure.

In Figure 20, we see an abnormal type of failure mode in which the failure occurred at both the intermetallic layers.

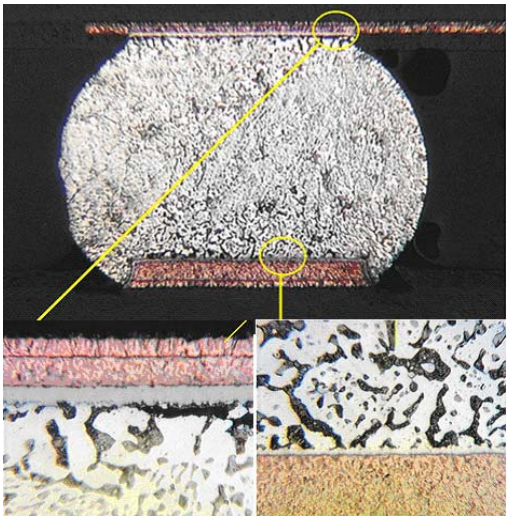

Figure 18 - Failed PBGA225 with SAC-Bi/OSP Solder Alloy Exposed to 1008 Cycles

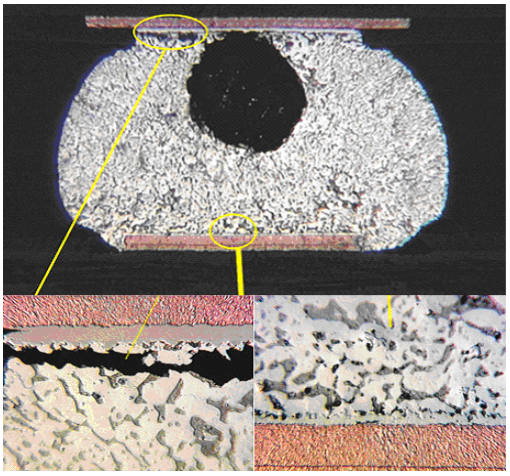

Figure 19 - Failed PBGA225 with SAC-Bi/FST Solder Alloy Exposed to 1008 Cycles

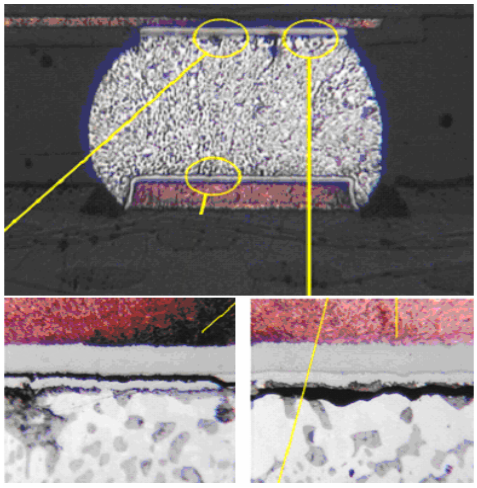

Figure 20 - Failed PBGA256 with Sn-Pb/OSP Solder Alloy Exposed to 1008 Cycles

Conclusions

The length of the thermal exposure treatment was considerably smaller, viz. 1008 for Air-to-Air and 300 thermal shock cycles for Liquid-to-Liquid, with temperature range of -55°C and 125°C. Exposure of this length was not sufficient to generate enough failures to calculate MTTF.

Advanced means of monitoring the accelerated environmental tests must be employed to make sure that consistent failure data is collected.

Lead-pull testing revealed that Pb-free solder alloys provide comparable solder joint strength to that of the eutectic Sn-Pb solder alloys. Thermal shock reduced the strength due to coarser intermetallic layer. However, the strength of Pb-free joints, even after thermal shock test, was comparable to that of the eutectic Sn-Pb solder.

The failure modes appear to depend on the geometry of a joint, the solder alloy used, and the type of lead termination. Two types of failure modes were identified for the discrete chip resistors. BGAs and μBGAs showed significant amount of coarsening. However, they did not show proportionate growth in the intermetallic layer thickness, which stresses the necessity of longer thermal exposure.

As of yet, the study did not reveal any failed joints in case of either PLCCs or QFPs, and a very small number of failures for R0603s and R0805s. A probable reason for no failures in the above active components could be the flexible leads that take up thermal stresses and more than half of the failed components were not outright "open" failures; instead, they were near-threshold or *transient failures*. Smaller size of the R0603s and R0805s plays in favor for their performance without failing. Since the size of these chips is smaller, the bending due to the thermal coefficient mismatch does not induce a critical amount of stress for the joints to fail. Also in this study, R1206s were the only resistors that had possible Sn-Pb termination, versus Ni-Sn terminations on the other smaller resistors and the active components. In order to relate any effects of Sn-Pb finish with a large number of R1206 cracked resistors requires SEM/EDX analysis to identify metallurgical effects of Pb-rich interface on reliability of the solder joints.

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