Presented at IPC Printed Circuits Expo®
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Designers Summit 04

Automatic Generation of RC Network Models for a BGA Package

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Abstract
The need for dynamic compact models for Integrated Circuits (ICs) is a well-recognized problem in electronics cooling simulations of electronic systems. Simplified thermal models have been reported in literature to simulate steady-state and transient thermal behavior of IC devices. Most of the simplification approaches require a pre-determined topology of a resistance-capacitance (RC) network. Multigrid technique allows for automatically constructing both the topology and characteristics of the reduced-order or compact models of devices (primarily IC packages) for use in system-level simulations. In this study, we report an approach where the topology of RC networks is automatically generated. The topology of the RC network is not predetermined and can be automatically changed to meet the modeling accuracy requirement. The procedure is robust for packages with various degrees of complexity in both automatic construction of RC network topology and automatic extraction of nodal RC values. The procedure is also applicable for complex IC sub-systems or systems like multi-chip modules, stacked die package, system-in-package, and CPU module, and hard drives.

In the study report herein, the method is applied to a 196-pin fine pitch ball grid array (FBGA15x15_196L) package. An RC network is created for the package and then used in a transient CFD simulation under single phase natural convective cooling in JEDEC chamber. The simulation results using the RC network model are compared to the corresponding detailed package simulation.

Introduction
The main problems in modeling of electronics systems are - the handling of disparate length scales ranging from sub-micron at the IC (Integrated Circuit) level to meters at the cabinet-levels, and, the accurate prediction of time-dependent temperature rises. As thermal simulations, both steady-state and transient, increasingly become part of tools in the overall product design process in the electronics industry, addressing these problems remains a key challenge in making the simulation tools more effective in the design cycle.

This requires that a reduced-order or compact model approach be used for IC packages in the system-level simulations. This is a very well recognized and documented approach. Many topologies of RC network representations for certain IC package types have been proposed.[1, 2, 3] The IC package types and their internal structures are becoming increasingly complex and RC networks of simple two-, four-, or shunted-network configuration have shown to produce large errors.[3, 4, 5] Alternate topologies have been proposed for different package types. In this exercise, describing the appropriate network topologies and the characterization of the resistances & capacitances that accurately describe the thermal behavior of the IC package under a variety of operating conditions becomes the central issue. Again topologies for specific package types and procedures to characterize the resistance have been proposed and are in the process of being accepted in the industry.[6-11]

The present approach proposes to further the concepts of generating thermal resistance network topologies by Boyalakuntla and Murthy.[12] In their COBRA approach, the multigrid operator is the basis for creating the network topology reduced-order model. The resistances were computed using an optimization process. They also required that spatial temperature distribution in the reduced model be compared to the detailed simulation of the package as a constraint in their procedure. This is a stringent requirement on the compact model representation. It should be sufficient to require that network representation of the package in question be compared to the junction or junctions (in multi-die or multi-chip modules) and the heat flow out of the package under different boundary (environmental) conditions the package is likely to experience. This paper uses this sufficiency condition, uses the fine-grid equations as the basis of computing the network resistances, and extends the approach to the inclusion of capacitance for transient thermal analysis.

The proposed compact model generation method, called the Automatic Compact model Extraction (ACE) method, allows for automatically creating hierarchical dynamic network models of increasing complexity, for use in steady-state as well as transient numerical simulations of IC packages. This method employs the multi-grid operator, a standard approach in solving large linear systems[12] on the discretized form of energy conservation equation for the package.

In the following sections, the methodology of employing the multigrid operator to extract both the network topology and the RC characteristics is described. Then the results obtained for steady-state simulations of three different IC packages and their comparison to the corresponding detailed package simulations are presented. The formal validation of the method for transient simulation under various operating conditions is a subject of subsequent investigation. It is assumed that the detailed model is validated for the IC package or device in question and is the starting point for the generation of the compact models. So, the validation is presented only with respect to the detailed model.

The ACE Formulation

The basic principle of the ACE method is to start with creating a mesh (grid) for the package configuration and generating the linear system of algebraic equations for the energy transport in the package. Using a multigrid procedure,[12-14] a sequence of linear equations is obtained at the coarser levels. The process of generating coarse-grid equations based on the fine-grid equations is the key difference between the proposed method and the straightforward coarse-grid discretization of the energy equation. In the proposed method, the material properties of the constituents of the package and geometry together determine the final RC network topology while in the straightforward coarse-grid discretization the network will be determined by the geometry alone.

For the purposes of illustration, we will describe the basics of the procedure using a two-dimensional (2D) example. The extension to three dimensions (3D) package configurations is natural and straightforward. This description is from Nagulapally and Zhao.[15] A 2-D network representation for a typical chip package is shown in Figure 1. For the purposes of illustration, the geometric network is shown in Fig. 1 with the understanding that, as mentioned above, the network generated using the proposed method will result in a different topology compared to the geometry-based simplified description shown. The network consists of a set of nodes connected by conductances. The temperatures T_i are stored at nodes, which may lie either in the interior or at the external surface of a package. In addition, we distinguish between nodes in the die from nodes elsewhere in the interior because the die generates heat. Each interior node is associated with a volume V_i.

Nodal temperatures are determined by performing a heat balance at the node to yield:

$$\sum_{j=1}^{M} C_{ij}\left(T_i - T_j\right) = q_i''' V_i \qquad (1)$$

where

C_{ij} is the conductance joining the nodes i and j.Ti is the temperature of the node of interest, and T_j is the temperature of neighbor node j. There are a total of M neighbor nodes; the total number of nodes may vary from node to node. The heat generation per unit volume, q_i''' is non-zero for nodes in the die. Everywhere else, it is zero.

At boundary nodes, the heat balance relation depends on the boundary condition associated with the boundary. Thus given a set of conductances, we obtain a set of linear algebraic equations for the nodal temperatures by applying energy conservation equation for steady state heat transfer.

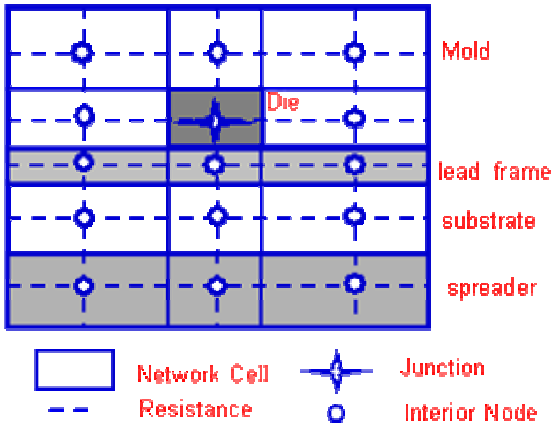

Figure 1 - Network Model for a Typical 2-D chip package

In the proposed method, the network topology is generated automatically using principles of multi-grid agglomeration as outlined in Mathur and Murthy.[12] Here, the procedure starts with a detailed mesh, either structured or unstructured, and utilizes the physics contained in the underlying finite volume discretization to deduce the network connectivity. The fine level finite volume discretization is viewed as a complex network with nodal connectivities implicit in the underlying mesh. The coefficients derived from the discretized energy equation are essentially the network conductances.

Consider a typical finite-volume discretization, such as that described in Mathur and Murthy[12] or Patankar.[13] The temperature at each cell P in the detailed mesh is related to its cell neighbors through the discretization process as:

$$a_P T_P = \sum_{nb} a_{nb} T_{nb} + b \tag{2}$$

where nb denotes neighbor cells and b denotes the source term. It is non-zero for all cells in heat generating regions and for boundary cells. For conduction heat transfer, the coefficients a_{nb} are the inverse of the conduction resistance between nodes p and nb.

Coarse cells are created from the detailed mesh by agglomerating adjacent cells, which are connected by the largest anb coefficient. As shown in Mathur and Murthy,[12] this has the effect of agglomerating together cells in regions likely to have similar temperatures. The extent of agglomeration depends on the desired number of final agglomerates. The procedure can be applied recursively to create arbitrarily coarse meshes. Thus, a series of hierarchical networks can be created, ranging from the most complex (at the finest mesh level) to the simplest (at the coarsest level). The user may use any of these in system simulations.

The cell agglomeration procedure starts with the first cell on the list, and the selection of the group size, typically either two or four. A neighbor cell that is of the same type of material (die, mold, lead) is picked, and the process is continued until the group size is met, or there are no more un-agglomerated neighbors available for the current cell. The procedure then moves to the next un-agglomerated cell on the cell list. One sweep of the domain in this manner yields the first coarse mesh level. The cell faces of the coarse mesh are composites of the cell faces of the fine mesh. The coarse mesh produced in this manner is in general unstructured regardless of whether the underlying fine mesh is structured or not. The procedure is repeated recursively to form successively coarser levels of mesh. The neighbor coefficients for the coarse level are formed by summing the neighbor coefficients of the constituent cells from the immediate fine level, in keeping with the practice used for algebraic multi-grid schemes (Hutchinson and Raithby.[14]

One additional feature of this procedure is that there is no "unique" network for any physical package or package type. It will depend on the initial fine-grid description of the package and the levels of coarsening selected. As long as the fine-grid description captures the physical elements of the package in question, all levels of resulting RC network descriptions will inherit the properties of the package. It is shown through examples in the following sections that very coarse RC network descriptions produce reasonably accurate predictions of the junction temperatures and heat flow out of the surfaces of the packages.

FBGA Package

The FBGA package analyzed using the above methodology is shown schematically in Figure 2. The package has a body size of 15mm × 15mm × 1.62mm. The package has a 4-layer substrate on which a semiconductor die is attached to the center region using a thin layer (0.03 mm) of die attach epoxy. A plastic mold cap encapsulates the semiconductor die. The mold has a thickness of 0.7mm and a thermal conductivity of 0.7 W/m·K. The die is silicon and has a dimension of 5mm × 5mm × 0.33mm. The die dissipates 2 W of power on its top surface. A matrix of 14 × 14 (196) solder balls is attached to the bottom surface of the substrate. Dimensions and thermal properties for the components of the package are given in Table 1.

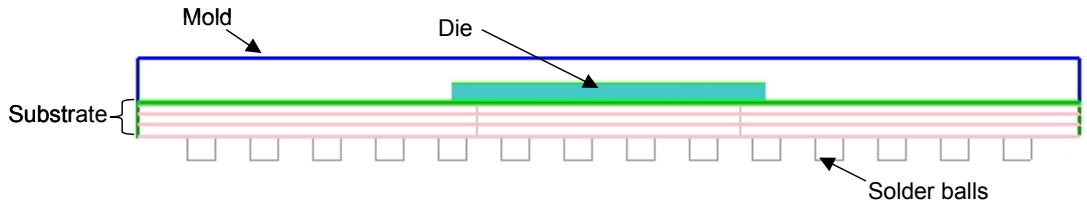

Figure 2 – Schematic of Detailed Model of FBGA Package

Table.1 – Layer Details for FBGA

Layer	*Thickness (mm)*	*Density (kg/m^3)*	*Specific Heat (J/kg-K)*	*Thermal Conductivity (W/m. K)*
Die	0.33	2330	660	140
Die attach	0.03	500	2000	2
Substrate	0.5	1250	1300	Anisotropic
Mold	0.7	865	2000	0.7
Vias	0.5	8933	385	Anisotropic: k_x, k_z =0.02, ky = 8.8
Solder	0.4	8500	196.6	50

Numerical Simulations

A detailed transient CFD simulation of the FBGA package under natural convective cooling was performed to evaluate the compact model. For this purpose, the FBGA package is mounted on a four-layer JEDEC thermal test board of thickness 1.6mm. The board and IC package assembly are placed in a JEDEC still-air thermal characterization chamber. The ambient air temperature surrounding the chamber is at 70 ^{o}C.

An RC network was then extracted for the packages using the present methodology. The network consists of multiple internal nodes: a node each for every component in the package. Components with very small volumes in comparison to neighboring components are merged to form single nodes. For example, the ball grid array region forms a single node denoting the entire region. Mold regions are typically split into multiple nodes because of their relative size. Our experience with earlier networks showed that splitting the mold into two or more nodes resulted in more accurate predictions for the package case-center temperatures. This is to be expected because splitting the mold into multiple nodes implies the heat flow spreading pathways from the die region to the top surface of the package are modeled; hence improving the accuracy of the networks. This network was then used in CFD simulations under the same conditions employed for the detailed simulation. A comparison of results is presented in the following section.

Results

Transient CFD simulations were performed for the detailed and network models of the FBGA package. The simulations were carried out to an end time of 50 seconds using a uniform time-step of 0.05 s. In the detailed simulation a uniform power of 2 W was specified to the top surface of the die at time, t=0 s. The power was specified to the junction node in the network model simulation. At the end of each time step the temperatures are extracted at three points: the die source, the center of the top surface of the package (case-center) and the center of the printed circuit board. These three temperatures are compared for the detailed and network simulations.

Figure 3, 4 and 5 show a comparison of the three temperatures for the detailed and network simulations. Qualitatively the curves follow similar trends in all three cases. The network simulation temperatures for the junction and the case center are slightly higher compared to the corresponding detailed simulation temperatures. The network simulation temperatures for the PCB are slightly lower compared to the corresponding detailed PCB temperatures. Figure 6 plots the % error for the three temperatures as a function of time. The plot shows that the errors for the junction temperatures were initially high, with a maximum error of approximately 25% at 0.4 seconds, but decreased rapidly with time at an exponential rate. Though the values of the errors are initially high, the actual difference in junction temperatures was less than 2 ^{o}C. The error for the steady-state temperature was less than 5%. For the case center the errors were similarly higher at initial times with a maximum error of about –33% at 0.1 seconds. The errors for the temperatures of the case center were in general lower compared to the junction temperature errors. The errors for the temperatures of the PCB center followed a similar pattern with higher values at initial times. The maximum error in the PCB center temperatures was approximately -14%. Again, the errors decreased rapidly with increasing time. The error in the steady-state temperature of the PCB center was approximately –2%.

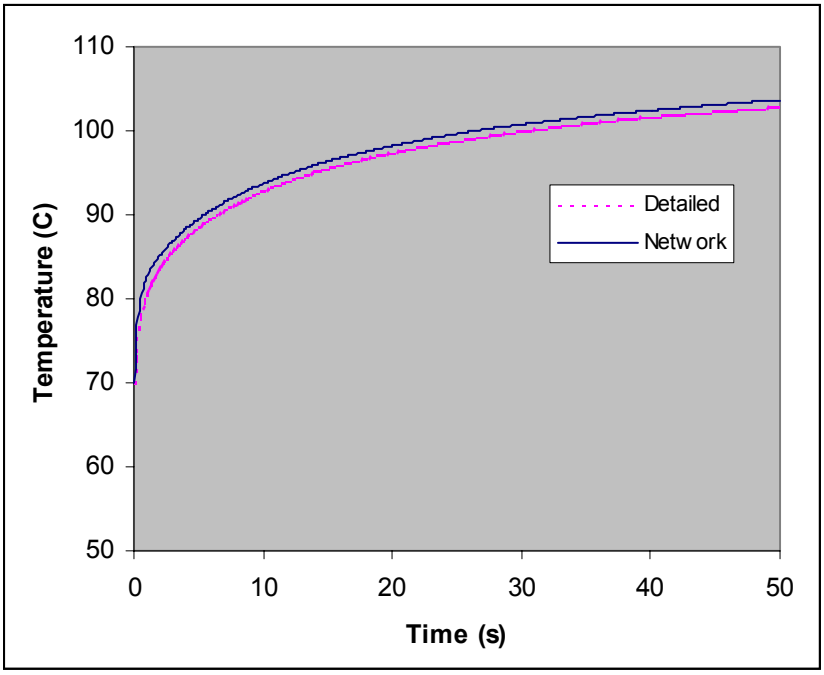

Figure .3 – Comparison of Junction Temperatures

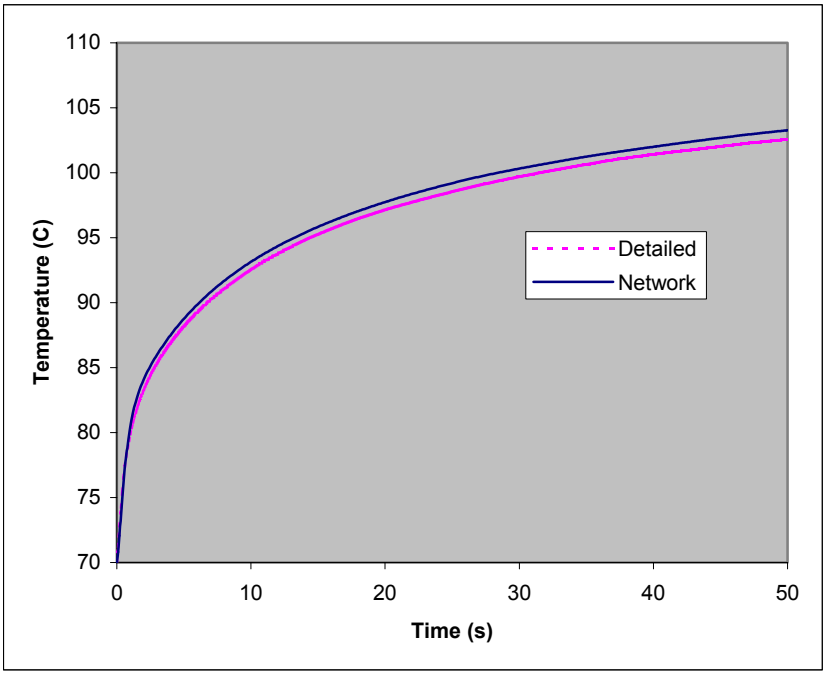

Figure 4 – Comparison of Case Center Temperatures

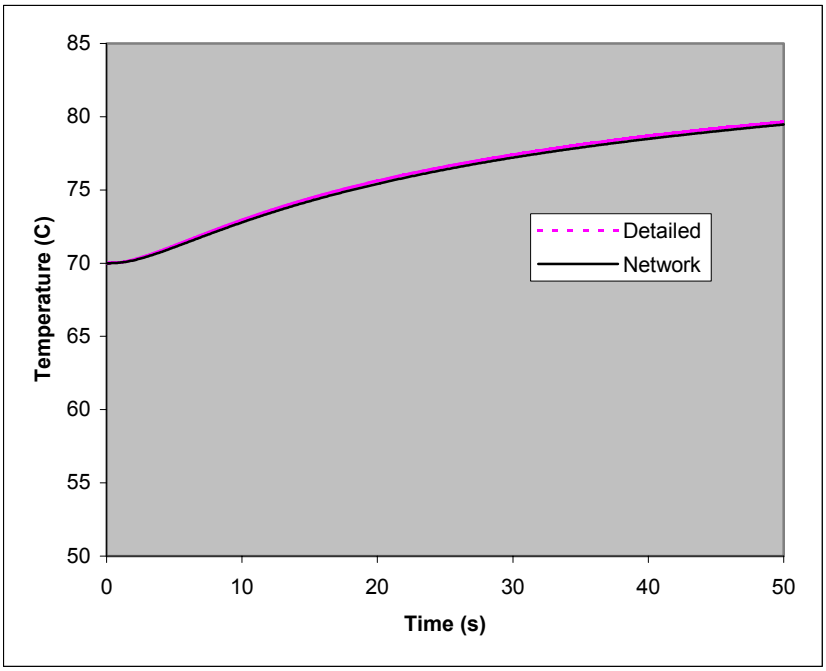

Figure 5 – Comparison of PCB Center Temperatures

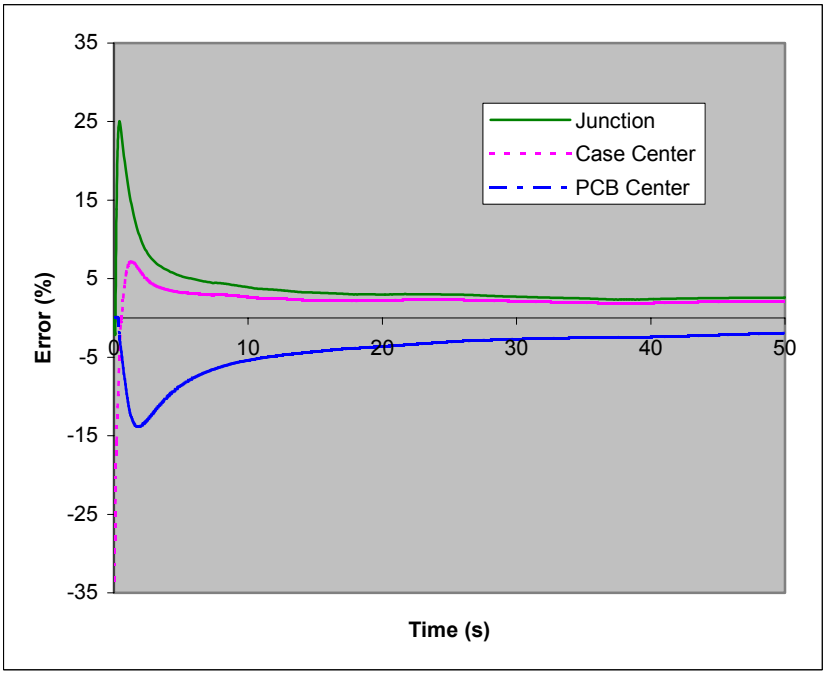

Figure 6 – Error (%) vs. Time for the Junction, Case Center and PCB Center

This level of error in comparison to the detailed simulation of the package is well within the acceptable range in the published forms of compact thermal models. Mesh count reduction of about 50% was observed for the compact network simulation. This implied computational savings of up to 5 times over the detailed simulations.

Summary

This paper describes the use of the ACE procedure to extract network topologies and RC characteristics of the network for generating compact models for any IC package type. The extraction is automatic and the method is applicable to any package type. The applicability of the method to an FBGA package is demonstrated.

The method is shown to be accurate to below 5% for steady state simulations. The errors in the transient simulations, though initially high, decreased rapidly at an exponential rate with time. The computational savings are shown to be up to 5 times over the corresponding detailed simulation of the packages. The method is extendable to other components (power converters, hard disk, batter packs) in electronics systems whose detailed implementation in the system level simulation renders the computation problem intractable.

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Motivation

- Detailed “Devices” on “PCBs” in “Systems” in “Data-Centers” is (as of today) an unsolvable problem !
- Reduced order or Compact models are the practical way to make this problem tractable
- More effective the compact model is…more useful is the computational methods in real design…
- Compact models have been in effect since Day 1 of CFD in design

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Compact Models…

- **Models for application in computational tools**
  - Lumped models
    - Blocks or something like them
    - More elaborate approaches (Blocks, plates, etc.)
  - Network Models (Computational efficiency higher)
    - Fix network topology, determine coefficients/resistances
      - Two resistor models
      - Delphi approach
    - Determine network topology & coefficients/resistances
      - COBRA approach
      - ACE…(Automatic Compact model Extraction)

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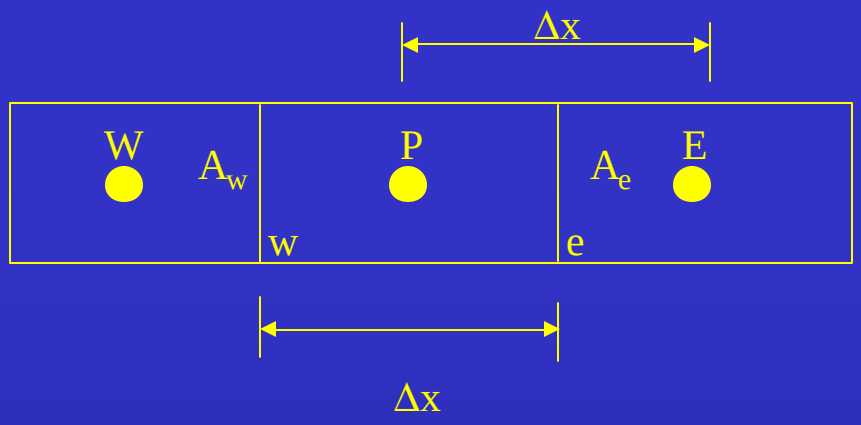
Basic Principles



$$q_e A_e - q_w A_w = q''' V$$

$$q_e A_e = -k_e A_e \left(\frac{dT}{dx}\right)_e = -\frac{k_e A_e}{\Delta x}(T_E - T_P) = a_E (T_P - T_E)$$

$$q_w A_w = -k_w A_w \left(\frac{dT}{dx}\right)_w = -\frac{k_w A_w}{\Delta x}(T_P - T_W) = a_W (T_W - T_P)$$

$$a_E (T_P - T_E) + a_W (T_W - T_P) = q''' V$$

The coefficients a_E and a_W are essentially conductances

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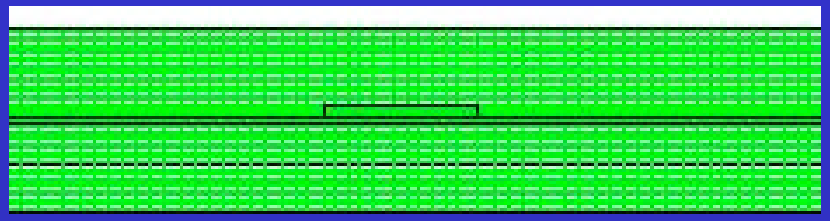
Multigrid Details

Level 1



User defined mesh

Level 2

Agglomerated mesh

and so on …

Agglomerated mesh

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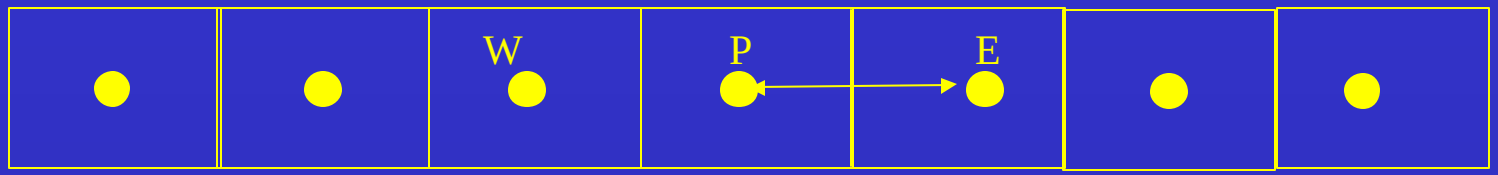
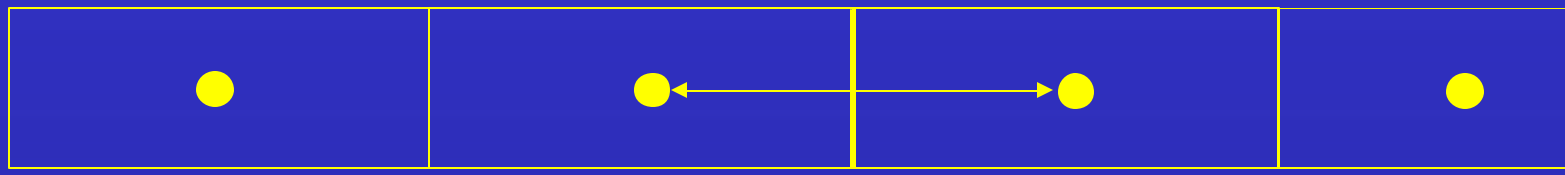
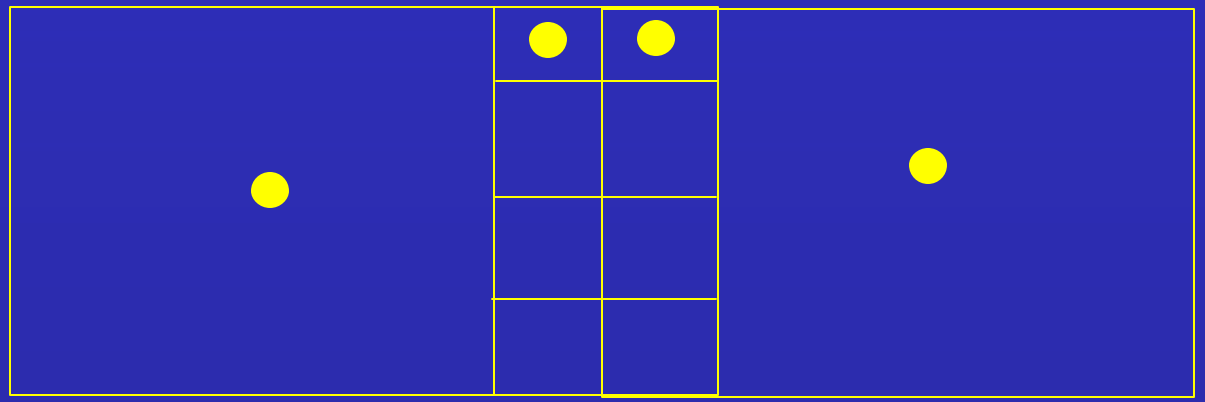
AMG Basic Principles—correction equation

$$a_P T_P = \sum_{nb} a_{nb} T_{nb} + b$$







Current implementation: Scale coefficients by 2/level

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Multigrid Details…

- **Neighboring cells with similar coefficients are agglomerated to form a single cell (can have many faces)**
  - Cell agglomeration is based on material properties and geometric parameters of neighboring cells
    - In the limit, all cells with the same conductivity would form a single cell
- **The final "agglomerated" or coarse-grid**
  - Connectivity is the topology the network
  - Coefficients are a measure of the final network conductances.

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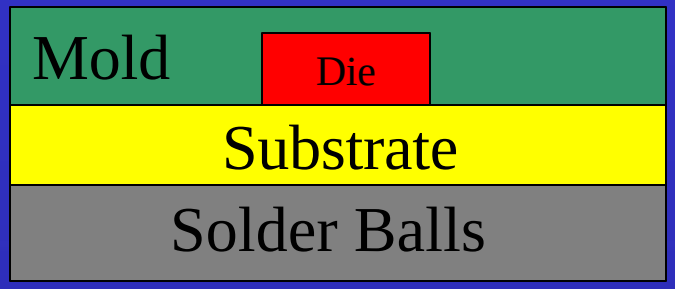
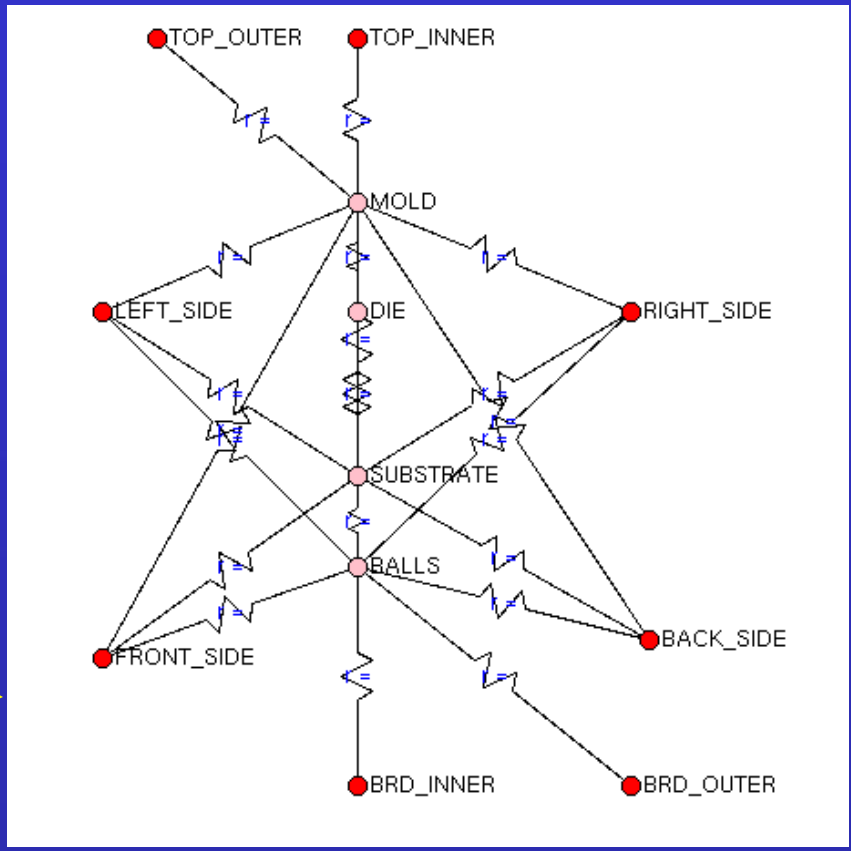
Simple example…





“Completely” agglomerated mesh

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Properties of ACE

- **Approach combines the "physical-ness" of the detailed model with the advantages of a network model (few nodes)**
  - Automatically accounts for heat flow paths
- **Network topologies can be**
  - Arbitrarily complex or simple
    - dictated by the specific package or component detailed model
  - Multiple internal nodes are permitted
    - MCM's and stacked die
  - Boundary condition independent
  - Steady or transient analysis

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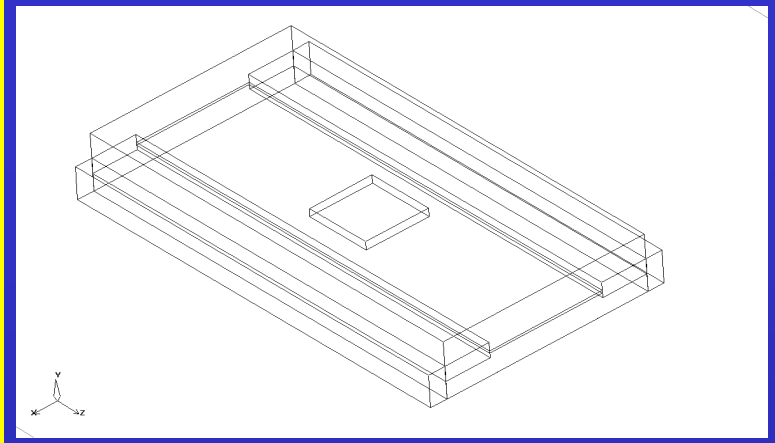
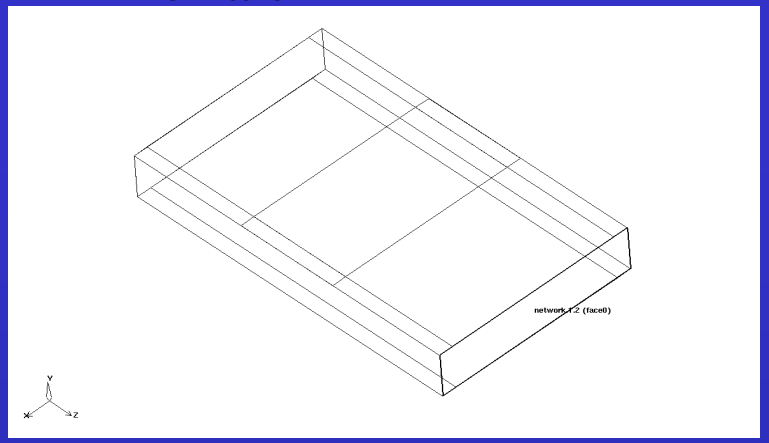
24 Lead TSOP Package Validation

Physical Model



ACE Network



- **TSOP Details**
  - Package: 15.96 mm X 8 mm
  - Die: 2.5 mm X 2.5 mm and dissipates 1 W
- **Validation in Simulated JEDEC wind tunnel with 4 layer board**
  - Inlet velocity of 0.5, 1, 2 and 4 m/s

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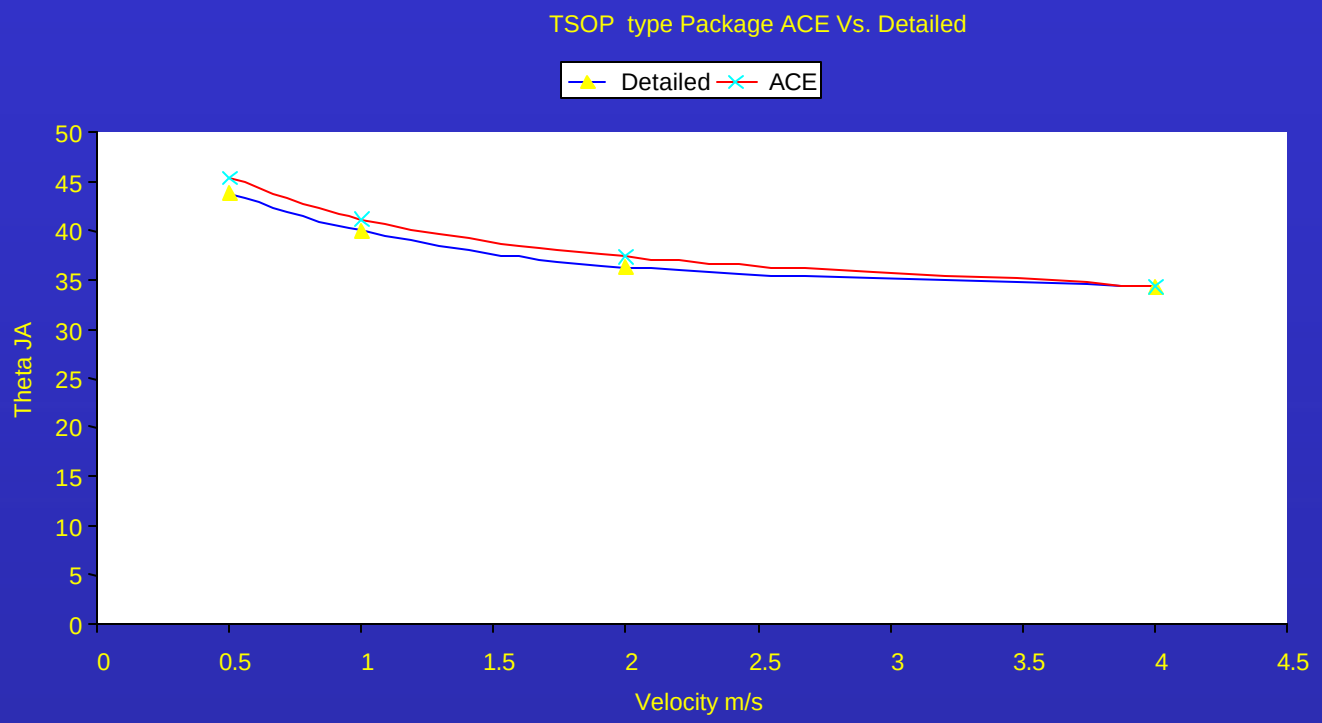
24 Lead TSOP Package Validation



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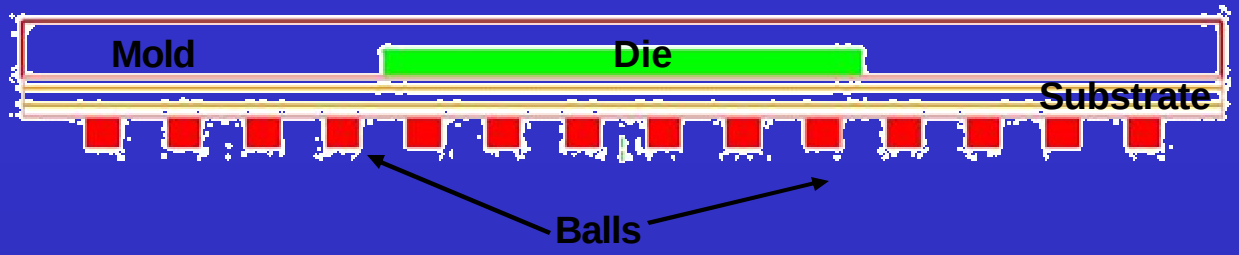
196 Full Ball Grid Array (FBGA)



Layer	Thickness (mm)	K (W/mK)
Die (2W)	0.33	140
Substrate	0.52	Anisotropic
Mold	0.7	0.7
Vias	0.52	Anisotropic
Mask	0.027	0.2125
Solder Balls	0.4	50

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196 Full Ball Grid Array (FBGA)

Boundary Condition	Multi-grid Level	% Error T_j	% Error T_c	% Error q_{jb}
Natural Convection	10 (25 nodes)	1.0	4.1	3.4
	11 (14 nodes)	2.3	4.2	3.4
	12 (12 nodes)	6.9	4.6	3.2

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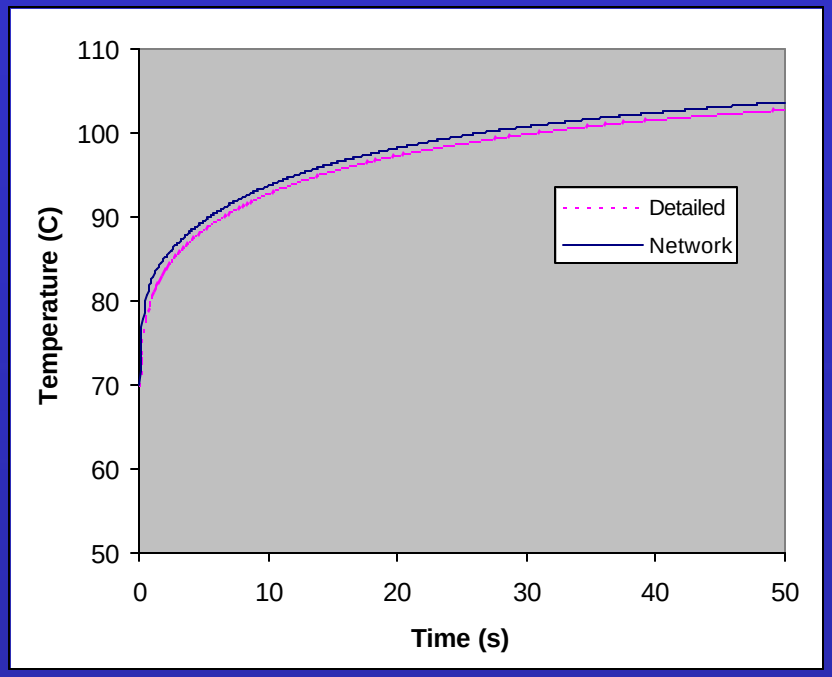
196 Full Ball Grid Array (FBGA)

Boundary Condition		Multi-grid Level	% Error T_j	% Error T_c	% Error q_{jb}
Forced Convection	100 LFM	10 (25 nodes)	0.6	4.9	2.7
		11 (14 nodes)	0.5	4.7	2.7
		12 (12 nodes)	6.2	5.4	2.7
	200 LFM	10 (25 nodes)	1.2	4.9	3.4
		11 (14 nodes)	1.5	5.0	3.4
		12 (12 nodes)	8.9	5.1	3.5
	400 LFM	10 (25 nodes)	0.9	4.5	3.5
		11 (14 nodes)	1.5	4.7	3.5
		12 (12 nodes)	8.3	5.5	3.5
	600 LFM	10 (25 nodes)	1.5	6.7	4.1
		11 (14 nodes)	2.3	7.2	4.1
		12 (12 nodes)	9.1	7.4	4.2

196 Full Ball Grid Array (FBGA) : Transient
Junction Temperature



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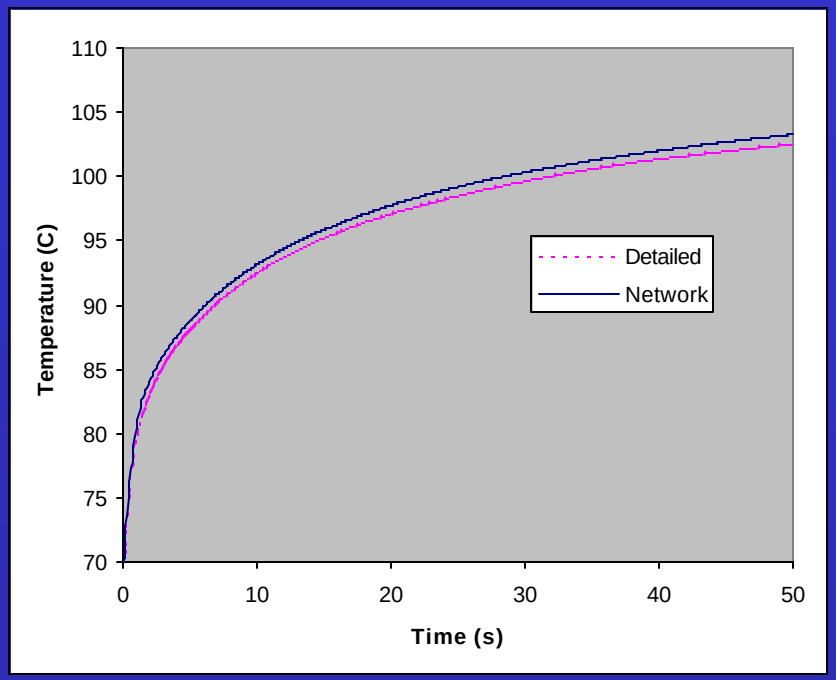
196 Full Ball Grid Array (FBGA) : Transient Case Temperature



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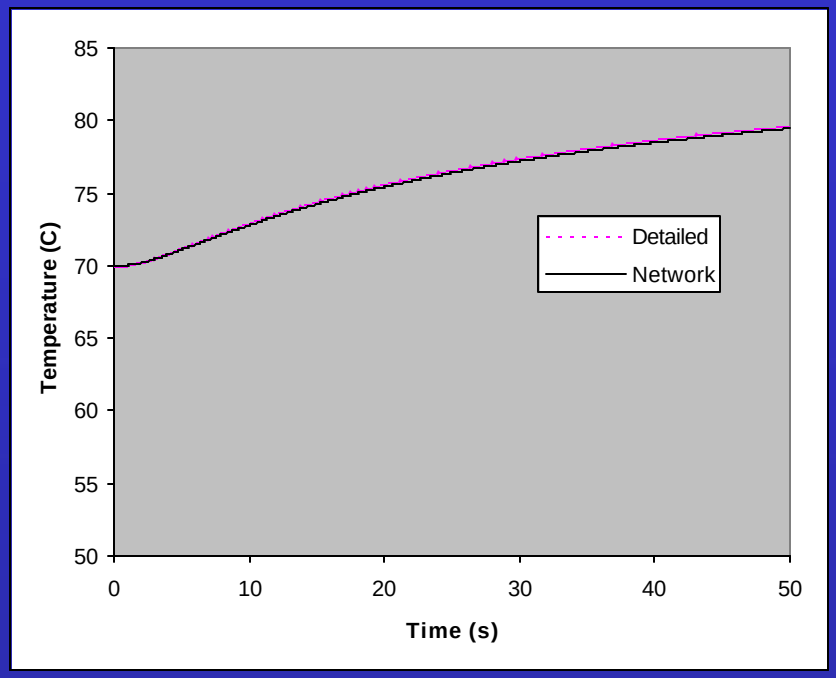
196 Full Ball Grid Array (FBGA): Transient PCB Temperature



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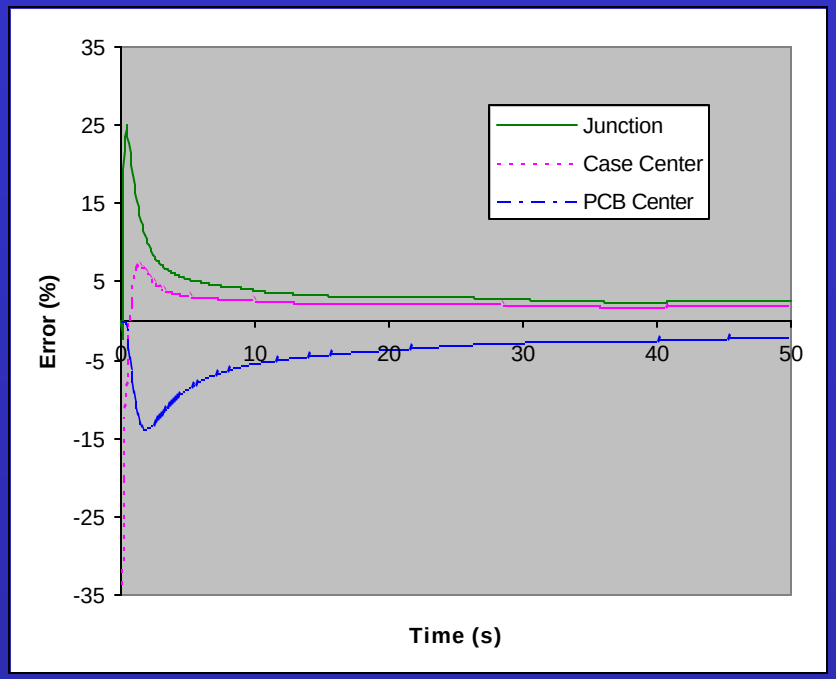
196 Full Ball Grid Array (FBGA) : Transient Errors



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Concluding Remarks

- **The ACE approach automatically**
  - Extracting the network topologies
  - Estimating the resistances
  - Applicability to a large range of IC device types and operating conditions
    - Steady or transient
    - Multiple internal nodes allow modeling of MCMs, Stacked Die, and
    - In principle, to other component types such as hard disk drives, etc.
- **Scope for further research exists along the same line…**
  - Coefficient scaling based on the “geometry” of the “coarse mesh”

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