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SMEMA Council APEX®
Designers Summit 04

Advanced Microvia Design

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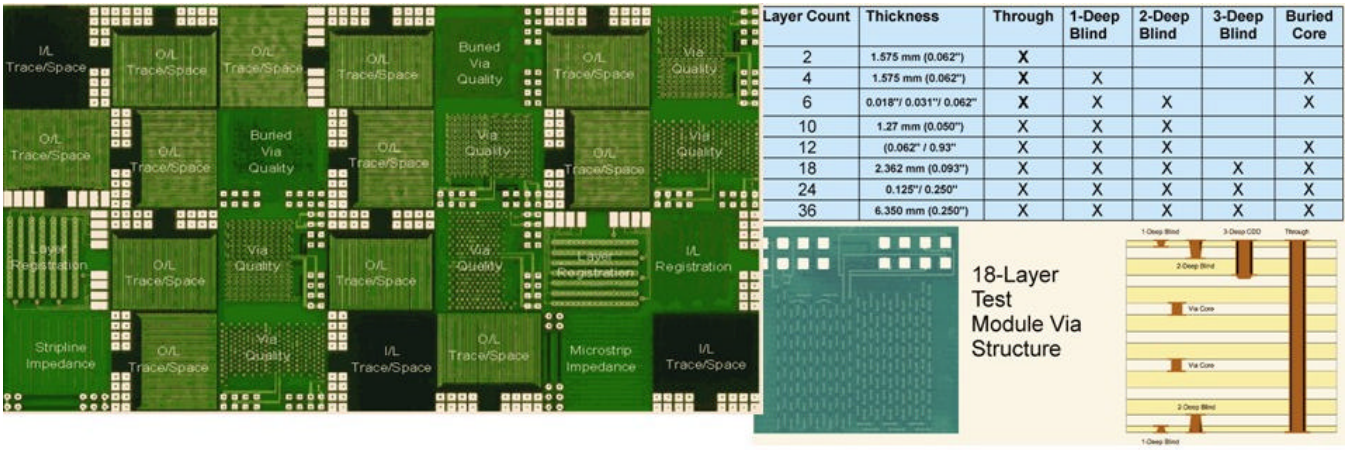
Abstract
Microvias are the fastest growing new technology for printed circuits. Once you understand the basics, the advanced topics bring the real advantage to light. This talk will highlight the procedures and conditions that designers needs to consider making microvias the most productive and profitable architecture for their designs. These ideas go beyond the IPC standards, but are essential for any designer using microvias. The talk will cover: Vendor Qualification, Component / Assembly issues, Planning the Design, Signal Integrity concerns and Channel Routing procedures.

Vendor Qualification
Selecting an HDI fabricator can be very challenging. One-way to discover the HDI capabilities of PCB fabricators is the new IPC-9151 Capabilities Benchmarking Panel. This standardized multilayer panel can be seen in Figure 1a. It is provided in 2, 4, 6, 10, 12, 18, 24 and 36 layer structures with high and low density design rules, 5 thicknesses—for PCB and backplanes and in a large panel size of 18" x 24". The IPC Committee is planning other new Benchmarking Panels for substrates.

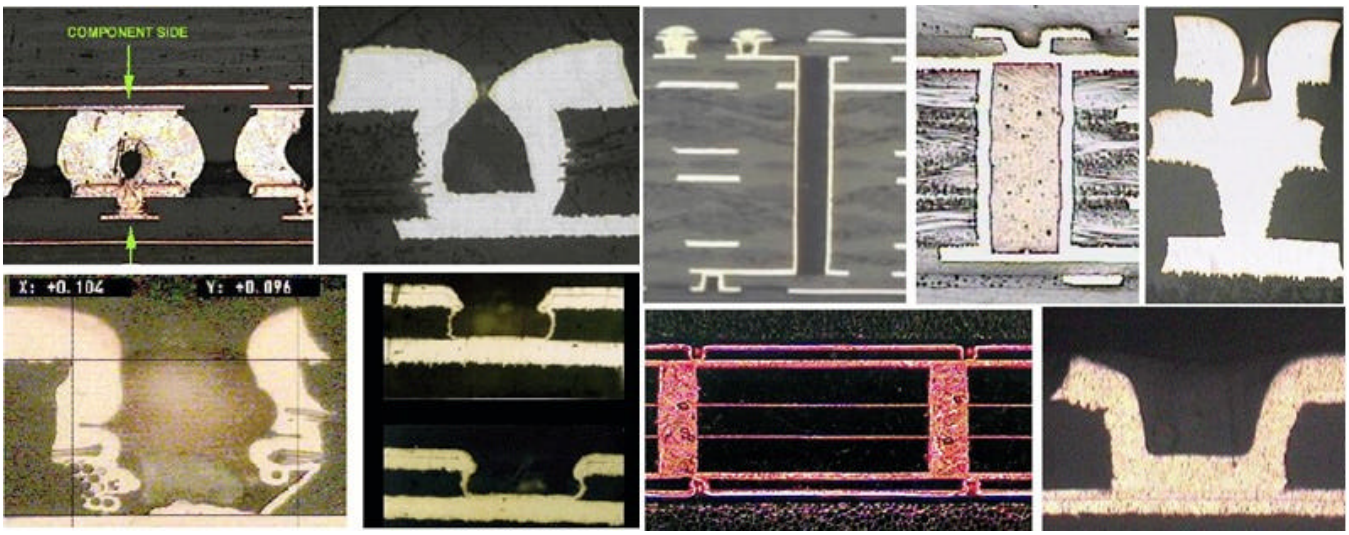
The via structure of the various designs is shown in Figure 1b. The blind vias are optional, but provide significant data on the fabricators capabilities.[1]



(a) (b)

Figure 1(a) - New IPC-9151 Capability Benchmark (PCQR[2]) is an Ideal Way to Evaluate what Fabricators are Capable of Manufacturing HDI Boards with High Yields[2] – (b) IPC-9151 has 8 Different Layer Counts and Several Design-Rule Variations to Select as Standard Capability

Microvia Quality
Microvias are nearly impossible to inspect visually and extremely difficult to cross-section. This necessitates a more indirect approach to verification of proper fabrication. Proper microvias, as seen in Figure 2b, can be distinguished from defective microvias, as seen in Figure 2a by using the Copyrighted CAT[3] coupons on production panel borders. These coupons are the same as used in IPC-9151 and correlate to a statistically measured via-chain resistance and accelerated thermal-cycling tests (HATS).[3] The criteria for quality microvia production is no more than 50 defective microvias per million microvias and a covariance of the standard deviations of the daisy chain Kelvin resistances of 5%.



(a) (b)

Figure 2 – (a) These Four Cross-Sections are all Defective and Rejected Microvias (b) These Five Microvias are Properly Drilled, Metallized and Plated[4]

Via-In-Pad (VIP)

In a few cases, assemblers may have difficulty with the microvia-in-pad design approach. Technical papers published by OEMs that have used microvias and VIP technology indicate that a finer-mesh solder-paste should be employed and that OSP, HASL and Immersion Silver are the preferred final-finishes for the bare board. One alternative solution is to specify a "flat microvia pad". There are four alternatives to accomplish this, where as, only three are fabricator controlled and add extra costs. The four 'flat pads' filling processes are seen in Figure 3a. A surface plane flood (GND) is designed with panel and pattern plating metalization. b**.** Microvia non-conductive fill and plating cap. c. The effect of specialized copper plating baths with normal DC plating**.** d**.** The effect of pulse plating with periodic reversal but using normal copper plating baths.

The advantage of 'flat and filled' microvias is ease of assembly and more copper to carry current and heat.

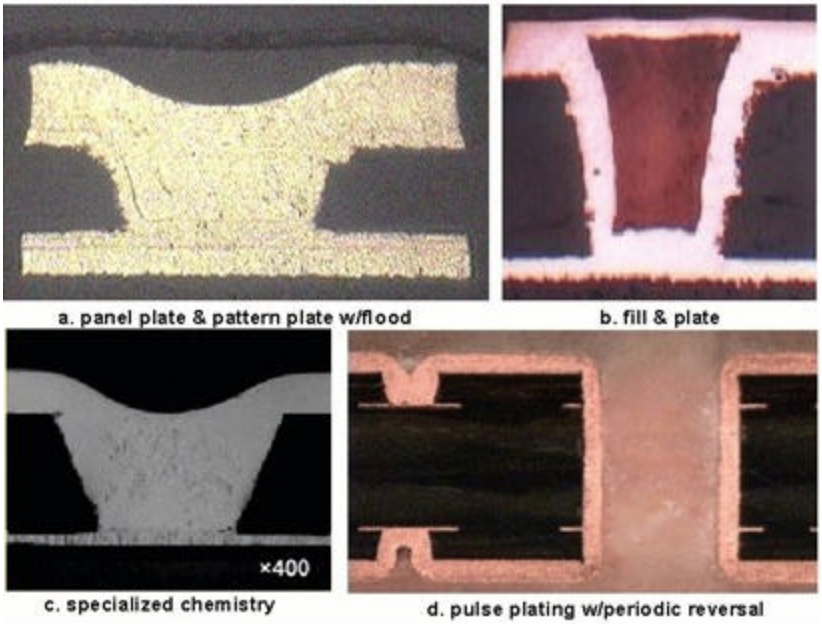


Figure 3 - Four Via Filling Processes for 'Flat Pads'.(a) Surface Plane Flood with Panel and Pattern Plating (b) Microvia Non-Conductive Fill and Plating Cap (c) the Effect of Specialized Copper Plating Baths with Normal DC Plating (d) The Effect of Pulse Plating with Periodic Reversal but using Normal Copper Plating Baths

Planning the Design
Wiring Predictions

The selection of signal layer stackup and design rules determine the *maximum wiring capability* (Wc) for a design. The schematic and total component parts list, along with their connections, can be used to estimate the total wiring lengths required to connect this design. This is the *wiring demand* (Wd). The *actual wiring capacity* is the *maximum wiring capacity* multiplied by the designs *Layout Efficiency* (LE). The actual wiring capacity must always be larger than the wiring demand, Wd<= LE * Wc.[5] Details on these calculation are in the IPC-2315 and IPC-2226.

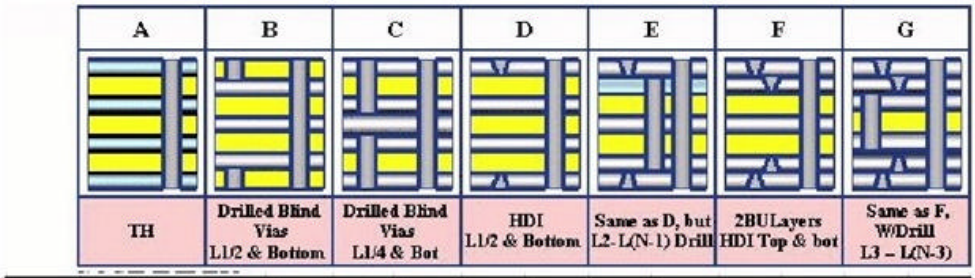
HDI Tradeoffs to Through-holes

Figure 4 is a summary of the HDI equivalents to through-hole multilayers. The RCI's in the matrix are our 'Floor' numbers (or minimums). But the 'Ceiling' number for a range is out of our ability to calculate or set up at this time. The 'Max.' could be as high as the 'Sky'. It all depends on the various factors in the design. Yields are very sensitive to min. diameter, annular rings, min. trace and spacing, material thicknesses, total number of holes and their density. Other cost factors such as final finish, hole filling, and tolerances will affect the price.

There is a column for "Density" (DEN). This is the maximum number of electrical connections (called 'pins') per square inch of surface (for both sides). The solid lines are "Equivalent" PCBs. So, as an example, an 18-Layer TH (through-hole) board with an average of 100 'pins' per sq. in could have been designed as a 10-layer HDI board (1+8+1) because it can handle 200 'pins' per sq. in (p/si). Or, it could have been designed as a 6-layer HDI board with 2+2+2 (also 200 p/si).

The RCI does not show the "Relative" cost savings in this example. The "Absolute" cost saving is 52.2% for the 10-layer and 47.1% for the 6-layer HDI 'equivalents'. But a smaller board could result in more boards up per panel and the 'PRICE" would be even lower than the above numbers. In the range of 8L to 18L, the HDI boards, especially the 2+N+2 are *NOT* the equivalent of 8L to 18L TH boards, they represent boards with *12X- 20X* the density of TH boards. Even the 1+N+1 HDI boards represent TH boards with 14L to 30L layers!

This Matrix is based on FR-4. This has two important implications. The TH RCI scale (4L – 10L) represents competitive pricing set by China. This scale is depressed compared to the HDI pricing. So the HDI pricing, if equal or lower, *is very competitive*. If the material of construction is *NOT FR-4*, but a more expensive, low Dk or low Dj material, then the savings from HDI will be *MUCH LARGER* as you reduce layers!



	A THRU-HOLE		B SEQ-LAM/Dr BV		C SEQ-LAM/Dr BV		D HDI BLIND		E HDI BL/BU		F 2BU BLIND		G 2BU BL.BU	
	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN
4L	0.44	20					1.20	40	1.45	80	1.65	120		
6L	0.63	20	2.10	60	3.40	80	1.40	60	1.85	160	2.21	200	3.84	260
8L	1.00	30	2.70	80	4.35	100	1.45	120	2.00	180	2.54	240	4.23	300
10L	1.20	40	3.50	120	5.75	140	2.00	200	3.00	210	3.00	260	4.81	400
12L	1.54	60	4.10	140	6.70	160	2.90	210	4.00	230			7.62	600
14L	2.66	70	4.78	160	7.49	180	3.27	220	5.01	250			9.60	800
16L	3.42	80	5.80	200	9.45	220	4.64	260	6.27	300			11.40	1000
18L	4.18	100					5.13	300	8.15	400				
20L	4.80	105							9.99	500				
22L	5.74	110												
24L	6.42	125												
26L	7.11	130												
28L	10.19	135												
30L	12.48	140												

Figure 4 - Layer Count is not a Good Way to Compare Through-Hole (TH) Multilayers to HDI - HDI has a Much Higher Density for the Same Layers - To use this Table, the Diagonal Lines show the HDI Equivalents

Signal Integrity

Signal integrity improvements are certainly available to all who take the time to respect Mother Nature. HDI's contribution comes mainly from the adage, "Smaller and Closer is Better!" That is, HDI's main contribution is ***miniaturization***! The signal integrity improvements for HDI come from three phenomena:

1. Noise reduction
2. EMI radiation reduction
3. Improved signal propagation and lower attenuation

Noise

Four categories of noise describe the various effects (see **Figure 5**).[6]

1. **Signal quality** of one net and its return path (ringing due to reflections)
2. **Cross talk** between two or more nets (noise pulses due to switching on neighboring lines)
3. **Switching noise** (noise on power and ground lines/planes)
4. **EMI**

Noise can come from many sources in the board layout, such as:

- Changes in trace width
- Plane splits
- Cutouts in Power/Ground planes
- Via antipads
- Insufficient plane capabilities
- Excessive stubs, branched or bifurcated traces
- Component lead frames
- Improper impedance matching and termination networks
- Coupling between signals
- Varying loads and logic families

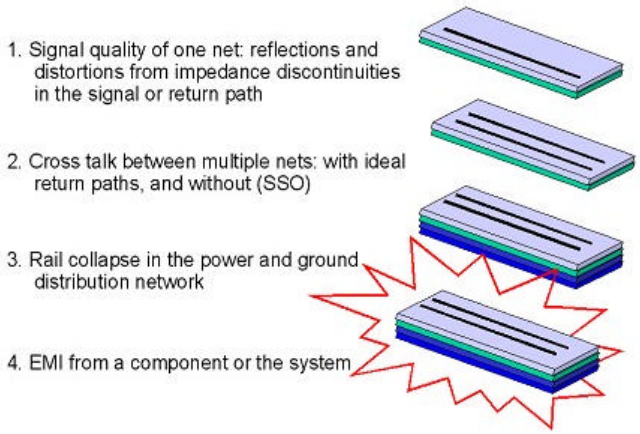


Figure 5 - Four Families of SI Problems

Surface Ground Planes

A paper by Dr. Eric Bogatin provides the partial self inductance of a microvia 2 mils deep and 1 mil in diameter as less than 10 pH, while a drilled via, 10 mils in diameter and 32 mils deep has a partial self inductance of almost 200 pH.[6] This is significant for higher frequency designs. Dr. Bogatin goes on to point out that at 300 MHz, the impedance of an HDI microvia is only 18 milliohms compared to the through-hole via which is 400 milliohms.

The via-in-pad reduction of inductance is even more dramatic. One of the largest sources of inductance to devices and decoupling capacitors is the trace-via combination to power and ground. By placing the microvia in the SMT pad, this inductance is decreased to practically nothing. This is compared to a conventional trace to a through-hole that at 20 mils would add as much as 500pH to the loop inductance.

Using a via-in-pad microvia and a surface ground plane, there is essentially no inductance to ground, and if power is used as the second layer under the microvia, only a minimum inductance to power. The close nature of this power/ground combination will lower loop inductance and provide a significant amount of decoupling capacitance. A final advantage is the reduction of part spacing and a shortening of all the signal tracks. Figure 6a and Figure 6b show high-speed controlled

impedance multilayer redesigned with only the use of microvias-in-pads.[6] No parts were changed and current assembly minimum spacing was observed. The advantages from a cost and size point-of-view is nearly 40 percent lower cost, from 18 layers to 10 layers, and 40 percent smaller in size, allowing more up on a fabrication panel. The signal integrity was improved significantly.

For signal returns, the ideal return path is continuous and uniform. This is usually not the case in high-speed dense circuit boards. The more the return path is non-ideal (with discontinuities), the more it produces ground loops. The characteristic of continuous and uniform is illustrated in Figure 6b. In Figure 6a, the ground planes of a high-speed dense multilayer are shown. For this 9.2-inch by 6.3-inch 18-layer board, 8.46 square inches of copper is etched away to make room for the through-holes. Figure 6b is the 10-layer HDI multilayer that replaced the original 18-layer multilayer. The surface ground plane (primary side, Figure 6b) has only 6.63 square inches removed and the secondary side has only 6.35 square inches removed. This is 21.6 percent and 24.9 percent respectively less discontinuities for the return path. In addition, you can see that at the fine-pitch BGA devices, the ground copper goes substantially all the way into the center ground pins.

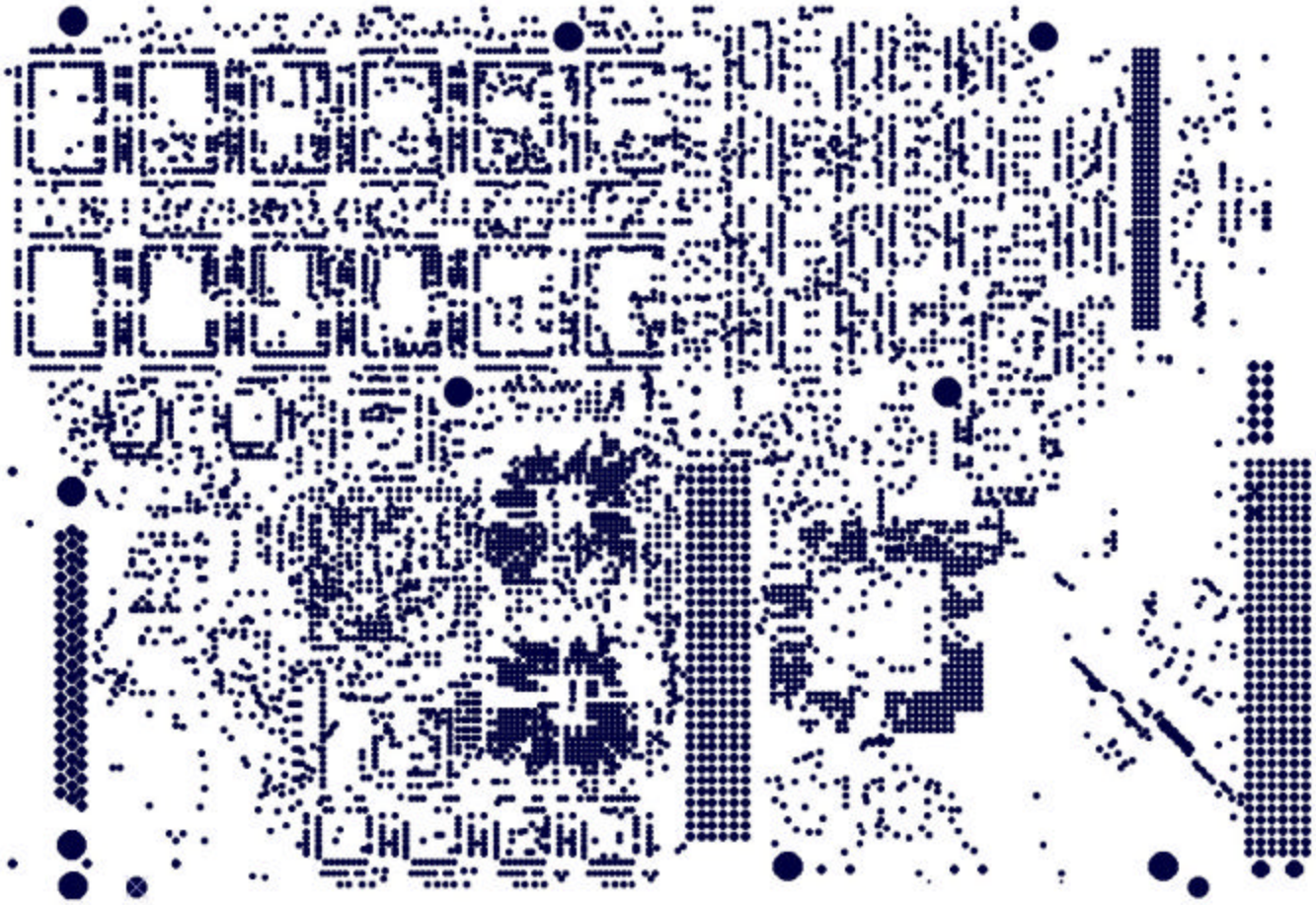


Figure 6a - Innerlayer Plane Ground Plane Relief

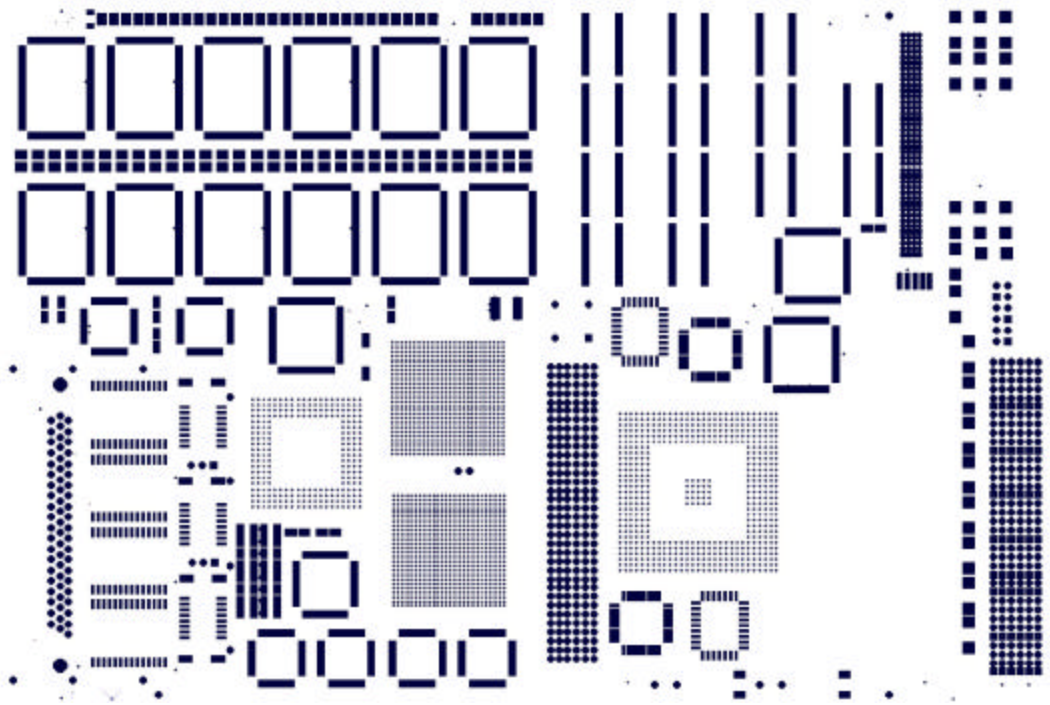


Figure 6b - Primary Side Ground Plane Relief (with the ground removed for clarity)

Channel Routing[7]

High I/O Components

One very useful HDI design technique is to use the blind vias to open up more routing space on the inner layer. This is shown in Figure 7a. By using blind vias, the routing space effectively double on the innerlayers and many more traces can be used to connect pins on the inner rows of a BGA. Nortel Networks patented channel routing in 2002.[7] With this technique, 1/2 to 1/3 the number of signal layers is required to connect a complex, high-I/O BGA.

As an example, Figure 7b shows a 1089 pin, 1.0mm pitch BGA. On the left side of the device is the original design (Layer 1) using a 20-layer TH board, on the right, Layer 1 for the 14 layer HDI version. The TH version used pad-via dogbones, so the surface GND flood ends at the border of the device. The HDI version shows channel routing , with GND connections on the surface., blind microvias for PWR-VCC to layer 2 and blind microvias to layer 3 for signals. All of these create the channels. Figure 7c shows layers 2 (PWR), layer 3 (Signal 1), layer 4 (Signal 2) and layer 5 (GND). The channels are evident on layers 3, 4 and 5. These open channels are now available on all layers including the BACK SIDE (Figure 7d).

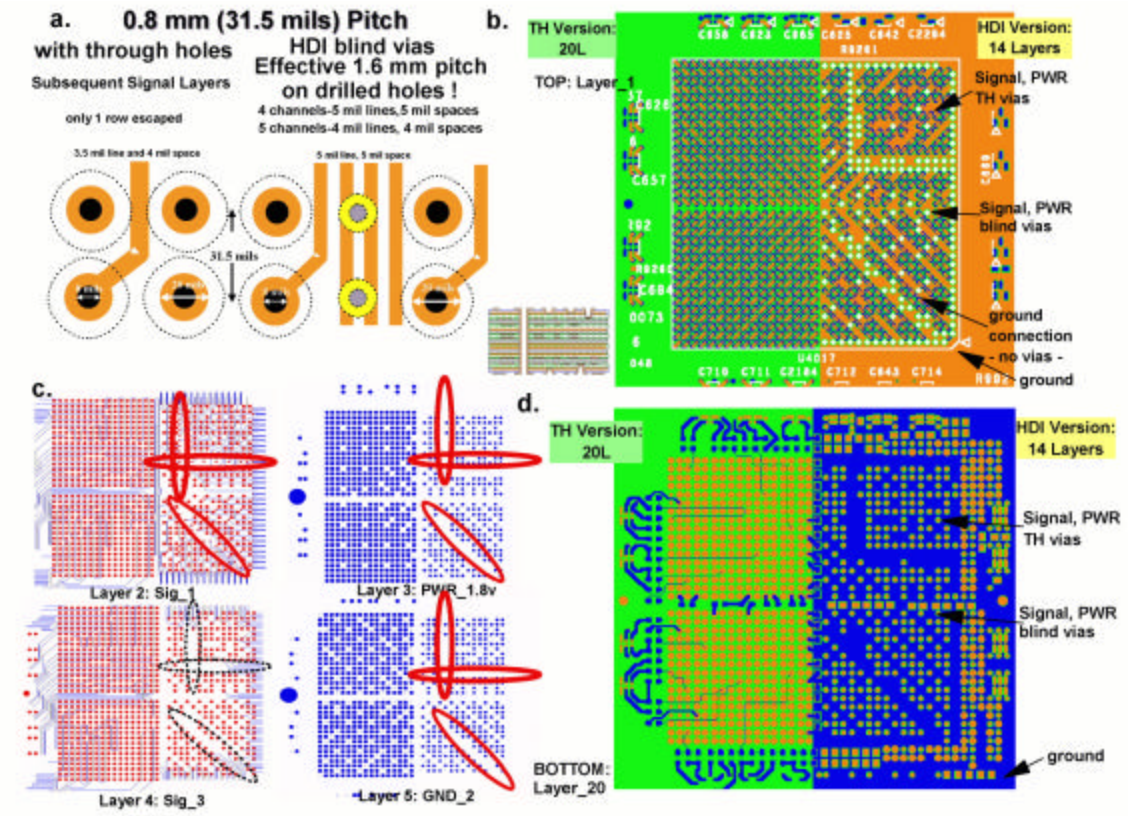


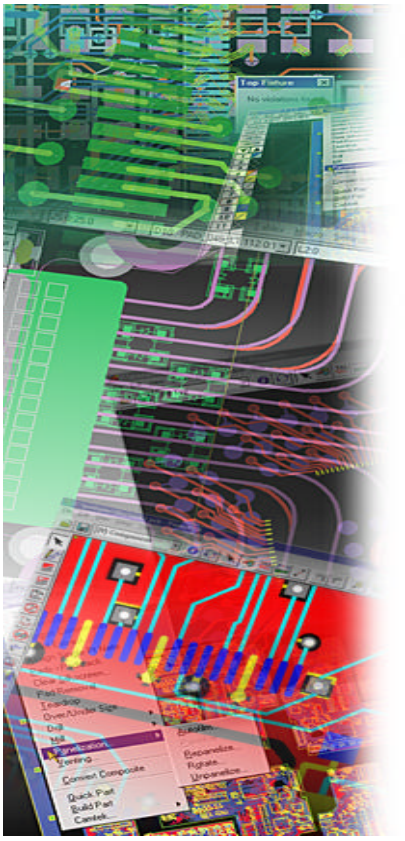
Figure 7 – (a) Channel Routing Utilizes Blind Vias to Create an Inner-Layer Channel To Route Out Interior Pins on Devices[8] For this 1089 pin, 1.0mm BGA, the Original 20-Layer TH boaRd, on the Left, Layer 1 for the (b)14-Layer HDI Version on the Right - The TH Version used Pad-Via Dogbones - The HDI Version Shows Channel Routing, with GND Connections on the Surface., Blind Microvias for PWR-VCC to Layer 2 and Blind Microvias to Layer 3 for Signals (c) Shows Layers 2 (PWR), Layer 3 (Signal 1), Layer 4 (Signal 2) and Layer 5 (GND) (d) The Back Side, Layer 20 on the Left and Layer 14 on the Right.

Conclusion

Although microvias have been around 20 years, in high performance products, it is the current fine-pitch and high I/O BGAs that now require their services. The design of HDI-Microvia boards are not that complex, but many new techniques are being developed.

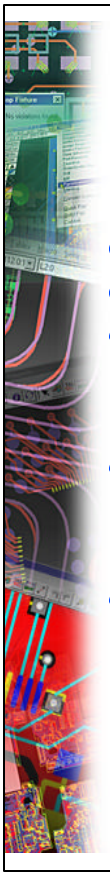
References

1. Details, artwork and a sample report is available on the IPC 9151 Website: www.pcbquality.com
2. Holden, H., How To Get Started In HDI With Microvias, Internet Article at www.circuitree.com, Nov, 2003,
3. Rhodes, R, HDI Performance Validation (Updated), The Board Authority, Vol.2 No.1, April 2000, pp22-27, Conductor Analysis Technology, www.cat-test.info/
4. Carano, M, Metalization Processes for High Density Interconnect Structures (Updated), The Board Authority, Vol.2 No.1, April 2000, pp76-80.
5. Holden, H, Balancing The Density Equation, Column, CircuiTree magazine, OCT, 1998, pp.42
6. Holden, H., HDI's BENEFICIAL INFLUENCE ON HIGH-FREQUENCY SIGNAL INTEGRITY, Mentor Technical paper at www.mentor.com/pcb/tech_paper
7. Nortel Networks owns US Patents 6,388,890 and 6,545,876 directed to Channel Routing.
8. Source: DDi conference, 1999



Advanced HDI-Microvia Design

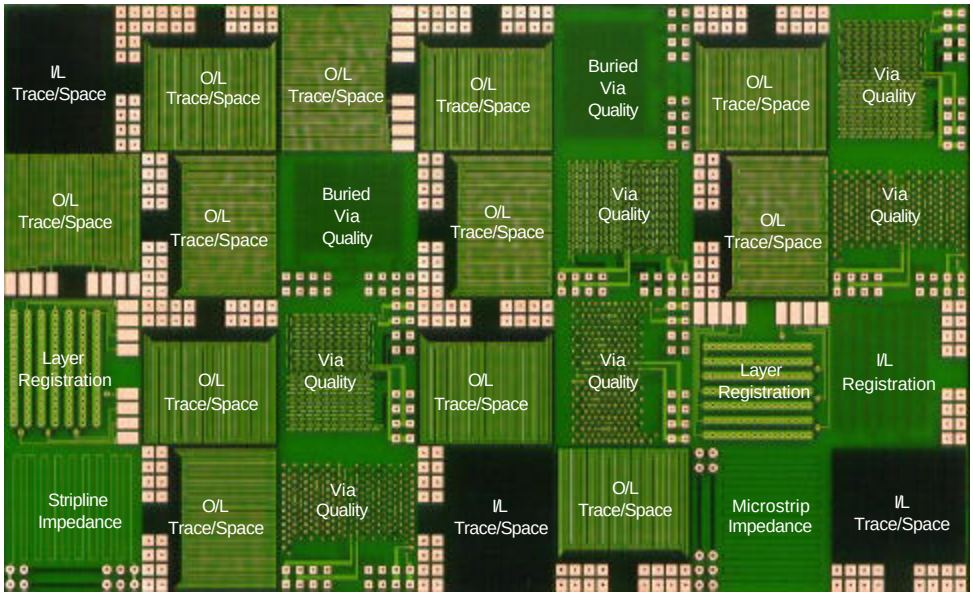
Happy Holden - Westwood



Outline

- Vendor Qualification
- Component / Assembly Issues
- Planning the Design
  - ►Modeling
  - ►Tradeoffs to Through-holes
- Signal Integrity
  - ►Surface Ground Planes
  - ►Noise
- Channel Routing
  - ►High I/O Components

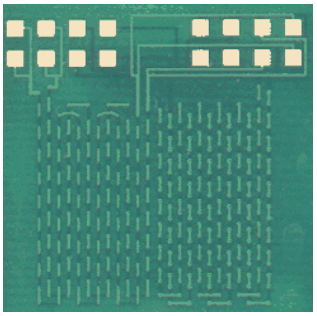
Process Capability, Quality and Relative Reliability (PCQR^2) Test Standards (IPC-9151)



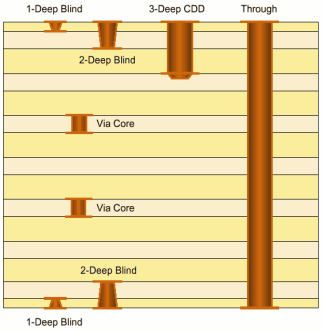
IPC-9151 Process Capability

panel size: 457.2mm x 609.6mm (18"x24)
2 trace densities: Medium & High

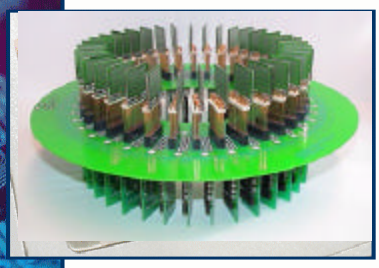
Layer Count	Thickness	Through	1-Deep Blind	2-Deep Blind	3-Deep Blind	Buried Core
2	1.575 mm (0.062")	X				
4	1.575 mm (0.062")	X	X			X
6	0.018"/ 0.031"/ 0.062"	X	X	X		X
10	1.27 mm (0.050")	X	X	X		
12	(0.062" / 0.93"	X	X	X		X
18	2.362 mm (0.093")	X	X	X	X	X
24	0.125"/ 0.250"	X	X	X	X	X
36	6.350 mm (0.250")	X	X	X	X	X

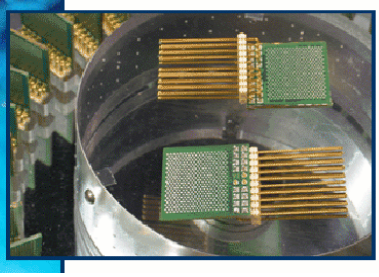


18-Layer Test Module Via Structure

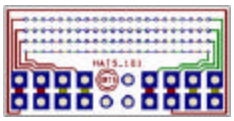


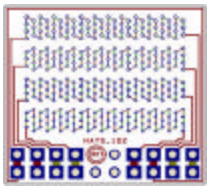
HATS Testing





Air-to-air methodology with stationary coupons
Single chamber, high volume airflow with large heat transfer capacity
Temperature range of -60C to +160C
Air transition time of 30 seconds (-60 to +160C)
Air Stability ± 2C
36 coupons (144 nets) per chamber load

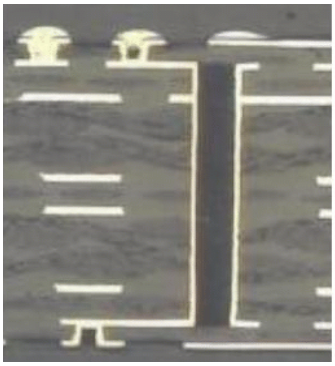
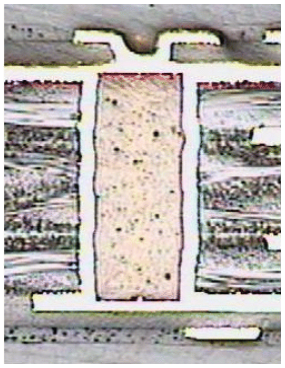
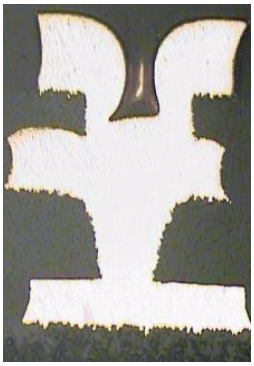
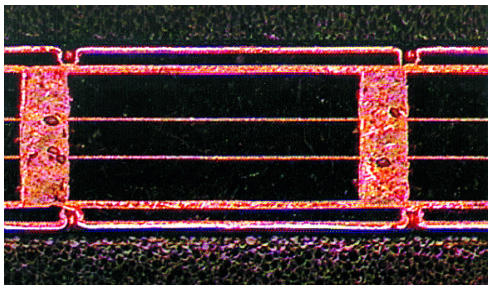
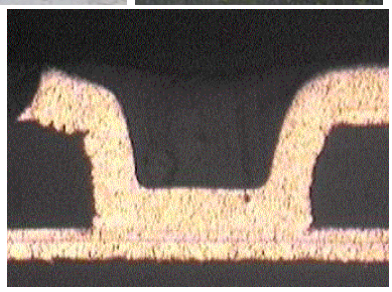




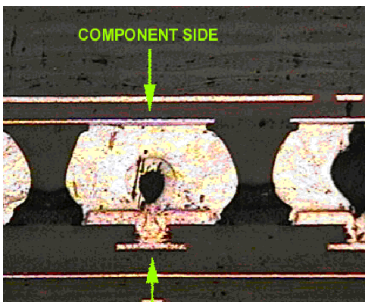
Microvia Component / Assembly Issues

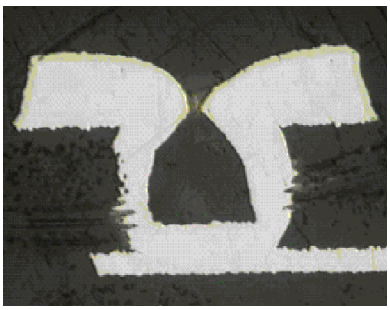
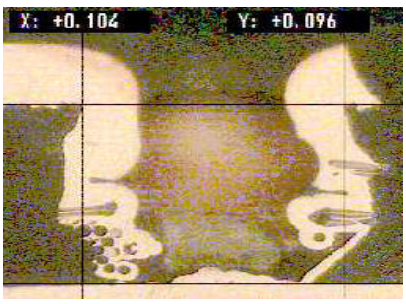
- Microvia Hole Quality
- Microvia Plating
- Via Plugging
- Via-in-Pad
- ICT

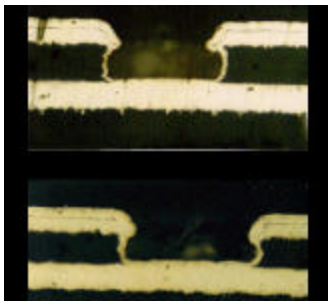
Good Blind Via Plating

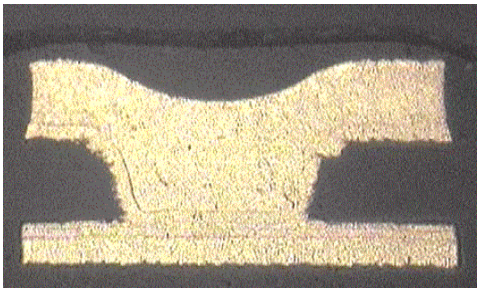
Blind Via Plating Problems



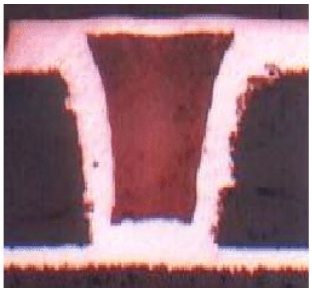





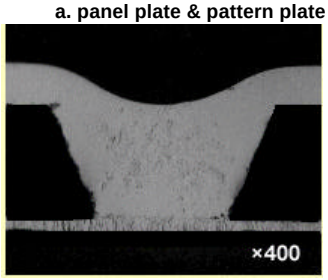
"Filled" Microvia Plating



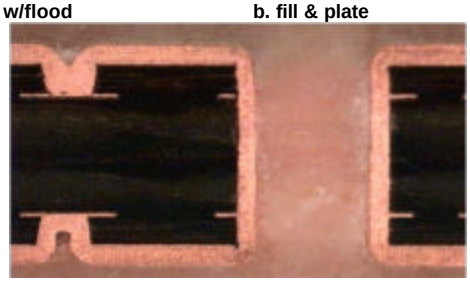
a. panel plate & pattern plate w/flood



b. fill & plate

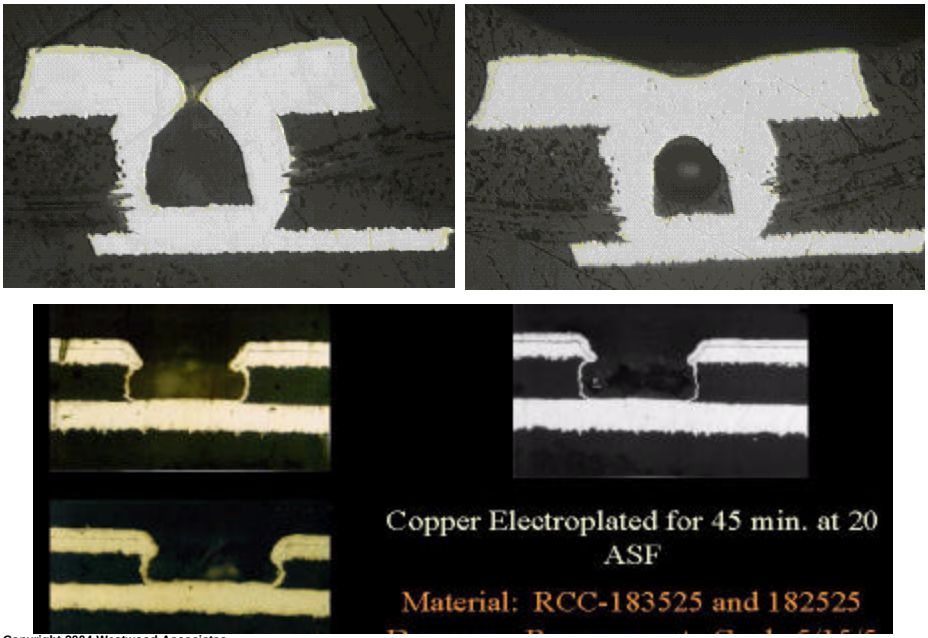


c. specialized chemistry



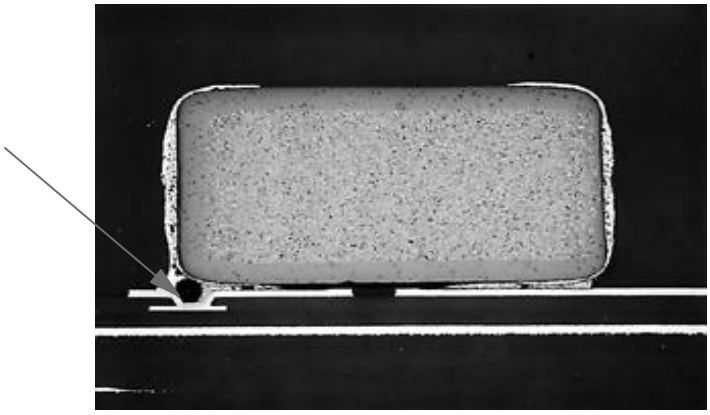
d. pulse plating w/periodic reversal

Blind Via Plating Problems



"unknown" soldering void

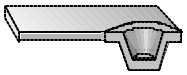
If solder 'foot' is good, will go undetected
These have been around since 1993.

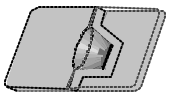


These microsections are from purchased notebook computers.

HDI MicroVia Structures (SMT Chip)

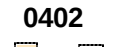
Edge of via hole is .001" away from device body outline

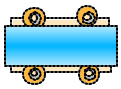


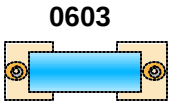


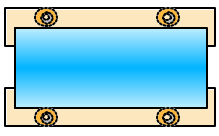
Via is tangential to inside edge of device pad farthest away from device center

2-microvias in parallel cancels the mutual-self inductance



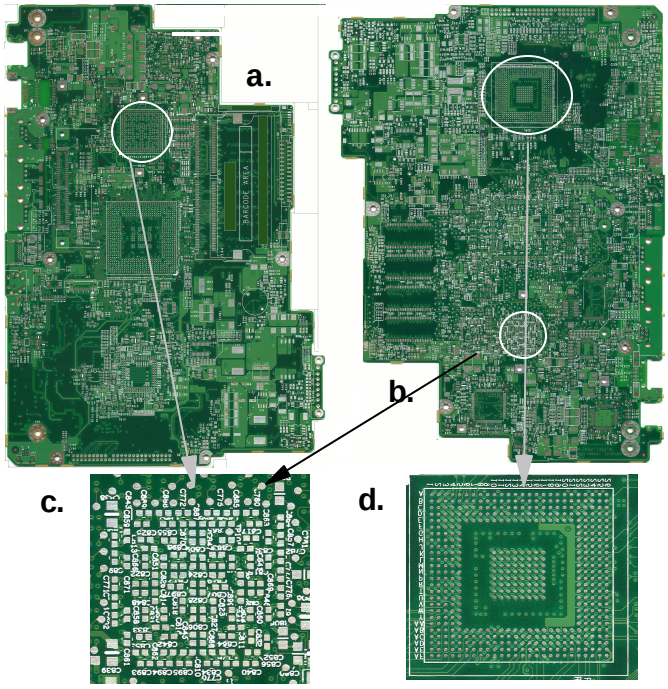






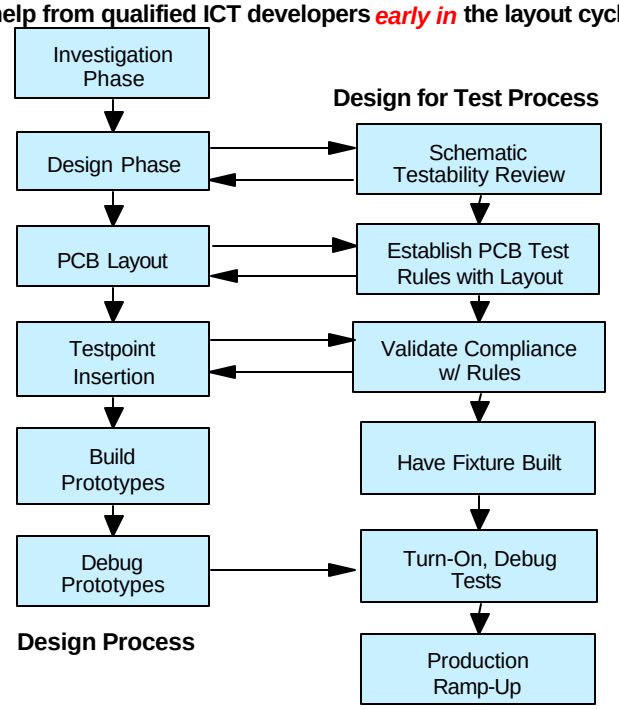
Through-Hole Conductive VIP

TH's filled with conductive paste and surface-cap plated can increase density and postpone going to microvias. But on BGAs, they are limited to 1.0 mm pitch (20mil pads).



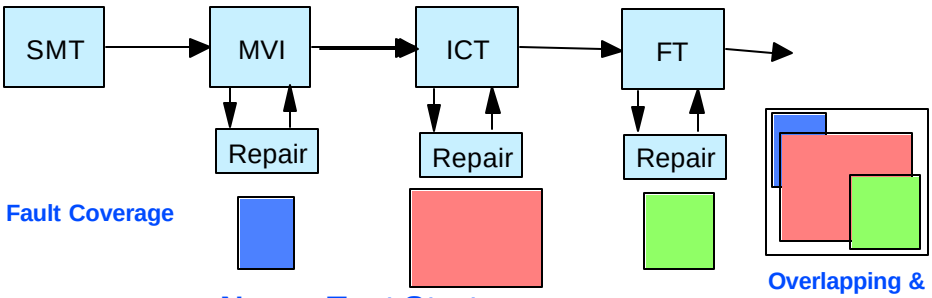
Design for Test

- Seek help from qualified ICT developers *early in* the layout cycle



Design for Test

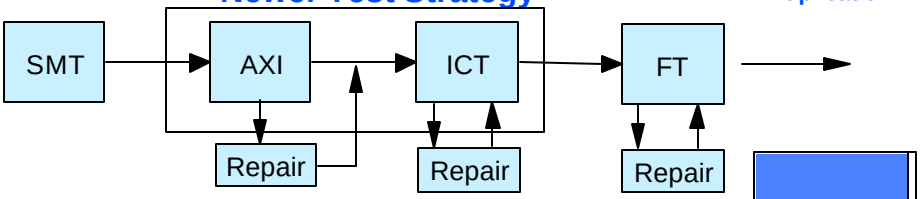
Traditional Test Strategy



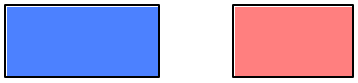
Fault Coverage

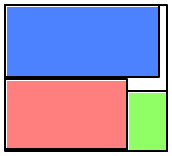
Overlapping & Duplication

Newer Test Strategy



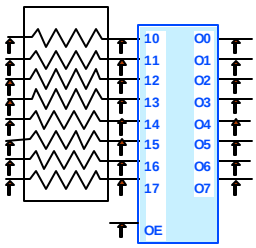
Fault Coverage





Design for Test

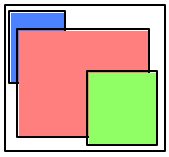
Example - a Resistor Pack & Buffer



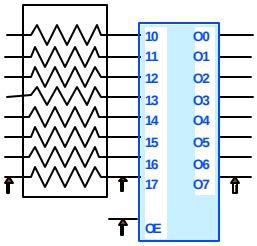
Traditional testing:
Test shorts

Test all resistors in the resistor pack, find wrong value and component problems.

25 test probes needed.



Newer Test Strategy

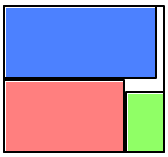


New strategy:
Intelligent ICT

Shorts, opens, and missing component already found in IXT.

"Part library test" for resistors
"Digital unit test' for buffer

4 test probes needed.



Design for Test

Example - AwareTest xi Early Results

Board Type	Nets on board	Probe* reduction	Probes* needed	Probes* removed
A	308	44.2%	172	136
B	773	52.7%	366	407
C	790	27.0%	577	213
D	1399	30.2%	977	422
E	2629	42.6%	1509	1120
F	3955	43.2%	2248	1707
G	4464	24.2%	3384	1080
H	4836	55.9%	2133	2703
I	5659	54.0%	2602	3057
J	5822	59.5%	2358	3464
K	6108	44.4%	3396	2712
L	6317	62.0%	2400	3917
M	6947	76.3%	1646	5301
N	7719	77.6%	1729	5990
O	9669	69.1%	2988	6681

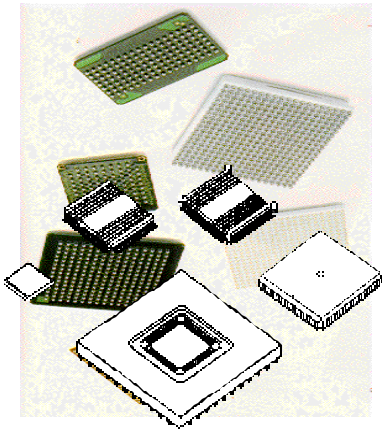
Example Board ←

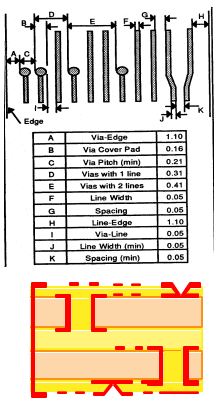
***Not counting extra Vcc and GND probes**

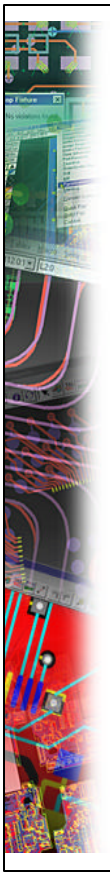
Example - 16" x 11", 2,240 comp. (756 top, 1,484 bottom)
880 resistors, 137 r-packs, 825 capacitors, 148 IC's (27 boundary scan)
24,233 solder joints including test points (137 / sq. inch
Current ICT fixture uses 5,659 probes for signal plus 317 ground and 182 Vcc for a total of 6,158 probes. Long wires and twisted pair used.
New fixture: 2,602 signal pins (54% reduction) @ $15,000 less than original fixture, completed in 2 weeks w/ short wires only (& no shorts seen).

Balancing The Density Equation

Component's PWB Wiring Demand **<** **PWBs Design Rules & Construction Wiring Capabilities**



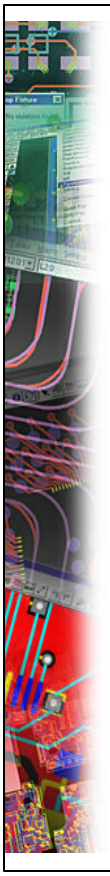




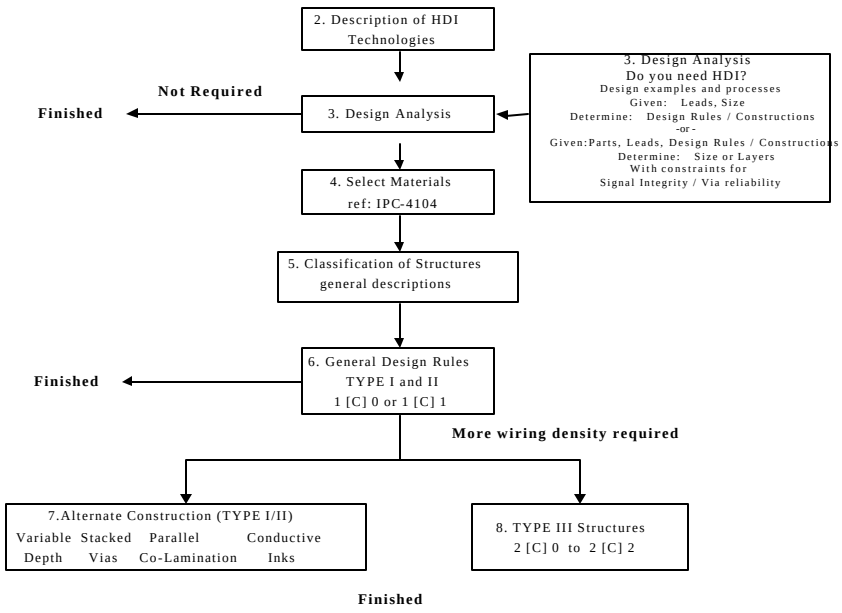
Three Cases of Wiring Demand

- **Break-out from a component**
- **Wiring between two or more tightly coupled components (CPU & cache)**
- **The demand produced by all components on both sides of a board**

Ó Co



FLOWCHAT OF HDI DESIGN GUIDELINE



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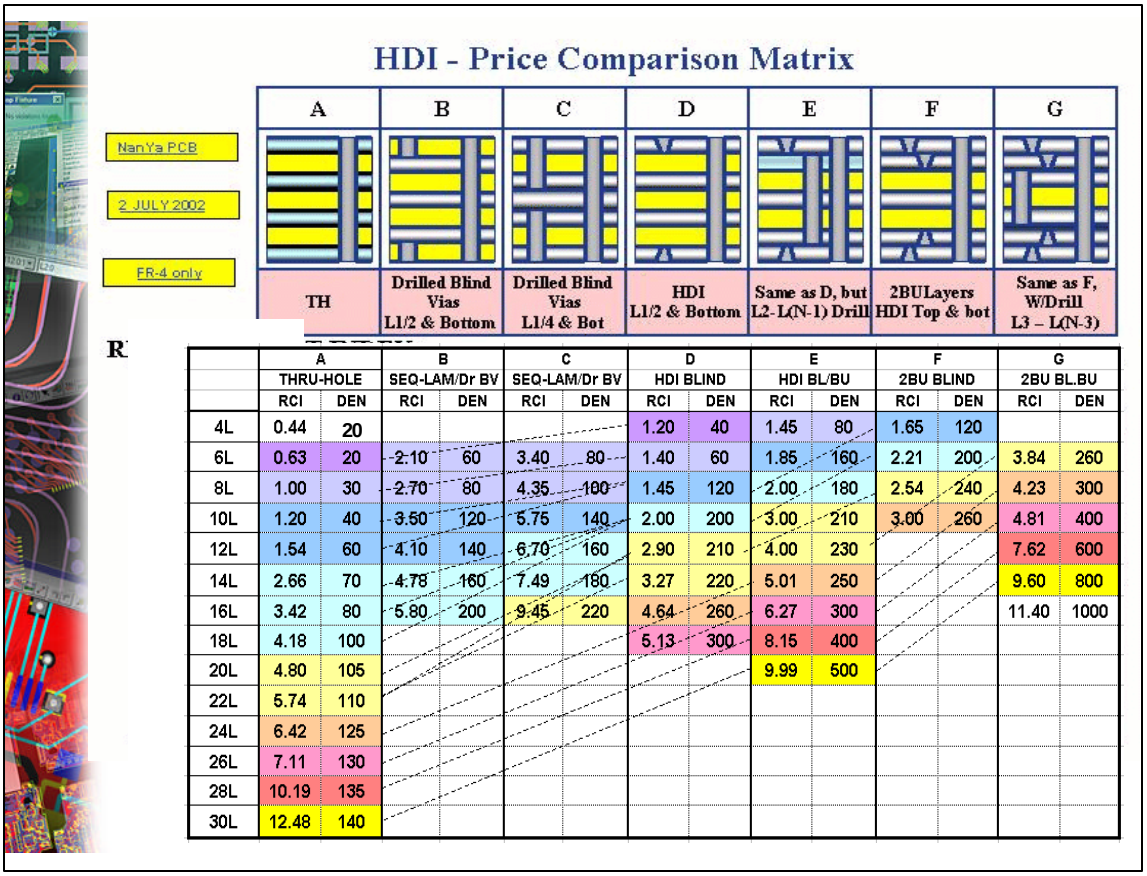
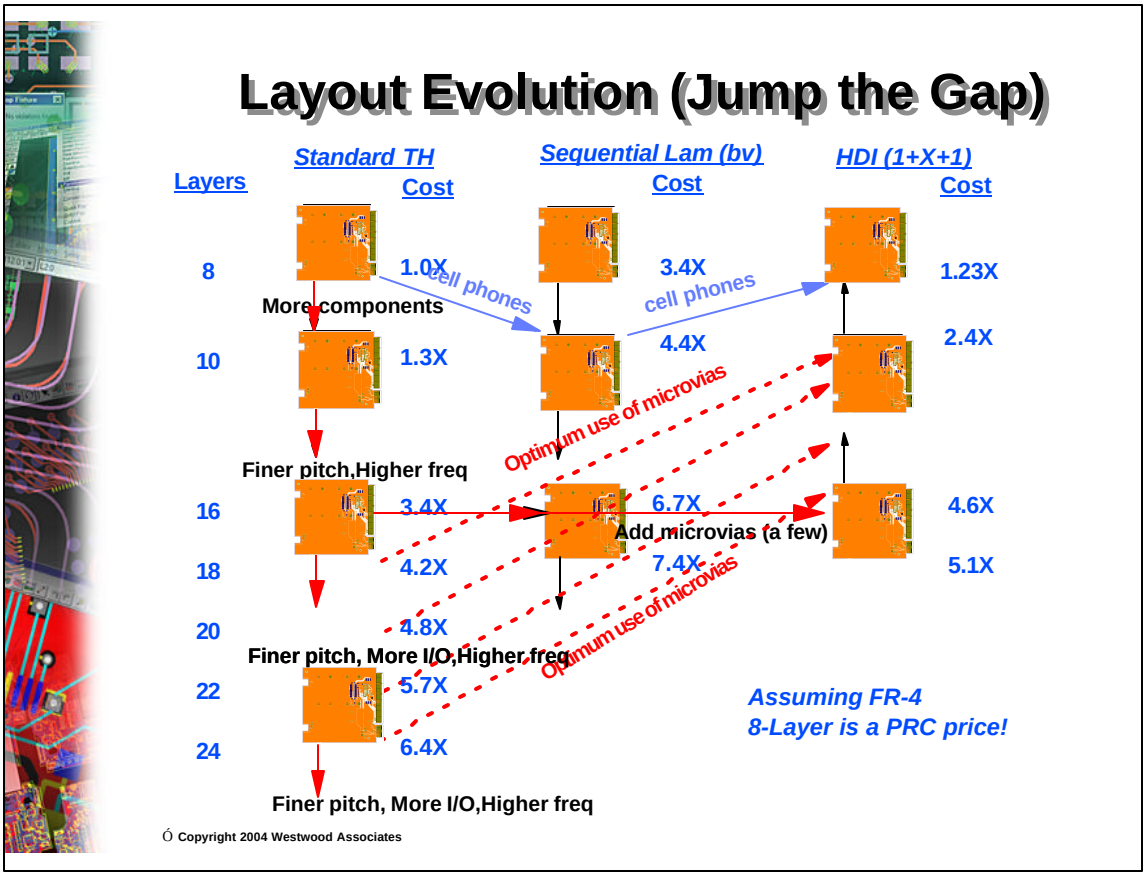
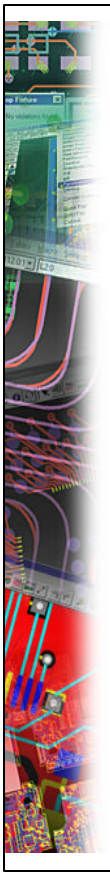


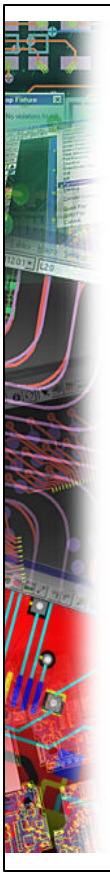
	A THRU-HOLE		B SEQ-LAM/Dr BV		C SEQ-LAM/Dr BV		D HDI BLIND		E HDI BL/BU		F 2BU BLIND		G 2BU BL.BU	
	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN
4L	0.44	20					1.20	40	1.45	80	1.65	120		
6L	0.63	20	2.10	60	3.40	80	1.40	60	1.85	160	2.21	200	3.84	260
8L	1.00	30	2.70	80	4.35	100	1.45	120	2.00	180	2.54	240	4.23	300
10L	1.20	40	3.50	120	5.75	140	2.00	200	3.00	210	3.00	260	4.81	400
12L	1.54	60	4.10	140	6.70	160	2.90	210	4.00	230			7.62	600
14L	2.66	70	4.78	160	7.49	180	3.27	220	5.01	250			9.60	800
16L	3.42	80	5.80	200	9.45	220	4.64	260	6.27	300			11.40	1000
18L	4.18	100					5.13	300	8.15	400				
20L	4.80	105							9.99	500				
22L	5.74	110												
24L	6.42	125												
26L	7.11	130												
28L	10.19	135												
30L	12.48	140												





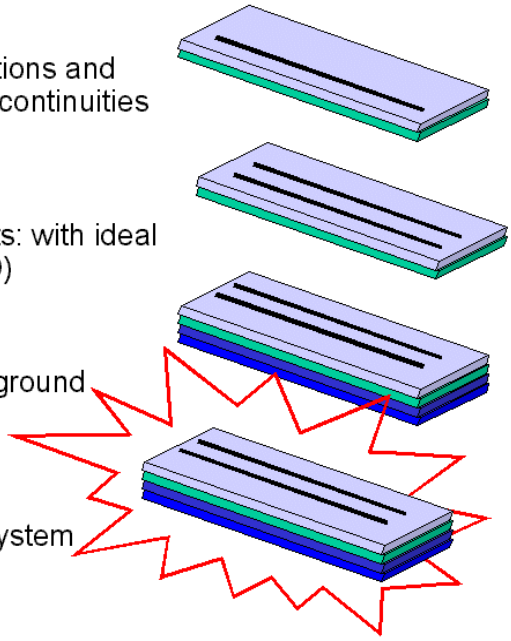
Circuitry
(Signal Integrity Issues)

- Characteristic Impedance
- Low Voltage Differential Signals
- Signal Loss
- Noise Sensitivity
- Power Supply Inductance
- Crosstalk
- Via Inductance



Four Families of SI Problems

1. Signal quality of one net: reflections and distortions from impedance discontinuities in the signal or return path
2. Cross talk between multiple nets: with ideal return paths, and without (SSO)
3. Rail collapse in the power and ground distribution network
4. EMI from a component or the system



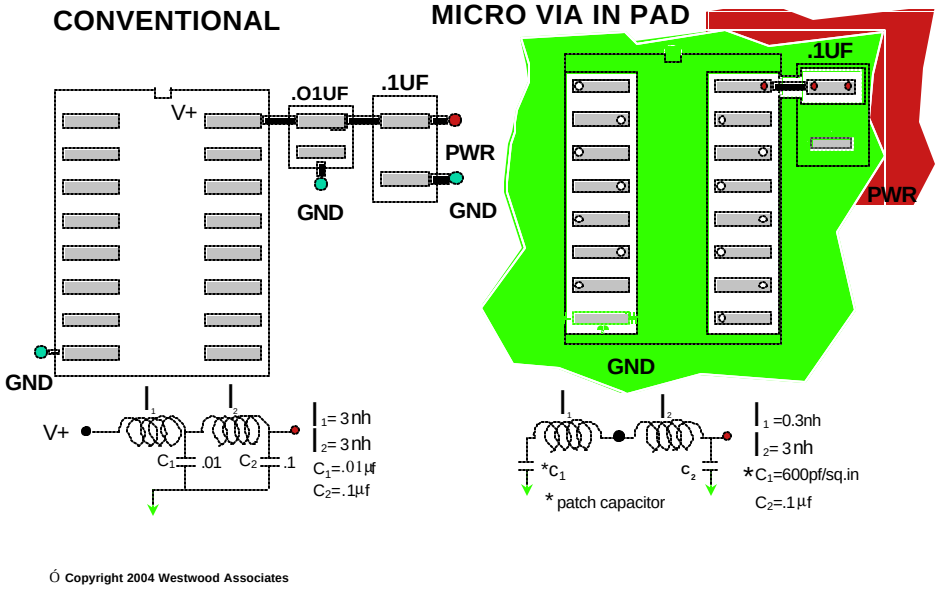
Source: Eric Bogatin, "Signal Integrity and HDI Substrates",The Board Authority, Vol 1 no.2, June 1999

HDI Features and SI Problems They Help Solve

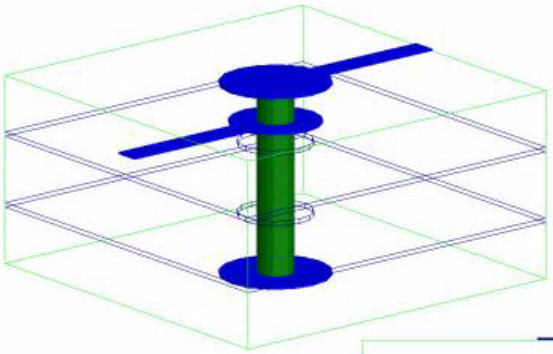
- **Reduction of noise**
  Reflections
  Crosstalk
  Simultaneous switching
- **EMI reduction**
- **Improved signal propagation and lower attenuation**

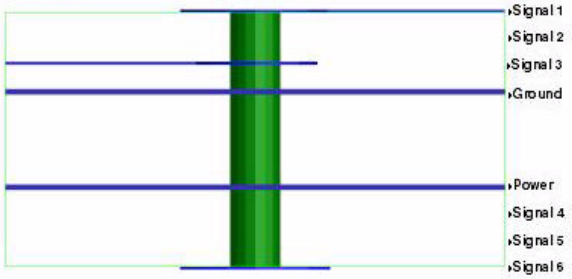
HDI features	Signal quality	Cross talk	Switching Noise	EMI
Short interconnect lengths	X	X		
Low dielectric constant	X	X		
Small vias and small features	X		X	
Vias in pads			X	
Fine lines and thin dielectric		X	X	X
Support for fine-pitch components			X	X

Switching Noise - Bypassing

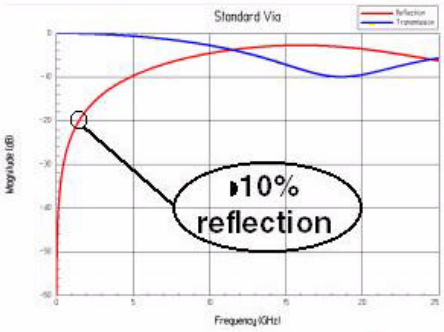


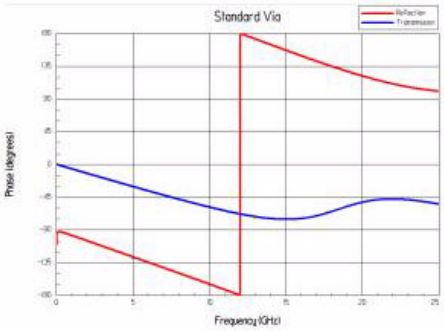
Characterizing a Standard Via

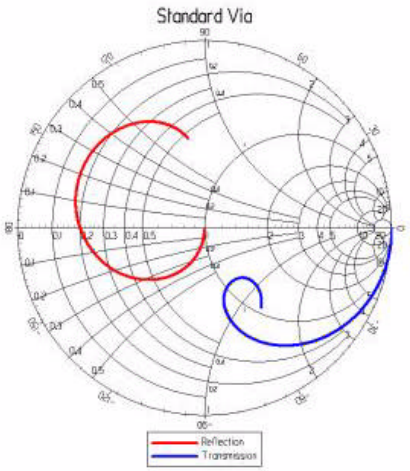




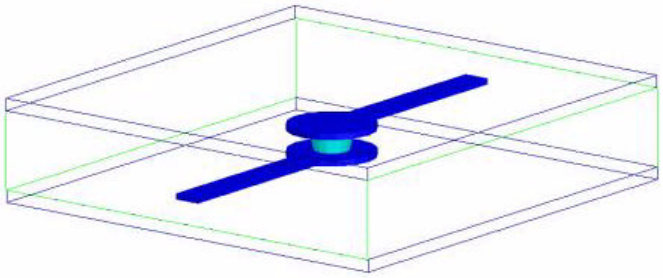
Electrical Performance of a Standard Via

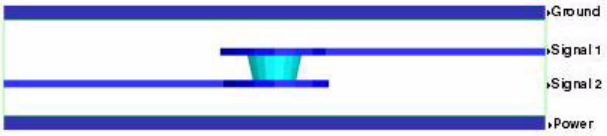




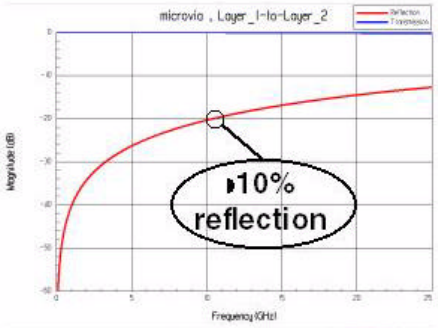


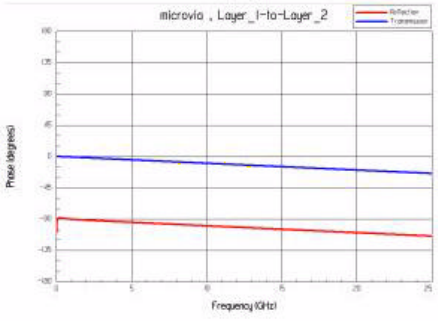
Characterizing a Micro Via

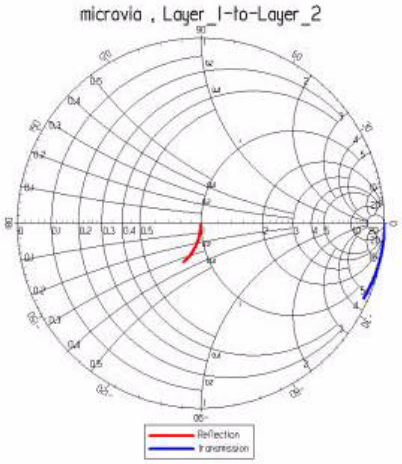




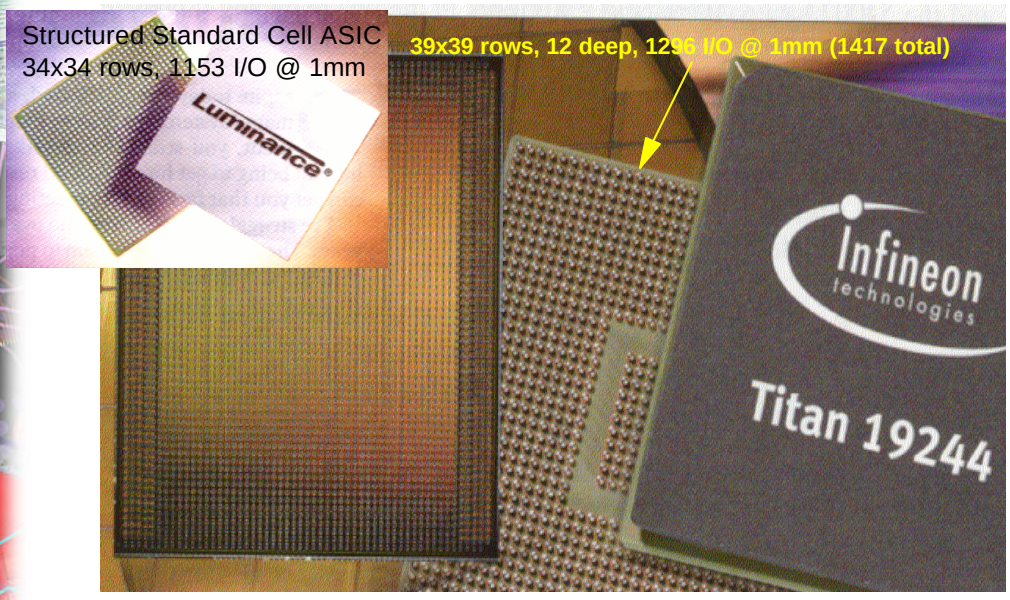
Electrical Performance of a Micro Via





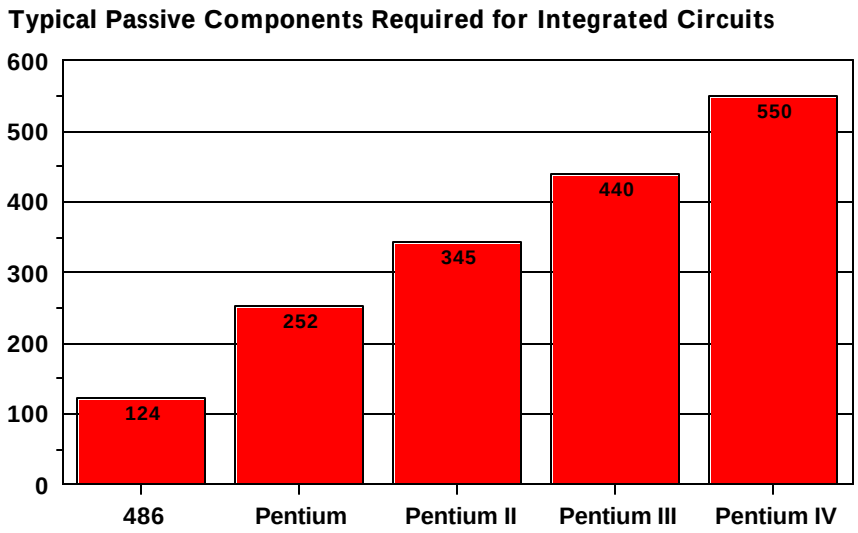


Bigger FPGA are Coming !



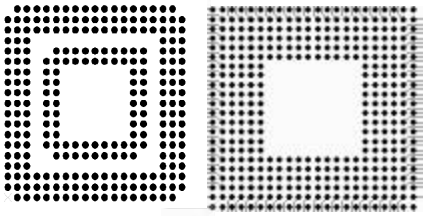
New Actel, Infineon, Xilinx & Altera FPGAs have 256, 348, 396, 456, 564, 692, 804, 860, 996, 1020, 1164, 1296, 1508, 1696, & 1704 I/Os.

Typical Passive Component Requirements for Integrated Circuits

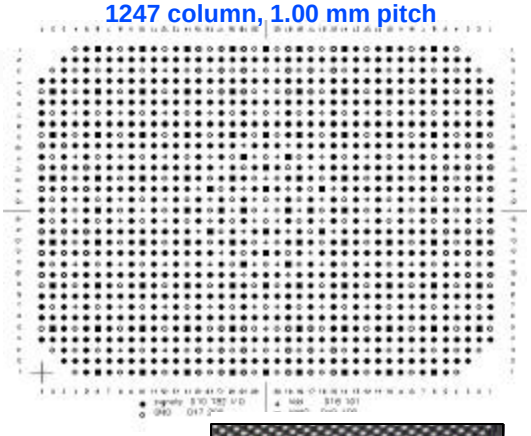


Consider: These new Components

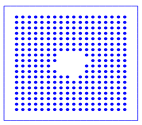
Micro Ball Grid Array (18.0mm x 18.0mm) - 384 balls, 0.80 mm pitch



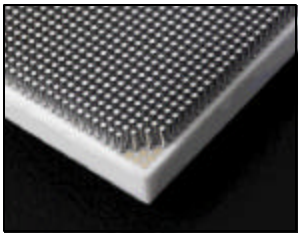
Ceramic column grid array (32.5mm x 42.5mm) - 1247 column, 1.00 mm pitch



Star Ball Grid Array (15.0mm x 15.0mm) - 257 balls, 0.80 mm pitch



Chip Scale Pkg.
(14.0 mm x 14.0 mm)
296 I/O 0.65 mm pitch (26 mils)



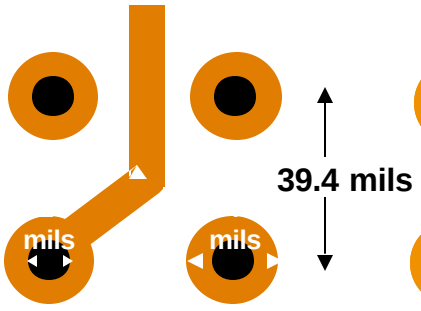
How Does This Work ?
Blind Vias Create I/L Channels

1 mm (39.4 mils) pitch with through holes

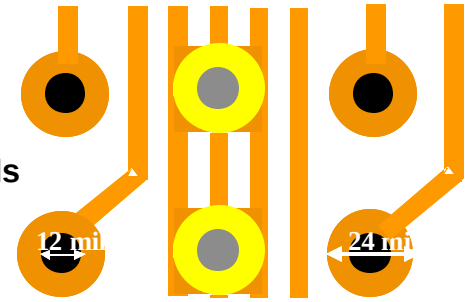
Subsequent Signal Layers only 1 row escaped

HDI blind vias Effective 2 mm pitch on drilled holes !

5.0 mil line and 5.2 mil space



5 channels at 5/5 line/space or
6 channels at 4/4.5 lines/space

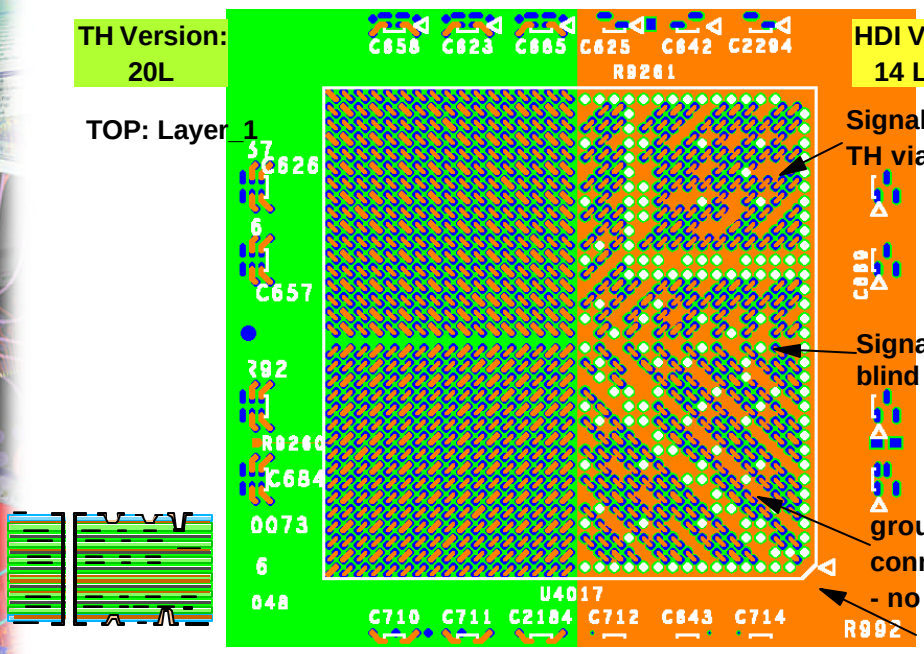


Channel Routing Using Blind Vias*

TH Version: 20L

HDI Version: 14 Layers

TOP: Layer_1



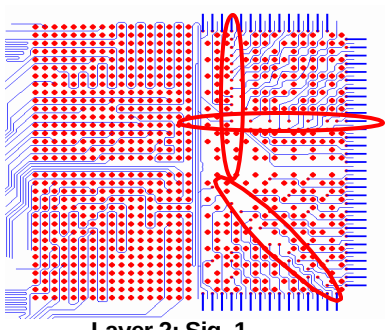
Signal, PWR TH vias

Signal, PWR blind vias

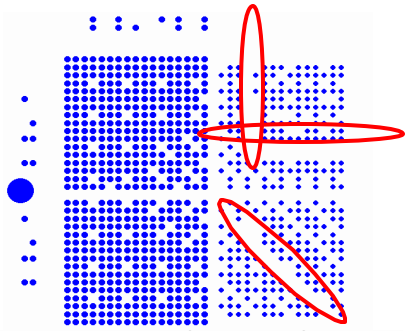
ground connection - no vias - ground

*Channel Routing is a Patented Procedure of Nortel Networks,#6,388,890 & #6,545,876

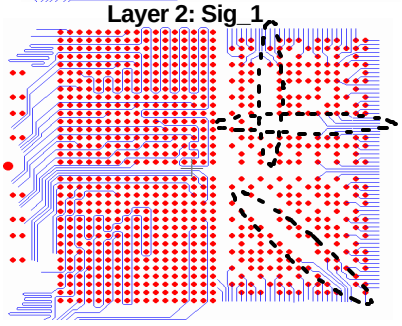
Channel Creation*



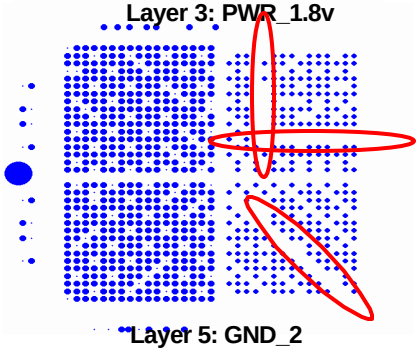
Layer 2: Sig_1



Layer 3: PWR_1.8v



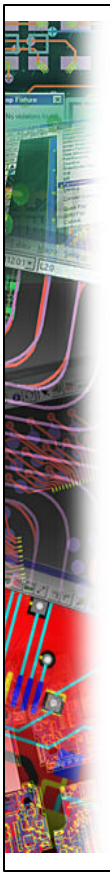
Layer 4: Sig_3

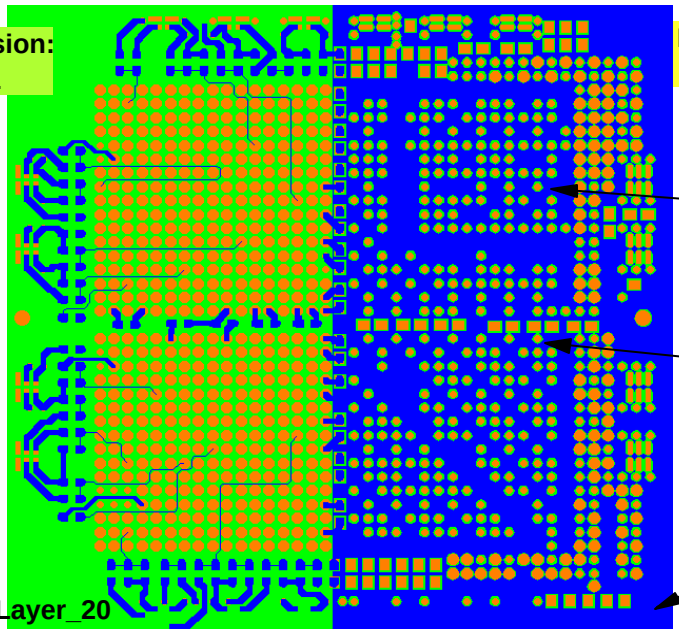


Layer 5: GND_2

*Channel Routing is a Patented Procedure of Nortel Networks,#6,388,890 & #6,545,876

Channel Routing Using Blind Vias*

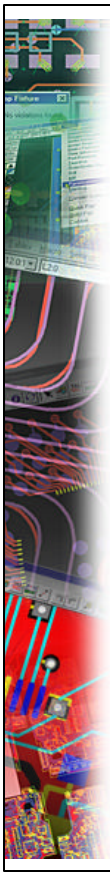


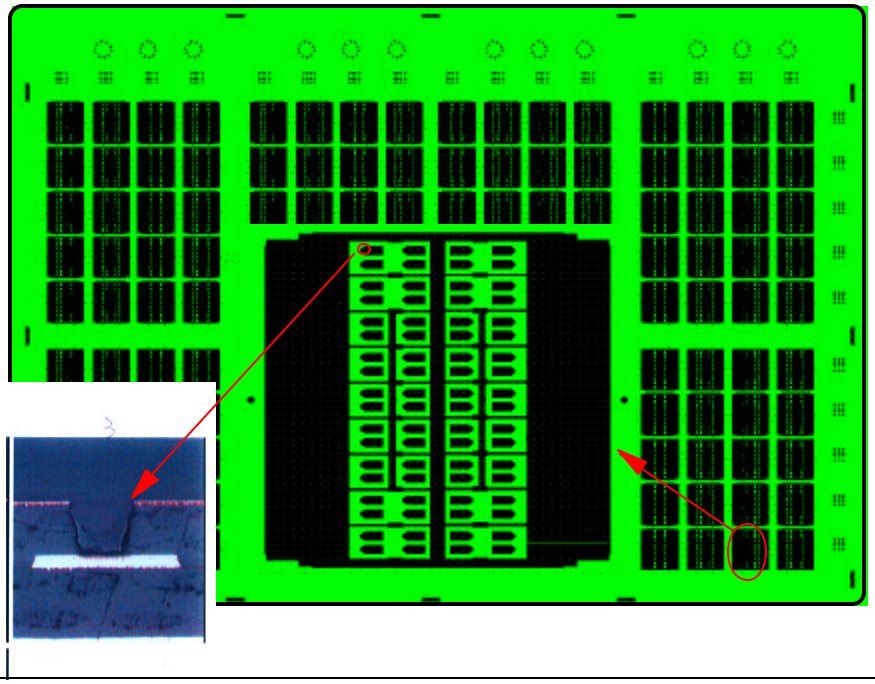


*Channel Routing is a Patented Procedure of Nortel Networks,#6,388,890 & #6,545,876

Large High-Frequency Backplanes

6 Layer HDI Midplane Replaced 2-30 Layer Backplanes

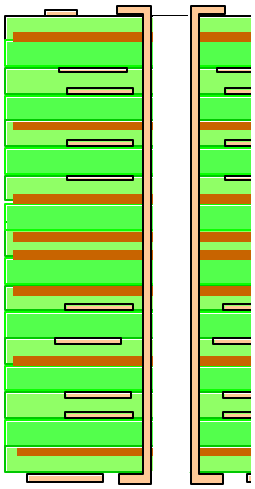




Conventional High Speed Construction Vs. HDI Constructions

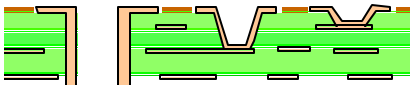
from this

1. SMT
2. GND
3. Sig_1
4. Sig_2
5. GND
6. Sig_3
7. Sig_4
8. GND
9. PWR
10. PWR
11. GND
12. Sig_5
13. Sig_6
14. GND
15. Sig_7
16. Sig_8
17. GND
18. SMT



to this

1. SMT/GND
2. Sig_1
3. Sig_2
4. PWR
5. .....



or this

1. SMT/GND
2. PWR
3. Sig_1
4. Sig_2
5. GND
6. .....

D.Cap

or this

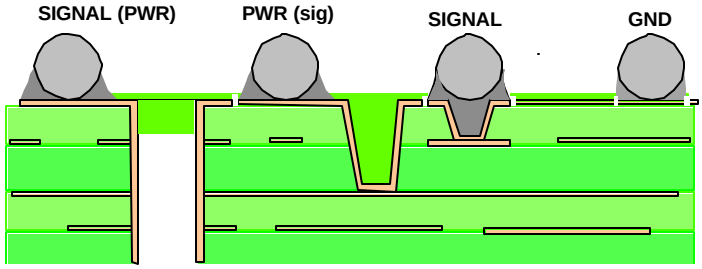
1. SMT/GND
2. PWR / Sig_1
3. PWR / Sig_2
4. GND
5. PWR / Sig_3
6. PWR / Sig_4

D.Cap
D.Cap
D.Cap

HDI Constructions

to this

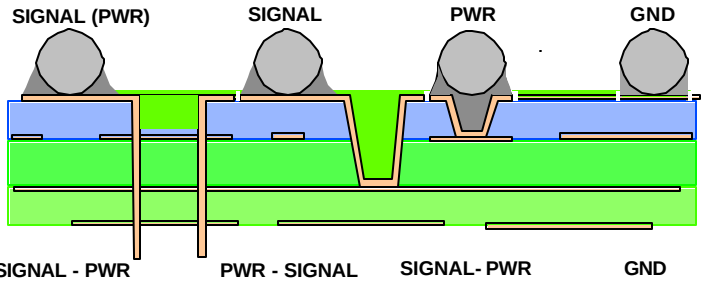
1. SMT/GND
2. Sig_1
3. PWR (Sig_2)
4. Sig_2 (PWR)
5. .....



or this

1. SMT/GND
2. PWR
3. Sig_1
4. Sig_2
5. GND
6. .....

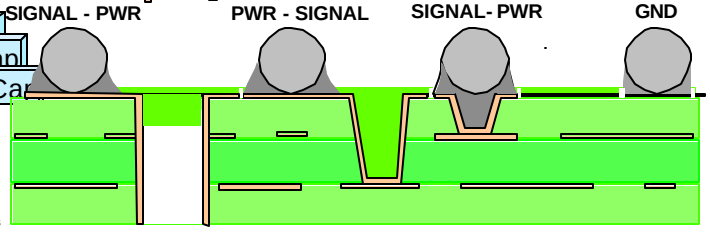
D.Cap

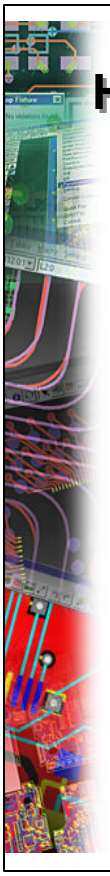


or this

1. SMT/GND
2. PWR / Sig_1
3. PWR / Sig_2
4. GND

D.Cap
D.Cap
D.Cap





How To Get Started in HDI With Microvias

1. Do you need HDI?

- Density
- Fine-pitch BGAs
- High I/O area Arrays

2. OK - You Do !

- IPC Standards: 2315, 4104, 6016
- Select Materials (IPC-4104)
- Determine Stackup and Design Rules: (IPC-2315)
- Layout Efficiency
- Evaluate Fabricators (IPC-9151)

3. Start with a test vehicle

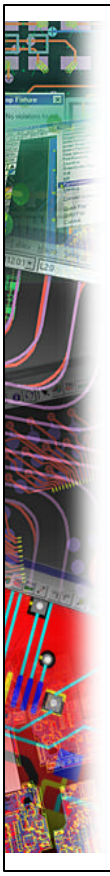
- Learn to assemble and test
- HDI Reliability
- Validate higher electrical performance

4. Redesign a HLC Board

- Gain volume experience

5. Pick a Project or Candidate for HDI

- Evaluate CAD limits and issues
- Channel routing
- Surface ground planes
- Auto routing tuning



FINISH