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High Frequency Conductor Loss Impact of Oxide and Oxide Alternative Processes

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Abstract
In most of today's high speed digital interconnects, the signal loss associated with the printed circuit board (PCB) is the dominate factor. Material selection, trace geometry, and choice of copper foil all play a role in establishing the signal loss associated with the PCB interconnect. Silicon and system designers have techniques for dealing with signal loss and compensating for lossy interconnects; but, these techniques require accurate modeling and characterization of each source of interconnect loss. Previous work has shown the impact of dielectric material selection on loss, as well as conductor loss due to high frequency skin effects associated with copper roughness, copper foil tooth structures, and surface finish selection. For innerlayer stripline traces, surface preparation processes such as oxide and oxide alternative alter the conductor surface to improve adhesion. This alteration to the conductor surface geometry affects conductor loss and can influence supplier-supplier variation. Furthermore oxide processing can affect lot to lot variation of impedance and line loss. This paper investigates the differences between several oxide and oxide alternative processes on high frequency conductor loss and the impact of process parameters such as rework.

Introduction
The most efficient routing of signals for high density interconnects is achieved through the use of multilayered printed circuit board substrates. To achieve multiple layers of insulated copper circuitry, PCB fabrication facilities form circuitry patterns on double-sided layers, and then laminate the double-sided layers into multi-layered packages. When laminating the double-sided innerlayer cores, additional dielectric material is needed to achieve sufficient insulation between conducting copper traces. The dielectric material also needs to provide good adhesion among layers so that the interconnection package does not delaminate under subsequent thermal operations such as soldering. The dielectric is added to the package by the use of 'b-stage' partially cured layers of dielectric-impregnated glass cloth. When stacked together in a hydraulic press and heated, the resin flows against the innerlayers, bonding the innerlayers once cooled.

In early manufacturing of multilayer PCB's, adhesion among innerlayers was inadequate between the untreated copper and the dielectric. Improvements were made to the adhesion of the multilayer packages by chemical and geometric bonding. Chemically, it was determined that copper might degrade the dielectric material by decomposing epoxy and other polymeric materials, especially those composed of flame-retardant (halogenated) monomers. An oxide formed on the copper tended to offer better thermal durability, theoretically providing a barrier coating between elemental copper and polymer dielectrics. It is generally agreed that the geometric benefit of copper oxide treatments overwhelmed the chemical benefits. In this case, the roughness of the copper oxide allowed a geometric texture to which the flowed polymer could lock onto once cooled.

Copper oxide systems were optimized to provide uniformity of function and appearance. Eventually, a hot immersion bath of sodium chlorite and caustic became the industry standard method for producing thick black oxide treatments. (See Figure 1.) More problems arose as circuit boards became more complex. As circuit layers reached 20 or more and board thickness increased, the ability to route signals pushed the interconnection mechanism between layers, the through-hole (PTH), to very small diameters. Small diameter drilling led to rough PTH sidewalls, and 'wedges' between the copper and polymer. In addition to the physical defect of innerlayer wedging, the chemical defect of 'pink ring' became prevalent. The pink-ring defect was mainly overcome through the use of an additional chemical step following oxide. In one type of system, the oxide was purposely 'reduced' with dimethyl amine borane DMAB. (See Figure 2.) In an alternative method, the oxide was treated with a chelating chemical, dissolving most of the leafy black oxide and leaving the rough copper structure with just a thin amount of barrier oxide.

Cleaner	5 minutes	65°C
Microetch	1 minute	35°C
Pre-Dip	1 minute	30°C
Oxide	5 minutes	75°C

Figure 1 - Traditional Thick Black Oxide Process

Cleaner	5 minutes	65°C
Microetch	1 minute	35°C
Pre-Dip	1 minute	30°C
Oxide	5 minutes	75°C
Reduction/ Dissolution	2 minutes	35°C

Figure 2 - "Reduced" Oxide Process

Another revolution occurred in oxide treatment systems during the past ten years. The PCB fabrication industry began demanding automated, conveyorized systems for handling the increasingly thin innerlayers. The new 'oxide alternative' systems used far less chemicals, employed safer, milder chemicals based on chemical microethants, and operated at lower temperatures for a far shorter dwell time. The oxide alternative systems combined the microetching and oxide-forming chemical steps, but introduced a novel 'conversion coating' ideal for copper-dielectric adhesion. An even newer feature of the oxide alternative systems is the use of chemicals which remove less copper. (See Table 1) In this manner, the signals traveling through very fine traces retain their integrity. New dielectric B-stage systems may also benefit from the 'low-etch' oxide altematives since the flow of these polymers at lamination may be reduced. Low-flow polymers can mate better with low-topography copper oxide surfaces. (See Figures 3-6)

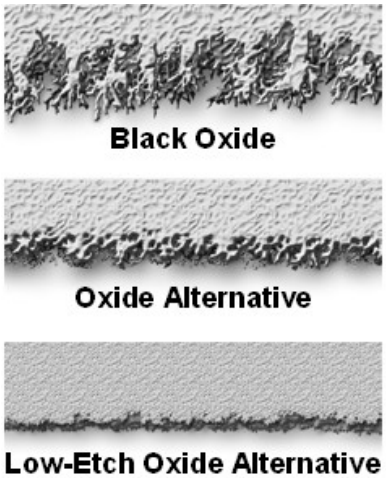

Figure 3 - Schematic Representation of Oxide and Oxide Alternative Surfaces

Cleaner	0.5 minutes	50°C
Pre-Dip	0.5 minutes	25°C
Conversion Coating	1 minutes	40°C

Figure 4 - Alternative Oxide Process

Cleaner	0.5 minutes	50°C
Pre-Dip	0.5 minutes	25°C
Conversion Coating	1 minutes	30°C

Figure 5 - Low-Etch Alternative Oxide Process

Figure 6 - Vertical and Conveyorized Innerlayer Oxide Systems

Table 1 – Metal Removal of Innerlayer Bonding Processes

Thick Black Oxide	1.3 µm
"Reduced" Oxide	1.3 µm
Oxide Alternative	1.5 – 2.5 µm
Low Etch Oxide Alternative	0.5 – 0.8 µm

Test Vehicle

A set of test boards, using Intel's material characterization test board design[3], were fabricated to quantify the electrical differences that may result from the selection of oxide and oxide alternative processes and the effect of rework processes. The test boards contained stripline structures on both layer 2 and layer 7 that consisted of 1inch, 3inch, and 5inch line segments. (See Figure 7) Microvias were used to access the stripline structures to reduce the effects of via parasitics and push the resonant frequency beyond the 20GHz test range. The selection of FR4 as the dielectric material is known to result in higher loss, but is indicative of common designs at Intel.

The test matrix consisted of four innerlayer bonding processes, each at standard process conditions, and at one or two rework process conditions. The matrix is shown in Table 2. The test was conducted by processing all cores together through the innerlayer fabrication steps of Develop-Etch-Strip and Optical Inspection. As a result, the material, artwork, imaging, and etching conditions of the test matrix was constant across the test matrix, so that any variation of trace geometries could be associated with the innerlayer bonding matrix condition. The innerlayer cores were then sent to MacDermid where they were randomized, marked, and processed under the different matrix conditions. After processing, the innerlayer cores were returned, laminated, and completed as a single work order at TTM California.

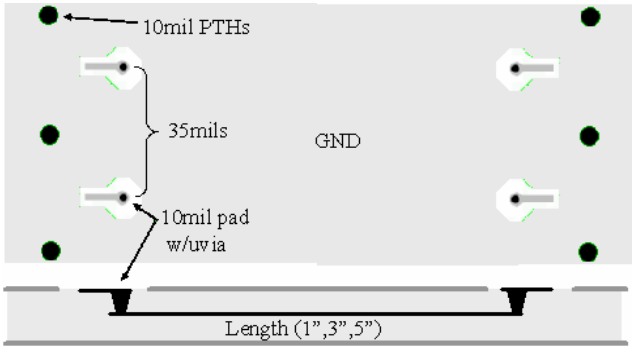

Figure 7 - Test Structure Schematic

Table 2 – Test Vehicle Matrix

Process ID	Process	Reworks	#Panels	#Innerlayer Cores
A	*OmniBond* Black Oxide	0	3	6
A	*OmniBond* Black Oxide	1	3	6
B	*OmniBond*+ Oxide Dissolution	0	3	6
B	*OmniBond*+ Oxide Dissolution	1	3	6
C	*MultiBond 100* Oxide Alternative	0	3	6
C	*MultiBond 100* Oxide Alternative	1	3	6
D	*MultiBond LE* Low-Etch Oxide Alternative	0	3	6
D	*MultiBond LE* Low-Etch Oxide Alternative	1	3	6
D	*MultiBond LE* Low-Etch Oxide Alternative	2	3	6

Physical Measurement Results

Surface topography analysis of the process conditions involved using both Scanning Electron Microscopy (SEM) and laser profilometry. SEMs were taken of all process conditions. (See Figure 8.) Laser profilometry measurements were performed on the alternative oxide process conditions only due to the high light absorbing properties of black oxide. See Appendix. In SEMs the structures of both black oxide and oxide dissolution processes showed small oxide structures or nodules in a fairly even distribution across the surface. The surface topography of the black oxide and oxide dissolution after rework remained visually identical. The oxide alternative processes utilize a grain boundary etch to form a roughened surface, and produces slightly larger scale structures in this study compared to the oxide dissolution process. The surface features of the oxide alternative processes contained more localized variations in terms of nodule sizes and peak to value heights; but, were uniform over areas greater than 10-20? ms.

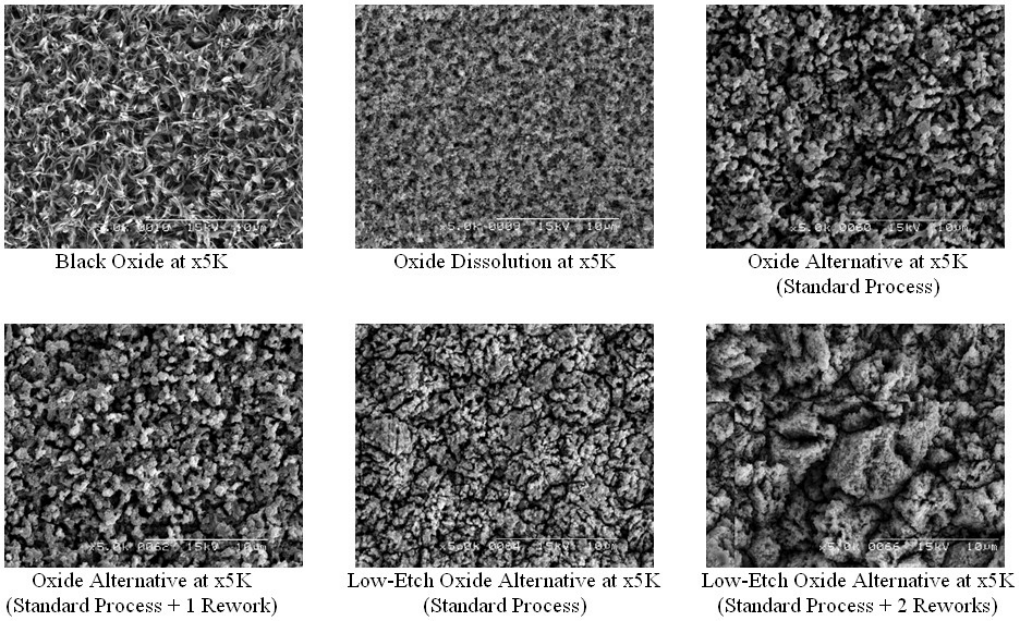

Figure 8 - SEM Pictures of Process Factors

The impact of rework on the oxide alternative processes was visible in SEM pictures as well as the laser profilometry measurements. Summarized in Table 3. Rework not only increased the peak to valley height; but also increased nodule sizes. Interestingly, SEM pictures did not show as significant of a change in surface roughness after a single rework of the MultiBond 100 Oxide Alternative as shown in corresponding laser profilometry measurements. For the low-etch oxide alternative the impact of two rework processes was substantial in terms of roughness measurements and physical trace measurements.

Cross-section measurements were taken and showed a correlation of surface roughness versus the resulting trace width and trace height. The trace height variations between the four process chemistries followed closely to that given in Table 1. As seen in the Table 3, Figure 9, and Figure 10, low-etch oxide alternative process resulted in the thickest copper heights and widest traces after processing. The impact of rework appeared to also follow the predicted Cu height loss with the exception of Process D (low-etch oxide alternative) which showed an overly aggressive first rework result and a sequentially less aggressive second rework condition. The Process D condition at two reworks was within the expected range of two sequential reworks. It is noted that Process D physical results (conductor width and conductor height) of the standard one rework and two rework conditions correlate to the following electrical property analysis.

Table 3 - Physical Measurement Comparison

Process ID	Process	Reworks	Ra (um)	Rms (um)	Ave Trace Width (mils)	Ave Trace Height (mils)
A	*Black Oxide*	0	n/a	n/a	4.3	0.68
A	*Black Oxide*	1	n/a	n/a	3.5	0.55
B	*Oxide Dissolution*	0	n/a	n/a	3.9	0.61
B	*Oxide Dissolution*	1	n/a	n/a	3.3	0.45
C	*Oxide Alternative*	0	0.505	0.659	4.2	0.66
C	*Oxide Alternative*	1	0.681	0.922	3.6	0.57
D	*Low-Etch Oxide Alternative*	0	0.469	0.579	4.5	0.71
D	*Low-Etch Oxide Alternative*	1	0.531	0.683	3.9	0.61
D	*Low-Etch Oxide Alternative*	2	1.436	1.768	3.8	0.59

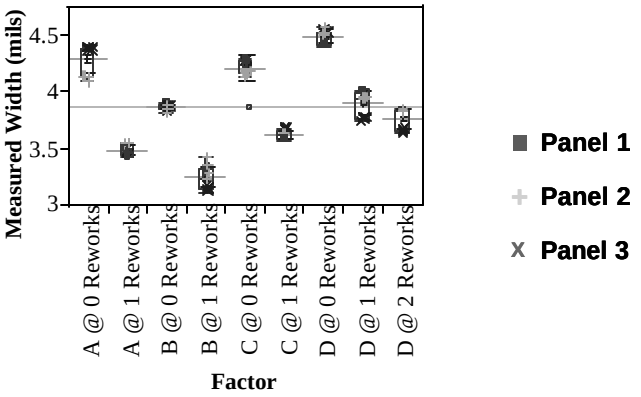

Figure 9 - Measured Trace Widths

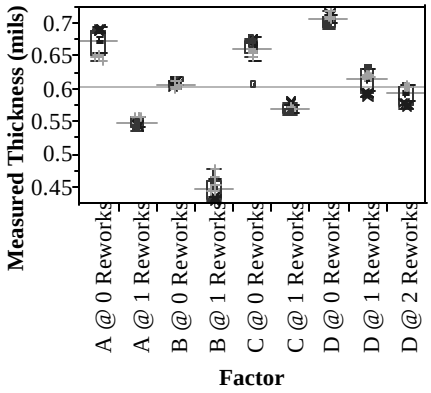

Figure 10 - Measured Trace Thickness

Electrical Measurement Results

Electrical measurements were performed by taking S-parameter measurements through 20GHz using an Agilent Vector Network Analyzer (VNA). The measurements were taken with Cascade 250um pitch Ground-Signal-Ground Pico-Probes to minimize launch parasitics. The VNA was calibrated with using SLOT methodology and a ceramic calibration standard. The VNA was configured to sample 801 data points from 50MHz to 20.05GHz. For each of the matrix conditions in Table 3, fifteen traces were measured with five measurements per panel of each of the three panels per matrix condition. The electrical parameters of the traces were then extracted from the S-parameters using the equations and identities giving in Figure 13 and Figure 15. The measurements for the panel sets Panel 1, Panel 2, and Panel 3 were each taken on separate days and with separate equipment calibrations.

The measured dielectric constant was not different between the factors or influenced by rework processes. (See Figure 11) The variation in dielectric constant within a process factor and between two process factors was consistent with the variation reported due to spatial dielectric constant of glass woven composites.[2] In cross-section analysis, the factors with the narrowest range of measured dielectric values showed a slight orientation skew of the traces to the glass weave fabric resulting in a more consistent dielectric constant between traces.

The measured impedance differences between the factors variation followed the physical geometry variations seen in cross-section analysis. (See Figure 12) Low-etch oxide alternative (Process Factor D) resulted in the widest traces and lowest impedance. The impact of rework on impedance was also obvious with the impedance rising between 2.5-4 ohms as a result

of a single oxide or alternative oxide rework process. The 2.5-4 ohm range results in a swing of 5-8% shift in impedance for a nominal 50ohm transmission line and may be an issue in tight impedance controlled designs. This also showed a consistent delta between the different process chemistries with the extremes being oxide dissolution compared to the low-etch oxide alternative.

Using the physical parameters of each trace and the measured dielectric constant of each trace, the transmission line impedance, inductance, and capacitance values were modeled. See Figure 14. While there was good correlation between the model prediction and the measured values, the wide confidence windows can in part be attributed to the errors and gage accuracy associated with the physical measurements taken from cross sectioning. As with the impedance chart in Figure 12, the inductance and capacitance of the transmission line varied by the process factors with the most notable differences seen with the change due to a single rework process.

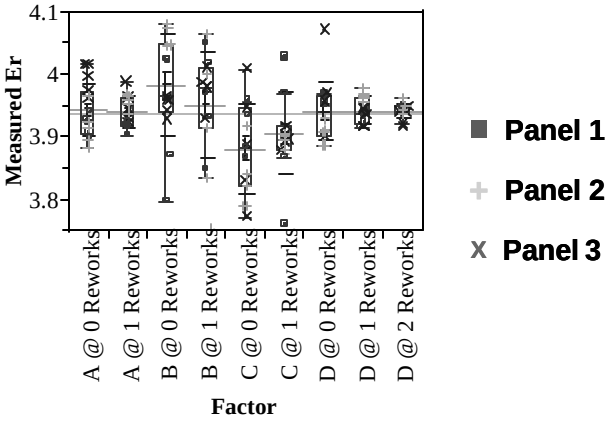

Figure 11 - Measured Dielectric Constant

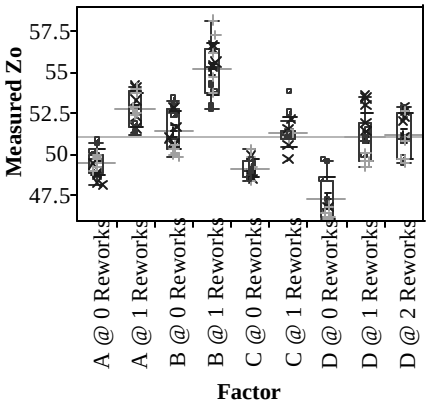

Figure 12 - Measured Impedance

$$1a)\quad Er = \left(\frac{T_d c}{x}\right)^2 \qquad 1b)\quad T_d = \frac{\Phi}{2\pi f} \qquad \left.\begin{array}{l} \\ \\ \end{array}\right\} where \quad \begin{array}{l} x = trace\_length \\ \Phi = measured\_phase\_angle \end{array}$$

Figure 13 - Dielectric Constant Extraction Equations

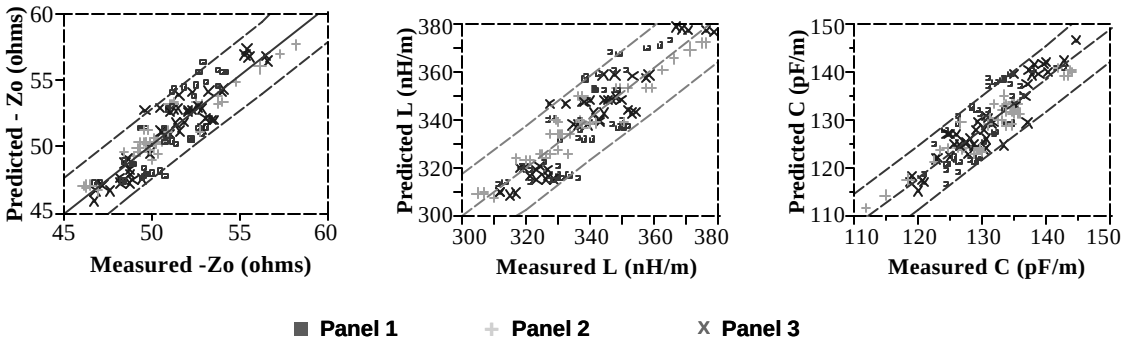

Figure 14 - Modeled vs Measured Transmission Properties.

The transmission line loss analysis of the process factors was obtained from the S-Parameter measurements. (See Figure 15.) The loss was calculated across the frequency by using the identity of loss, denoted by α, (Figure 16) as being the real part of gamma, γ, as defined in equation 2e. The measured transmission loss results are shown in Figure 17. As shown in Figure 18, the differences between any of the conditions were small relative to the total magnitude of the overall loss. The worst case difference between any two measurements was 0.32dB per inch at 20GHz which represented about 15% increase in loss. At lower frequencies, the worst case measured difference between any two measurements was smaller in magnitude; but, the

percentage difference remained at approximately 15% which indicates that any difference in modeling of loss between the measurements would be essentially linear with frequency.

$$2a)\ \ \Gamma_{Short} = S_{11} - \frac{S_{12}S_{21}}{1+S_{22}} \qquad 2b)\ \ \Gamma_{Open} = S_{11} + \frac{S_{12}S_{21}}{1-S_{22}}$$

$$2c)\ \ Z_{inShort} = Z_O \frac{1+\Gamma_{Short}}{1-\Gamma_{Short}} \qquad 2d)\ \ Z_{inOpen} = Z_O \frac{1+\Gamma_{Open}}{1-\Gamma_{Open}}$$

$$2e)\ \ g = arcTanh\left(\sqrt{\frac{Z_{inShort}}{Z_{inOpen}}}\right) = \sqrt{(R+jwL)(G+jwC)}$$

$$2f)\ \ Z = \sqrt{\frac{Z_{inShart}}{Z_{inOpen}}} = \sqrt{\frac{(R+jwL)}{(G+jwC)}}$$

$$2g)\ \ L = \mathrm{Im}\{g * Z\} \qquad 2h)\ \ C = \mathrm{Im}\left\{\frac{g}{Z}\right\}$$

Figure 15 - S-Parameter Extraction Equations

$$3a)\ \ a_{measured} \equiv \Re e\{g\} \ \ in \ \ Nepers/length$$

$$= \Re e\left\{\sqrt{(R+jwL)(G+jwC)}\right\} = \Re e\left\{\sqrt{-w^2LC}\left\{1-\left[\frac{RG}{w^2LC} + jw\left(\frac{G}{w^2C}+\frac{R}{w^2L}\right)\right]\right\}^{1/2}\right\}$$

$$\approx \frac{R}{2\sqrt{L/C}} + \frac{G}{2}\sqrt{L/C} \qquad ; from \ \ (1\pm v)^{1/2} \approx 1 \pm \frac{v}{2} - \frac{v^2}{8} \ \ for\ small \ \ v$$

$$3b)\ \ a_{\mathrm{modelled}} = \frac{R_{ac\_\mathrm{modelled}}}{2Z_o} + \frac{wCZ_o \tan d}{2} \qquad ; R = R_{ac\_\mathrm{modelled}} \ ; G = wC\tan d \ \ ; \sqrt{L/C} = Z_o$$

Figure 16 - Transmission Line Loss Characterization Equations

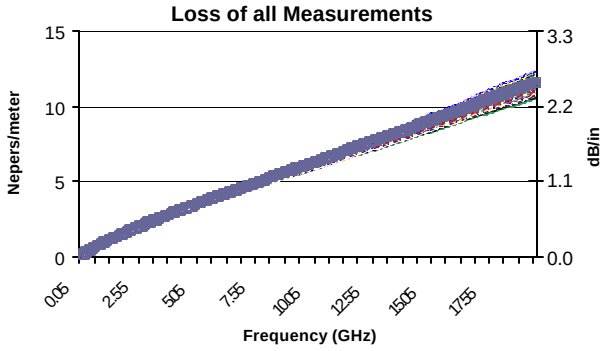

Figure 17 - Loss Measurements of All Traces

Figure 18 provides additional detail on the specific loss measurements at 2.5GHz and 17.5GHz detailing the differences by process factor and rework condition. For the black oxide condition and the alternative oxide condition, the losses were essentially identical between panels processed with a standard process and panels under going a rework process after the standard process. Through conductor loss modeling of R_{ac} using the measured trace geometries; it was found that the small measured differences matched the modeled loss differences across the frequency range. A reasonable conductor loss model for R_{ac} which was developed from conformal mapping techniques can be found in reference 9. At 17.5GHz the conductor

loss difference due to the measured geometry change was modeled at 0.02-0.03dB/in. This compares to a measured difference of black oxide with a standard process versus black oxide after a single rework of 0.027dB/in.

Both the oxide dissolution (Process B) and the low-etch alternative oxide (Process D) showed a loss delta between panels using the standard process and panels under going rework processes that exceeded the expected loss due to conductor geometry changes. The low-etch alternative oxide process was selected for additional investigation as there were more process conditions available as well as a large range of surface roughness conditions.

Within a given innerlayer bonding chemistry, the measured loss impact of rework was consistent with predicted in terms of impedance and trace widths as the wider traces produced the lowest loss at the higher frequencies. However, in a comparison between innerlayer bonding chemistries, the low-etch oxide alternative showed a very small but slightly larger loss at high frequencies that ran counter to the process resulting in the widest line widths. At lower frequencies, below 2-3GHz, where the conductor loss dominates, the low-etch alternative oxide with zero reworks did result in the overall lowest loss factor. The change in the relative loss ranking of the innerlayer bonding chemistries between low and high frequencies could be a result of slightly higher loss tangent or highlight a small frequency dependent measurement error.

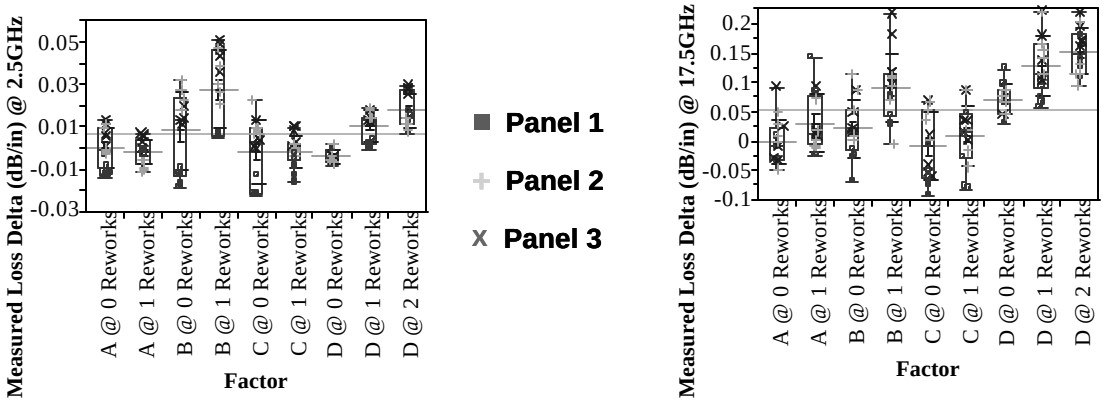

Figure 18 - Loss Measurement Detail at 2.5 GHz and 17.5GHz

Low-etch oxide alternative was used to check whether incorporating a surface roughness component into the loss model would improve the model accuracy. In order to check this, the modeled loss was subtracted from the measured loss to yield a loss residual. In the modeled loss, equation 3b, the measured values of the capacitance C and the impedance Zo were used to model each trace. Likewise, the physical measured trace geometries were used to calculate the modeled Rac component. The loss tangent value used in the model was 0.0175 plus a frequency dependent component of 0.00019 per GHz. These loss tangent values were obtained from measurement using a split post cavity on non-laminated material. The loss residuals were then compared to check if a systematic shift existed between rework factors that would indicate a loss component attributable to the change in surface roughness between the process factors. (Figure 19.)

Figure 15 shows the resulting loss residuals from the measured losses and modeled losses, only 4 of the 15 measurements for each condition are plotted to improve the clarity of the graph. What can be seen in Figure 15 is that the loss residuals for all three rework factors span the same range within a frequency measurement. This leads to the conclusion that the differences due to the physical geometries and resulting changes in impedance and capacitance account for the differences noted in Figure 18. Similar results were obtained for oxide dissolution (Process B).

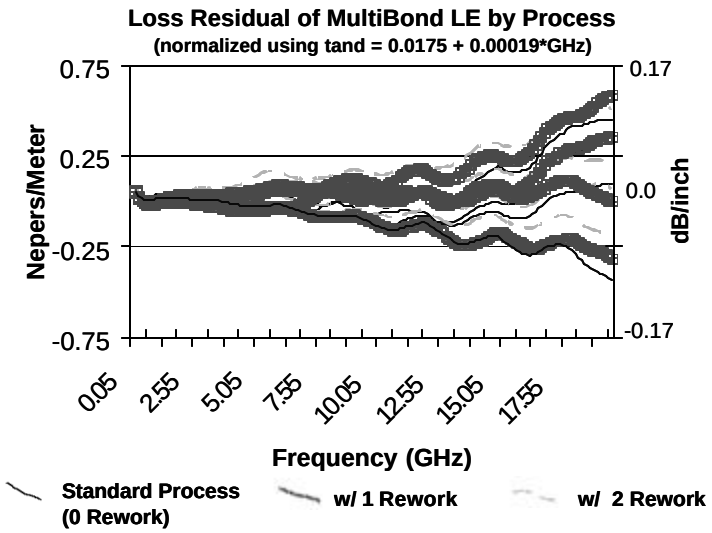

Figure 19: $a_{measured} - a_{modeled}$ for Low-Etch Oxide Alternative

Summary

For the scope of testing presented in this paper, the result of changes in oxide or oxide alternative chemistries or the use of rework processes during manufacturing do have a small measurable loss difference. It is shown that the differences are easily attributed to changes in the trace width and height geometries with surface roughness not contributing a measurable impact. It was also shown that the most pronounced electrical difference occurred in trace impedance shifts of 5-8% on 50ohm traces as a result of rework. The testing did confirm that newer low etch processes have the least impact on trace width and height compared to traditional processes.

SEM and Laser Profilometry demonstrated that the more aggressive processing with oxide alternative chemistries produced increased surface roughness. This was true when comparing oxide alternatives to low-etch oxide alternatives, as well as when comparing the impact of rework of each process on the surface topography.

In this study of stripline transmission lines, it was determined that adding a surface roughness loss component would not improve the current stripline models. This is in conflict with studies of microstrip transmission lines of varied surface topographies that indicated that there is a sizeable influence of copper foil roughness and loss. The primary difference between microstrip and stripline configurations is that in microstrip, the current is forced to concentrate in the copper tooth region closest to the ground plane where as in a stripline construction, the current is split between both the top and bottom faces of the trace with current densities depending on surface conductivity and proximity to nearest ground plane. This potentially would allow the current density to shift slightly as the surface roughness is altered and subsequently mask the loss impact. It is unclear at this time whether the loss effect of surface roughness differences was not noticeable in the stripline test because of potential differences in current density due to the physical changes resulting from the different processes, or that the overall impact is small compared to measurement noise, or that the magnitude of the physical change in trace width and height combined with cross section measurement gage capability resulted in errors that were larger than loss due to surface roughness.

Future testing may improve on the testing presented in this paper through the use of slightly offset stripline structures. This method would force additional current to the surfaces impacted by the surface prep chemistries. The use of homogenous lower loss materials would also decrease the dielectric loss impact and heighten the differences between the various surface topologies. Other improvements also include optimizing line widths for each process condition to yield identical impedance structures with similar trace widths

Regardless of above arguments on the relative impacts of factors, this study indicates that the implementation of oxide and oxide alternative processes do not substantially impact the transmission line losses through a frequency range of 20GHz. This conclusion pertains to the relative lossy systems of FR4, more importance may be placed on innerlayer bonding processes employed with very low loss substrate materials.

References

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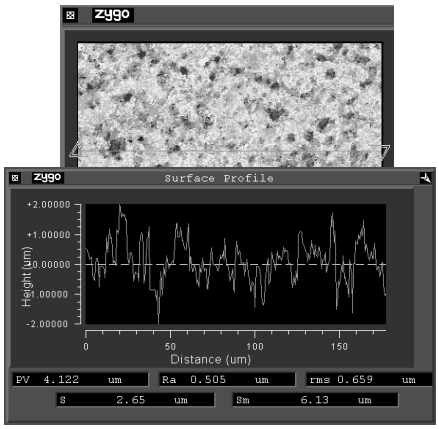
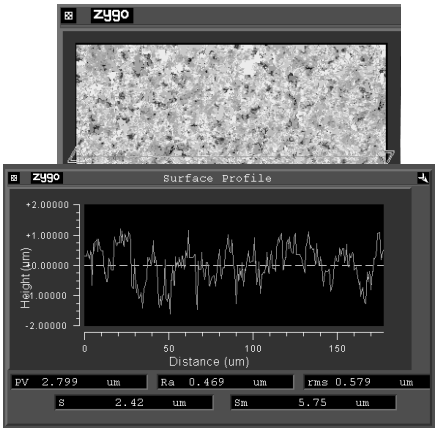
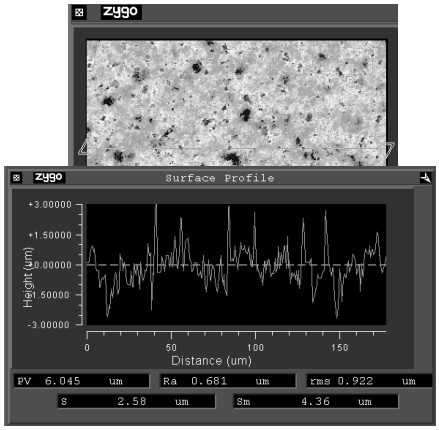
APPENDIX A - Profilometry Results on MultiBond 100 and MultiBond LE



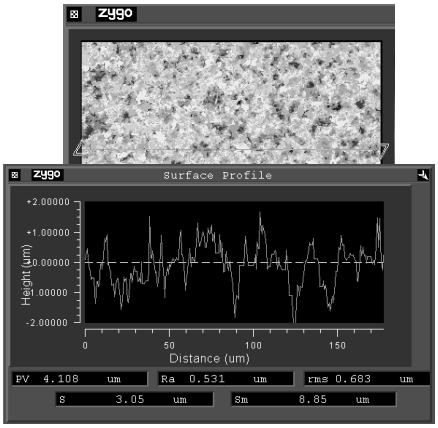
MultiBond 100
(Standard Process)



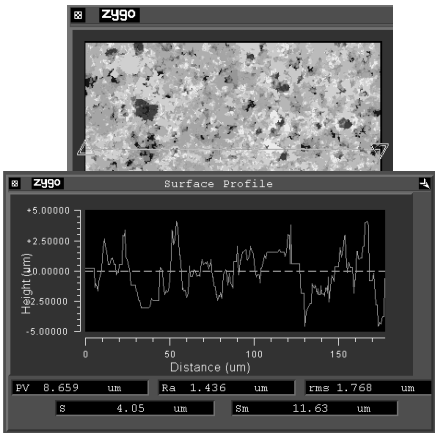
MultiBond LE
(Standard Process)



MultiBond 100
(Std Process + 1 Rework)



MultiBond LE
(Std Process + 1 Rework)



MultiBond LE
(Std Process + 2 Reworks)