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Effects of Conductor Surface Condition on High Frequency Loss

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Abstract
Efforts to reduce high frequency signal losses associated with dielectric materials have driven development and commercialization of more cost effective low loss laminate materials. These developments have been facilitated by the use of a variety of standardized dielectric test methods.

As dielectric losses are reduced, the relative contribution of conductor materials to overall loss increases. In order to better understand the implications of conductor material and surface finish choices, efforts have been made to quantify the impacts of these factors on loss.

While conductor material and surface finish influences may be directly measured using printed wiring board test structures, interpretation of the results are complicated by the influence of both the laminate material and the particular geometry selected for the test structure (microstrip versus stripline versus differential pair). The results of such measurements accurately reflect the specific test geometry examined, but are difficult to extrapolate to different systems.

An alternative test approach has been identified which provides a measure of conductor performance, decoupled from both system geometry and the influence of laminate material.

The basic test method described in IPC TM-650 2.5.5.5.1. (Stripline Test for Complex Relative Permittivity of Circuit Board Materials to 14 GHz) has been modified by comparing the results obtained using ideal smooth copper conductors and with those obtained with samples of alternative conductor materials, while maintaining a constant dielectric material. Changes in the resonator loss factor between the two tests allow calculation of the relative performance of the alternative material versus the ideal conductor.

Using this test method, the performance of a number of surface finishes, PWB foil treatments and inner-layer adhesion-promotion processes relative to a control smooth copper surface are reported.

Introduction
Understanding the impact of printed wiring board material properties on electrical performance at high frequencies has become increasingly important, as semiconductor device rise times have fallen and system speeds have risen.[1]

In order to create correctly functioning systems without extensive prototyping, the influence of design rules and material choices on system signal integrity must be assessed at the design stage. A variety of electromagnetic modeling tools[2,3] are available to printed wiring board designers, allowing such simulations.

In order to use electromagnetic modeling tools, a variety of system design attributes must be entered into the model. Such attributes include both geometric parameters such as conductor dimensions (trace widths, heights and lengths) and dielectric spacing, and also material electrical properties such as dielectric constant, dissipation factor and conductivity of the conductor material.

There are a number of methods for measurement of dielectric electrical properties over the ranges of frequencies relevant to system designers. Such test methods are necessary, since there is no simple physical model that can accurately predict the values for dielectric constant and dissipation factor from other physical properties of the dielectric.

In contrast, it has generally been possible to adequately predict conductor properties using the material DC conductivity and a skin depth model for high frequency conductivity.

However modeling of more complex situations, such as those involving conductor roughness or the use of surface coating on conductors (for either adhesion promotion or solderability enhancement), has required the use of more empirical approaches.[4]

Conductor Dissipative Losses

Any conductor with a finite conductivity presents resistance to flow of current. The resistance to flow of direct current of a material is characterized by its resistivity. The relative behavior of conductors towards DC current flow may be inferred from their respective values of resistivity.

Table 1 below shows resistivity values for metals commonly used in electronics applications.[5, 6]

At DC, several observations may be made about the relative performance of metals:

- Resistivity of silver is approximately 7% lower than that of copper
- Resistivity of nickel is approximately 4.5 times larger than that of copper

Table 1 - Resistivity of Metals used in Electronics Applications (at 20°C)

Metal	**Resistivity (microohm . cm)**
Silver	1.59
Copper	1.72
Gold	2.44
Aluminum	2.82
Nickel	7.80
Tin	11.5
Tin 99.3 Copper 0.7	11.7
Tin 96.5 Silver 3.5	12.3
Tin 63 Lead 37	15
Electroless Ni-P	ca. 50 - 120

In contrast to the DC model, resistivity is not the only parameter responsible for characterizing the resistance posed by a conductor to the flow of alternating current.

The "skin-effect" phenomenon introduces a more complex relationship, involving both material properties and the frequency of the alternating current.

Passage of a signal along an interconnection corresponds to the presence of time-varying electric and magnetic fields around the conductor. The degree to which these fields penetrate into a conductor is governed by two properties of the conductor material:

- Conductivity - electric field
- Permeability - magnetic field

Solution of Maxwell's equations allows calculation of the magnetic and electric fields as a function of depth within the conductor.[7]

The form of the solution shows that the magnitude of both the magnetic field and current density decrease exponentially with penetration into the conductor. The flow of alternating current is therefore concentrated towards the surface or "skin" of the conductor.

A parameter that usefully characterizes the distribution of current within the conductor is known as the skin depth (δ), the depth at which current and magnetic field have decreased to 1/e of their surface values.

$$\delta = 1/(\rho\ f\sigma\mu)^{1/2}$$

Where f is the frequency (Hz)
σ is the conductivity (S/m)
μ is the permeability (H/m) = $\mu_o\mu_r$

If the depth dependent current distribution is integrated, an equivalent surface resistivity to alternating current (R_s) can be calculated. R_s is found to be identical to the DC resistance of a planar conductor of thickness δ:

$$R_s = 1/\delta\sigma = (\rho f\mu/\sigma)^{1/2}$$

At frequencies where the skin depth is much less than the thickness of the conductor, the relative behavior of conductors towards AC current flow may be inferred from their respective values of surface resistivity.

The table below shows calculated values of surface resistivity for metals commonly used in electronics applications.

Since surface resistivity is proportional to the square root of both $(\text{conductivity})^{-1}$ and permeability, the relative behavior of metals at AC frequencies differs from than at DC.

Two observations can be made about these values for surface resistivity of metals:

- Surface resistivities of non-magnetic metals differ by a smaller proportion than their DC resistivities; for example, the value for silver is about 4% less than that of copper.
- Surface resistivities of magnetic metals differ by a greater proportion than their DC resistivities; for example, the value for nickel is more than 50 times larger than that of copper.

The data shown in Table 2 would be expected to accurately reflect relative performance for cases where the conductor consists of a single ideal material with a smooth surface.

Table 2 - Calculated Surface Resistivity of Metals used in Electronics Applications (at 20ºC)

Metal	**Surface Resistivity (ohm)**
Silver	2.51×10^{-7} ($f^{1/2}$)
Copper	2.61×10^{-7} ($f^{1/2}$)
Gold	3.10×10^{-7} ($f^{1/2}$)
Aluminum	3.33×10^{-7} ($f^{1/2}$)
Tin	6.74×10^{-7} ($f^{1/2}$)
Tin 99.3 Copper 0.7	6.80×10^{-7} ($f^{1/2}$)
Tin 96.5 Silver 3.5	6.97×10^{-7} ($f^{1/2}$)
Tin 63 Lead 37	7.69×10^{-7} ($f^{1/2}$)
Electroless Ni-P	$1.4 - 2.2 \times 10^{-6}$ ($f^{1/2}$)
Nickel	1.36×10^{-5} ($f^{1/2}$)

A number of cases can be identified where the frequency dependence of the surface resistivity would be expected to differ from the ideal $f^{1/2}$ behavior.

In the case of a conductor with a surface finish, consisting of one or more layers of different materials over a substrate, the distribution of the current between the substrate and the surface finish will depend on the frequency. As the frequency rises (and current becomes more and more concentrated towards the surface of the conductor), the effective surface resistivity will gradually transition from the value for the substrate material towards the value for the surface finish material.

A conductor with significant surface roughness would also be expected to show higher values of effective surface resistivity at frequencies where the skin depth is comparable to or smaller than the rms roughness.

Just as the DC resistance of a conductor is inversely proportional to its cross sectional area, the AC resistance of a conductor is inversely proportional to its perimeter length:

- For a typical PWB interconnection:
- Perimeter $\propto$ (trace width + trace thickness)

Reduction in conductor loss can therefore be achieved by two obvious design approaches, increased conductor width or reduced conductor length.

Use of increased conductor widths comes at the price of reduced wiring density and increased layer-to-layer separations (so as to maintain the original transmission line impedance).

While industry roadmaps understandably emphasize the evolving needs for finer line capabilities, many high frequency applications ranging from backplanes to 10 Gbit optical interface modules use relatively wide traces.[8, 9]

Conductor Dissipative Losses – Surface Roughness Effects

Additional conductor losses at high frequencies, associated with surface roughness, have been well known since the 1930's. In 1949 Morgan[10] published the first quantitative analysis of the effect of surface roughness on conductor losses.

His analysis, based on numerical solution, provides values for relative power dissipation (versus a smooth surface) for a number of well-defined surface geometries, including square, rectangular and triangular grooves, oriented both parallel to and perpendicular to the direction of current flow.

Morgan characterized the surface roughness effects in terms of the ratio of root means square roughness (?) to skin depth (δ).

For a surface with regular square grooves, of depth and width x and period 2x:

? = x/2

Table 3 shows the values that Morgan derived for relative power dissipation for the case of square grooves aligned transversely to the direction of current flow.

In order for a reduction in surface roughness of a conductor to yield a significant reduction in conductor loss, ? / δ must be greater than approximately 0.5 for the frequencies of interest.

Table 3 - Effect of Surface Roughness on Conductor Loss (after Morgan)

RMS Roughness / Skin Depth (? / d)	Relative Power Dissipation
0	1.00
0.25	1.04
0.50	1.17
1.00	1.57
1.75	1.75

The IPC specification[11] for printed wiring board foil, IPC-4562 describes surface morphology using two parameters; foil profile and surface finish.

Foil profile is characterized using the parameter R_z DIN (average maximum peak to valley height), while surface roughness is described using the parameter R_a (average deviation of the roughness profile from center line).

Since R_z is a measure of distance between extremes, rather than an average, values of R_z for a particular profile will be greater than the corresponding values for R_a or root means square roughness (?).

Table 4 shows the specifications for the four defined classes of foil profile.

Table 4 - Specification for Maximum Foil Profile (from IPC-4562)

Foil Profile	Designation	R_z (microns)
Standard	S	Not applicable
Low Profile	L	10.2
Very Low Profile	V	5.1
No treatment	X	Not applicable

While the use of lower profile foils will improve performance at high frequencies, adhesion between conductor surfaces and dielectric materials might eventually become a problem if the roughness is reduced too much.

In order to obtain the best combination of electrical performance and adhesion, the surface roughness of foils is aimed to fall just short of the level at which additional losses would be caused.

Experimental Measurement of Interconnection Loss – Review of Recent Publications
Approaches to measurements of interconnection loss may be divided into two groups:

- Measurements of total system loss
- Measurements of fundamental parameters controlling loss

The testing approach adopted will depend on the intended use of the data.

A design engineer may wish to carry out measurements to validate the results of modeling experiments. As long as the measured results are acceptably close to the predicted values, there is little incentive to develop a more refined model or to isolate the root cause of any deviations.

In contrast, a supplier of PWB materials may wish to record data to either ensure consistency of supplied product or to develop improved products. In these circumstances, it is desirable to be able to make measurements that enable isolation of the contributions of separate loss mechanisms.

Cullen et al.[12, 13] have carried out several investigations of the effects of dielectric materials and surface finish on high frequency signal loss.

In their first paper[12], the test vehicles used were microstrip circuits, fabricated from three different dielectric constant materials (all 500 micron thickness). In order to maintain a constant 50 ohm characteristic impedance, it was necessary to use different microstrip conductor widths for each of the laminate materials.

For each dielectric material, samples were prepared with each of a number of different surface finishes (OSP, ENIG, immersion silver and HASL) to allow evaluation of their effects on total system loss.

The measured differences in loss between the surface finishes were relatively small (less than 0.04 dB/cm at 10GHz). The authors hypothesized that larger differences would be seen at higher frequencies.

Results of a second phase of measurements [13], carried out using a differential pair test structure, were presented at the 2002 SMTA conference.

Under those test conditions, the effect of surface finish was found to be more pronounced, due the presence of surface finish at the conductor surfaces adjacent to the zones of greatest electromagnetic field magnitude.

Immersion tin was found to exhibit an increase of attenuation of approximately 0.2 db/cm (over OSP and immersion silver), while a 5.4 micron thick EN with immersion gold showed an increase of approximately 0.6 db/cm.

Overall levels of loss were found to be higher in the second study. The higher losses were attributed at least in part due to differences in effective conductor cross-section and width between single ended microstrip and differential pair test structures.

Analysis of this data demonstrates the difficulties of experimental design and interpretation when many factors influencing both dielectric and conductor loss are varied.

Separation of Conductor and Dielectric Loss
It is desirable to be able to make measurements that clearly separate conductor and dielectric effects. Examples of this type of approach are the standard IPC methods used to measure dielectric loss tangents.

IPC TM 650 2.5.5.5 and 2.5.5.5.1[14-17] both use an approach in which the conductor losses of a well-characterized electrical structure (a resonant stripline) are subtracted from total system losses to yield values for dielectric loss.

Previously derived equations[18,19] for conductor loss in a stripline resonator are used to calculate the conductor correction. The most accurate measurements of loss tangent are obtained when the use of smooth copper foils eliminates the need to adjust conductor losses for the influence of surface roughness.

In the present work, a modification of the 2.5.5.5.1 test method has been evaluated which allows the measurement of relative surface resistivity versus a control, smooth copper surface.

Description of Modified IPC TM 650 2.5.5.5.1 Test Method

The 2.5.5.5.1 method is based on the stripline resonator test structure shown in Figure 1.

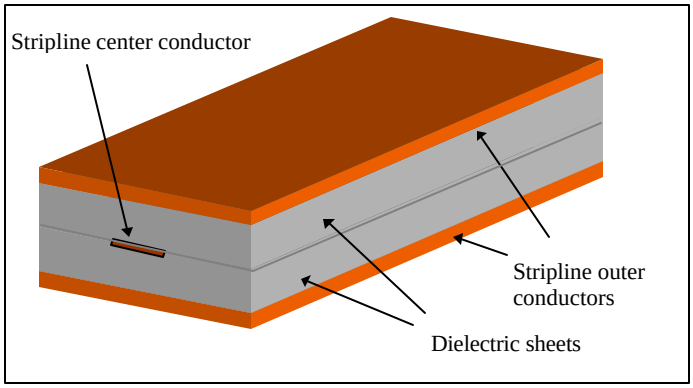

Figure 1 - Stripline Resonator Structure

This structure resonates both at a fundamental frequency and at a number of higher nodes (integral multiples of the fundamental frequency). At these resonant frequencies, the attenuation (return loss) of microwave energy in the structure is diminished.

The width at half power (3dB points) of each of these resonances can be used to derive the Q (quality) factor of the structure, which is, in turn, related to the total system loss.

The Q factor derived from the measured resonance (Q_{loaded}) requires adjustment to eliminate the effect of the measurement process, so as to provide the value of $Q_{unloaded}$.

The measurement consists of the measurement of the width of the resonances of the different nodes across the desired range of frequencies (at a specified level of power). The applied power level is maintained within the specified range through use of a coupling fixture with an adjustable gap dimension.

Signal generation and measurement of the resonant frequencies and power levels are most easily achieved using a network analyzer.

The overall losses are related by the following equation:

Loss Tangent $= (1/Q_{unloaded}) - (1/Q_{conductor})$

$1/Q_{conductor}$ is the conductor loss factor

The (complex) equations for the conductor loss are as follows [13,14]:

$$1/Q_{conductor} = a_c \, c / (p \, f_r \, (\varepsilon_r)^{0.5})$$

$$a_c = 4 \, R_s \, \varepsilon_r \, Z_o \, Y / (377^2 \, B)$$

$$R_s = 0.00825 \, (f_r)^{0.5} \quad \text{(surface resistivity)}$$

$$Z_o = 377 / (4 \, (\varepsilon_r)^{0.5} \, (C_f + (W / (B-T))))$$

$377 = 120 \, p$ Free space impedance, ohm

$C_f = (2X \log_e (X+1) - (X-1) \log_e (X^2-1))/ p$

$Y = X + 2 W X^2 / B +$
$X^2 (1+T/B) \log_e [(X+1) / (X-1)] / p$

$X = 1 / (1-T/B)$

ε_r = Relative Permittivity of dielectric

B = Ground plane spacing, mm

c = 299.976 Speed of light (mm/ns)

W = Resonator width, mm

T = Resonator conductor thickness, mm

f_r = Node resonant frequency (GHz)

The only parameters in these equations that are not simple functions of the physical dimensions of the test structure are the relative permittivity of the dielectric, the surface resistivity of the conductor and the frequency of the resonance.

Since the relative permittivity can be calculated from the measured frequencies at which a resonance occurs, the only remaining variables are the surface resistivity and the frequency.

The equation for $1/Q_{conductor}$, at a particular resonance frequency f, can therefore be expressed in a simplified form as follows:

$$1/Q_{conductor} = K R_s / K' f_r$$

An estimate of the surface resistivity of a conductor versus that of a reference sample may be made as follows:

- An initial series of measurements of $(1/ Q_{unloaded})$ are made with smooth copper conductors and two sheets of dielectric material.
- Values of $(1/Q_{Reference\ conductor})$ for the smooth copper conductors are calculated from the conductor loss equations, as a function of frequency.
- Values of loss tangent for the dielectric material are then calculated from the values of $(1/ Q_{unloaded})$ and $(1/Q_{conductor})$.
- The smooth copper conductors are removed and replaced with the conductors to be tested. These tests are run with the same sheets of dielectric material.
- Values for $Q_{unloaded}$ are obtained as a function of frequency.
- The values of $Q_{unloaded}$ and the previously measured values for the loss tangent of the dielectric material are used to calculate values for $(1/Q_{test\ conductor})$.
- The ratio of the measured conductor loss to the reference conductor loss provides a measure of their relative surface resistivities:

$$\frac{1/Q_{test\ conductor}}{1/Q_{reference\ conductor}} = \frac{K R_{s\ test} / K' f_r}{K R_{s\ reference} / K' f_r}$$

$$= \frac{R_{s\ Test}}{R_{s\ Reference}}$$

Use of a dielectric material with as low as possible a loss tangent, will increase the proportion of the loss associated with the conductor, and thus improve the measurement accuracy of the conductor loss.

Experimental

Reference data was obtained from a 15.2 cm long resonator structure, prepared from smooth, mechanical wrought copper foil (52 micron thick). The widths of the two ground planes and the center conductor were 2.54 cm and 0.64 cm respectively.

Test samples were either prepared by further processing of samples of the wrought foils (surface finishes / inner-layer adhesion promotion) or cutting samples of commercially available PWB foil materials to the required dimensions.

Two 1.55 mm thick sheets of RT/duroid® 5880 PTFE composite laminate (Rogers Corporation, Rogers, CT) were used as the low loss dielectric material.

Measurements were made using a Hewlett Packard 8510C Network Analyzer over a range of frequencies from 600 MHz to 14 GHz.

The overall test matrix was as follows:

Sample Type / Description

Electroless Nickel 8%P: 1.25 microns
Electroless Nickel 8%P: 2.5 microns
Electroless Nickel 8%P: 3.75 microns
Electroless Nickel 8%P: 5 microns
Electroless Nickel 8%P: 6.25 microns

Immersion Tin: 0.5 microns
Immersion Tin: 1.5 microns

Black Oxide
Converted Black Oxide
Oxide Replacement: 1 micron etch
Oxide Replacement: 3 micron etch

ED[20] Foil A: Vendor Treat Side
ED Foil B: Vendor Treat Side
ED Foil B: RTF[21] Side

The results of tests of electroless Ni-P (8wt.% P) surface finishes, varying from 1.25 to 6.25 microns, shown in Figure 2 clearly illustrate the effects of both coating thickness and frequency on relative surface resistivity (relative R_s).

Results and Discussion – Electroless Nickel

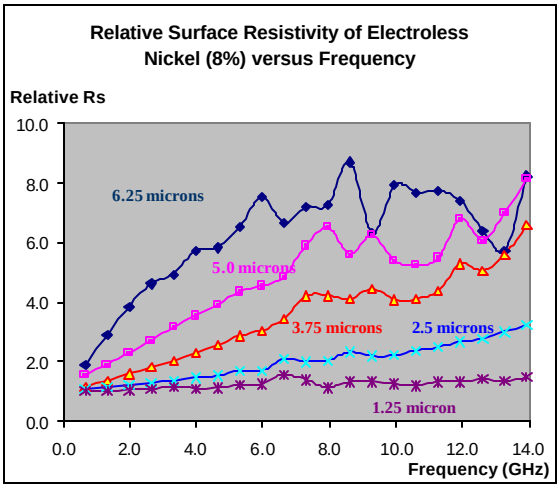

Figure 2 - Relative Surface Resistivity of Electroless Nickel over a Copper Substrate

At low frequencies, all values of relative R_s tend towards 1, as the behavior of the conductor approximates to that of the underlying copper.

As frequency rises, the relative R_s of all the electroless nickel samples rises. The degree of increase is strongly affected by deposit thickness.

At an electroless nickel thickness of 5 microns or less, values of R_s increase progressively over the range of frequencies evaluated. The degree of increase of the thinner coatings is smaller (x 1.5 for the 1.25 micron thickness and x 3.3 for the 2.5 micron thickness).

The relative R_s for the sample with a thickness of 6.25 microns, reaches a stable value (approximately 8) above 6 GHz, presumably as the current flow above that frequency becomes restricted to the coating alone.

The value of the relative R_s at frequencies above 6 GHz corresponds to a resistivity 8^2, i.e., 64 times larger, than copper, since the surface resistivity is proportional to the square root of the resistivity.

Based on a value of copper resistivity of 1.7 microohm.cm, the value of resistivity for electroless nickel (8 wt.% P) is calculated to be approximately 110 microohm.cm, in good agreement with previously published values.

Results and Discussion – Immersion Tin

The results of tests of two different thickness (0.5 and 1.5 microns nominal) samples of immersion tin are shown in Figure 3.

The samples show behavior that is analogous in form to that of the electroless nickel samples, with low frequency relative R_s tending towards 1.

The relative R_s of the 1.5 micron thick sample reaches a limiting value (of approximately 4.4) at about 4 GHz.

The observed limiting value corresponds to a relative resistivity versus copper of $(4.4)^2$ i.e., 19.4. Based on this value, the value of resistivity for an immersion tin coating is calculated to be approximately 33 mic roohm.cm.

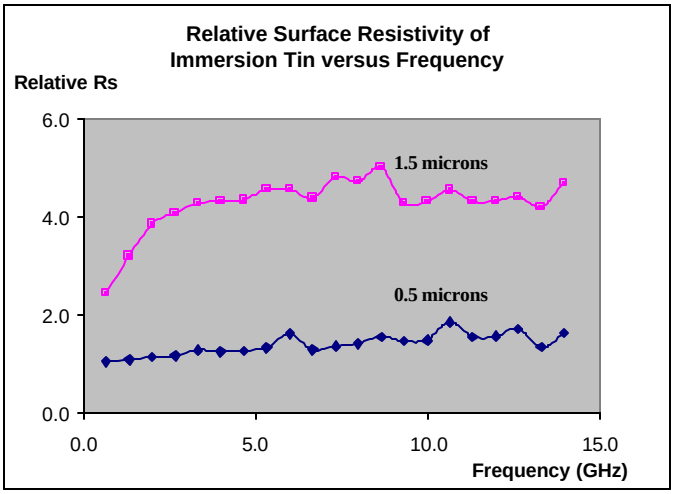

Figure 3 – Relative Surface Resistivity of Immersion Tin over a Copper Substrate

While this value is substantially larger than the value for pure tin (11 microohm.cm), it is certainly not unreasonable, given the formation mechanism and structure of immersion tin deposits.

The lower thickness required to reach limiting relative R_s (versus electroless nickel) may be a consequence of the lower resistivity of the immersion tin deposit, since lower resistivity yields smaller values of skin depth.

The 0.5micron thick sample shows much lower values of relative R_s, suggesting that the copper substrate dominates performance over the range of frequencies examined

Results and Discussion – PWB Foil Adhesion Treatments

Results of tests carried out on PWB foil surfaces are shown in Figure 4.

Results obtained for the vendor side treatment of Foil A showed an increase in relative Rs from 1 at 600 MHz to approximately 1.7 at 14 GHz.

The relative R_s behavior of the vendor and RTF sides of Foil B was quite similar (and considerably superior to Foil A).

The values of relative Rs at low frequencies were less than 1, possibly reflecting the effects of measurement errors. At higher frequencies, the relative R_s rose with the values reaching 1.1 at 14 GHz.

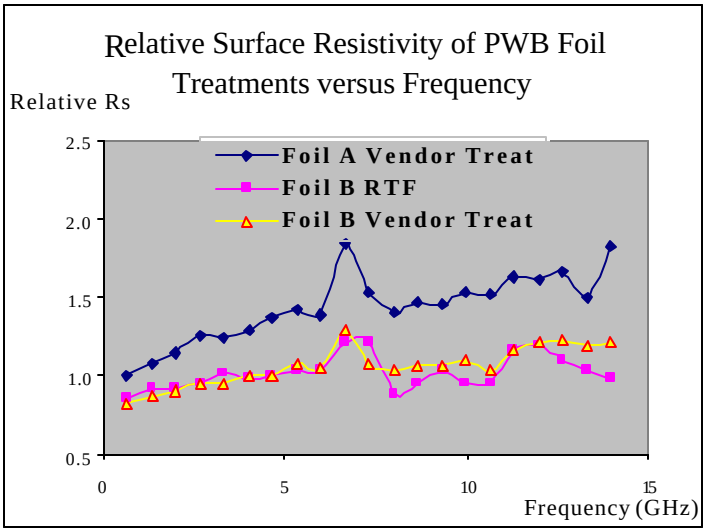

Figure 4 - Relative Surface Resistivity of PWB Foil Treatments

Measurements of the surface roughness of the foil samples were made using a Dektak (Model 200v) stylus profilometer. Results were derived from 256 parallel scans, covering a total sampled area of 500 microns x 500 microns.

The measured values of RMS deviation (variance) and Ra (mean deviation) for each of the three foil samples are shown in Table 5. These measurements confirm that the sample exhibiting the highest relative R_s (Foil A) was the roughest of the three samples.

Table 5 - Surface Roughness Measurements of PWB Foil Adhesion Treatments (microns)

Sample	Treatment	RMS	Ra
Foil A	Vendor side	3.05	2.42
Foil B	RTF side	1.42	1.13
Foil B	Vendor side	1.00	0.72

However, while the surface roughness measurements show a significant difference between the two sides of Foil B, the relative R_s behavior of the two sides is very similar. The data suggests that factors other than surface roughness, such as surface composition, are also contributing to the measured loss behavior.

Results and Discussion - Inner-layer Adhesion Promotion

The behavior of the four adhesion promotion processes evaluated was found to be indistinguishable from wrought copper foil (within experimental error) between 600 MHz and 14 GHz.

These results indicate that the surface composition and morphology changes produced by these inner-layer adhesion promotion processes are too small to have a measurable impact on loss.

Repetition of these experiments on electrodeposited foil substrates is planned, in order to determine if differences in copper grain structure might have an influence on performance.

Conclusions

- A simple modification of an existing dielectric test method IPC TM-650 2.5.5.5.1, allows measurement of conductor surface resistivity relative to a reference conductor (a smooth copper foil) at frequencies up to 14 GHz.
- Preliminary results using this technique demonstrate the ability to quantitatively measure the effects of the both the nature and thickness of surface finishes and surface roughness of PWB foil surfaces on conductor surface resistivity.
- Values of electroless nickel resistivity derived from these measurements are consistent with values previously reported.
- Values of immersion tin resistivity derived from these measurements are about three times higher than literature values for pure tin.
- Inner-layer adhesion promotion processes, applied to the wrought copper foil surface, were found to have almost no influence on relative surface resistivity.

Acknowledgements
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References M. Bayes, "Printed Wiring Board Material Sets – Implications of High Frequency Applications", IPC EXPO, March 2003
2. Ansoft HFSS™ (www.ansoft.com)
3. Mayo Clinic Special Purpose Processor Development Group (http//:www.mayo.edu/sppdg)
4. A. Byers, "Accounting for High Frequency Transmission Line Effects in HFSS", Presentation at Ansoft Design Conference, Las Angeles CA, 2002 http://www.ansoft.com/hfworkshop03/andy_Byers_Tektonix.pdf
5. Handbook of Chemistry and Physics, CRC Press, 2002
6. Z. Karim, "Lead-Free Solder Bump Technologies for Flip Chip Packaging Applications", Proceedings Advanced Packaging Technology Conference, SMTA, 2001
7. S. Ramo, J. Whinnery, T. Van Duzer, Fields and Waves in Communication Electronics; John Wiley, 1993
8. E. Sayre et al, "OC-48 / 2.5 Gbps Interconnect Engineering Design Rules", Digital Communication System Design Conference, 1999
9. L. Williams et al, "Simulating the XFP Electrical Interface", CommsDesign, January 2003. (www.commsdesign.com /design_corner/OEG20030129S0013)
10. S. Morgan, J. Applied Phys., 20 (4), 352 – 362, 1949
11. IPC-4562, "Metal Foil for Printed Wiring Applications", May 2000
12. D. Cullen et al, "Effects of Surface Finish on High Frequency Signal Loss Using Various Substrate Materials, " IPC Expo, April 2001
13. G. Brist et al, "Reduction of High-Frequency Signal Loss Through the Control of Conductor Geometry and Surface Metallization", SMTA Conference 2002
14. IPC-TM-650, Method 2.5.5.5 "Stripline Test for Permittivity and Loss Tangent at X-Band", Revision C, 1998
15. IPC-TM-650, Method 2.5.5.5.1 "Stripline Test for Complex Relative Permittivity of Circuit Board Materials to 14 GHz", 1998
16. G. R. Traut, "Complex Permittivity over a Wide Frequency Range by Adjustable Air Gap Probing a Stripline Resonator", IPC EXPO, March 1997
17. G. R. Traut, "Complex Permittivity of RF Circuit Board Materials by Resonances of a Stripline Section in the 0.2 – 15 GHz Range", Measurement Science Conference, January 1997
18. S. B. Cohen, "Characteristic Impedance of the Shielded-Strip Transmission Line", IRE Trans. MTT, (2), 52 – 57, 1954
19. S. B. Cohen, "Problems in Strip Transmission Lines", IRE Trans. MTT, (3), 119 – 126, 1955
20. Electrodeposited foil
21. Reverse Treated Foil

ROHM AND HAAS ELECTRONIC MATERIALS

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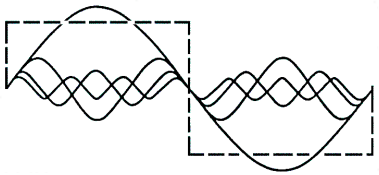


Outline of Presentation

- **Introduction**
- **Conductor Loss Mechanisms**
- **Modeling of PWB Electrical Performance**
- **Description of Conductor Loss Measurement Technique**
- **Experimental Results**
- **Summary**

Signal Loss / Distortion

- Digital signals contain energy over a range of frequencies:
  - Higher frequencies associated with faster pulse repetition rates and shorter pulse rise times
- In order to preserve the shape of a signal pulse an ideal interconnection should transmit all signal frequencies:
  - Without energy loss
  - At equal propagation velocities

Dissipative Signal Loss

- Dissipative signal loss involves the conversion of signal energy to heat through two mechanisms:
  - Conductor Resistance controlled by:
    - Conductor high frequency resistance
    - Conductor length and cross sectional geometry
  - Dielectric Material Losses:
    - Dielectric loss tangent
    - Transmission line geometry

Conductor Losses at Low Frequencies

- At DC and at low frequencies, current flow within a conductor is essentially uniform
- Conductor resistance can be calculated from knowledge of material resistivity and its geometry
  - Low frequency resistance is proportional to resistivity

Conductor Losses at Low Frequencies

Metal	Resistivity (microohm . cm)	Relative Resistivity (versus copper)
Silver	1.59	0.92
Copper	1.72	1.00
Aluminum	2.82	1.64
Nickel	7.80	4.5
Electroless Ni-P	ca. 50 - 120	ca. 30 - 70

Conductor Losses at High Frequencies

- The depth to which a time varying electromagnetic field penetrates into a conductor is controlled by two material properties and the field frequency:
  - Conductivity - Electric field
  - Permeability - Magnetic Field
- Solution of Maxwell's equations shows that the field strengths decrease exponentially with depth into the conductor and current flow is therefore concentrated near the surface
  - "Skin Effect"

Conductor Losses at High Frequencies

- The mathematics of high frequency current distribution allow the calculation of a conductor depth δ ("skin depth") which would have an equivalent resistance to DC current flow

$$\delta = 1/(\pi f \sigma \mu)^{1/2}$$

f is the frequency (Hz)

σ is the conductivity (S/m)

μ is the permeability (H/m) = $\mu_o \mu_r$

Surface Resistivity

- A material property, termed the Surface Resistivity (R_s), can now be derived as

$$R_s = 1/\delta\sigma = (\pi f\mu/\sigma)^{1/2}$$

- R_s is proportional to $f^{1/2}$
- Since R_s is proportional to $(1/\text{conductivity})^{1/2}$, differences between the behavior of non-magnetic materials are less than at DC conditions

Conductor Losses at High Frequencies

Metal	Surface Resistivity (ohm)	Relative Surface Resistivity (versus copper)
Silver	$2.51 \times 10^{-7} (f^{1/2})$	0.96
Copper	$2.61 \times 10^{-7} (f^{1/2})$	1.00
Aluminum	$3.33 \times 10^{-7} (f^{1/2})$	1.28
Nickel	$1.36 \times 10^{-5} (f^{1/2})$	52
Electroless Ni-P	$1.4\text{-}2.2 \times 10^{-6} (f^{1/2})$	approx 6.7

Effects of Surface Roughness

- Influence of conductor roughness on high frequency loss noted during early development of microwave technology (1930's onwards)
- Morgan (Bell Labs) published a theoretical treatment in 1949
- He derived relationships between rms roughness and relative loss for several ideal surface morphologies
  - Rectangular and triangular grooves
  - Groove orientation parallel and perpendicular to direction of current flow

Effects of Surface Roughness

- While the impact of surface roughness is often described as being caused by an increased path length for current flow, it is better visualized as being caused by "shielding" of parts of the surface from the electromagnetic field
  - For example, grooves oriented parallel to current flow also cause loss
- Increase in loss occurs over a relatively wide frequency range - approximately f $\rightarrow$10f
  - Onset at rms roughness / skin depth ratio of approximately 0.5
  - Loss tends towards 2 x when ratio exceeds 1.75

Overall System Loss

- Overall signal losses within a PWB interconnection are the sum of conductor and dielectric losses
  - Conductor loss proportional to (frequency)$^{1/2}$
  - Dielectric loss proportional to frequency
- Three possible zones of behavior
  - Conductor loss control - lower frequency
  - Mixed loss control – intermediate frequencies
  - Dielectric loss control – higher frequencies

PWB Performance Measurement versus Modeling

- Fabrication and characterization of PWB prototypes is time-consuming and expensive
- Electromagnetic modeling allows the performance of a PWB design to be characterized and/or optimized before board fabrication
- Inputs to the model:
  - Physical dimensions of the interconnect structure
    - Conductor locations, width and thickness
  - Material properties
    - Dielectric Constant
    - Loss Tangent
    - Metal Conductivity

Interconnection Loss Modeling

- Advantages
  - Easy to extract the relative contributions of conductor and dielectric dissipative loss
  - Easy to assess impacts of material substitutions or changes in design rules
- Disadvantages
  - The PWB model is only as good as the material property inputs
    - Bulk dielectric properties are well characterized by existing test methods
    - Conductor properties are currently extrapolated from DC values of bulk conductivity

Interconnect Loss Modeling Future Needs

- Develop test methods that allow direct measurement of conductor performance, including factors that cause loss to deviate from ideal behavior, such as:
  - Surface roughness
  - Surface finish
  - Foil treatments
- Options
  - Test structures with insignificant dielectric loss
  - ✓ Test structures where dielectric loss can be accurately measured and subtracted from total loss

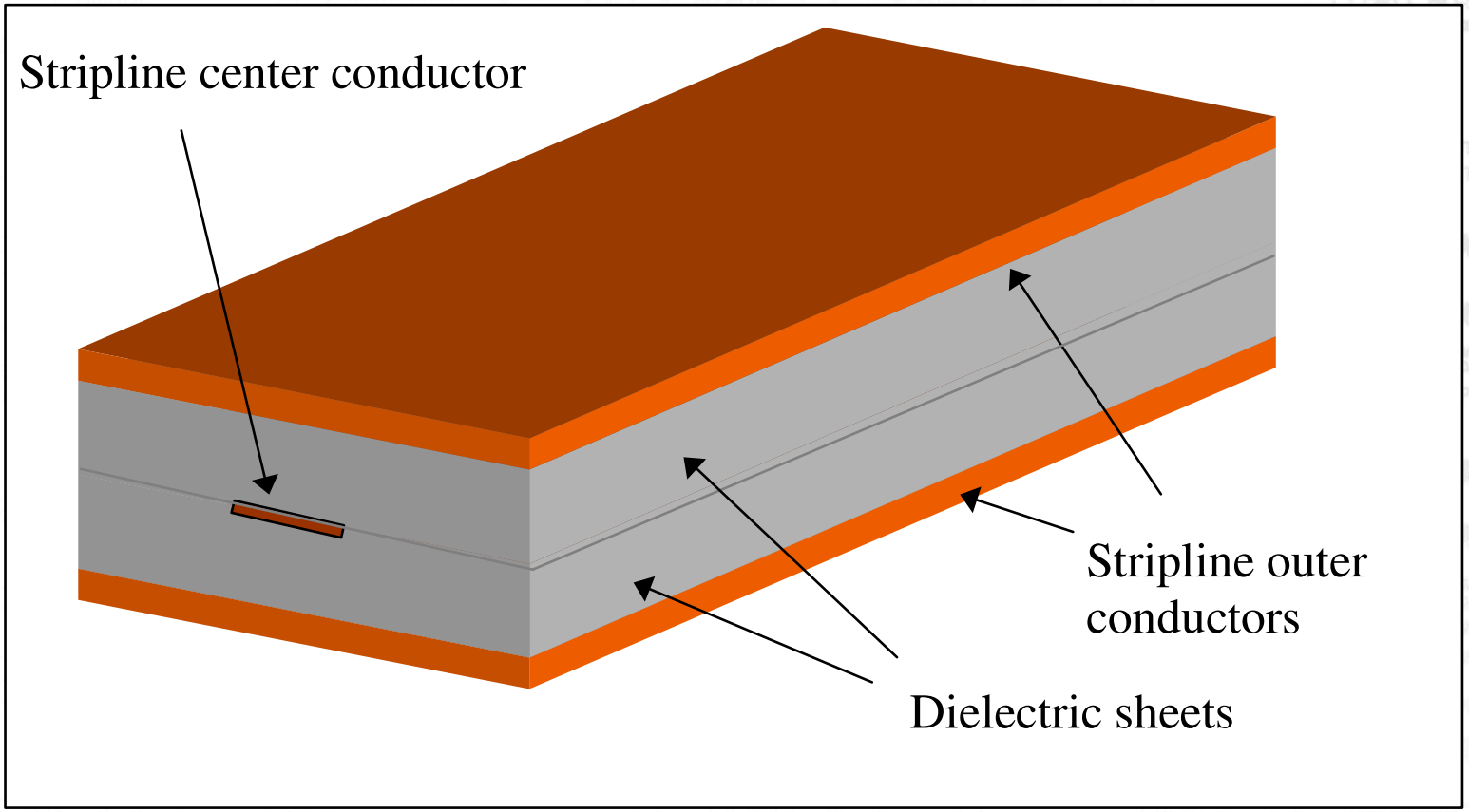
IPC TM 650 2.5.5.5.1

- "Stripline Test for Complex Relative Permittivity of Circuit Board Materials to 14 GHz"
- Sharpness of stripline resonances is controlled by total system loss at resonant frequencies
- The test method derives dielectric loss tangent by subtracting a calculated conductor Q factor from the measured system Q factor

$$\text{Dielectric Loss Tangent} = (1/Q_{\text{unloaded}}) - (1/Q_{\text{conductor}})$$

- A theoretical model for stripline circuit loss behavior may be used to calculate conductor loss if an "ideal" conductor is used
  - Smooth copper foil is sufficiently ideal

IPC TM 650 2.5.5.5.1 Test Structure



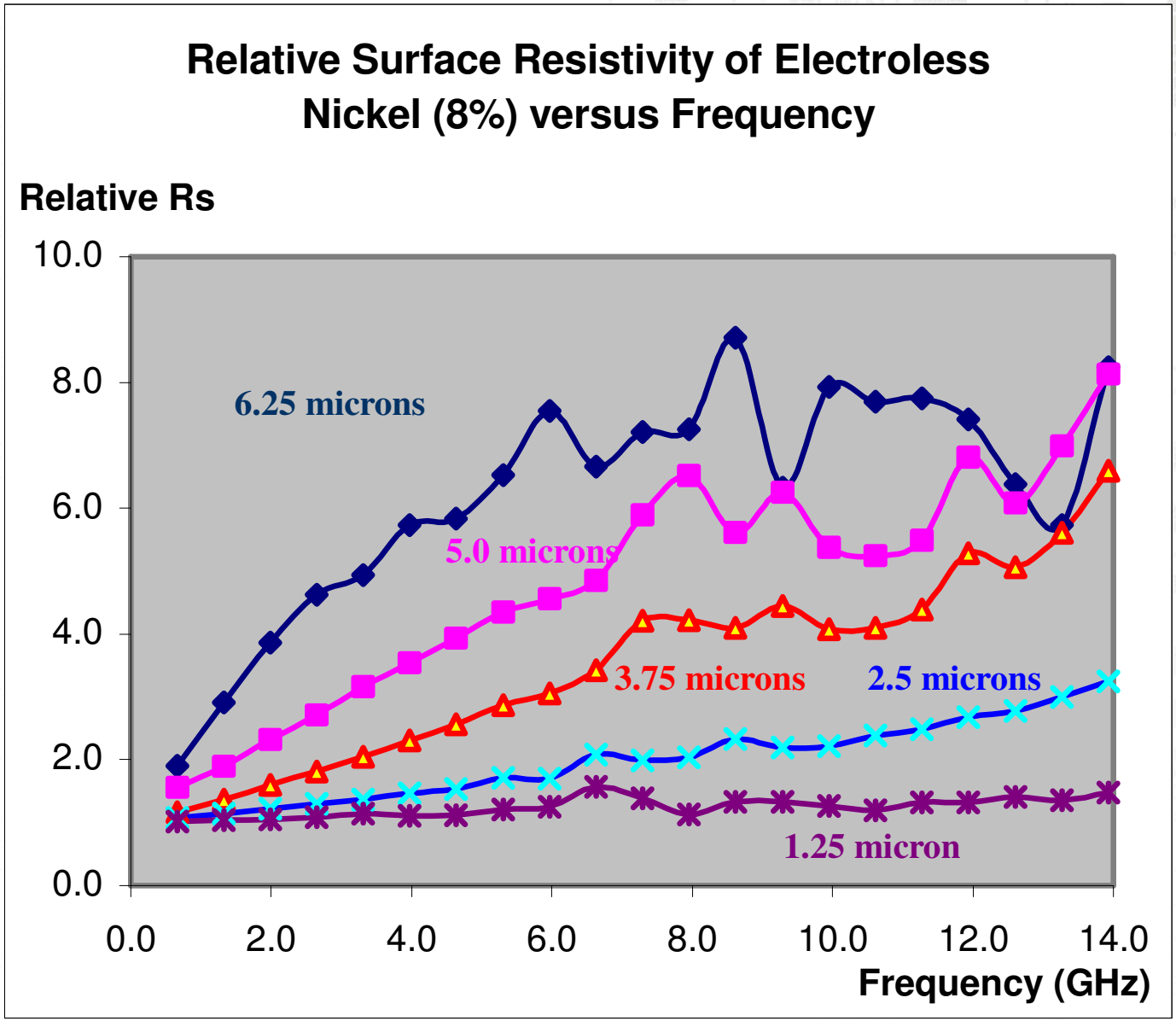
Conductor Loss Measurement Using the 2.5.5.5.1 Method

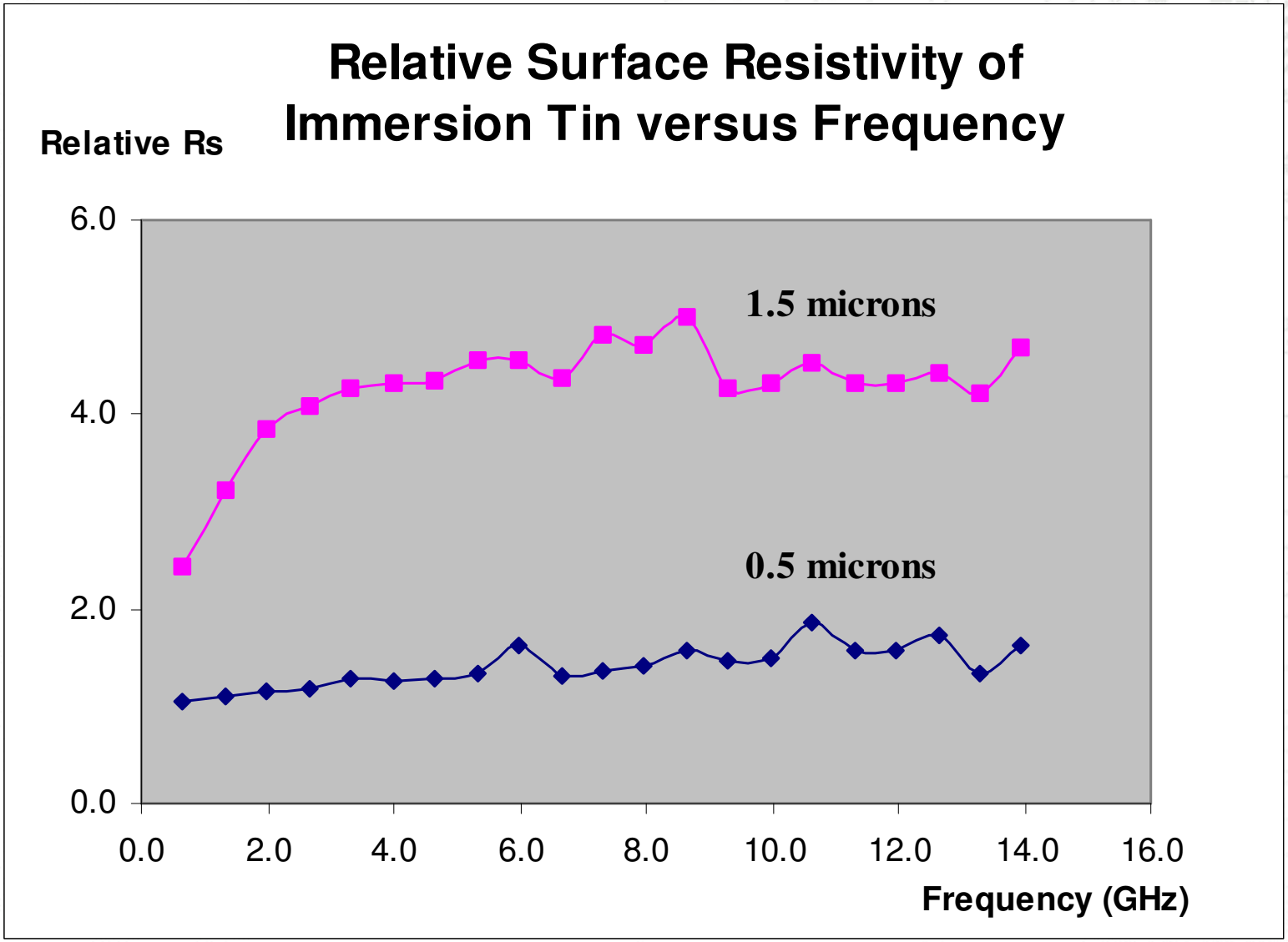
1. Measure the loss tangent of a selected low loss tangent dielectric material, with smooth copper conductors, by measurement of stripline loss per 2.5.5.5.1
2. Replace conductors with test samples, but use the same (already characterized) dielectric material. Re-measure stripline loss.
3. Calculate the conductor loss by subtracting the previously derived values of loss tangent from the measured overall loss

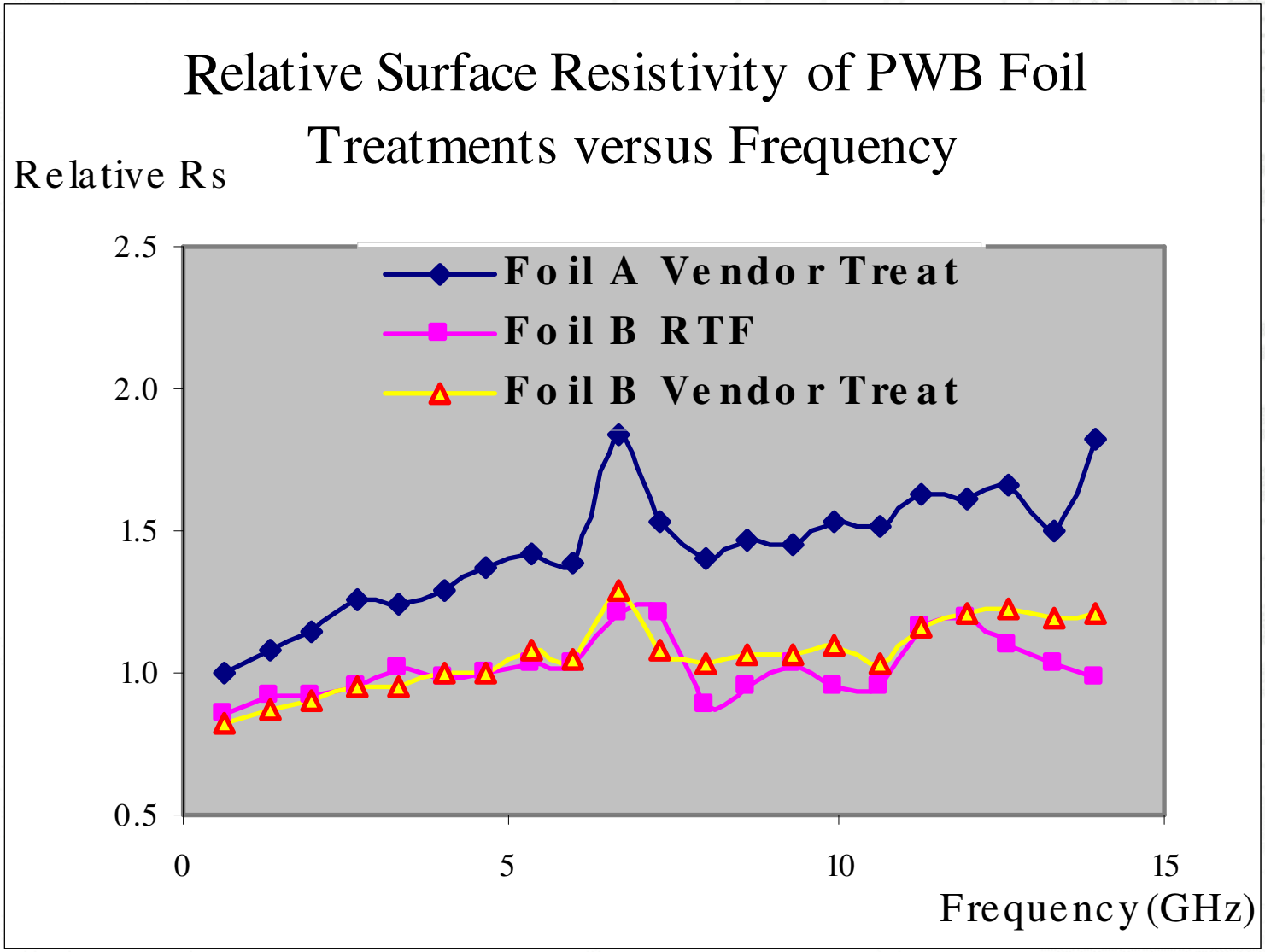
$$(1/Q_{\text{test conductor}}) = (1/Q_{\text{unloaded}}) - \text{Loss Tangent}$$

Conductor Loss Measurement Using the 2.5.5.5.1 Method

- $(1/Q_{conductor})$ is proportional to R_s, the surface resistivity.
- Substituting the test conductor for the ideal conductor only changes the value of one variable, R_s
- The ratio of $(1/Q_{test\ conductor}) / (1/Q_{ideal\ conductor})$ represents the ratio of the values of R_s for the test and ideal conductors
- This ratio will be referred to as "Relative R_s"
- Relative R_s includes the effects of differences in material conductivity, surface composition and roughness


Relative Surface Resistivity of Electroless Nickel (8%) versus Frequency
Relative Rs
10.0
8.0
6.0
4.0
2.0
0.0
6.25 microns
5.0 microns
3.75 microns
2.5 microns
1.25 micron
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
Frequency (GHz)


Relative Surface Resistivity of Immersion Tin versus Frequency
Relative Rs
6.0
4.0
2.0
0.0
1.5 microns
0.5 microns
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
Frequency (GHz)


Relative Surface Resistivity of PWB Foil Treatments versus Frequency
Relative Rs
2.5
2.0
1.5
1.0
0.5
0
5
10
15
Frequency (GHz)
Foil A Vendor Treat
Foil B RTF
Foil B Vendor Treat

Innerlayer Adhesion Promotion Processes

- Processes evaluated (on wrought copper foil)
  - Black Oxide
  - Bronze Oxide
  - Reduced Oxide
  - Oxide Replacement (at both 1 and 3 micron material removal)
- No detectable impact on Relative R_s
- Level of roughness created by these processes is sufficiently small that no additional loss is seen up to 14GHz

Summary

- The test procedure described in IPC TM 650 2.5.5.5.1 has been modified to allow measurement of values of surface resistivity (R_s) relative to an ideal control conductor
- Measurements of the values of Relative R_s for two surface finishes and several different foil vendor treatments have been presented
- The relative R_s of thin (1.25 micron) electroless nickel plated samples is close to 1, indicating that the impact of EN on conductor loss up to 14 GHz is negligible at that thickness

Summary

- As deposit thickness increases, the relative R_s of electroless nickel plated samples show a greater degree of increase with frequency
- At a thickness of 5 microns or above, the relative R_s of electroless nickel reaches a limiting value of approximately 8, indicating that the current flow is completely within the electroless nickel deposit at those frequencies
- Similar behavior is seen for samples of immersion tin, although the limiting behavior is seen at lower deposit thickness (due to the higher conductivity / thinner skin depth)

Summary

- Measurements of relative R_s for three copper foil vendor treatments show measurable increases in R_s across the range 1 – 14 GHz
- The roughest surface treatment gives the largest increase in R_s, with values rising from 1 at 1 GHz to approximately 1.7 at 14 GHz
- This test approach offers a means of directly isolating and characterizing the performance of conductors at high frequencies

Thank you !

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